SECTION 5
HIGH SPEED ADC APPLICATIONS
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DRIVING ADC INPUTS FOR LOW DISTORTION AND WIDE DYNAMIC RANGE

In order to achieve wide dynamic range in high speed ADC applications, careful attention must be given to the analog interface. Many ADCs are designed so that analog signals can be interfaced directly to their inputs without the necessity of a drive amplifier. This is especially true in ADCs such as the AD9220/21/23 family and the AD9042, where even a low distortion drive amplifier may result in some degradation in AC performance. If a buffer amplifier is required, it must be carefully selected so that its distortion and noise performance is better than that of the ADC.

Single-supply ADCs generally yield optimum AC performance when the common-mode input voltage is centered between the supply rails (although the optimum common-mode voltage may be skewed slightly in either direction about this point depending upon the particular design). This also eases the drive requirement on the input buffer amplifier (if required) since even "rail-to-rail" output op amps give best distortion performance if their output is centered about mid-supply, and the peak signals are kept at least 1V from either rail.

Typical high speed single-supply ADC peak-to-peak input voltage ranges may vary from about 0.5V to 5V, but in most cases, 1V to 2V peak-to-peak represents the optimum tradeoff between noise and distortion performance.

In single-supply applications requiring DC coupling, careful attention must be given to the input and output common-mode range of the driving amplifier. Level shifting is often required in order to center a ground-referenced signal within the allowable common-mode input range of the ADC.

Small RF transformers are quite useful in AC coupled applications, especially if the ADC has differential inputs. Significant improvement in even-order distortion products and common-mode noise rejection may be realized, depending upon the characteristics of the ADC.

An understanding of the input structure of the ADC is therefore necessary in order to properly design the analog interface circuitry. ADCs designed on CMOS processes typically connect the sample-and-hold switches directly to the analog input, thereby generating transient current pulses. These transients may significantly degrade performance if the settling time of the op amp is not sufficiently fast. On the other hand, ADCs designed on bipolar processes may present a relatively benign load to the drive amplifier with minimal transient currents.

The data sheet for the ADC is the prime source an engineer should use in designing the interface circuits. It should contain recommended interface circuits and spell out relevant tradeoffs. However, no data sheet can substitute for a fundamental understanding of what's inside the ADC.

HIGH SPEED ADC INPUT CONSIDERATIONS

- **Selection of Drive Amplifier (Only if Needed!)**
- **Single Supply Implications**
- **Input Range (Span): Typically 1V to 2V peak-to-peak for best distortion / noise tradeoff**
- **Input Common-Mode Range: V_S / 2 (Nominally) for Single Supply ADCs**
- **Differential vs. Single-Ended**
- **AC Coupling Using Transformers**
- **Input Transient Currents**

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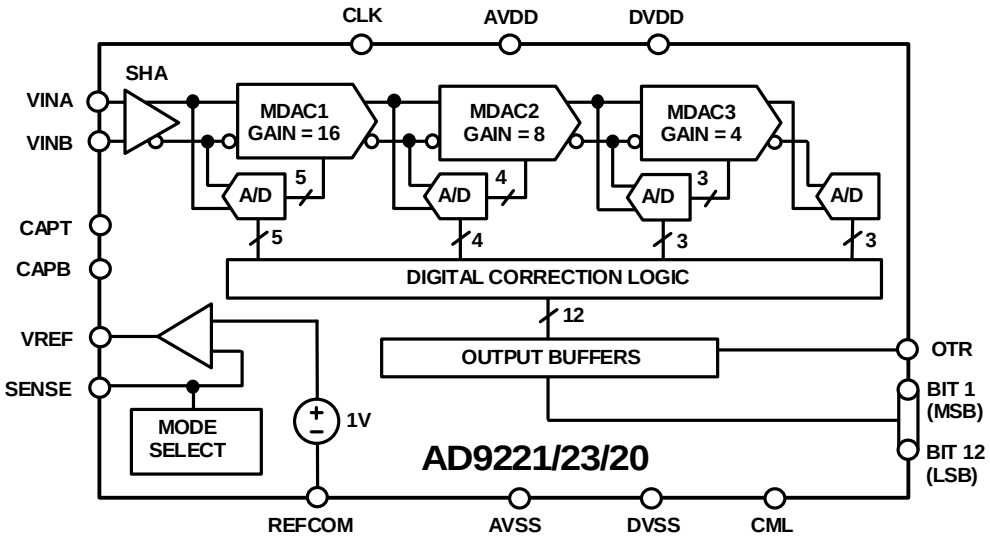
5.1

Switched-Capacitor Input ADCs

The AD9220/21/23-series of ADCs are excellent examples of the progress that has been made in utilizing low-cost CMOS processes to achieve a high level of performance. A functional block diagram is shown in Figure 5.2. This family of ADCs offers sampling rates of 1.25MSPS (AD9221), 3MSPS (AD9223), and 10MSPS (AD9220) at power dissipations of 60, 100, and 250mW respectively. Key specifications for the family of ADCs are given in Figure 5.3. The devices contain an on-chip reference voltage which allows the full scale span to be set at 2V or 5V peak-to-peak (full scale spans between 2V and 5V can be set by adding two external gain setting resistors).

AD922X-SERIES ADC FUNCTIONAL DIAGRAM



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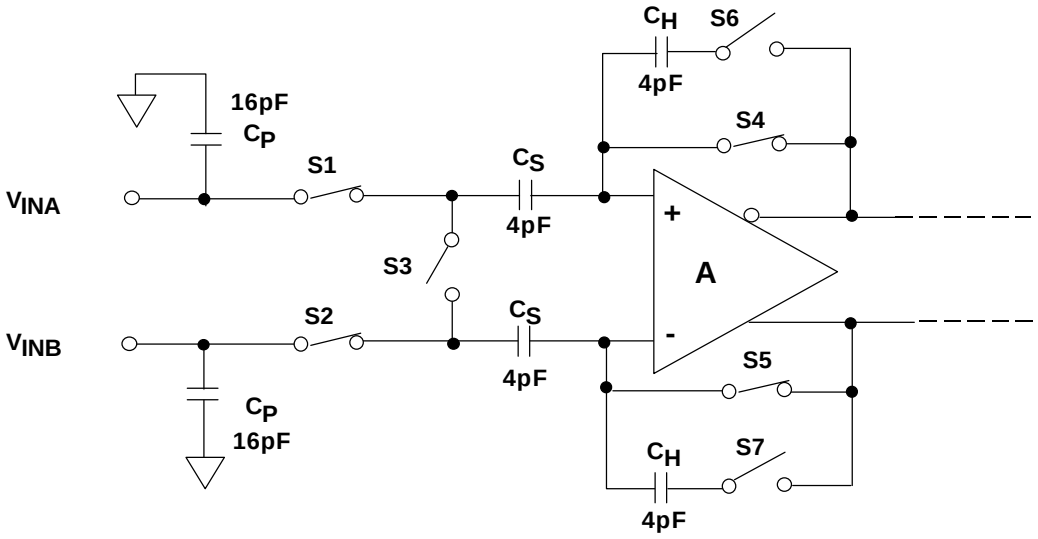
5.2

AD9220, AD9221, AD9223
CMOS 12-BIT ADCs KEY SPECIFICATIONS

- **Family Members:**
  AD9221 (1.25MSPS), AD9223 (3MSPS), AD9220 (10MSPS)
- **Power Dissipation: 60, 100, 250mW, Respectively**
- **FPBW: 25, 40, 60MHz, Respectively**
- **Effective Input Noise: 0.1LSB rms (Span = 5V)**
- **SINAD: 71dB**
- **SFDR: 88dBc**
- **On-Chip Reference**
- **Differential Non-Linearity: 0.3LSB**
- **Single +5V Supply**
- **28-Pin SOIC Package**

The input circuit of the AD9220/21/23-series of CMOS ADCs contains the differential sample-and-hold as shown in Figure 5.4. The switches are shown in the track mode. They open and close at the sampling frequency. The 16pF capacitors represent the effective capacitance of switches S1 and S2 plus the stray input capacitance. The C_S capacitors (4pF) are the sampling capacitors, and the C_H capacitors are the hold capacitors. Although the input circuit is completely differential, the ADC can be driven either single-ended or differential. Optimum SFDR, however, is obtained using a differential transformer drive.

SIMPLIFIED INPUT CIRCUIT OF AD922X ADC FAMILY



SWITCHES SHOWN IN TRACK MODE

In the track mode, the differential input voltage is applied to the C_S capacitors. When the circuit enters the hold mode, the voltage across the sampling capacitors is transferred to the C_H hold capacitors and buffered by the amplifier A. (The switches are controlled by the appropriate phases of the sampling clock). When the SHA returns to the track mode, the input source must charge or discharge the voltage stored on C_S to the new input voltage. This action of charging and discharging C_S, averaged over a period of time and for a given sampling frequency fs, makes the input impedance appear to have a benign resistive component. However, if this action is analyzed within a sampling period ($1/f_S$), the input impedance is dynamic, and hence certain precautions on the input drive source should be observed.

The resistive component to the input impedance can be computed by calculating the average charge that is drawn by C_H from the input drive source. It can be shown that if C_S is allowed to fully charge to the input voltage before switches S1 and S2 are opened that the average current into the input is the same as if there were a

resistor equal to $1/(C_S f_S)$ connected between the inputs. Since C_S is only a few picofarads, this resistive component is typically greater than several kΩ for an f_S = 10MSPS.

If one considers the SHA's input impedance over a sampling period, it appears as a dynamic load to the input drive source. When the SHA returns to the track mode, the input source should ideally provide the charging current through the R_{on} of switches S1 and S2 in an exponential manner. The requirement of exponential charging means that the source impedance should be both low and resistive up to and beyond the sampling frequency.

The output impedance of an op amp can be modeled as a series inductor and resistor. When a capacitive load is switched onto the output of the op amp, the output will momentarily change due to its effective high frequency output impedance. As the output recovers, ringing may occur. To remedy this situation, a series resistor can be inserted between the op amp and the SHA input. The optimum value of this resistor is dependent on several factors including the sampling frequency and the op amp selected, but in most applications, a 30 to 50Ω resistor is optimum.

The input voltage span of the AD922X-family is set by pin-strap options using the internal voltage reference (see Figure 5.5). The common-mode voltage can be set by either pin strap or applying the common-mode voltage to the VINB pin. Tradeoffs can be made between noise and distortion performance. Maximum input range allowable is 5V peak-to-peak, in which case, the common-mode input voltage must be one-half the supply voltage, or +2.5V. The minimum input range is 2V peak-to-peak, in which case the common-mode input voltage can be set from +1V to +4V. For best DC linearity and maximum signal-to-noise ratio, the ADC should be operated with an input signal of 5V peak-to-peak. However, for best high frequency noise and distortion performance, 2V peak-to-peak with a common-mode voltage of +2.5V is preferred. This is because the CMOS FET on-resistance is a minimum at this voltage, and the non-linearity caused by the signal-dependence of R_{on} (R_{on} modulation effect) is also minimal.

AD922X ADC INPUT VOLTAGE RANGE OPTIONS

SINGLE-ENDED INPUT

Input Signal Range (Volts)	Peak-to-Peak Signal (Volts)	Common-Mode Voltage (Volts)
0 to +2	2	+1
0 to +5	5	+2.5
+1.5 to +3.5	2	+2.5

DIFFERENTIAL INPUT

Input Signal Range	Peak-to-Peak Signal	Common-Mode Voltage

(Volts)	Differential (Volts)	(Volts)
+2 to +3	2	+2.5
+1.25 to +3.75	5	+2.5

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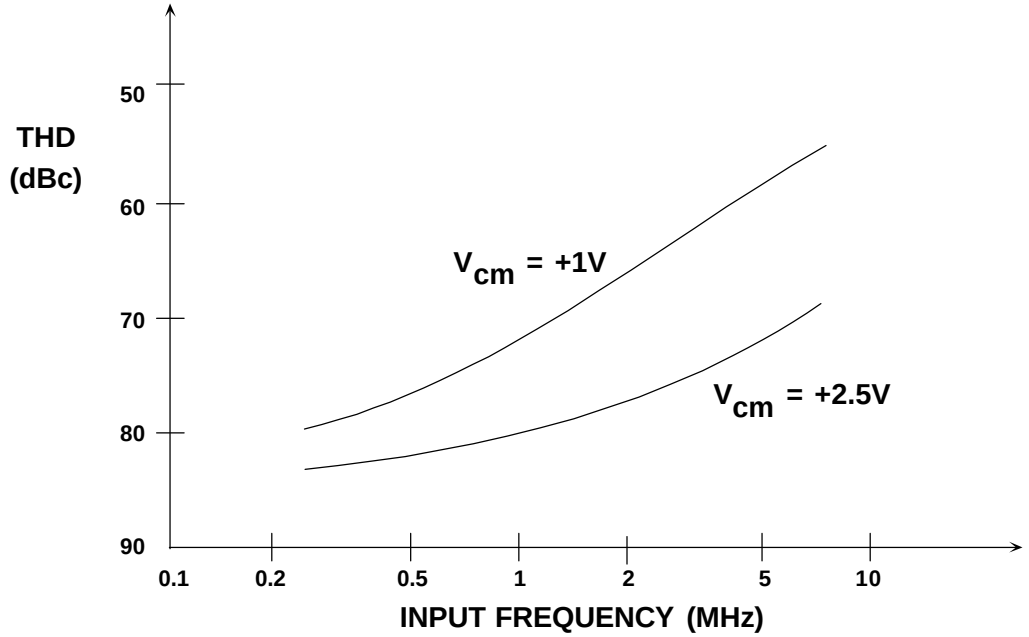
5.5

Figure 5.6 shows the THD performance of the AD9220 for a 2V peak-to-peak input signal span and common-mode input voltage of 2.5V and 1V. The data was taken with a single-ended drive. Note that the performance is significantly better for V_{cm} = +2.5V.

AD9220 THD VS. INPUT FREQUENCY: SINGLE-ENDED DRIVE 2V p-p INPUT, V_{cm} = +1V AND V_{cm} = +2.5V, f_S = 10MSPS



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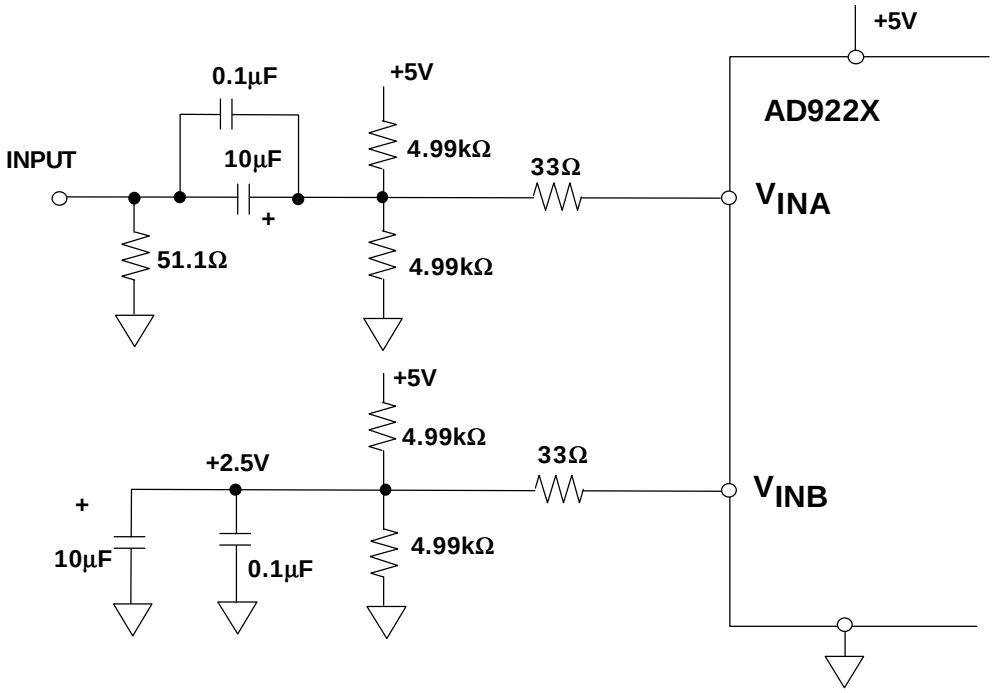
5.6

A simple single-ended circuit for AC coupling into the inputs of the AD9220-family is shown in Figure 5.7. Note that the common-mode input voltage is set for +2.5V by the 4.99kΩ resistors. The input impedance is also balanced for optimum distortion performance.

SINGLE-ENDED AC-COUPLED DRIVE CIRCUIT FOR AD922X ADC



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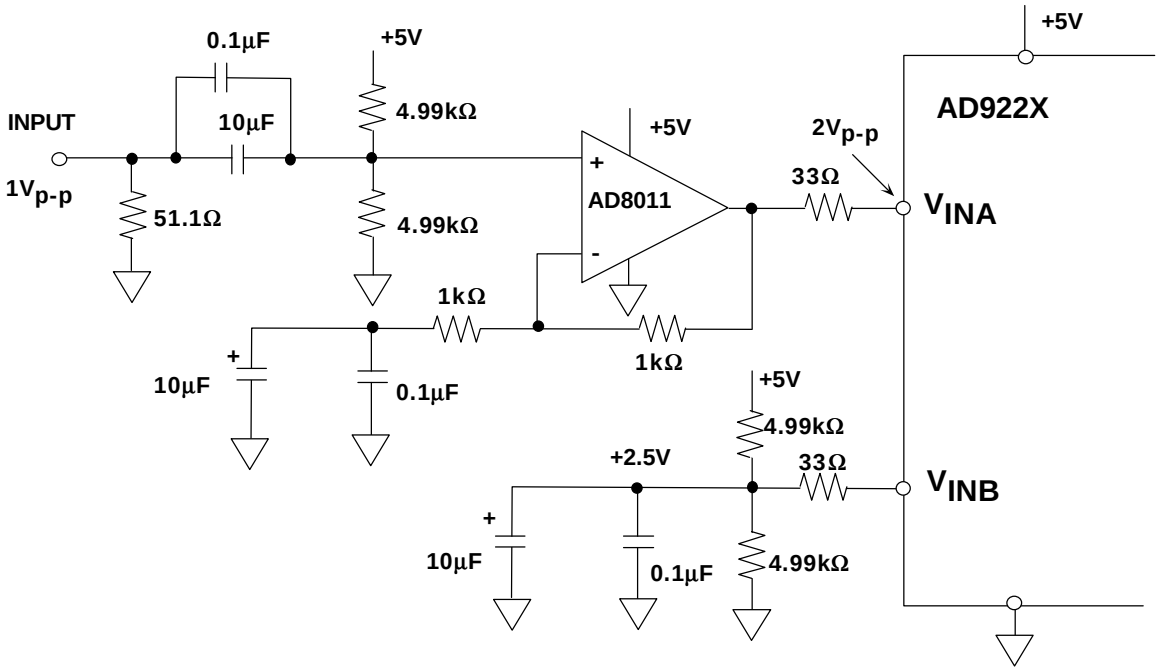
5.7

If the input to the ADC is coming from a long coaxial cable run, it may be desirable to buffer the transient currents at the ADC inputs from the cable to prevent problems resulting from reflections, especially if the cable is not source-terminated. The circuit shown in Figure 5.8 uses the low distortion AD8011 op amp as a buffer which can optionally provide signal gain. In all cases, the feedback resistor should be fixed at 1kΩ for best op amp performance, since the AD8011 is a current-feedback type. In this type of arrangement, care must be taken to observe the allowable input and output range of the op amp. The AD8011 input common-mode range (operating on a single +5V supply) is from +1.5 to +3.5V, and its output +1V to +4V. The ADC should be operated with a 2V peak-to-peak input range. The 33Ω series resistor is required to isolate the output of the AD8011 from the effective input capacitance of the ADC. The value was empirically determined to yield the best high-frequency SINAD.

BUFFERED AC-COUPLED INPUT DRIVE CIRCUIT FOR AD922X ADC



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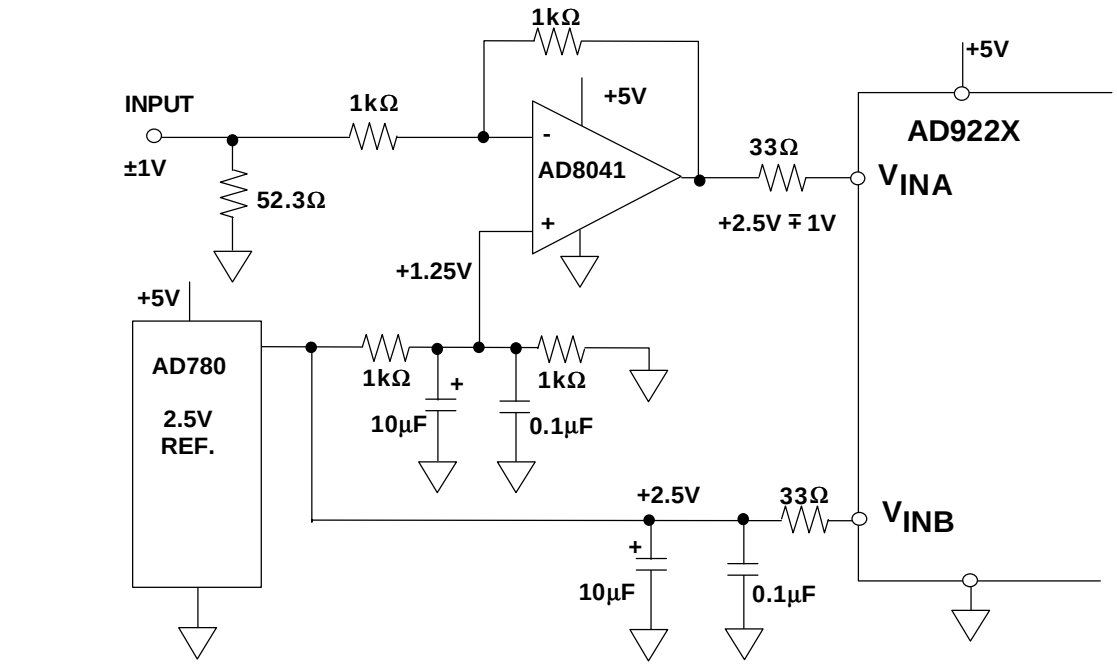
5.8

Direct coupling of ground-referenced signals using a single supply requires the use of an op amp with an acceptable common-mode input voltage, such as the AD8041 (input can go to 200mV below ground). The circuit shown in Figure 5.9 level shifts the ground-referenced bipolar input signal to a common-mode voltage of +2.5V at the ADC input. The common-mode bias voltage of +2.5V is developed directly from an AD780 reference, and the AD8041 common-mode voltage of +1.25V is derived with a simple divider.

DIRECT-COUPLED LEVEL SHIFTER FOR DRIVING AD922X ADC INPUT



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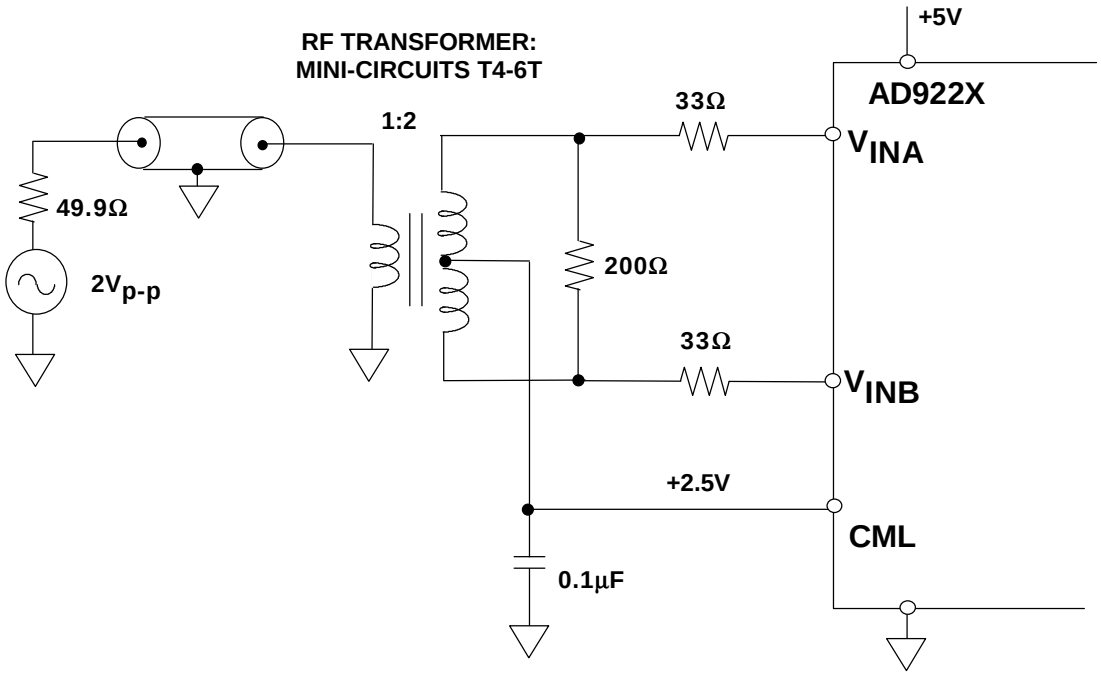
5.9

Transformer coupling provides the best CMR and the lowest distortion. Figure 5.10 shows the suggested circuit. The transformer is a Mini-Circuits RF transformer, model #T4-6T which has an impedance ratio of four (turns ratio of 2). The schematic assumes that the signal source has a 50Ω source impedance. The 1:4 impedance ratio requires the 200Ω secondary termination for optimum power transfer and VSWR. The Mini-Circuits T4-6T has a 1dB bandwidth from 100kHz to 100MHz. The center tap of the transformer provides a convenient means of level shifting the input signal to the optimum common-mode voltage. The AD922X CML pin is used to provide the +2.5 common-mode voltage.

TRANSFORMER COUPLING INTO AD922X ADC



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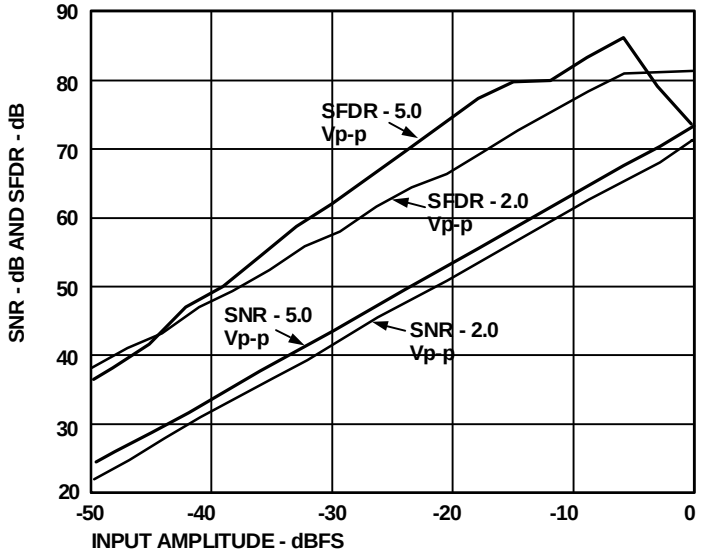
5.10

Transformers with other turns ratios may also be selected to optimize the performance for a given application. For example, a given input signal source or amplifier may realize an improvement in distortion performance at reduced output power levels and signal swings. Hence, selecting a transformer with a higher impedance ratio (i.e. Mini-Circuits #T16-6T with a 1:16 impedance ratio, turns ratio 1:4) effectively "steps up" the signal level thus reducing the driving requirements of the signal source.

Note the 33Ω series resistors inserted between the transformer secondary and the ADC input. These values were specifically selected to optimize both the SFDR and the SNR performance of the ADC. They also provide isolation from transients at the ADC inputs. Transients currents are approximately equal on the VINA and VINB inputs, so they are isolated from the primary winding of the transformer by the transformer's common-mode rejection.

Transformer coupling using a common-mode voltage of +2.5V provides the maximum SFDR when driving the AD922X-series. By driving the ADC differentially, even-order harmonics are reduced compared with the single-ended circuit. Figure 5.11 shows a plot of SFDR and SNR for the transformer-coupled differential drive circuit using 2V p-p and 5V p-p inputs and a common-mode voltage of +2.5V. Note that the SFDR is greater than 80dBc for input signals up to full scale with a 5MHz input signal.

AD9220 SFDR AND SNR FOR 5Vp-p AND 2Vp-p INPUT: V_{cm} = +2.5V, 5MHz INPUT, f_S = 10MSPS TRANSFORMER-COUPLED DIFFERENTIAL DRIVE



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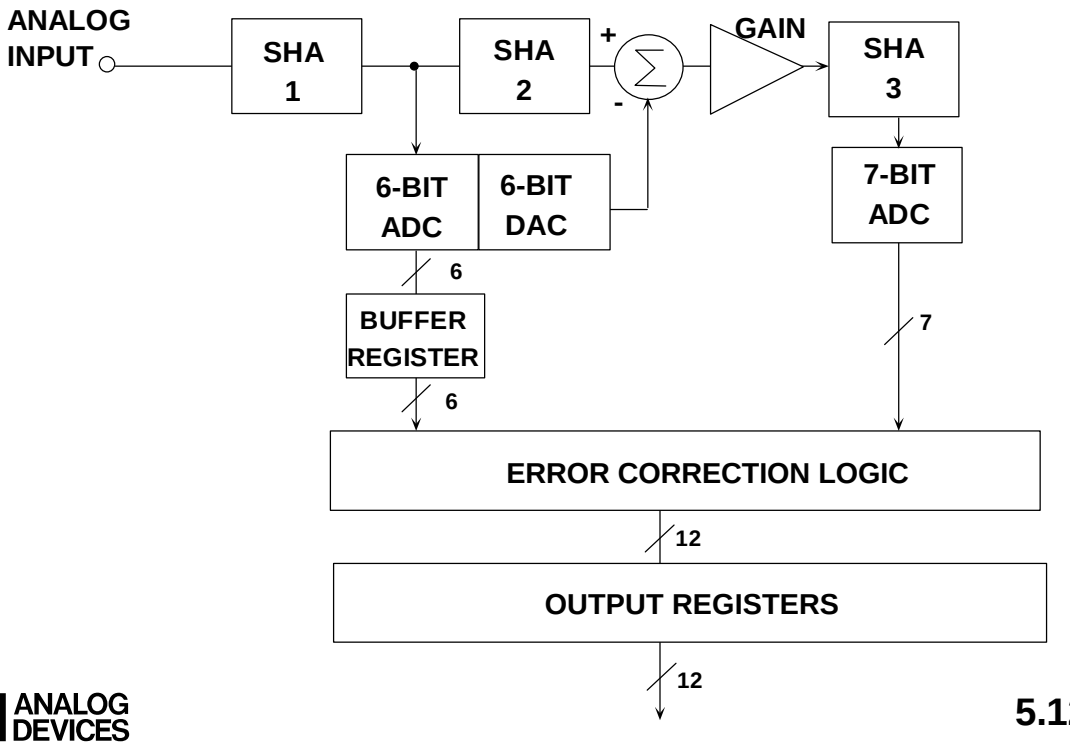
5.11

Figure 5.11 also shows differences between the SFDR and SNR performance for 2V p-p and 5V p-p inputs. Note that the SNR with a 5V p-p input is approximately 2dB to 3dB better than that for a 2V p-p input because of the additional dynamic range provided by the larger input range. Also, the SFDR performance using a 5V p-p input is 3 to 5dB better for signals between about –6dBFS and –36dBFS. This improvement in SNR and SFDR for the 5V p-p input range may be advantageous in systems which require more than 6dB headroom to minimize clipping of the ADC.

Driving Bipolar Input ADCs

Bipolar technology is typically used for extremely high performance ADCs with wide dynamic range and high sampling rates such as the AD9042. The AD9042 is a state-of-the-art 12-bit, 41MSPS two stage subranging ADC consisting of a 6-bit coarse ADC and a 7-bit residue ADC with one bit of overlap to correct for any DNL, INL, gain or offset errors of the coarse ADC, and offset errors in the residue path. A block diagram is shown in Figure 5.12 and key specifications in Figure 5.13. A proprietary gray-code architecture is used to implement the two internal ADCs. The gain alignments of the coarse and residue, likewise the subtraction DAC, rely on the statistical matching of the devices on the process. As a result, 12-bit integral and differential linearity is obtained without laser trim. The internal DAC consists of 126 interdigitated current sources. Also on the DAC reference, there are an additional 20 interdigitated current sources to set the coarse gain, residue gain, and full scale gain. The interdigitization removes the requirement for laser trim. The AD9042 is fabricated on a high speed dielectrically isolated complementary bipolar process. The total power dissipation is only 575mW when operating on a single +5V supply.

AD9042 12-BIT, 41MSPS ADC BLOCK DIAGRAM



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5.12

AD9042 12-BIT, 41MSPS ADC KEY SPECIFICATIONS

- **Input Range: 1V peak-to-peak, V_{cm} = +2.4V**
- **Input Impedance: 250Ω to V_{cm}**
- **Effective Input Noise: 0.33LSBs rms**
- **SFDR at 20MHz Input: 80dB**
- **SINAD at 20MHz Input = 66dB**
- **Digital Outputs: TTL Compatible**
- **Power Supply: Single +5V**
- **Power Dissipation: 575mW**
- **Fabricated on High Speed Dielectrically Isolated Complementary Bipolar Process**

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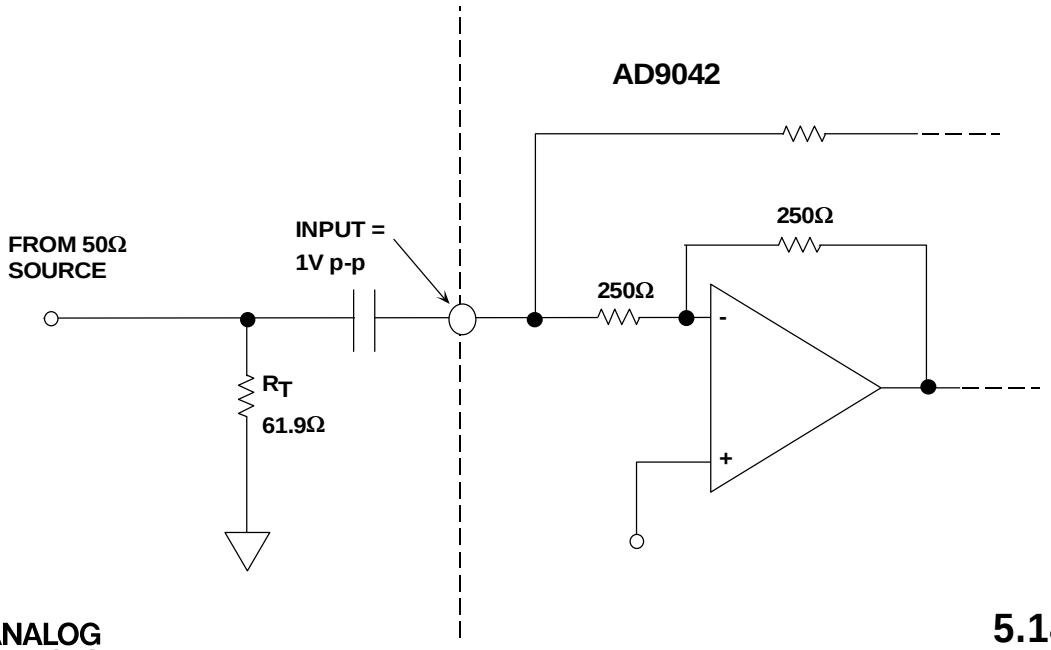
5.13

The outstanding performance of the AD9042 is partly due to the use of differential techniques throughout the device. The low distortion input amplifier converts the single-ended input signal into a differential one. If maximum SFDR performance is

desired, the signal source should be coupled directly into the input of the AD9042 without using a buffer amplifier. Figure 5.14 shows a method using capacitive coupling. Transformer coupling can also be used if desired.

INPUT STRUCTURE OF AD9042 ADC IS DESIGNED TO BE DRIVEN DIRECTLY FROM 50Ω SOURCE FOR BEST SFDR



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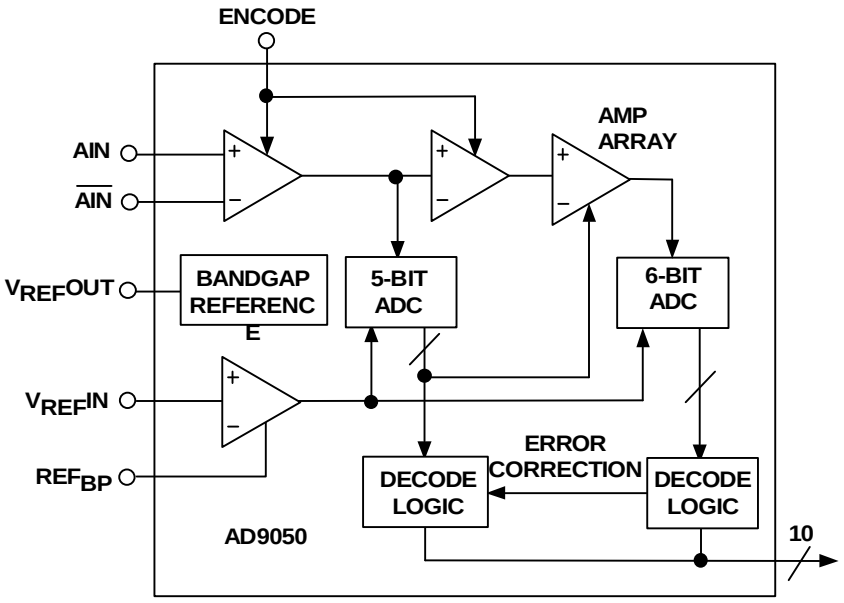
5.14

The AD9050 is a 10-bit, 40MSPS single supply ADC designed for wide dynamic range applications such as ultrasound, instrumentation, digital communications, and professional video. Like the AD9042, it is fabricated on a high speed complementary bipolar process. A block diagram of the AD9050 (Figure 5.15) illustrates the two-step subranging architecture, and key specifications are summarized in Figure 5.16.

AD9050 10-BIT, 40MSPS SINGLE SUPPLY ADC



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5.15

AD9050 10-BIT, 40MSPS ADC KEY SPECIFICATIONS

- 10-Bits, 40MSPS, Single +5V Supply
- Selectable Digital Supply: +5V, or +3V
- Low Power: 300mW on BiCMOS Process
- On-Chip SHA and +2.5V reference
- 56dB S/(N+D), 9 Effective Bits, with 10.3MHz Input Signal
- No input transients, Input Impedance 5kΩ, 5pF
- Input Range +3.3V ±0.5V Single-Ended or Differential
- 28-pin SOIC / SSOP Packages
- Ideal for Digital Beamforming Ultrasound Systems

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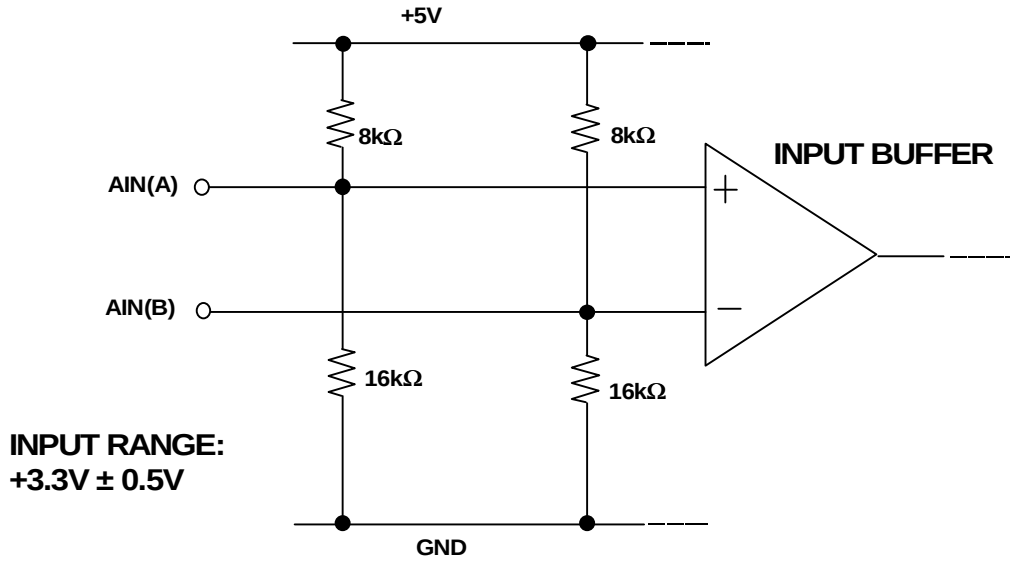
5.16

The analog input circuit of the AD9050 (see Figure 5.17) is differential, but can be driven either single-endedly or differentially with equal performance. The input signal range of the AD9050 is ±0.5V centered around a common-mode voltage of

+3.3V, which makes single supply op amp selection more difficult since the amplifier has to drive +3.8V peak signals with low distortion.

AD9050 SIMPLIFIED INPUT CIRCUIT



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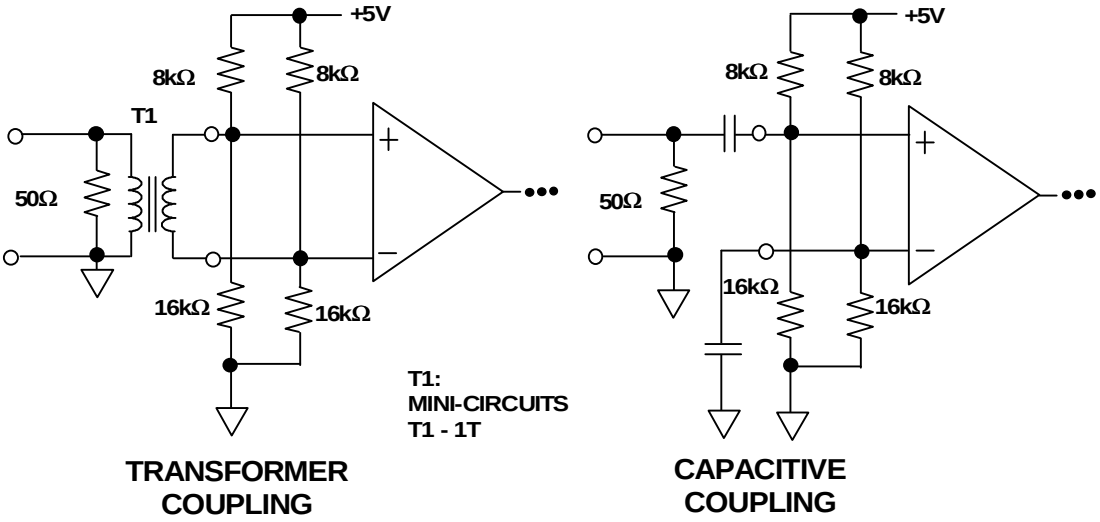
5.17

The input circuit of the AD9050 is a relatively benign and constant 5kΩ in parallel with approximately 5pF. Because of its well-behaved input, the AD9050 can be driven directly from 50, 75, or 100Ω sources without the need for a low-distortion buffer amplifier. In ultrasound applications, it is normal to AC couple the signal (generally between 1MHz and 15MHz) into the AD9050 differential inputs using a wideband transformer as shown in Figure 5.18. The Mini-Circuits T1-1T transformer has a 1dB bandwidth from 200kHz to 80MHz. Signal-to-noise plus distortion (SINAD) values of 57dB (9.2 ENOB) are typical for a 10MHz input signal. If the input signal comes directly from a 50, 75, or 100Ω single-ended source, capacitive coupling as shown in Figure 5.18 can be used.

AC COUPLING INTO THE INPUT OF THE AD9050 ADC



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5.18

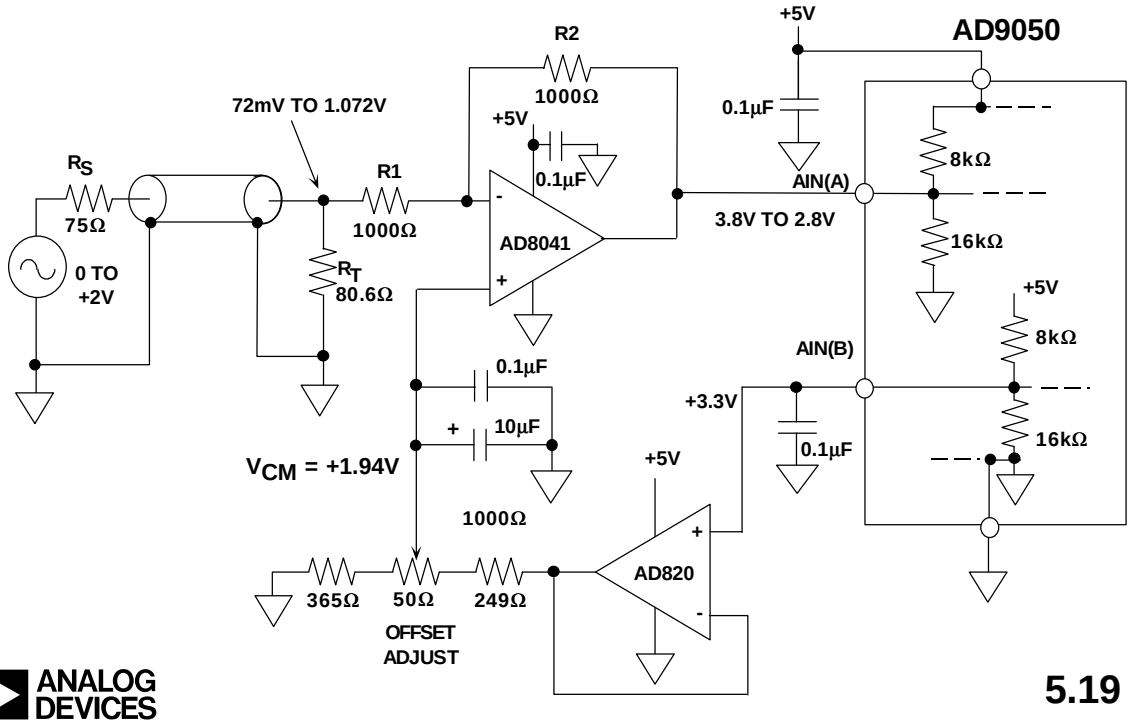
If DC coupling is required, the AD8041 (zero-volt in, rail-to-rail output) op amp can be used as a low distortion driver. The circuit shown in Figure 5.19 level shifts a ground-referenced video signal to fit the +3.3V ±0.5V input range of the AD9050. The source is a ground-referenced 0 to +2V signal which is series-terminated in 75Ω. The termination resistor, R_T, is chosen such that the parallel combination of R_T and R1 is 75Ω. The AD8041 op amp is configured for a signal gain of –1. Assuming that the video source is at zero volts, the corresponding ADC input voltage should be +3.8V. The common-mode voltage, V_{cm}, is determined from the following equation:

$$V_{cm} = 3.8\left(\frac{R_S||R_T + R1}{R_S||R_T + R1 + R2}\right) = 3.8\left(\frac{38.8 + 1000}{38.8 + 1000 + 1000}\right) = 1.94V$$

The common-mode voltage, V_{cm}, is derived from the common-mode voltage at the inverting input of the AD9050. The +3.3V is buffered by the AD820 single-supply FET-input op amp. A divider network generates the required +1.94V for the AD8011, and a potentiometer provides offset adjustment capability.

The AD8041 voltage feedback op amp was chosen because of its low power (26mW), wide bandwidth (160MHz), and low distortion (–69dBc at 10MHz). It is fully specified for both ±5V,+5V, and +3V operation. When operating on a single +5V supply, the input common-mode range is –0.2V to +4V, and the output swing is +0.1V to +4.9V. Distortion performance of the entire circuit including the ADC is better than –60dBc for an input frequency of 10MHz and a sampling rate of 40MSPS.

DC-COUPLED SINGLE-SUPPLY DRIVE CIRCUIT FOR AD9050 10-BIT, 40MSPS ADC USING AD8041 OP AMP



ANALOG DEVICES

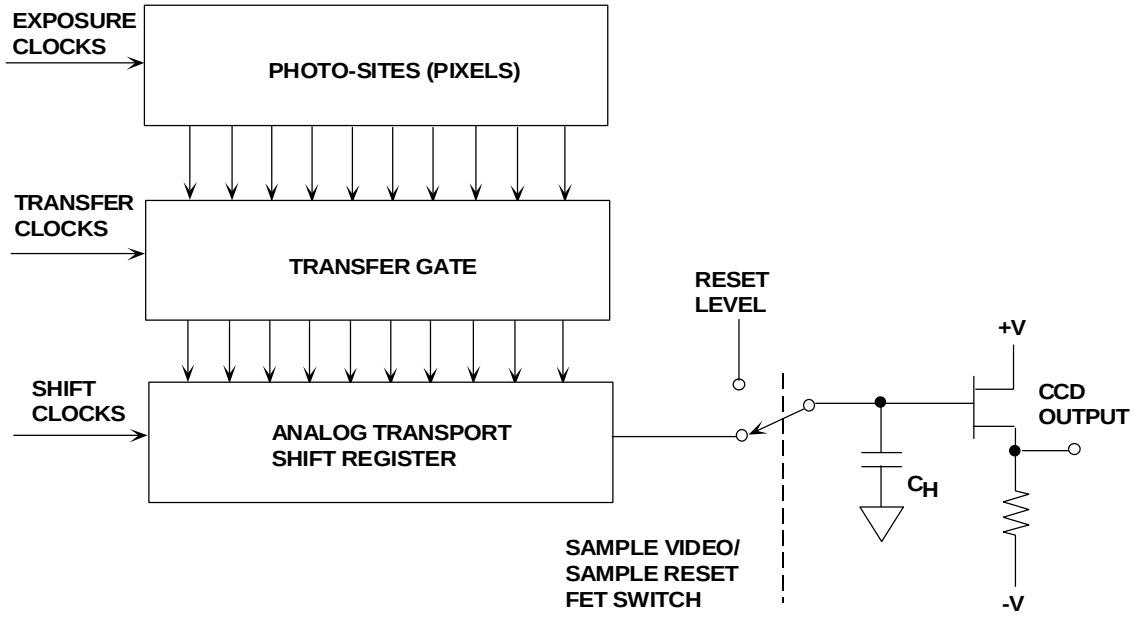
5.19

APPLICATIONS OF HIGH SPEED ADCS IN CCD IMAGING

Charge coupled devices (CCDs) contains a large number of small photocells called photosites or pixels which are arranged either in a single row (linear arrays) or in a matrix (area arrays). CCD area arrays are commonly used in video applications, while linear arrays are used in facsimile machines, graphics scanners, and pattern recognition equipment.

The linear CCD array consists of a row of image sensor elements (photosites, or pixels) which are illuminated by light from the object or document. During one exposure period each photosite acquires an amount of charge which is proportional to its illumination. These photosite charge packets are subsequently switched simultaneously via transfer gates to an analog shift register. The charge packets on this shift register are clocked serially to a charge detector (storage capacitor) and buffer amplifier (source follower) which convert them into a string of photo-dependent output voltage levels (see Figure 5.20). While the charge packets from one exposure are being clocked out to the charge detector, another exposure is underway. The analog shift register typically operates at frequencies between 1 and 10MHz.

LINEAR CCD ARRAY



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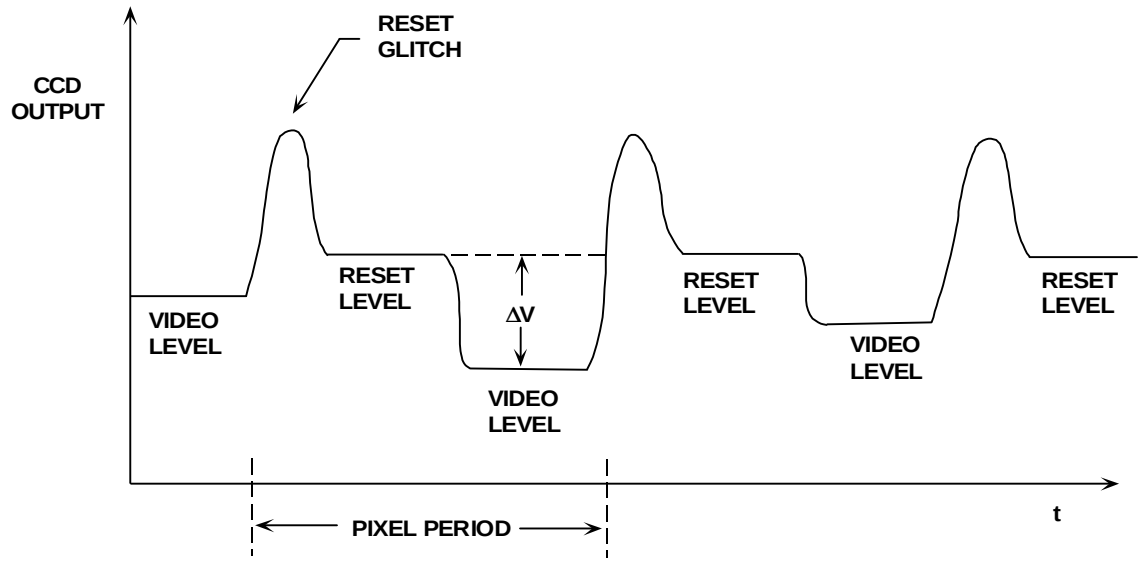
5.20

The charge detector readout cycle begins with a reset pulse which causes a FET switch to set the output storage capacitor to a known voltage. Switching the FET causes capacitive feedthrough which results in a reset glitch at the output as shown in Figure 5.21. The switch is then opened, isolating the capacitor, and the charge from the last pixel is dumped onto the capacitor causing a voltage change. The difference between the reset voltage and the final voltage (video level) shown in Figure 5.21 represents the amount of charge in the pixel. CCD charges may be as

low as 10 electrons, and a typical CCD output sensitivity is 0.6µV/electron. Most CCDs have a saturation output voltage of about 1V (see Reference 1).

CCD OUTPUT WAVEFORM

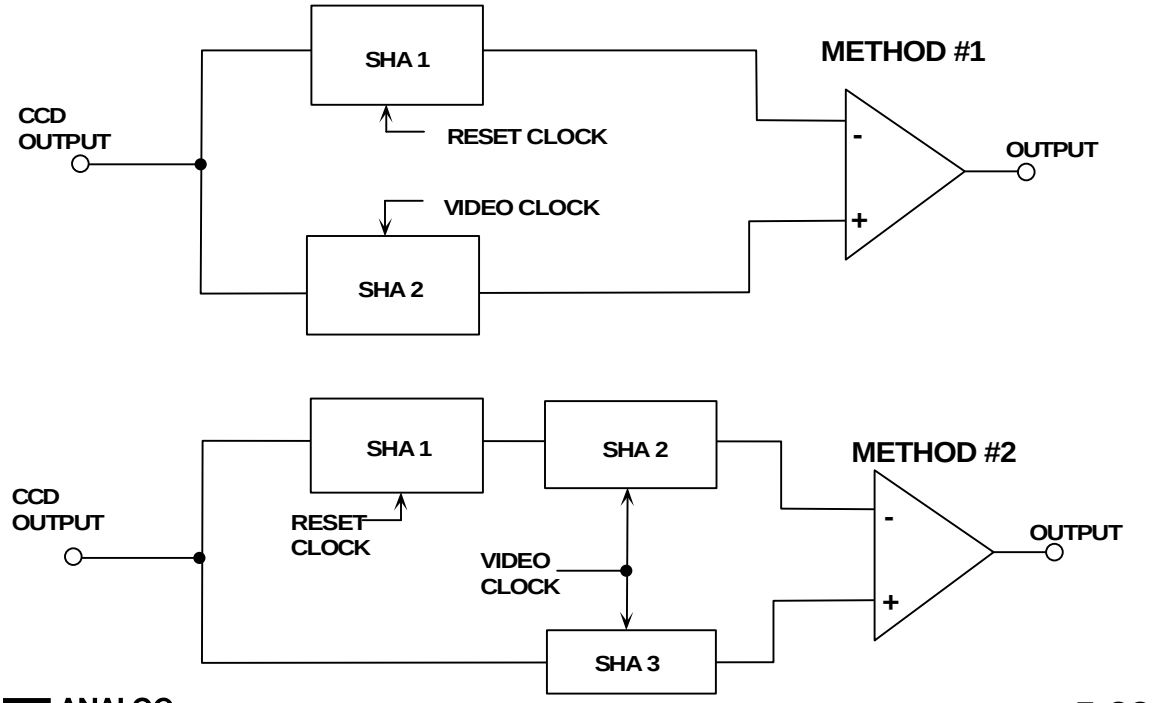


Since CCDs are generally fabricated on MOS processes, they have limited capability to perform on-chip signal conditioning. Therefore, the CCD output is generally processed by external conditioning circuits.

CCD output voltages are small and quite often buried in noise. The largest source of noise is the thermal noise in the resistance of the FET reset switch. This noise may have a typical value of 100 to 300 electrons rms (approximately 60 to 180mV rms). This noise occurs as a *sample-to-sample* variation in the CCD output level and is common to both the reset level and the video level for a given pixel period. A technique called *correlated double sampling* (CDS) is often used to reduce the effect of this noise. Figure 5.22 shows two circuit implementations of the CDS scheme. In the top circuit, the CCD output drives both SHAs. At the end of the reset interval, SHA1 holds the reset voltage level. At the end of the video interval, SHA2 holds the video level. The SHA outputs are applied to a difference amplifier which subtracts one from the other. In this scheme, there is only a short interval during which both SHA outputs are stable, and their difference represents ΔV, so the difference amplifier must settle quickly to the desired resolution.

Another arrangement is shown in the bottom half of Figure 5.22, which uses three SHAs and allows either for faster operation or more time for the difference amplifier to settle. In this circuit, SHA1 holds the reset level so that it occurs simultaneously with the video level at the input to SHA2 and SHA3. When the video clock is applied simultaneously to SHA2 and SHA3, the input to SHA2 is the reset level, and the input to SHA3 the video level. This arrangement allows the entire pixel period (less the acquisition time of SHA2 and SHA3) for the difference amplifier to settle.

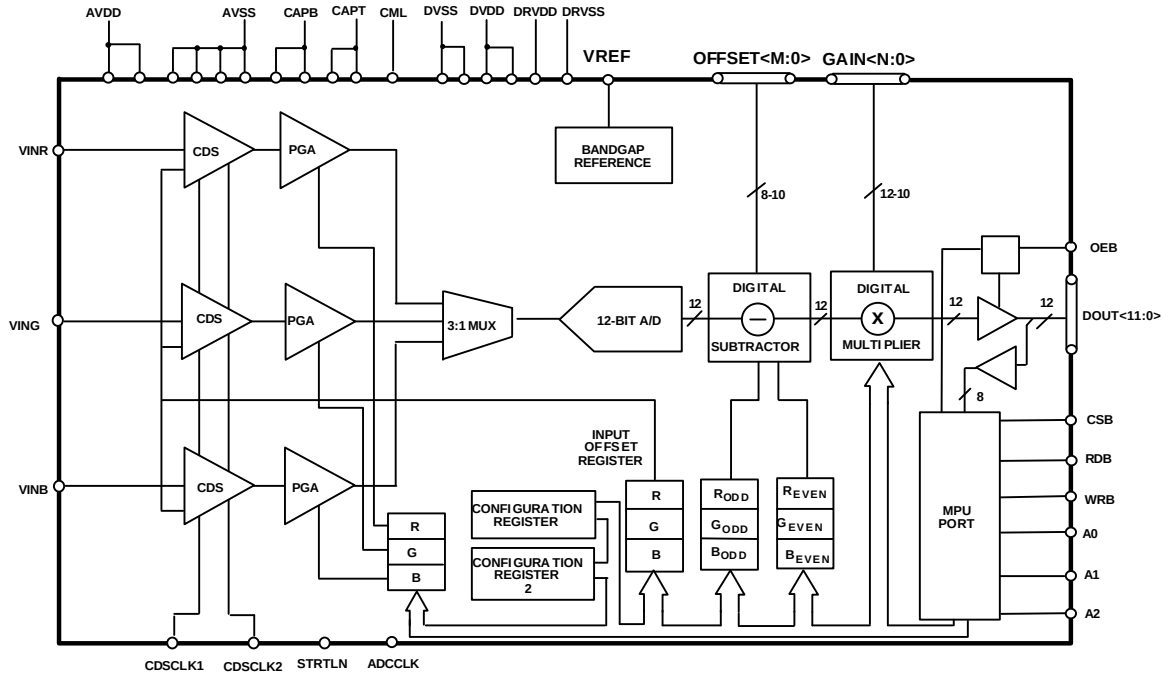
CORRELATED DOUBLE SAMPLING (CDS) MINIMIZES SWITCHING NOISE AT OUTPUT



ANALOG DEVICES

5.22

The AD9807 is a complete CCD imaging decoder and signal processor on a single chip (see Figure 5.23). The input of the AD9807 allows direct AC coupling of the CCD outputs and includes all the circuitry to perform three-channel correlated double sampling (CDS) and programmable gain adjustment (1X to 4X in 16 increments) of the CCD output. A 12-bit ADC quantizes the analog signal (maximum sampling frequency 6MSPS). After digitization, the on-board DSP allows pixel rate offset and gain correction. The DSP also corrects odd/even CCD register imbalance errors. A parallel control bus provides a simple interface to 8-bit microcontrollers. The device operates on a single +5V supply and dissipates 500mW. The AD9807 comes in a space saving 64-pin plastic quad flat pack (PQFP). By disabling the CDS, the AD9807 is also suitable for non-CCD applications that do not require CDS. The AD9807 is also offered in a pin-compatible 10-bit version, the AD9805, to allow upgradeability and simplify design issues across different scanner models.



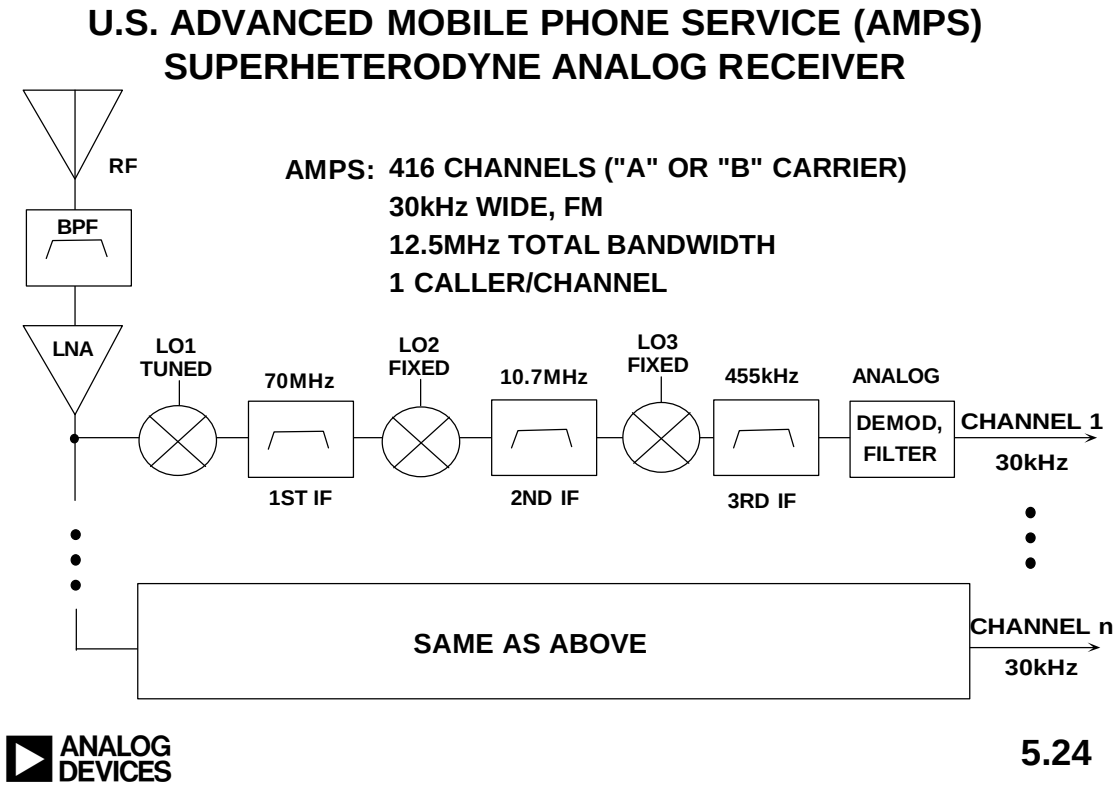
ANALOG DEVICES

5.23

HIGH SPEED ADC APPLICATIONS IN DIGITAL RECEIVERS

Introduction

Consider the analog superheterodyne receiver invented in 1917 by Major Edwin H. Armstrong (see Figure 5.24). This architecture represented a significant improvement over single-stage direct conversion (homodyne) receivers which had previously been constructed using tuned RF amplifiers, a single detector, and an audio gain stage. A significant advantage of the superhetrodyne receiver is that it is much easier and more economical to have the gain and selectivity of a receiver at fixed intermediate frequencies (IF) than to have the gain and frequency-selective circuits "tune" over a band of frequencies.



The frequencies shown in Figure 5.24 correspond to the AMPS (Advanced Mobile Phone Service) analog cellular phone system currently used in the U.S. The receiver is designed for AMPS signals at 900MHz RF. The signal bandwidth for the "A" or "B" carriers serving a particular geographical area is 12.5MHz (416 channels, each 30kHz wide). The receiver shown uses triple conversion, with a first IF frequency of 70MHz and a second IF of 10.7MHz, and a third of 455kHz. The image frequency at the receiver input is separated from the RF carrier frequency by an amount equal to twice the first IF frequency (illustrating the point that using relatively high first IF frequencies makes the design of the image rejection filter easier).

The output of the third IF stage is demodulated using analog techniques (discriminators, envelope detectors, synchronous detectors, etc.). In the case of AMPS the modulation is FM. An important point to notice about the above scheme

is that there is *one receiver required per channel*, and only the antenna, prefilter, and LNA can be shared.

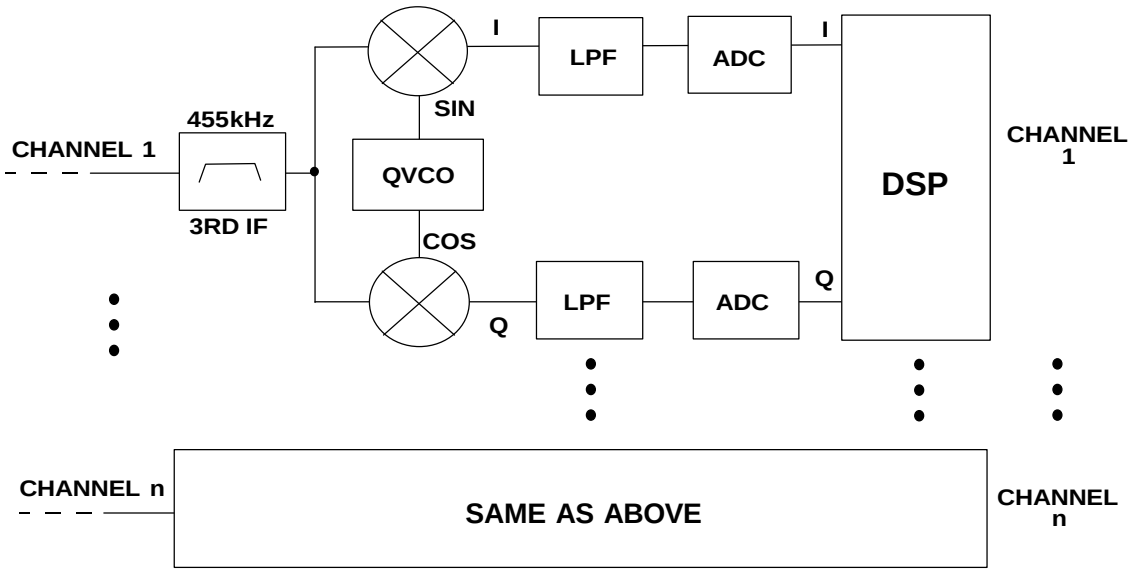
It should be noted that in to make the receiver diagrams more manageable, the interstage amplifiers are not shown. They are, however, an important part of the receiver, and the reader should be aware that they must be present.

Receiver design is a complicated art, and there are many tradeoffs that can be made between IF frequencies, single-conversion vs. double-conversion or triple conversion, filter cost and complexity at each stage in the receiver, demodulation schemes, etc. There are many excellent references on the subject, and the purpose of this section is only to acquaint the design engineer with some of the emerging architectures, especially in the application of digital techniques in the design of advanced communications receivers.

A Receiver Using Digital Processing at Baseband

With the availability of high performance high speed ADCs and DSPs (such as ADSP-2181 and the ADSP-21062), it is now becoming common practice to use digital techniques in at least part of the receive and transmit path, and various chipsets are available from Analog Devices to perform these functions for GSM and other cellular standards. This is illustrated in Figure 5.25 where the output of the last IF stage is converted into a baseband in-phase (I) and quadrature (Q) signal using a quadrature demodulator. The I and Q signals are then digitized by two ADCs. The DSPs then perform the additional signal processing. The signal can then be converted into analog format using a DAC, or it can be processed, mixed with other signals, upconverted, and retransmitted.

DIGITAL RECEIVER USING BASEBAND SAMPLING AND DIGITAL PROCESSING



ANALOG DEVICES

5.25

At this point, we should make it clear that *a digital receiver is not the same thing as digital modulation*. In fact, a digital receiver will do an excellent job of receiving an analog signal such as AM or FM. Digital receivers can be used to receive any type of modulation standard including analog (AM, FM) or digital (QPSK, QAM, FSK, GMSK, etc.). Furthermore, since the core of a digital radio is its digital signal processor (DSP), the same receiver can be used for both analog and digitally modulated signals (simultaneously if necessary), assuming that the RF and IF hardware in front of the DSP is properly designed. Since it is software that determines the characteristics of the radio, changing the software changes the radio. For this reason, digital receivers are often referred to as *software radios*.

The fact that a radio is software programmable offers many benefits. A radio manufacturer can design a generic radio in hardware. As interface standards change (as from FM to CDMA or TDMA), the manufacturer is able to make timely design changes to the radio by reprogramming the DSP. From a user or service-providers point of view, the software radio can be upgraded by loading the new software at a small cost, while retaining all of the initial hardware investment. Additionally, the receiver can be tailored for custom applications at very low cost, since only software costs are involved.

A digital receiver performs the same function as an analog one with one difference; some of the analog functions have been replaced with their digital equivalent. The main difference between Figure 5.24 and Figure 5.25 is that the FM discriminator in the analog radio has been replaced with two ADCs and a DSP. While this is a very simple example, it shows the fundamental beginnings of a digital, or *software* radio.

An added benefit of using digital techniques is that some of the filtering in the radio is now performed digitally. This eliminates the requirement of tight tolerances and matching for frequency-sensitive components such as inductors and capacitors. In addition, since filtering is performed within the DSP, the filter characteristics can be implemented in software instead of costly and sensitive SAW, ceramic, or crystal filters. In fact, many filters can be synthesized digitally that could never be implemented in a strictly analog receiver.

This simple example is only the beginning. With current technology, much more of the receiver can be implemented in digital form. There are numerous advantages to moving the digital portion of the radio closer to the antenna. In fact, placing the ADC at the output of the RF section and performing direct RF sampling might seem attractive, but does have some serious drawbacks, particularly in terms of selectivity and out-of-band (image) rejection. However, the concept makes clear one key advantage of software radios: they are programmable and require little or no component selection or adjustments to attain the required receiver performance.

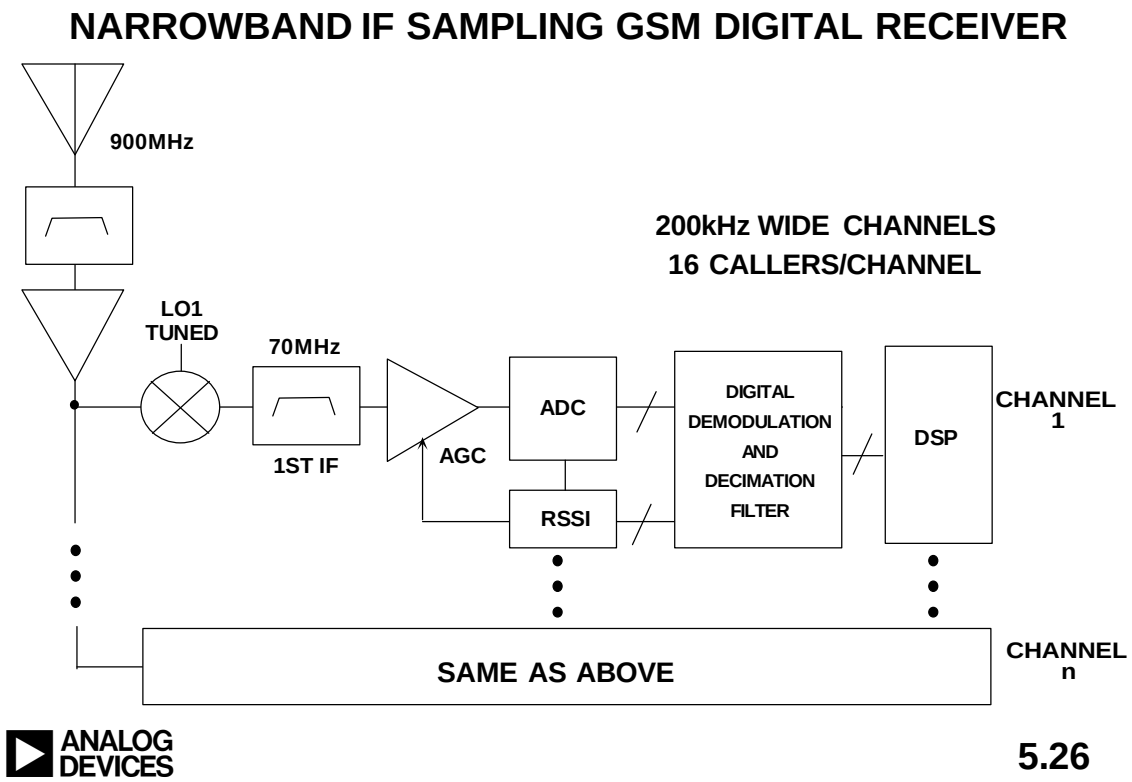
Narrowband IF-Sampling Digital Receivers

A reasonable compromise in many digital receivers is to convert the signal to digital form at the output of the first or the second IF stage. This allows for out-of-band signals to be filtered before reaching the ADC. It also allows for some automatic gain control (AGC) in the analog stage ahead of the ADC to reduce the possibility of in-band signals overdriving the ADC and allows for maximum signal gain prior to the A/D conversion. This relieves some of the dynamic range requirements on the ADC.

Additionally, IF sampling and digital receiver technology reduce costs by elimination of further IF stages (mixers, filters, and amplifiers) and adds flexibility by the replacement of fixed analog filter components with programmable digital ones.

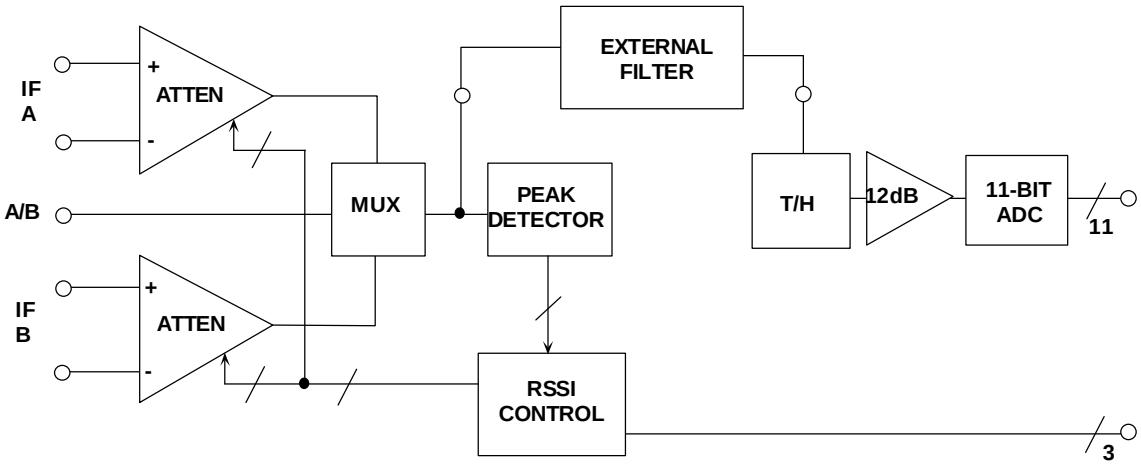
In analyzing an analog receiver design, much of the signal gain is after the first IF stage. This prevents front-end overdrive due to out-of-band signals or strong in-band signals. However, in an IF sampling digital receiver, all of the gain is in the front end, and great care must be taken to prevent in-band and out-of-band signals from saturating the ADC, which results in excessive distortion. Therefore, a method of attenuation must be provided when large in-band signals occur. While additional signal gain can be obtained digitally after the ADC, there are certain restrictions. Gain provided in the analog domain improves the SNR of the signal and only reduces the performance to the degree that the noise figure (NF) degrades noise performance.

Figure 5.26 shows a detailed IF sampling digital receiver for the GSM system . The receiver has RF gain, automatic gain control (AGC), a high performance ADC, digital demodulator/filter, and a DSP.



The heart of the system is the AD6600 dual channel, gain ranging 11-bit, 20MSPS ADC with RSSI (Received Signal Strength Indicator) and the AD6620 dual channel decimating receiver. A detailed block diagram of the AD6600 is shown in Figure 5.27 and key specifications in Figure 5.28.

AD6600 DUAL CHANNEL GAIN RANGING ADC WITH RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)



ANALOG DEVICES

5.27

AD6600 KEY SPECIFICATIONS

- **Dual Input, 11-bit, 20MSPS ADC Plus 3-bits RSSI**
- **Dynamic Range > 100dB**
  - **11-bit ADC → 62dB**
  - **3-bits RSSI → 30dB (5 levels, 6dB / level)**
  - **Process Gain → 12dB (6.5MSPS Sampling, 200kHz Channel)**
- **On-Chip Reference and Timing**
- **Single +5V Supply, 400mW**
- **44-pin TQFP Package**
- **Optimum Design for Narrowband Digital Receivers with IF Frequencies to 250MHz**

ANALOG DEVICES

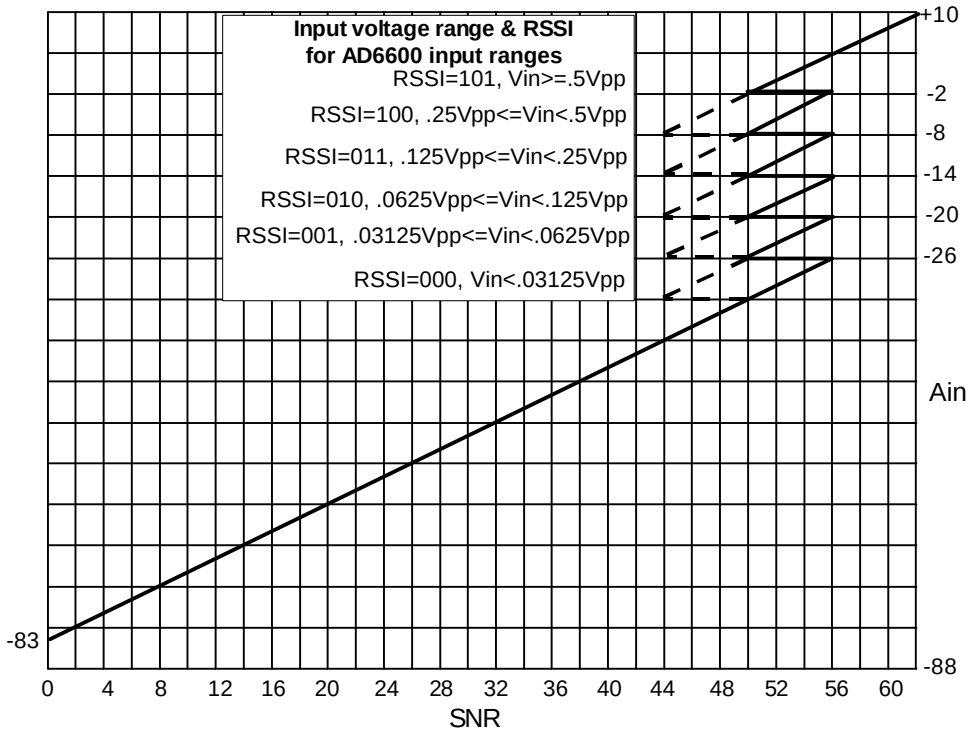
5.28

The AD6600 is a mixed signal chip that directly samples narrow band signals at IF frequencies up to 250MHz. The device includes an 11-bit, 20MSPS ADC, input attenuators, automatic gain ranging circuitry, a 450MHz bandwidth track-and-hold,

digital RSSI outputs, references, and control circuitry. The device accepts two inputs (for use with diversity antennas) which are multiplexed to the single ADC.

The AD6600 provides greater than 92dB dynamic range from the ADC and the auto gain-ranging/RSSI circuits. The gain range is 36dB in 6dB increments (controlled by a 3-bit word from the RSSI circuit). This sets the smallest input range at 31mV peak-to-peak, and the largest at 2V peak-to-peak. SFDR is 70dBc @ 100MHz and 53dBc @ 250MHz. Channel isolation is 70dB @ 100MHz and 60dB @ 250MHz. The SNR performance of the AD6600 is shown in Figure 5.29. The dynamic range of the AD6600 is greater than the minimum GSM specification of 91dB.

AD6600 INPUT VS. SNR



ANALOG DEVICES

5.29

The analog input to the AD6600 consists of two parallel attenuator stages followed by an output selection multiplexer. The attenuation levels can be set either by the on-chip automatic RSSI circuit (synchronous peak detector) or can be set digitally with external logic. The ADC T/H input can also be accessed directly by by-passing the front-end attenuators.

An external analog filter is required between the attenuator output and the track-and-hold input of the ADC section. This filter may be either a lowpass or a bandpass depending on the system architecture. Since the input bandwidth of the ADC is 450MHz, the filter minimizes the wideband noise entering the track-and-hold. The bandwidth of the filter should be set to allow sufficient settling time (1/2 the sampling period) during the RSSI peak detection period.

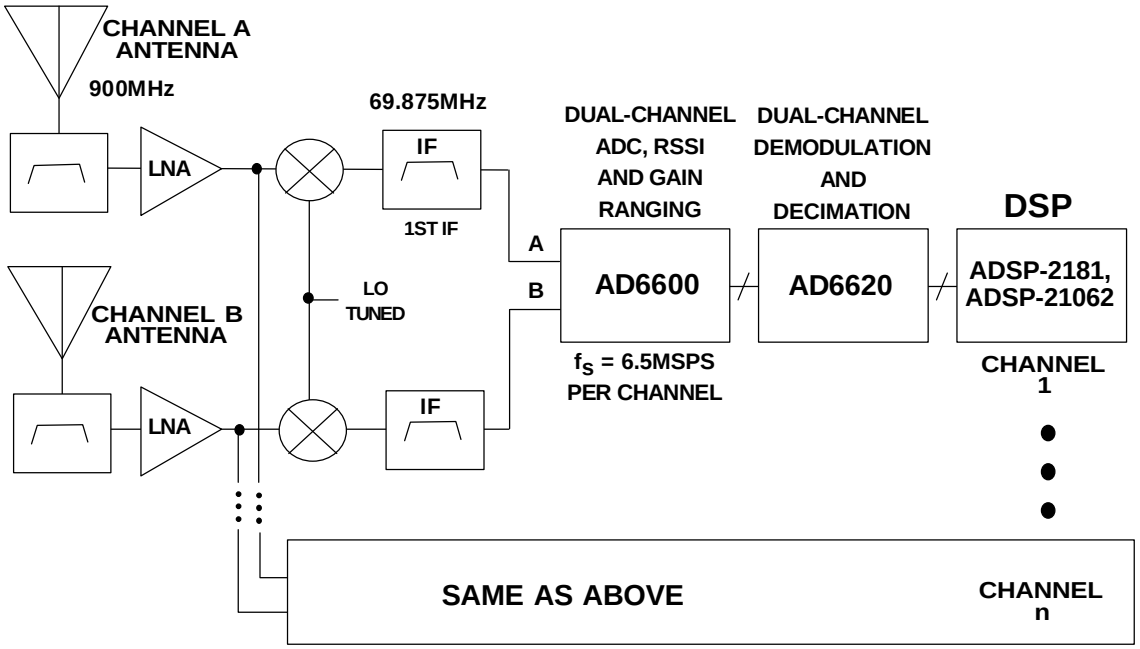
The ADC is based on the high dynamic range AD9042 architecture covered previously. The ADC input is designed to take advantage of the excellent small-signal linearity of the track-and-hold. Therefore, the full scale input to the ADC section is only 50mV peak-to-peak. The track-and-hold is followed by a gain block with a 6dB gain-select to increase the signal level for digitization by the 11-bit ADC. This amplifier only requires enough bandwidth to accurately settle to the next value during the sampling period (77ns for f_S = 13MSPS). Because of its reduced bandwidth, any high frequency track-and-hold feed through is also minimized.

The RSSI peak detector function consists of a bank of 5 high speed comparators with separate reference inputs. Each reference input is 6dB lower than the previous one. Each comparator has 6dB of built-in hysteresis to eliminate level uncertainty at the threshold points. Once one of the comparators is tripped, it stays in that state until it is reset by the negative-going edge of the sampling clock. The 5 comparator outputs are decoded into a 3-bit word that is used to select the proper input attenuation.

The RSSI follows the IF signal one clock cycle before the conversion is made. During this time period, the RSSI looks for the signal peaks. Prior to digitization, the RSSI word selects the correct attenuator factor to prevent the ADC from over-ranging on the following conversion cycle. The peak signal is set 6dB below the full scale range of the 11-bit ADC. The RSSI word can be read via the RSSI pins. The 11-bit ADC output functions as the mantissa, while the RSSI word is the exponent, and the combination forms a floating point number.

The AD6600 is ideal for use in a GSM narrowband basestation. Figure 5.30 shows a block diagram of the fundamental receiver. Two separate antennas and RF sections are used (this is often called *diversity*) to reduce the signal strength variations due to multipath effects. The IF output (approximately 70MHz) of each channel is digitized by the AD6600 at a sampling rate of 6.5MSPS (one-half the master GSM clock frequency of 13MHz). The two antennas need only be separated by a few feet to provide the required signal strength diversity (the wavelength of a 900MHz signal is about 1 foot). The DSP portion of the receiver selects the channel which has the largest signal amplitude.

NARROWBAND GSM BASESTATION WITH DIVERSITY



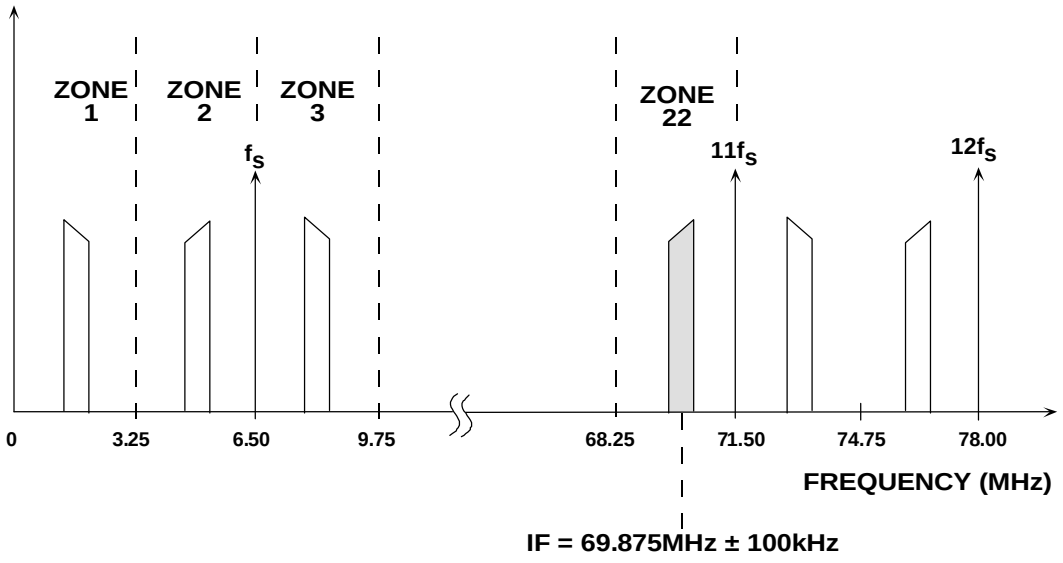
ANALOG DEVICES

5.30

The bandwidth of a single GSM channel is 200kHz, and each channel can handle up to 8 simultaneous callers for full-rate systems and 16 simultaneous callers for the newer one-half-rate systems. A typical basestation may be required to handle 50 to 60 simultaneous callers, thereby requiring 4 separate signal processing channels (assuming a one-half-rate system).

The IF frequency is chosen to be 69.875MHz, thus centering the 200kHz signal in the 22nd Nyquist zone (see Figure 5.31). The dual channel digital decimating receiver (AD6620) reverses the frequency sense of the signal and shifts it down to baseband.

NARROWBAND GSM RECEIVER BANDPASS SAMPLING OF A 200kHz CHANNEL AT 6.5MSPS



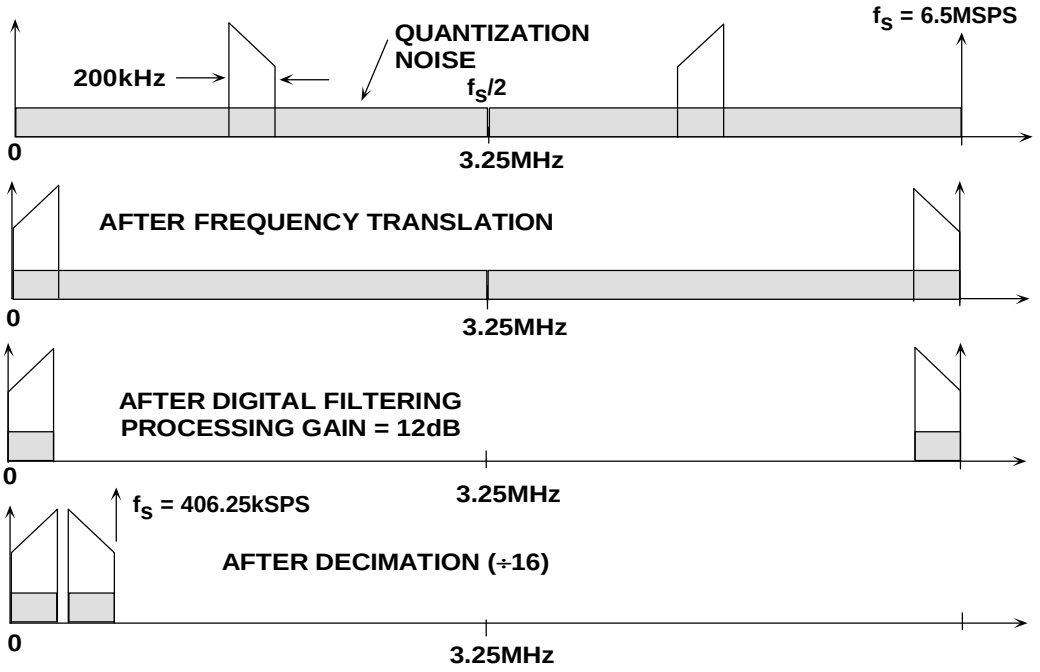
ANALOG DEVICES

5.31

We now have a 200kHz baseband signal (generated by undersampling) which is being *oversampled* by a factor of approximately 16 .

The signal is then passed through a digital filter (part of the AD6620) which removes all frequency components above 200kHz, including the quantization noise which falls in the region between 200kHz and 3.25MHz (the Nyquist frequency) as shown in Figure 5.32. The resultant increase in SNR is 12dB (processing gain). There is now no information contained in the signal above 200kHz, and the output data rate can be reduced (decimated) from 6.5MSPS to 406.25kSPS, a data rate which the DSP can handle. The data corresponding to the 200kHz channel is transmitted to the DSP over a simple 3-wire serial interface. The DSP performs such functions as channel equalization, decoding, and spectral shaping.

DIGITAL FILTERING AND DECIMATION OF THE 200kHz CHANNEL



ANALOG DEVICES

5.32

The concept of *processing gain* is common to all communications systems, analog or digital. In a sampling system, the quantization noise produced by the ADC is spread over the entire Nyquist bandwidth which extends from DC to $f_S/2$. If the signal bandwidth, BW, is less than $f_S/2$, digital filtering can remove the noise components outside this bandwidth, thereby increasing the effective SNR. The processing gain in a sampling system can be calculated from the formula:

$$\text{Processing Gain} = 10\log\left(\frac{f_S}{2 \cdot BW}\right).$$

The SINAD (noise and distortion measured over $f_S/2$ bandwidth) of the ADC at the bandwidth of the signal should be used to compute the actual SINAD by adding the processing gain determined by the above equation. If the ADC is an ideal N-bit converter, then its SNR (measured over the Nyquist bandwidth) is 6.02N + 1.76dB.

PROCESSING GAIN

- **Measure ADC SINAD (6.02N + 1.76dB Theoretical)**
- **Sampling Frequency = f_S**
- **Signal Bandwidth = BW**
- **Processing Gain =**

$$10\log\left(\frac{f_S}{2 \cdot BW}\right)$$

- **SINAD in Signal Bandwidth = SINAD + $10\log\left(\frac{f_S}{2 \cdot BW}\right)$**
- **SINAD (Theoretical) = 6.02N + 1.76dB + $10\log\left(\frac{f_S}{2 \cdot BW}\right)$**
- **Processing Gain Increases 3dB each time f_S is doubled**

ANALOG DEVICES **5.33**

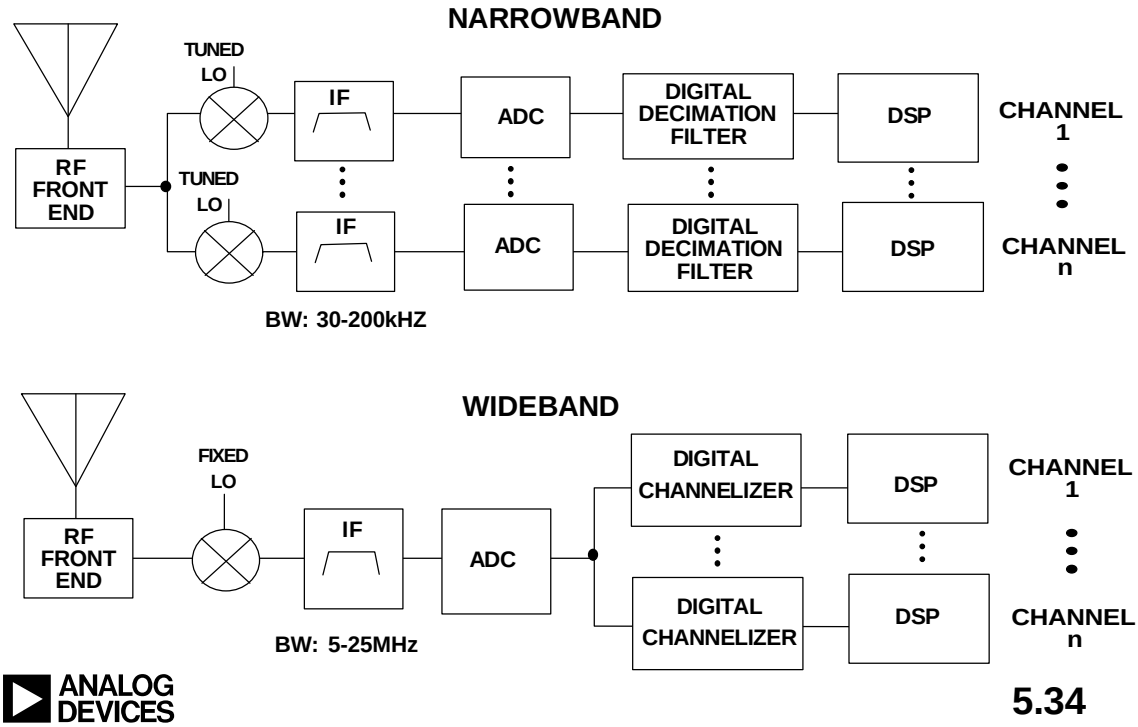
Notice that as shown in the previous narrowband receiver example, there can be processing gain even if the original signal is an undersampled one. The only requirement is that the signal bandwidth be less than $f_S/2$, and that the noise outside the signal bandwidth be removed with a digital filter.

Wideband IF-Sampling Digital Receivers

Thus far, we have avoided a detailed discussion of *narrowband* versus *wideband* digital receivers. A digital receiver can be either, but more detailed definitions are important at this point. By *narrowband*, we mean that sufficient pre-filtering has been done such that all undesired signals have been eliminated and that only the signal of interest is presented to the ADC input. This is the case for the GSM basestation example previously discussed.

Wideband simply means that a number of channels are presented to input of the ADC and further filtering, tuning, and processing is performed digitally. Usually, a wideband receiver is designed to receive an entire band; cellular or other similar wireless services such as PCS (Personal Communications Systems). In fact, one wideband digital receiver can be used to receive *all* channels within the band simultaneously, allowing almost all of the analog hardware (including the ADC) to be shared among all channels as shown in Figure 5.34 which compares the narrowband and the wideband approaches.

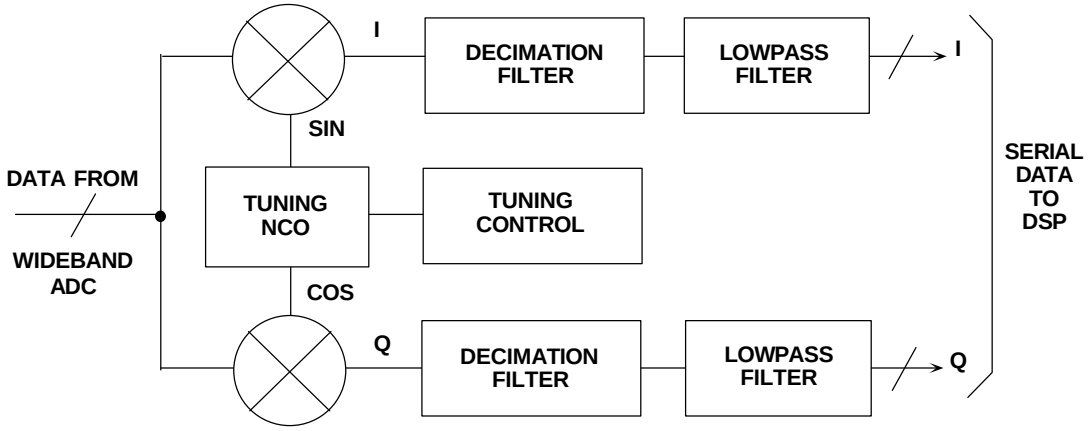
NARROWBAND VERSUS WIDEBAND DIGITAL RECEIVER



Note that in the narrowband digital radio, there is one front-end LO and mixer required per channel to provide individual channel tuning. In the wideband digital radio, however, the first LO frequency is fixed, and the "tuning" is done in the *digital channelizer* circuits following the ADC.

A typical wideband digital receiver may process a 5 to 25MHz band of signals simultaneously. This approach is frequently called *block conversion*. In the wideband digital receiver, the variable local oscillator in the narrowband receiver has been replaced with a fixed oscillator, so tuning must be accomplished digitally. Tuning is performed using a digital down converter (DDC) and filter chip frequently called a *channelizer*. The term channelizer is used because the purpose of these chips is to select one channel out of the many within the broadband spectrum actually present in the ADC output. A typical channelizer is shown in Figure 5.35.

DIGITAL CHANNELIZER IN WIDEBAND RECEIVER



ANALOG DEVICES

5.35

It consists of an NCO (Numerically Controlled Oscillator) with tuning capability, dual mixer, and matched digital filters. These are the same functions that would be required in an analog receiver, but implemented in digital form. The digital output from the channelizer is the demodulated signal in I and Q format, and all other signals have been filtered and removed. Since the channelizer output consists of one selected RF channel, one channelizer is required for each channel. The channelizer also serves to decimate the output data rate such that it can be processed by a DSP such as the ADSP-2181 or the ADSP-21062. The DSP extracts the signal information from the I and Q data and performs further processing. Another effect of the filtering provided by the channelizer is to increase the SNR by adding processing gain.

In the case of an AMPS signal, there are 416 channels, each 30kHz wide, for a total bandwidth of 12.5MHz (each of the two carriers in a given region are allocated 12.5MHz of the total 25MHz cellular band). Each channel carries one call, so there is a clear advantage in using the wideband approach versus the narrowband one in an AMPS basestation which must handle between 50 and 60 simultaneous calls. On the other hand, a 200kHz GSM channel can carry 16 calls simultaneously (for half-rate systems), so only three or four channels are required in the typical GSM basestation, and the narrowband approach is more cost-effective. Using today's technology (1996), the break-even cost point between narrowband and wideband ranges from two and eight channels.

In an ADC used for narrowband applications, the key specifications are SINAD, SFDR, and SNR. The narrowband ADC can take advantage of automatic gain ranging (as in the AD6600) to account for signal amplitude variations between individual channels and thereby achieve extra dynamic range.

On the other hand, an ADC used in a wideband receiver must digitize all channels simultaneously, thereby eliminating the possibility of per-channel analog gain ranging. For example, the GSM (European Digital Cellular) system specification requires the receiver to process signals between –13dBm and –104dBm (with a noise floor of –114dBm) in the presence of many other signals. This is a dynamic range of 91dB! This implies that the SFDR of the ADC and the analog front end must be approximately 95 to 100dBFS, allowing for additional headroom. In addition, the GSM system has 124 channels, each having a bandwidth of 200kHz for a total signal bandwidth of 25MHz. The minimum required sampling rate for an ADC suitable for wideband GSM is therefore greater than 50MSPS.

SFDR is a very important specification when a mobile phone is near the basestation because it is an indication of how strong signals interfere with signals in other channels. Strong signals usually produce the largest spurs due to front-end distortion, and these spurs can mask weaker signals from mobile phones near the cell fringes. The SFDR for weak signals provides an indication of the overall noise floor, or SINAD which can ultimately be related to the receiver bit error rate (BER).

When digitizing a wideband signal, full scale single-tone evaluations are no longer sufficient. Two-tone and multiple-tone intermodulation testing in conjunction with SFDR amplitude sweeps are better indicators of performance.

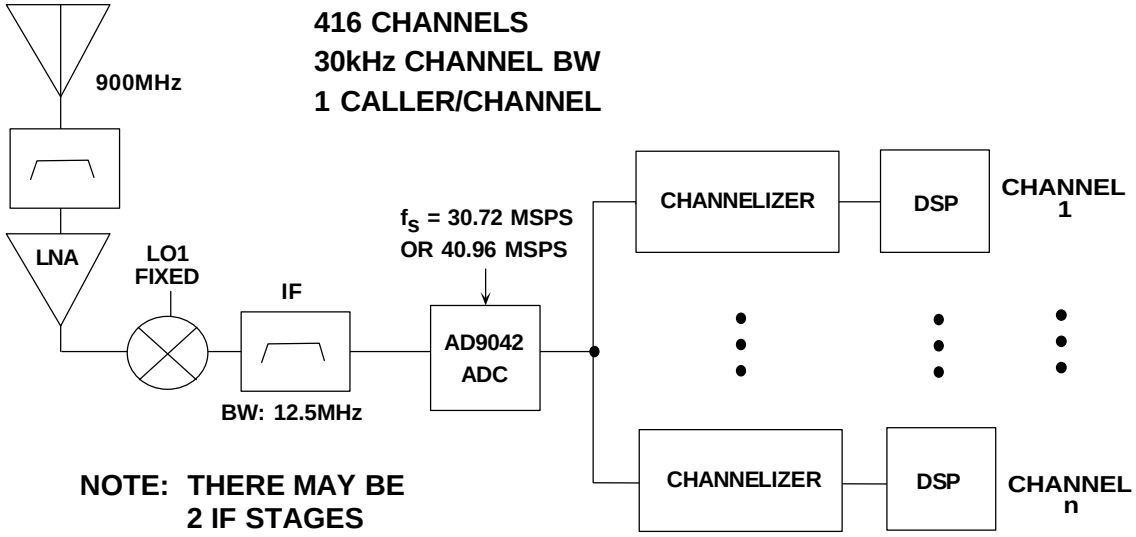
GSM VERSUS AMPS COMPARISONS

	GSM	AMPS
Digital Receiver	**Narrowband**	**Wideband**
# of Channels	**124**	**416**
Channel BW	**200kHz**	**30kHz**
Total BW	**25MHz**	**12.5MHz**
Callers/Channel	**16 (one-half rate)**	**1**
ADC Requirements	**11-bits with RSSI** **6.5 MSPS** **92dB Dynamic Range**	**12-bits** **30.72 MSPS** **80dB SFDR**
Process Gain	**12dB**	**27dB**

The AMPS cellular system basestation is ideally suited to the wideband digital receiver design, and a simplified diagram of one is shown in Figure 5.37. The AD9042 sampling frequency of 30.72MSPS is chosen to be a power-of-two multiple

of the channel bandwidth (30kHz x 1024). Another popular AMPS wideband receiver sampling frequency is 40.96MSPS. The choice of IF frequency is flexible, and a second IF stage may be required if lower IF frequencies are chosen.

AMPS WIDEBAND DIGITAL RECEIVER



With a sampling frequency of 30.72MSPS, the 12.5MHz bandwidth signal can be positioned in the first Nyquist zone (DC to 15.36MHz) with an IF frequency of 7.68MHz, or in the second Nyquist zone (15.36MHz to 30.72MHz) with an IF frequency of 23.04MHz.

With a sampling frequency of 40.96MSPS, the 12.5 MHz bandwidth signal can be positioned in the first Nyquist zone (DC to 20.48MHz) with an IF frequency of 10.24MHz, or in the second Nyquist zone (20.48MHz to 40.96MHz) with an IF frequency of 30.72MHz.

The digital channelizers provide the receiver tuning and demodulate the signal into the I and Q components. The output data rate to the DSPs after decimation is 60kSPS. The processing gain incurred is calculated as follows:

$$\text{Processing Gain} = 10\log\left(\frac{30.72}{2\times 0.03}\right) = 27.1\text{dB}.$$

AMPS WIDEBAND RECEIVER PROCESS GAIN

- **fs = 30.72MSPS (1024 · 30kHz)**
- **Channel BW = 30kHz**

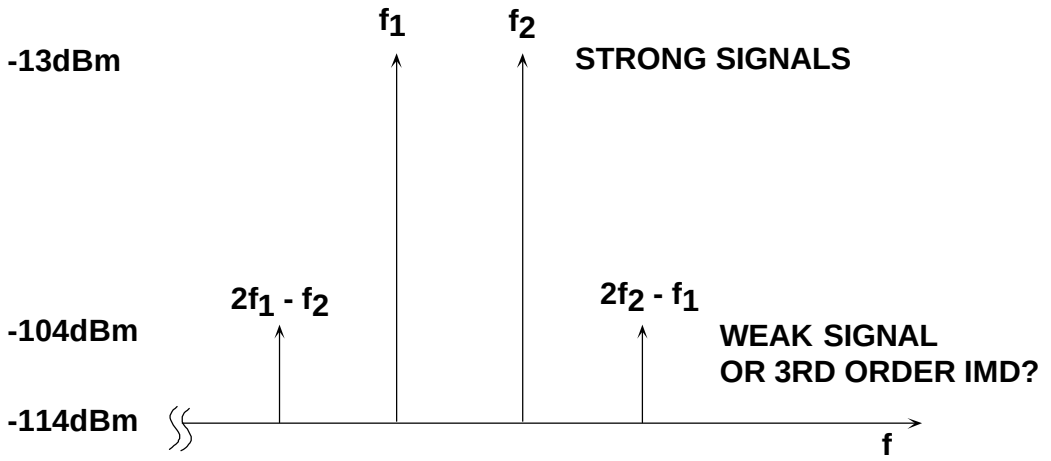
■ **Process Gain =** $10\log\left(\frac{f_S}{2 \cdot BW}\right)$ **= 27.1dB**

ANALOG DEVICES

5.38

In addition to SFDR, two-tone and multi-tone intermodulation distortion is important in an ADC for wideband receiver applications. Figure 5.39 shows two strong signals in two adjacent channels at frequencies f1 and f2. If the ADC has third-order intermodulation distortion, these products will fall at $2f_2–f_1$ and $2f_1–f_2$ and are indistinguishable from signals which might be present in these channels. This is one reason the GSM system is difficult to implement using the wideband approach, since the dynamic range requirement is greater than 91dB.

TWO-TONE INTERMODULATION DISTORTION IN MULTICHANNEL SYSTEM (GSM REQUIREMENTS SHOWN)

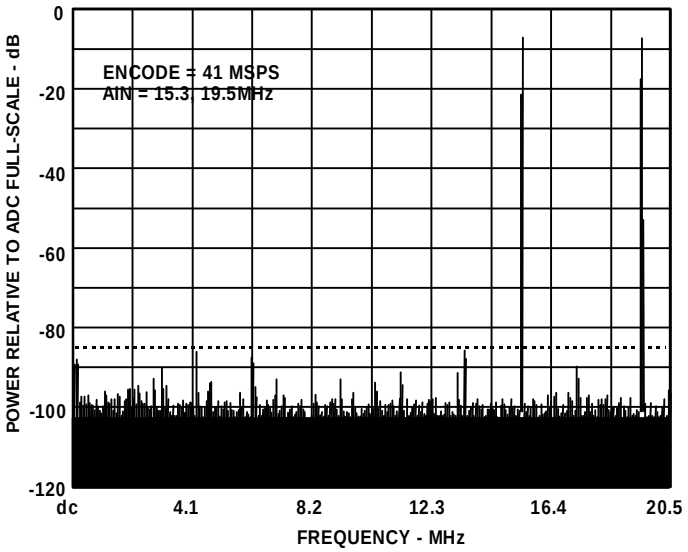


ANALOG DEVICES

5.39

The two-tone SFDR of the AD9042 is greater than 80dB with input tones at 15.3MHz and 19.5MHz as shown in Figure 5.40. Note than the amplitude of each tone must be 6dB below full scale in order to prevent the ADC from being overdriven. The two-tone SFDR as a function of input signal amplitude is shown in Figure 5.41 for tone frequencies of 19.3MHz and 19.51MHz. The upper curve is in dBFS, and the lower in dBc. Note that the SFDR is greater than 80dBFS for all input amplitudes. Figure 5.42 shows a multitone FFT output for the AD9042, and the ADC still maintains 85dBFS of SFDR.

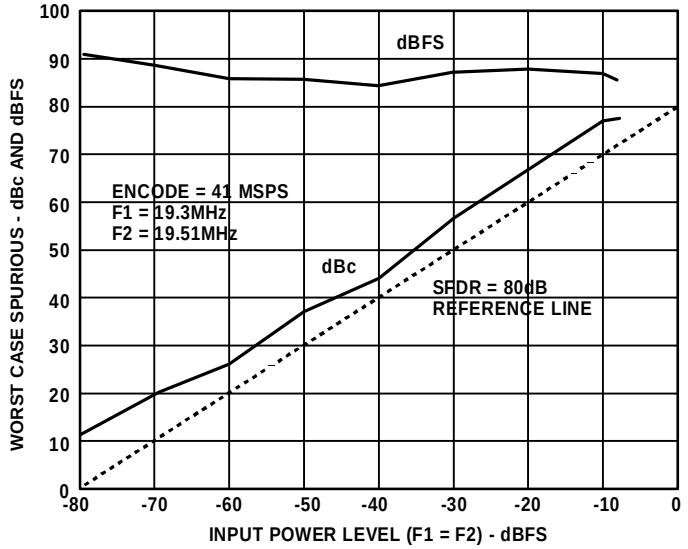
AD9042 TWO-TONE FFT OUTPUT
F1 = 15.3MHz, F2 = 19.5MHz, f_S = 41MSPS



ANALOG DEVICES

5.40

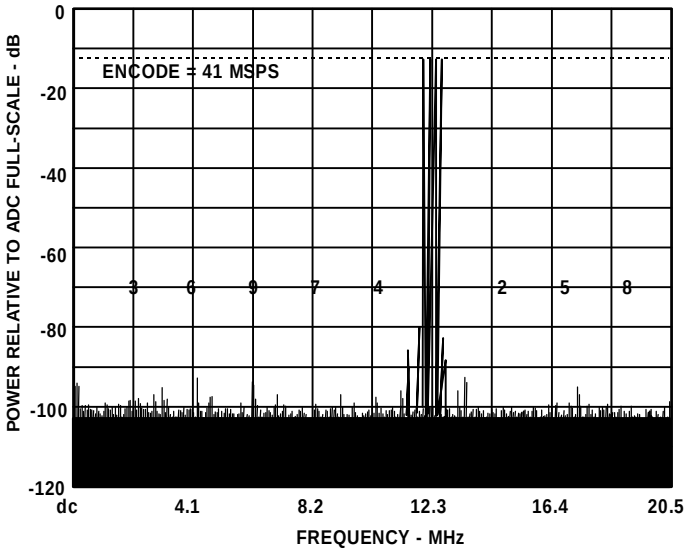
AD9042 TWO-TONE SFDR
F1 = 19.3MHz, F2 = 19.51MHz, f_S = 41MSPS



ANALOG DEVICES

5.41

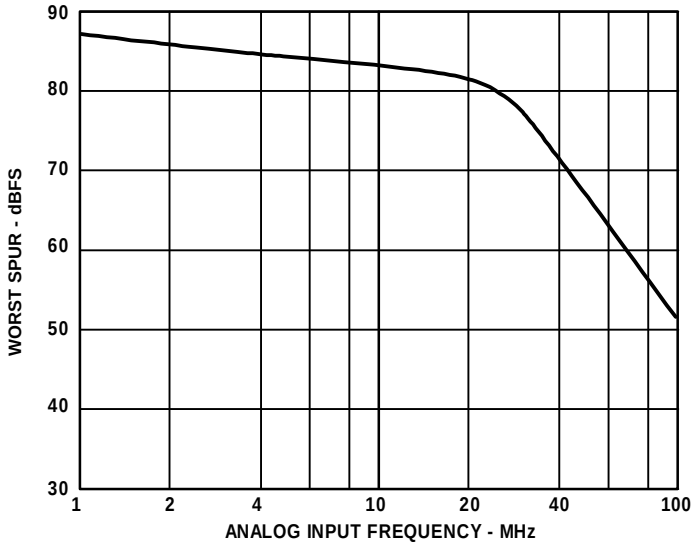
AD9042 MULTITONE PERFORMANCE (4 TONES)
f_S = 41MSPS



Direct IF-to-Digital Considerations

The dynamic performance of the AD9042 extends well beyond 20MHz analog input signals (see Figure 5.43). Therefore it can be used to perform direct IF-to-digital conversions using a wide range of IF frequencies. These IF signals can be undersampled as previously described, and the minimum sampling frequency required is determined by the bandwidth of the IF signal. Figure 5.44 shows a 21.4MHz signal sampled at 10MSPS using the AD9042. Note that under these conditions, the SFDR performance is greater than 80dBFS.

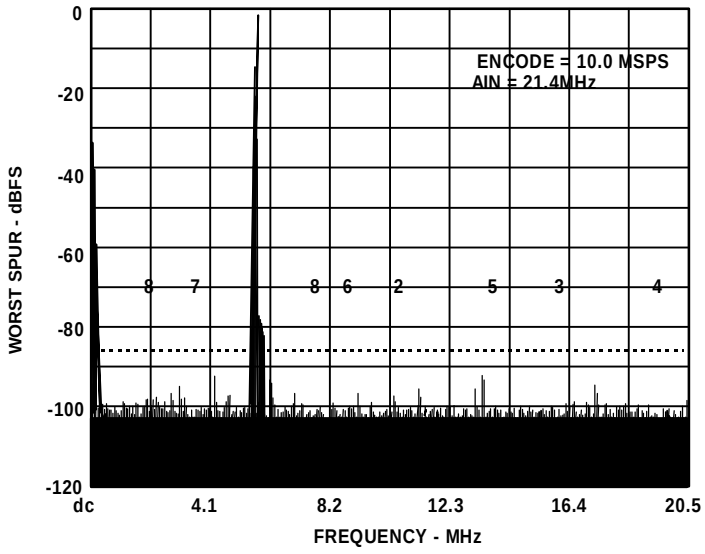
AD9042 SFDR VERSUS INPUT FREQUENCY



ANALOG DEVICES

5.43

AD9042 OUTPUT FOR IF SAMPLED INPUT: f_S = 10MSPS, ANALOG INPUT = 21.4MHz



ANALOG DEVICES

5.44

The AD6640 represents the next generation in IF sampling ADCs. Key specifications for the AD6640 are summarized in Figure 5.45. The architecture is similar to that of the AD9042, but the device is fabricated on a faster XFCB process. The input structure is fully differential and designed for transformer coupling for

minimum distortion. Maximum sampling frequency is 65MSPS, and the SINAD performance is 67dB at 60MHz analog input. SFDR is greater than 80dBFS for frequencies up to 25MHz. This device allows direct IF sampling in wideband communications systems having bandwidths up to 25MHz (such as the AMPS system, where each carrier is allocated 12.5MHz of spectrum). For systems with smaller bandwidths, the higher sampling frequency provided by the AD6640 will allow analog antialiasing filter requirements to be relaxed and provide processing gain. In undersampling applications, the device can be used to digitize 70MHz IF signals which lie in the second or third Nyquist zone. For instance, a 30MHz wideband signal bandwidth centered around a carrier frequency of 48.75MHz can be digitized at 65MSPS as shown in Figure 5.46. In narrowband applications, the high sampling frequency can be used to achieve additional processing gain.

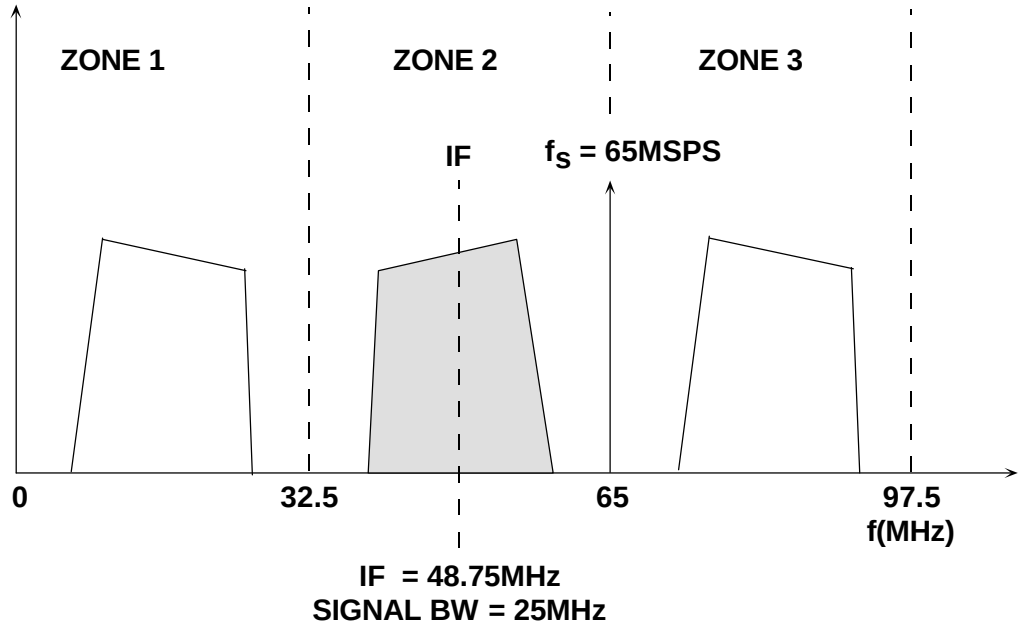
AD6640 12-BIT, 65MSPS ADC KEY SPECIFICATIONS

- **12-bit, 65MSPS IF-SAMPLING ADC**
- **Based on AD9042 architecture, but 1.5X faster CB process**
- **Fully differential inputs for optimum distortion performance**
- **SFDR Greater than 80dB up to 25MHz Input**
- **68dB SINAD for 60MHz IF input**
- **Single +5V Supply, 695mW**
- **44-Lead TQFP Package**

ANALOG DEVICES

5.45

SAMPLING A 25MHz BW SIGNAL USING AD6640: IF FREQUENCY = 48.75MHz, f_S = 65MSPS



ANALOG DEVICES

5.46

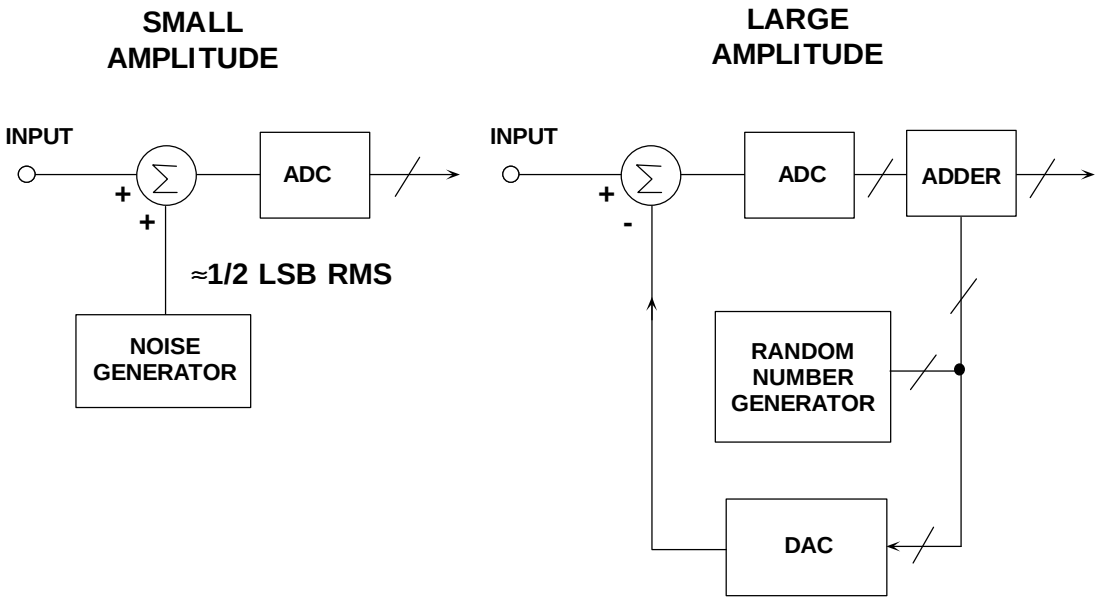
Achieving Wide Dynamic Range in High Speed ADCs Using Dither

There are two fundamental limitations to maximizing SFDR in a high speed ADC. The first is the distortion produced by the front-end amplifier and the sample-and-hold circuit. The second is that produced by non-linearity in the actual transfer function of the encoder portion of the ADC. The key to wide SFDR is to minimize the non-linearity of each.

There is nothing that can be done externally to the ADC to significantly reduce the inherent distortion caused by the ADC front end. However, the non-linearity in the ADC encoder transfer function can be reduced by the proper use of dither (external noise which is summed with the analog input signal to the ADC).

Dithering improves ADC SFDR under certain conditions. For example, even in a perfect ADC, there is some correlation between the quantization noise and the input signal. This can reduce the SFDR of the ADC, especially if the input signal is an exact sub-multiple of the sampling frequency. Summing broadband noise (about 1/2 LSB rms in amplitude) with the input signal tends to randomize the quantization noise and minimize this effect (see Figure 5.47). In most systems, however, there is enough noise riding on top of the signal so that adding additional dither noise is not required. Increasing the wideband rms noise level beyond an LSB will proportionally reduce the ADC SNR.

USING DITHER TO RANDOMIZE ADC TRANSFER FUNCTION



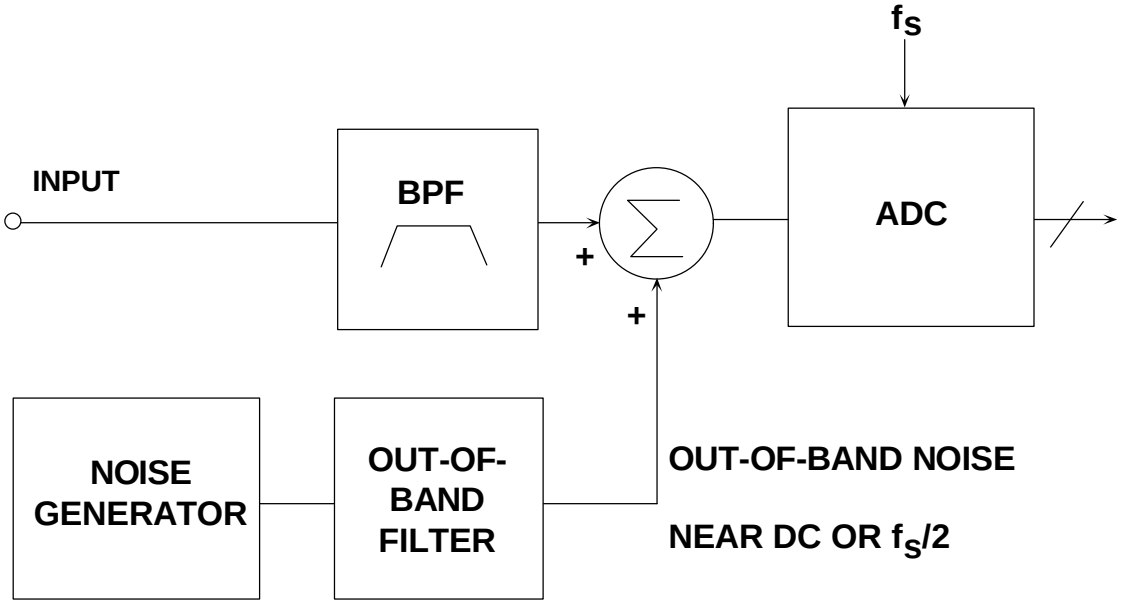
ANALOG DEVICES

5.47

Other schemes have been developed which use larger amounts of dither noise to randomize the transfer function of the ADC. Figure 5.47 also shows a dither noise source comprised of a pseudo-random number generator which drives a DAC. This signal is subtracted from the ADC input signal and then digitally added to the ADC output, thereby causing no significant degradation in SNR. An inherent disadvantage of this technique is that the allowable input signal swing is reduced as the amplitude of the dither signal is increased. This reduction in signal amplitude is required to prevent overdriving the ADC. It should be noted that this scheme does not significantly improve distortion created by the front-end of the ADC, only that produced by the non-linearity of the ADC encoder transfer function.

Another method which is easier to implement, especially in wideband receivers, is to inject a narrowband dither signal *outside the signal band of interest* as shown in Figure 5.48. Usually, there are no signal components located in the frequency range near DC, so this low-frequency region is often used for such a dither signal. Another possible location for the dither signal is slightly below $f_S/2$. Because the dither signal occupies only a small bandwidth relative to the signal bandwidth, there is no significant degradation in SNR, as would occur if the dither was broadband.

INJECTING OUT-OF-BAND DITHER TO IMPROVE ADC SFDR

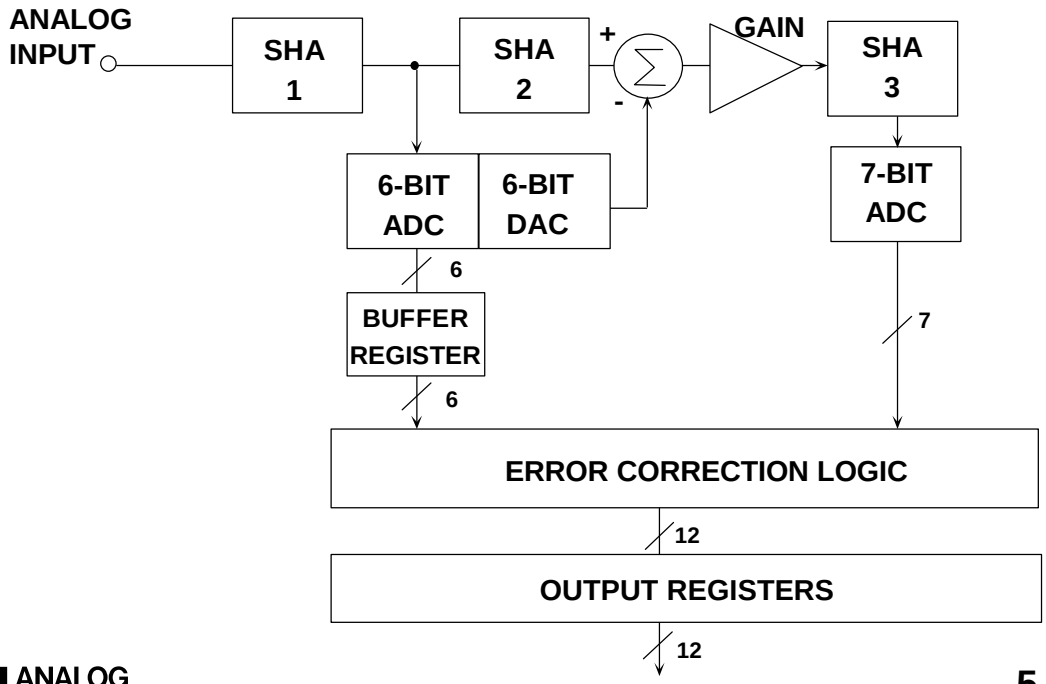


ANALOG DEVICES

5.48

A subranging ADC such as the AD9042 (see Figure 5.49) has small differential non-linearity errors that occur at specific regions across the ADC range. For instance, the AD9042 uses a 6-bit ADC followed by a 7-bit one. There are 64 decision points associated with the main-range 6-bit ADC, and they occur every 15.625mV for a 1V full scale input range. Figure 5.50 shows a greatly exaggerated representation of these non-linearities.

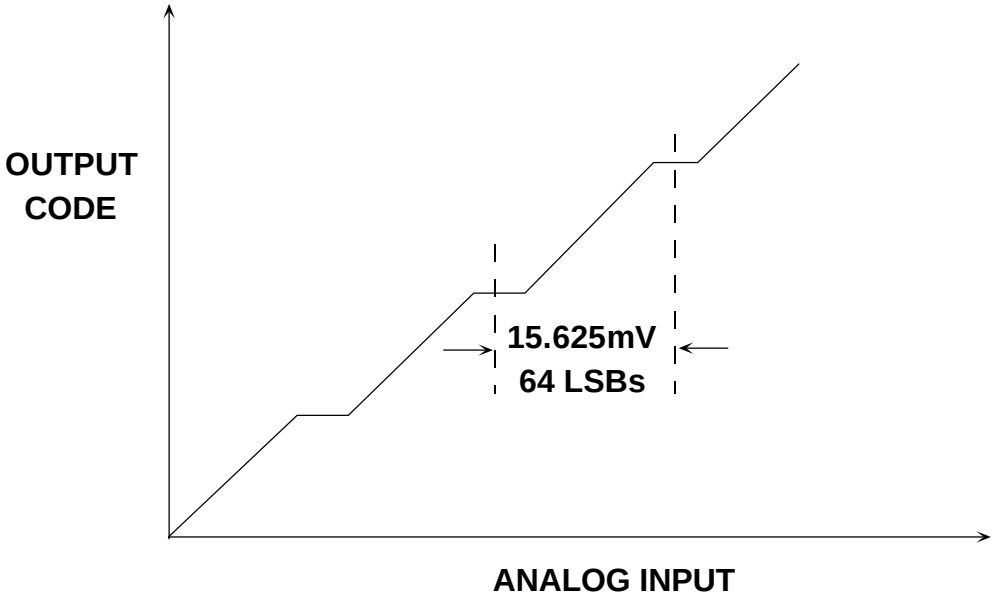
AD9042 12-BIT, 41MSPS PIPELINED SUBRANGING ADC WITH DIGITAL ERROR CORRECTION



ANALOG DEVICES

5.49

AD9042 SUBRANGING POINT DNL ERRORS (EXAGGERATED)



ANALOG DEVICES

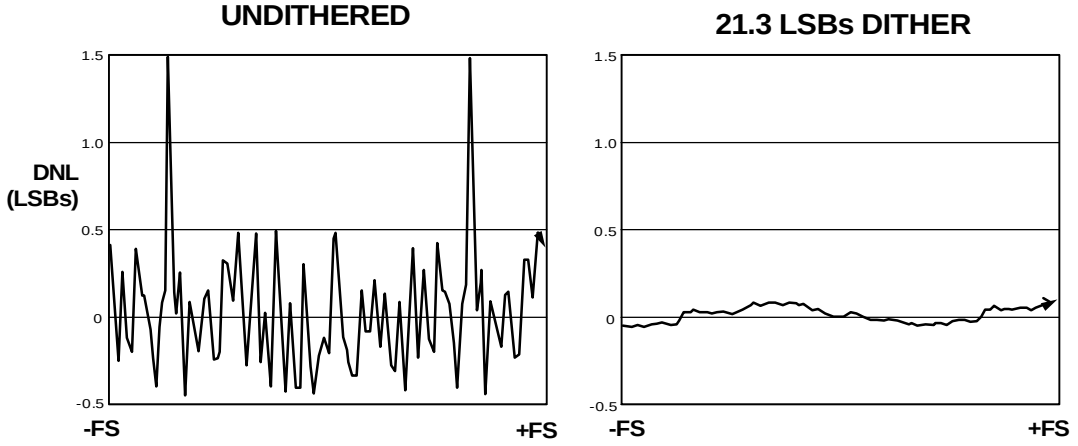
5.50

The distortion components produced by the front end of the AD9042 up to about 20MHz analog input are negligible compared to those produced by the encoder. That

is, *the static non-linearity of the AD9042 transfer function* is the chief limitation to SFDR.

The goal is to select the proper amount of out-of-band dither so that the effect of these small DNL errors are *randomized* across the ADC input range, thereby reducing the average DNL error. The first plot shown in Figure 5.51 shows the undithered DNL over a small portion of the input signal range. The horizontal axis has been expanded to show two of the subranging points which are spaced 15.625mV (64 LSBs) apart. The second plot shows the DNL after adding 5.3mV rms (22 LSBs rms) of dither. This amount of dither corresponds to –32.5dBm (1V p-p full scale corresponds to +4dBm). It was determined that further increases in dither amplitude provided no improvement in the AD9042 SFDR and would only serve to cause a loss in headroom and a decrease in SNR.

AD9042 UNDITHERED AND DITHERED DNL

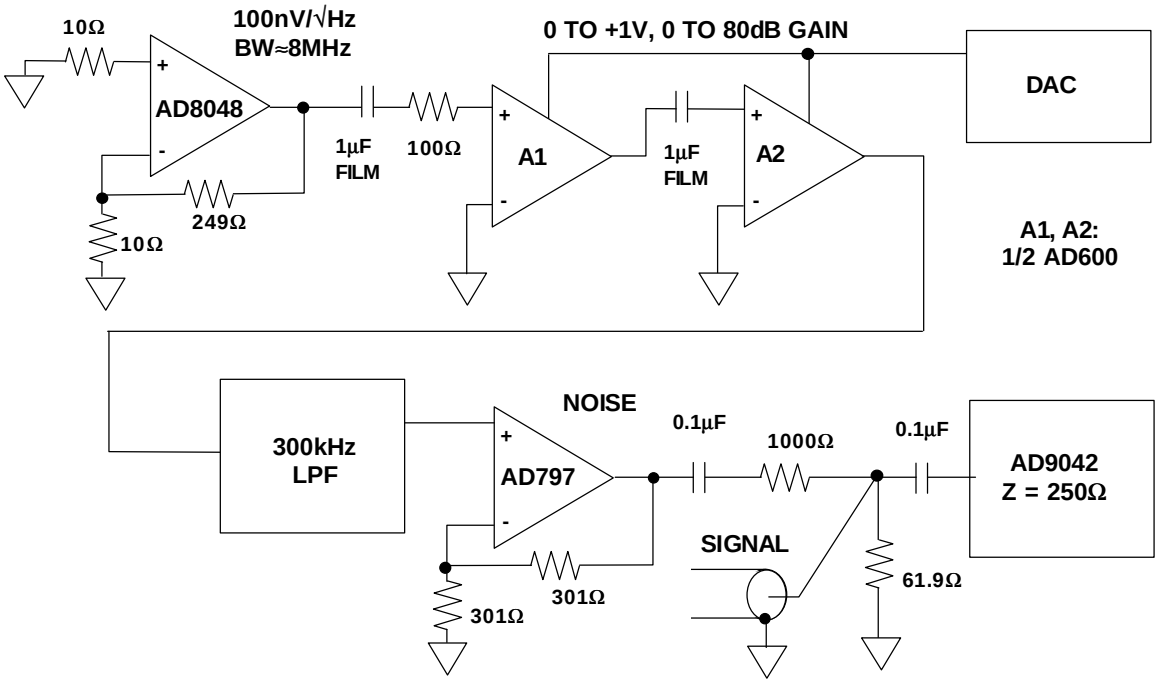


ANALOG DEVICES

5.51

The dither signal was generated using a voltage feedback op amp (AD8048, 3.8nV/√Hz input voltage noise, 200MHz gain-bandwidth product) as the noise source (see Figure 5.52). The op amp is configured for a gain of +26, and the output noise spectral density is about 100nV/√Hz over an 8MHz bandwidth. The output of the noise generator is then amplified by the AD600 dual wideband VCA which provides a gain (in dB) which is proportional to the control voltage. The control voltage can be fixed, or programmed using a DAC as shown. The gain of the AD600 can be set from 0dB to 80dB by varying the control voltage from 0 to +1V. The bandwidth of the noise is limited to about 300kHz with a lowpass filter. The filter can be either passive or active, but requires at least 4 poles in order to attenuate the out-of-band noise. The output of the lowpass filter is buffered with the AD797 low-noise op amp which also provides a gain of +2. The filtered noise is summed directly into the input circuit of the AD9042 through a capacitor and a 1kΩ series resistor. The net input impedance of the AD9042 is 50Ω (61.9Ω in parallel with the 250Ω AD9042 internal impedance).

DITHER NOISE GENERATOR



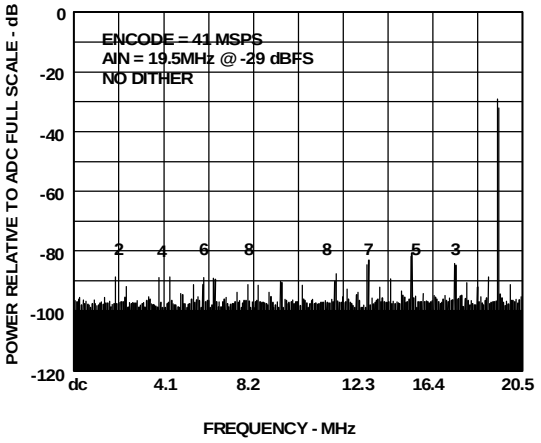
ANALOG DEVICES

5.52

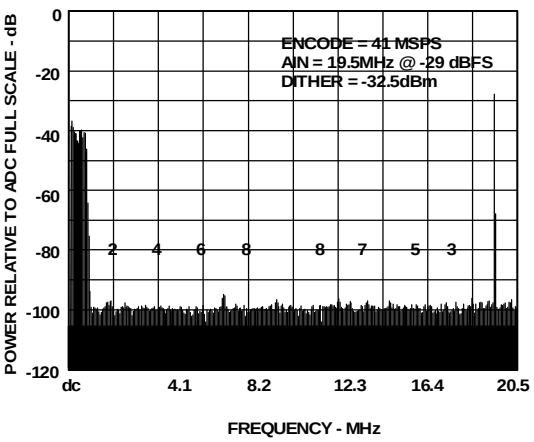
The dramatic improvement in SFDR obtained with out-of-band dither is shown in Figure 5.53 using a 4k FFT, where the AD9042 is sampling a 19.5MHz signal (–29dBFS) at 41MSPS. Note that the SFDR without dither is approximately 80dBFS compared to 94dBFS with dither, representing a 14dB improvement! This improvement is also shown in the SFDR amplitude sweeps shown in Figure 5.54. Note the similar improvement.

AD9042 UNDITHERED AND DITHERED 4k FFT OUTPUT

UNDITHERED

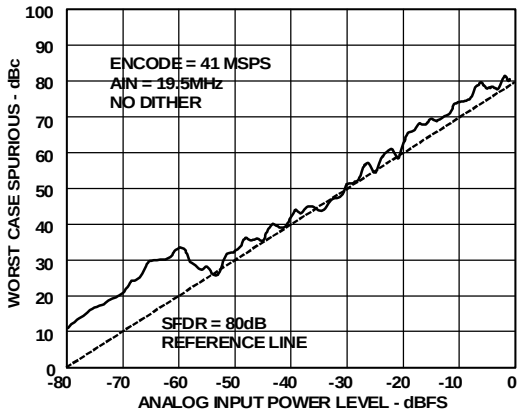


DITHERED

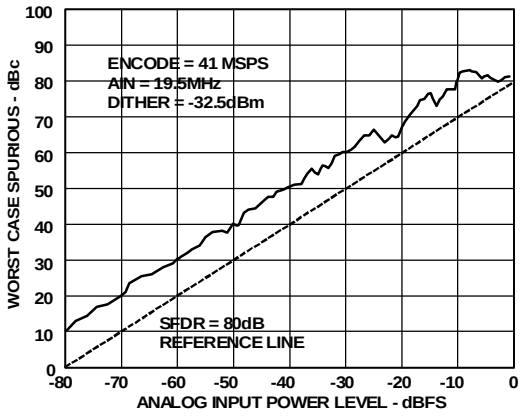


AD9042 UNDITHERED AND DITHERED SFDR

UNDITHERED



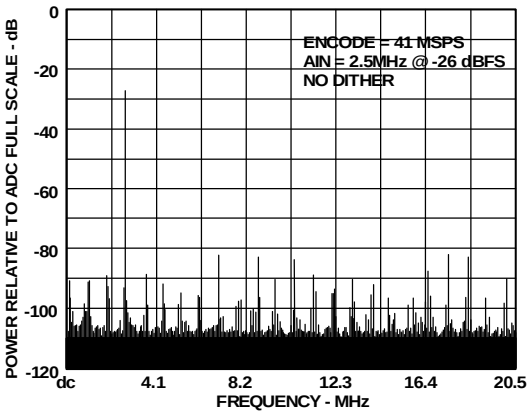
DITHERED



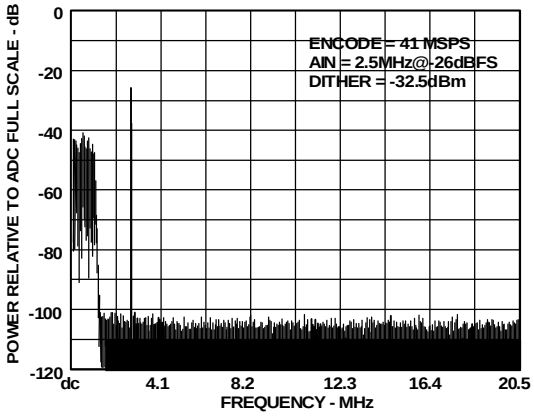
At lower frequencies, the FFT size must be increased from 4k to 128k (reducing the FFT noise floor by 15dB) in order to measure the dithered SFDR. Figure 5.55 shows the effects of dither using a 128k FFT and a 2.5MHz input signal. The SFDR with dither is greater than 100dBFS.

AD9042 UNDITHERED AND DITHERED 128k FFT OUTPUTS

UNDITHERED



DITHERED

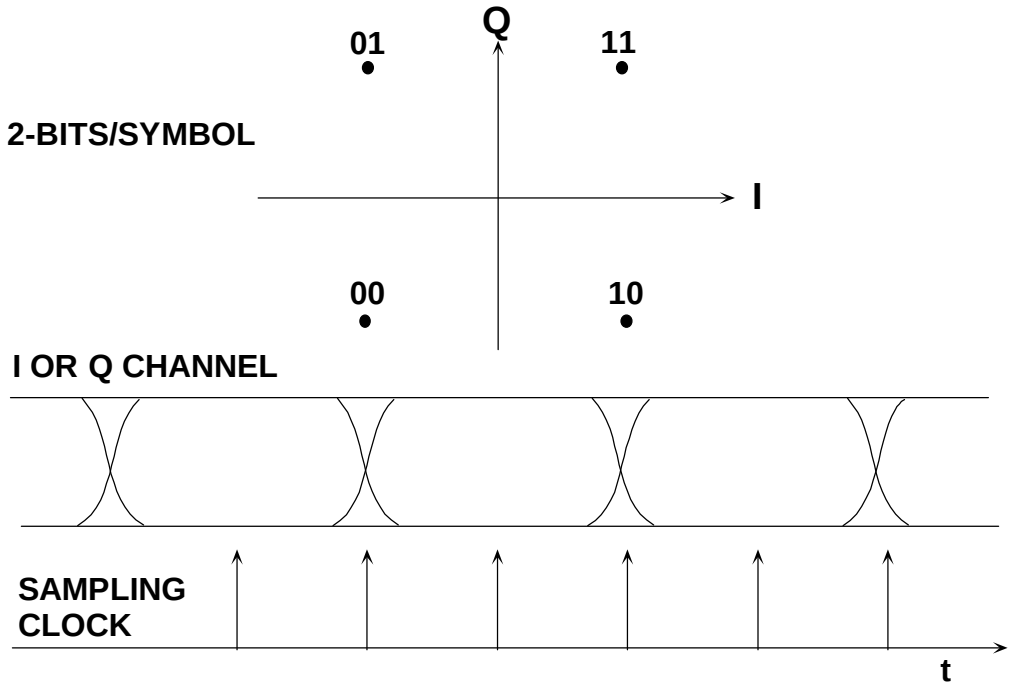


High Speed ADC Applications in Digital Communications Systems and Direct Broadcast Satellite (DBS) Set-Top Boxes

In a digital communications system, digital data (which can be digitized analog signals) is formatted and transmitted serially over an appropriate medium. The GSM cellular telephone system is an example. The ubiquitous modem (modulator/demodulator), which PCs and FAX machines use to transmit and receive data over the standard dial-up telephone connection, uses sophisticated modulation techniques to place huge amounts of data in the 4kHz bandwidth telephone channel.

Most digital transmission schemes use some form of in-phase and quadrature (I and Q) modulation to maximize the amount of data transmitted over a given channel bandwidth. Two examples are shown in Figure 5.56 and Figure 5.57. The first is called Quadrature Phase Shift Keying (QPSK) and is used in Direct Broadcast Satellite systems. The diagram (*constellation*) shows the four possible data points, each representing 2-bits of binary information. Each point in the constellation is called a *symbol* and has a specific I and Q value. In the case of QPSK, there are two bits of information per symbol. The symbol rate is often referred to as the *baud* rate. For example, in QPSK, if the symbol (or baud) rate is 30Mbaud (1baud = 1symbol/sec), the bit rate is 60Mbits/sec. It is common practice to sample these types of signals at twice the symbol (or baud) rate. The I and Q ADC and DSP must identify the signal as representing one of two possible levels, and ADCs of 4, 5, or 6-bits are commonly used in this application for additional noise margin and to achieve the overall system bit-error-rate (BER) requirement.

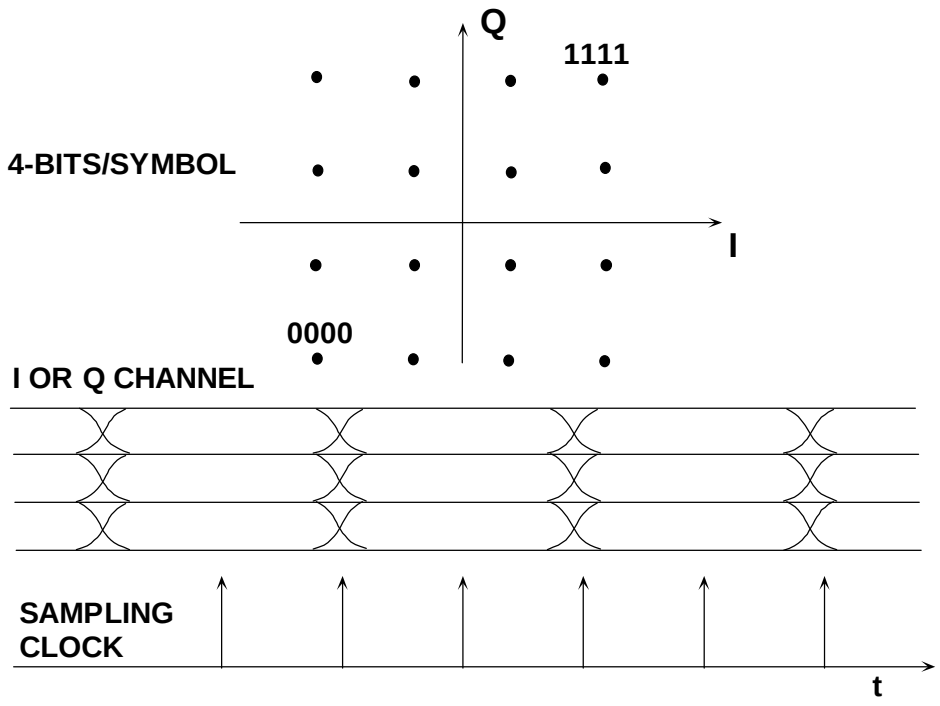
QPSK MODULATION



ANALOG DEVICES

5.56

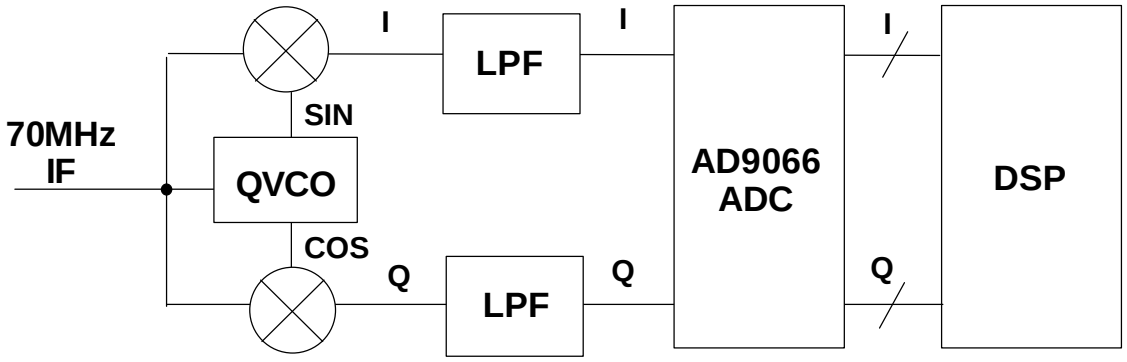
In the QPSK system, the magnitude of each symbol is equal, and only the phase is modulated. More complex modulation schemes such as QAM (Quadrature Amplitude Modulation), use more symbols on the constellation and thereby transmit more bits of information per symbol (at the expense of more sensitivity to noise and more complex digital signal processing). Figure 5.57 shows a 16-QAM constellation which contains 4-bits of information per symbol. Note that the I and Q channel receiver DSP must now identify the signal as representing one of the four possible levels. Although the 16-QAM signal carries more bits per symbol, it is more sensitive to noise, and the ADC requires more resolution (typically 8-bits) than for QPSK modulation (typically 4, 5, or 6 bits).



ANALOG DEVICES

In the digital receiver, the I and Q components are separated by a quadrature demodulator and digitized by two ADCs operating in parallel. The ADC sampling rate is generally twice the symbol rate. In the case of Direct Broadcast Satellite (DBS), the symbol rate is 30Mbaud (1baud = 1symbol/sec), the bit rate 60Mbits/sec, and the ADC sampling rate is 60MSPS. The actual signals at the ADC input are called "eye patterns" because the intersymbol interference due to noise and limited bandwidth *smears* the level transitions so that the regions where the data is valid are located in the center of the *eye* opening. Figure 5.58 shows a typical I/Q demodulator followed by a dual ADC such as the AD9066 (6-bits, 60MSPS).

IF SAMPLING USING AD9066 6-BIT, 60MSPS ADC



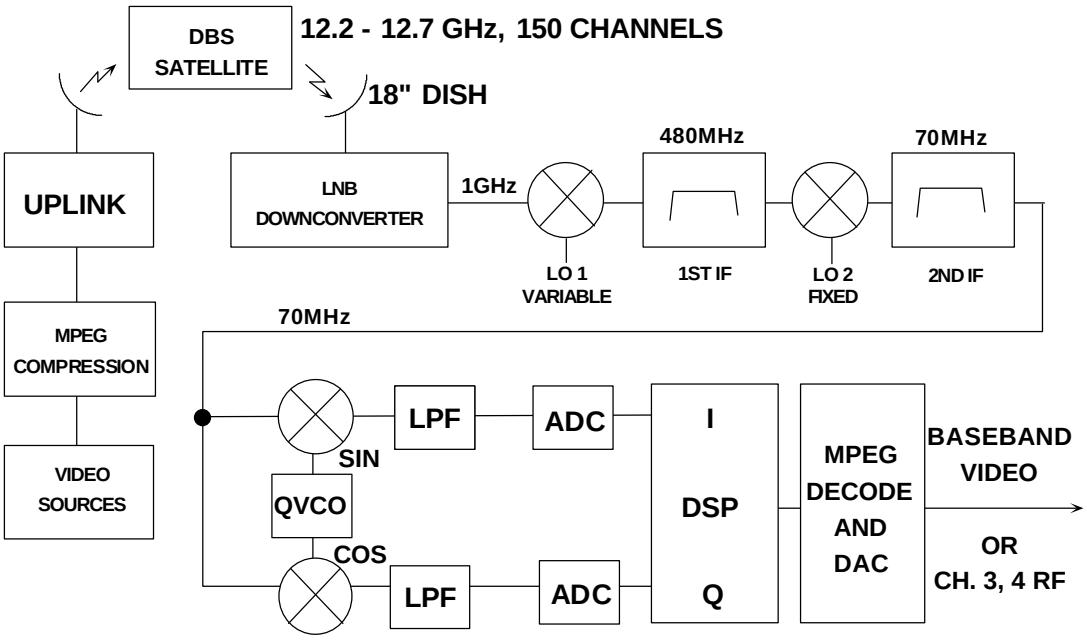
FOR DBS, SYMBOL (BAUD) RATE = 30MBAUD, QPSK
SAMPLING RATE = 60MSPS

ANALOG DEVICES

5.58

A recent popular consumer application of digital communications is in Direct Broadcast Satellite (DBS) systems. A simplified block diagram of a DBS system is shown in Figure 5.59. The objective is to transmit up to 150 channels of video programming to home receivers which use a small (18 inch) dish and an inexpensive (less than $500) receiver (set-top box). The subscription costs of the services is compatible with cable TV, but picture quality (because of digital transmission inherent noise immunity) is generally superior over all 150 channels.

DIRECT BROADCAST SATELLITE (DBS)



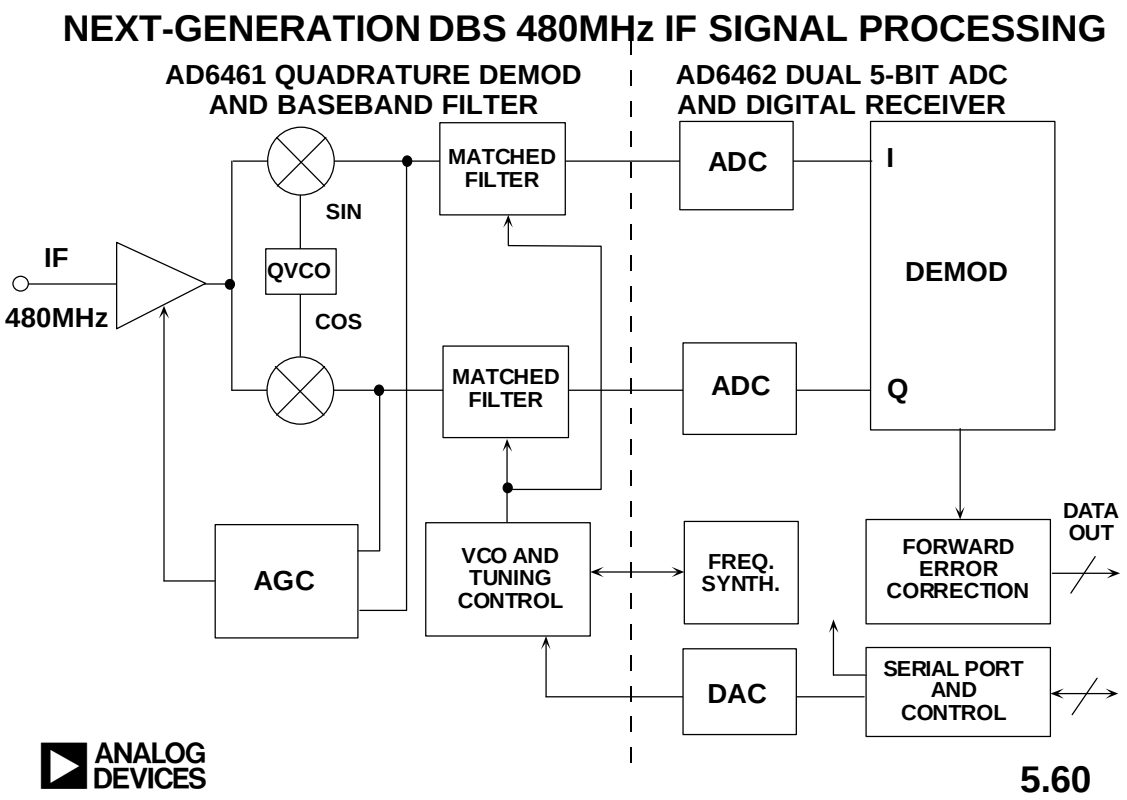
MPEG encoding and decoding reduces the data rates to fit the channel bandwidth. The MPEG (Motion Picture Experts Group) standard supports various data rates and minimizes the bandwidth used. For example, a typical 24-frame-per-second NTSC-quality movie needs about 3Mbits/sec after encoding. A more complex and fast-moving show, such as a soccer game, requires 5 to 6 Mbits/sec. In a DBS system, the MPEG encoding rate is kept at a minimum value compatible with the anticipated video signal characteristics. Multiple MPEG data streams are multiplexed and sent through a single satellite transponder. In addition, statistical multiplexing dynamically varies the data rate given to each source as the program content changes.

The satellite downlink frequency is Ku-band (12.2 to 12.7GHz), and the transponder output power is about 120W (10 to 20 times that of a typical communications satellite which is designed for much larger receiver antennas). The LNB (Low Noise Block Converter) converts the 12.2 to 12.7GHz untuned band down to 950MHz to 1450MHz, where the signal is easier to tune, filter, and bring into the home over standard coaxial cable. The lower frequency signal (1GHz) incurs less loss over standard coaxial cable from the outside antenna to the inside of the house (generally 50 feet or more) than the Ku-band signal (12GHz).

The set-top box mixes the RF (1GHz) signal down to the first fixed IF frequency of 480MHz. The LO which drives the mixer is used for channel tuning. A second fixed-frequency IF stage brings the tuned signal down to 70MHz where it is synchronously demodulated into baseband I and Q components. The modulation scheme is QPSK, the symbol rate is 30Mbaud, and the ADC sampling rate 60MSPS.

Figure 5.60 shows a two-chip solution to the front-end of the set-top box using the AD6461 (quadrature demodulator and baseband filter) and the AD6462 (dual 5-bit

ADC and digital receiver). The input to the AD6461 is the 480MHz DBS IF signal. The chip-set is designed to support symbol rates up to 42.5Mbaud. The AD6461 utilizes Analog Devices' XFCB process and is packaged in 28-pin SOIC dissipating about 500mW. The AD6462 utilizes a 0.6 micron CMOS process and is packaged in an 80-pin PQFP dissipating approximately 1.2W (operating dynamically).



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