SECTION 3
RF/IF SUBSYSTEMS
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DYNAMIC RANGE COMPRESSION

In many cases, a wide dynamic range is an essential aspect of a signal, something to be preserved at all costs. This is true, for example, in the high-quality reproduction of music and in communications systems. However, it is often necessary to compress the signal to a smaller range without any significant loss of information. Compression is often used in magnetic recording, where the upper end of the dynamic range is limited by tape saturation, and the lower end by the granularity of the medium. In professional noise-reduction systems, compression is "undone" by precisely-matched nonlinear expansion during reproduction. Similar techniques are often used in conveying speech over noisy channels, where the performance is more likely to be measured in terms of word-intelligibility than audio fidelity. The reciprocal processes of compressing and expanding are implemented using "compandors", and many schemes have been devised to achieve this function.

There is a class of *linear* dynamic range compression systems where the gain of the amplifiers in the signal processing chain is independent of the instantaneous amplitude of the signal, but is controlled by a closed loop system in such a way as to render the output (that is the peak, or rms value) essentially constant. The harmonic distortion is relatively low. These systems use what are often called *variable-gain amplifiers*. While correct, this lacks precision, because *nonlinear* amplifiers (such as log amps) also exhibit variable gain, but in direct response to the signal magnitude. The term *voltage controlled amplifier* (VCA) is preferred in this context; it clearly describes the way in which the gain control is implemented, while allowing latitude in regard to the actual circuit means used to achieve the function. The gain may be controlled by a *current* within the circuit, but usually a voltage. Analog multipliers may be used as VCAs, but there are other topologies which will be discussed later in this section.

Logarithmic amps find applications where signals having wide dynamic ranges (perhaps greater than 100dB) must be processed by elements, such as ADCs, which may have limited dynamic ranges. Log amps have maximum incremental gain for small signals; the gain decreases in inverse proportion to the magnitude of the input. This permits the amplifier to accept signals with a wide input dynamic range and compress them substantially.

Log amps provide nonlinear dynamic range compression and are used in applications where low harmonic distortion is not a requirement. All types of log amps produce a low dynamic range output without the need to first acquire some measure of the signal amplitude for use in controlling gain.

We will first examine *linear* compression techniques using voltage-controlled amplifiers within automatic-gain-control (AGC) loops. *Nonlinear* signal compression using log amps is then discussed.

Both AGC loops using VCAs and log amps make excellent building blocks for highly integrated RF/IF subsystems for signal processing in communications systems as will be demonstrated.

RF / IF SUBSYSTEM BUILDING BLOCKS

- **Signal Dynamic Range Compression Techniques**
  - **Linear: Automatic Gain Control Loop (AGC) using Voltage Controlled Amplifier (VCA) and Detector**
  - **Non-Linear: Demodulating / Limiting Logarithmic Amplifiers**
- **Modulation / Demodulation: In-Phase and Quadrature (I/Q) and Polar (Amplitude and Phase)**
  - **Dynamic Range Compression Required**
  - **IF Subsystems: AGC, Log / Limiting, RSSI, Mixers**

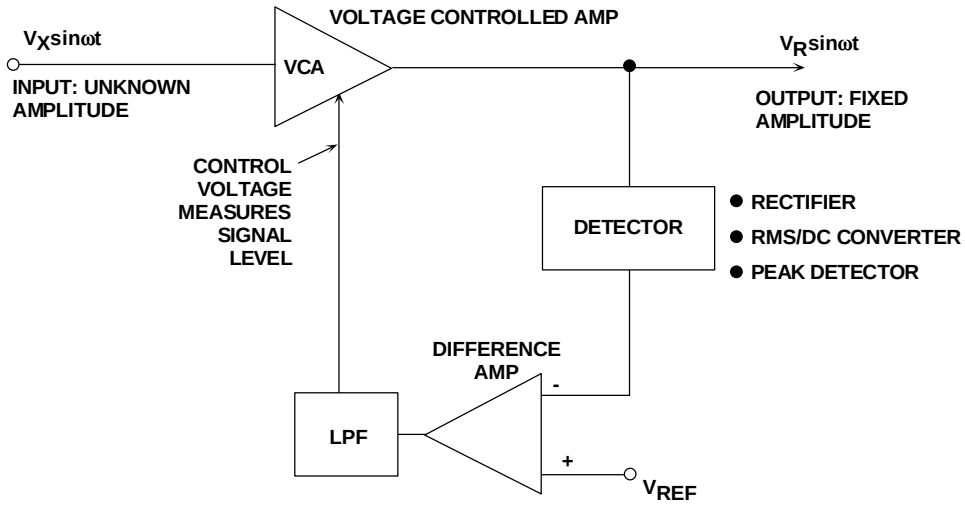
ANALOG DEVICES

3.1

AUTOMATIC GAIN CONTROL (AGC) AND VOLTAGE-CONTROLLED AMPLIFIERS (VCAS)

In radio systems, the received energy exhibits a large dynamic range due to the variability of the propagation path, requiring dynamic-range compression in the receiver. In this case, the wanted information is in the modulation envelope (whatever the modulation mode), not in the absolute magnitude of the carrier. For example, a 1MHz carrier modulated at 1kHz to a 30% modulation depth would convey the same information, whether the received carrier level is at 0dBm or –120dBm. Some type of automatic gain control (AGC) in the receiver is generally utilized to restore the carrier amplitude to some normalized reference level, in the presence of large input fluctuations. AGC circuits are dynamic-range compressors which respond to some metric of the signal – often its mean amplitude – acquired over an interval corresponding to many periods of the carrier. Consequently, they require time to adjust to variations in received signal level. The time required to respond to a sudden increase in signal level can be reduced by using peak detection methods, but with some loss of robustness, since transient noise peaks can now activate the AGC detection circuits. Nonlinear filtering and the concept of "delayed AGC" can be useful in optimizing an AGC system. Many tradeoffs are found in practice; Figure 3.2 shows a basic system.

A TYPICAL AUTOMATIC GAIN CONTROL (AGC) SYSTEM

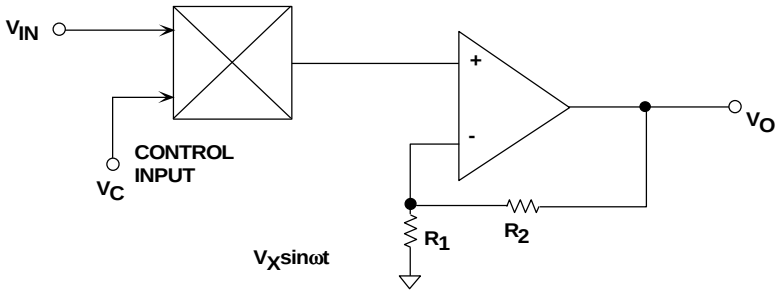


It is interesting to note that an AGC loop actually has two outputs. The obvious output is the amplitude-stabilized signal. The less obvious output is the control voltage to the VCA, which is in reality, a measure of the average amplitude of the input signal. If the system is precisely scaled, the control voltage may be used as a measure of the input signal, sometimes referred to as a *received signal strength indicator* (RSSI).

VOLTAGE CONTROLLED AMPLIFIERS (VCAS)

An analog multiplier can be used as a variable-gain amplifier as shown in Figure 3.3. The control voltage is applied to one input, and the signal to the other. In this configuration, the gain is directly proportional to the control voltage.

USING A MULTIPLIER AS A VOLTAGE-CONTROLLED AMPLIFIER (VCA)

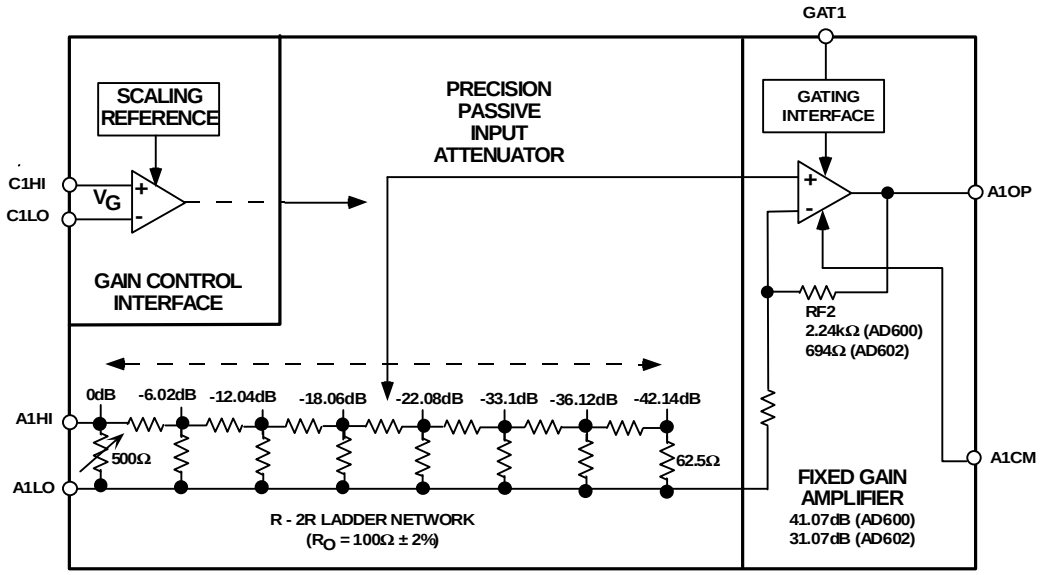


$$V_O = \frac{V_{IN}}{K} \bullet \left(1 + \frac{R_2}{R_1}\right) V_C$$

ANALOG DEVICES

3.3

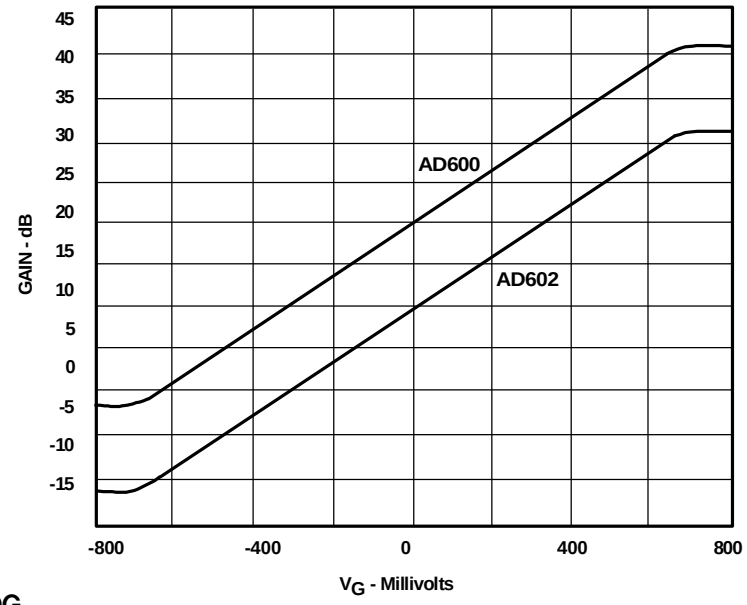
Most VCAs made with analog multipliers have gain which is *linear in volts* with respect to the control voltage, and they tend to be noisy. There is a demand, however, for a VCA which combines a wide gain range with constant bandwidth and phase, low noise with large signal-handling capabilities, and low distortion with low power consumption, while providing accurate, stable, *linear-in-dB* gain. The AD600, AD602, and AD603 achieve these demanding and conflicting objectives with a unique and elegant solution - the X-AMP™ (for *exponential amplifier*). The concept is simple: a fixed-gain amplifier follows a passive, broadband attenuator equipped with special means to alter its attenuation under the control of a voltage (see Figure 3.4). The amplifier is optimized for low input noise, and negative feedback is used to accurately define its moderately high gain (about 30 to 40dB) and minimize distortion. Since this amplifier's gain is fixed, so also are its ac and transient response characteristics, including distortion and group delay; since its gain is high, its input is never driven beyond a few millivolts. Therefore, it is always operating within its small signal response range.



The attenuator is a 7-section (8-tap) R-2R ladder network. The voltage ratio between all adjacent taps is exactly 2, or 6.02dB. This provides the basis for the precise linear-in-dB behavior. The overall attenuation is 42.14dB. As will be shown, the amplifier's input can be connected to any one of these taps, or even *interpolated* between them, with only a small deviation error of about ±0.2dB. The overall gain can be varied all the way from the fixed (maximum) gain to a value 42.14dB less. For example, in the AD600, the fixed gain is 41.07dB (a voltage gain of 113); using this choice, the full gain range is –1.07dB to +41.07dB. The gain is related to the control voltage by the relationship $G_{dB} = 32V_G + 20$ where V_G is in volts. For the AD602, the fixed gain is 31.07dB (a voltage gain of 35.8), and the gain is given by $G_{dB} = 32V_G + 10$.

The gain at $V_G = 0$ is laser trimmed to an absolute accuracy of ±0.2dB. The gain scaling is determined by an on-chip bandgap reference (shared by both channels), laser trimmed for high accuracy and low temperature coefficient. Figure 3.5 shows the gain versus the differential control voltage for both the AD600 and the AD602.

GAIN OF THE AD600/AD602 AS A FUNCTION OF CONTROL VOLTAGE

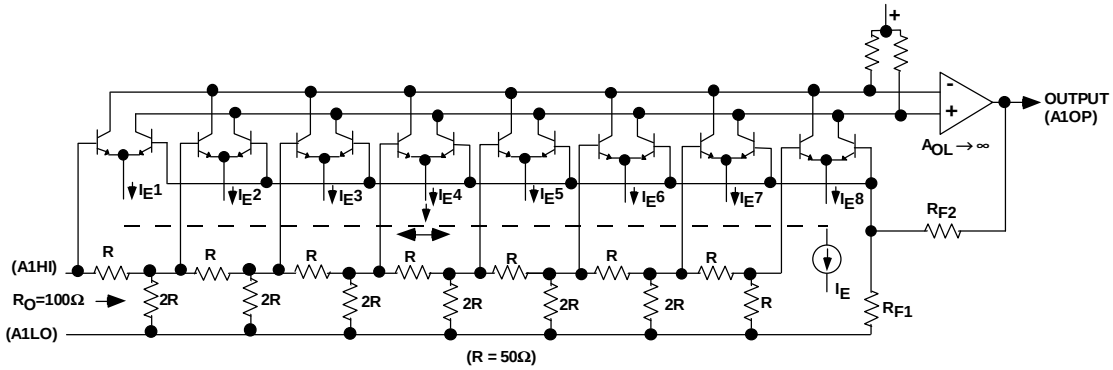


ANALOG DEVICES

3.5

In order to understand the operation of the X-AMP, consider the simplified diagram shown in Figure 3.6. Notice that each of the eight taps is connected to an input of one of eight bipolar differential pairs, used as current-controlled transconductance (g_m) stages; the other input of all these g_m stages is connected to the amplifier's gain-determining feedback network, R_{F1}/R_{F2}. When the emitter bias current, I_E, is directed to one of the 8 transistor pairs (by means not shown here), it becomes the input stage for the complete amplifier.

CONTINUOUS INTERPOLATION BETWEEN TAPS IN THE X-AMP IS PERFORMCE WITH CURRENT-CONTROLLED gm STAGES



ANALOG DEVICES

3.6

When I_E is connected to the pair on the left-hand side, the signal input is connected directly to the amplifier, giving the maximum gain. The distortion is very low, even at high frequencies, due to the careful open-loop design, aided by the negative feedback. If I_E were now to be abruptly switched to the second pair, the overall gain would drop by exactly 6.02dB, and the distortion would remain low, because only one g_m stage remains active.

In reality, the bias current is *gradually* transferred from the first pair to the second. When I_E is equally divided between two gm stages, both are active, and the situation arises where we have an op amp with two input stages fighting for control of the loop, one getting the full signal, and the other getting a signal exactly half as large.

Analysis shows that the effective gain is reduced, not by 3dB, as one might first expect, but rather by 20log1.5, or 3.52dB. This error, when divided equally over the whole range, would amount to a gain ripple of ±0.25dB; however, the interpolation circuit actually generates a Gaussian distribution of bias currents, and a significant fraction of I_E always flows in adjacent stages. This smoothes the gain function and actually lowers the ripple (see Reference 12). As I_E moves further to the right, the overall gain progressively drops.

The total input-referred noise of the X-AMP™ is 1.4nV/√Hz; only slightly more than the thermal noise of a 100Ω resistor which is 1.29nV/√Hz at 25°C. The input-referred noise is constant regardless of the attenuator setting, therefore the output noise is always constant and independent of gain. For the AD600, the amplifier gain is 113 and the output noise spectral density is therefore 1.4nV/√Hz×113, or 158nV/√Hz. Referred to its maximum output of 2V rms, the signal-to-noise ratio would be 82dB in a 1MHz bandwidth. The corresponding signal-to-noise ratio of the AD602 is 10dB greater, or 92dB. Key features of the AD600/AD602 are summarized in Figure 3.7

KEY FEATURES OF THE AD600/AD602 X-AMPS

- **Precise Decibel-Scaled Gain Control**
- **Accurate Absolute Gain Calibration**
- **Low Input-Referred Noise (1.4nV/√Hz)**
- **Constant Bandwidth (dc to 35MHz)**
- **Low Distortion: –60dBc THD at ±1V Output**
- **Stable Group Delay (±2ns Over Gain Range)**
- **Response Time: Less than 1µs for 40dB Gain Change**
- **Low Power (125mW per channel maximum)**
- **Differential Control Inputs**

ANALOG DEVICES

3.7

The AD603 X-AMP is a single version of the AD600/AD602 which provides 90MHz bandwidth. There are two pin-programmable gain ranges: –11dB to +31dB with 90MHz bandwidth, and +9dB to +51dB with 9MHz bandwidth. Key specifications for the AD603 are summarized in Figure 3.8.

KEY FEATURES OF THE AD603 X-AMP

- **Precise "Linear in dB" Gain Control**
- **Pin Programmable Gain Ranges:**

  –11dB to +31dB with 90MHz Bandwidth

  +9dB to + 51dB with 9MHz Bandwidth
- **Bandwidth Independent of Variable Gain**
- **Low Input-Referred Noise (1.3nV/√Hz)**
- **±0.5dB Typical Gain Accuracy**
- **Low Distortion: –60dBc, 1V rms Output @ 10MHz**
- **Low Power (125mW)**
- **8-pin Plastic SOIC or Ceramic DIP**

ANALOG DEVICES

3.8

AN 80 dB RMS-LINEAR-dB MEASUREMENT SYSTEM

RMS/DC converters provide a means to measure the rms value of an arbitrary waveform. They also may provide a low-accuracy logarithmic ("decibel-scaled") output. However, they have a fairly small dynamic range – typically only 50dB. More troublesome is that the bandwidth is roughly proportional to the signal level; for example, the AD636 provides a 3dB bandwidth of 900kHz for an input of 100mV rms, but only a 100kHz bandwidth for an input of 10mV rms. Its "raw" logarithmic output is unbuffered, uncalibrated, and not stable over temperature, requiring considerable support circuitry, including at least two adjustments and a special high-TC resistor.

All of these problems can be eliminated using an RMS/DC converter (i.e.,AD636) merely as *the detector element* in an AGC loop, in which the difference between the rms output of the AD636 and a fixed DC reference is nulled in a loop integrator. The

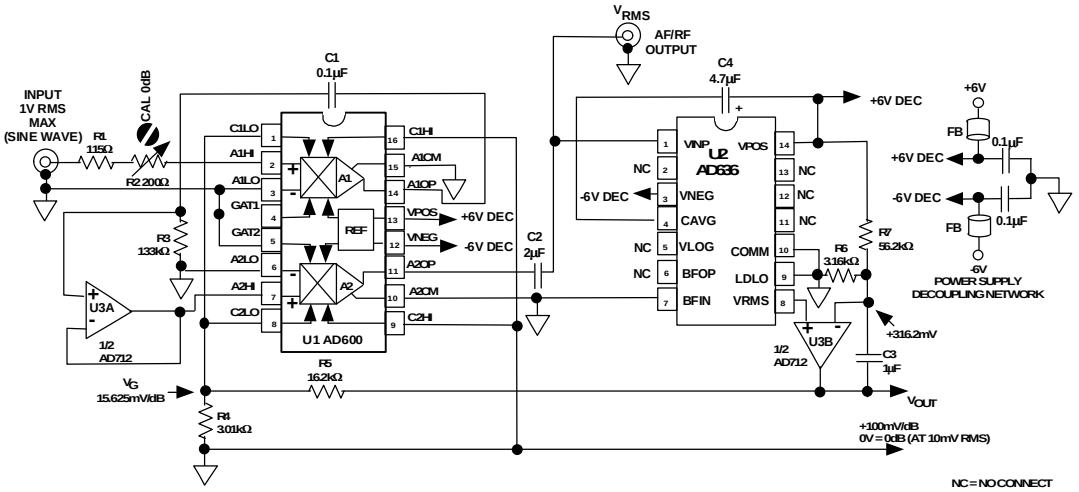
dynamic range and the accuracy with which the signal can be determined are now entirely dependent on the amplifier used in the AGC system. Since the input to the RMS/DC converter is forced to a constant amplitude, close to its maximum input capability, the bandwidth is no longer signal-dependent. If the amplifier has a precise exponential ("linear-dB") gain-control law, its control voltage is forced by the AGC loop to have the general form

$$V_{LOG} = V_S \log_{10} \frac{V_{IN(RMS)}}{V_Z}$$

where V_S is the logarithmic slope and V_Z is the logarithmic intercept, that is, the value of V_{IN} for which V_{LOG} is zero.

Figure 3.9 shows a practical wide-dynamic-range rms measurement system using the AD600. It can handle inputs from 100µV to 1V rms (4 decades) with a constant measurement bandwidth of 20Hz to 2MHz, limited primarily by the AD636 RMS/DC converter. Its logarithmic output is a buffered voltage, accurately-calibrated to 100mV/dB, or 2V per decade, which simplifies the interpretation of the reading when using a DVM, and is arranged to be –4V for an input of 100µV rms input, zero for 10mV, and +4V for a 1V rms input. In terms of the above equation, V_S is 2V and V_Z is 10mV.

A COMPLETE 80dB RMS-LINEAR-dB MEASUREMENT SYSTEM



Note that the peak "log-output" of ±4V requires the use of ±6V supplies for the dual op-amp U3 (AD712), although lower supplies would suffice for the AD600 and AD636. If only ±5V supplies are available, it will either be necessary to use a reduced value for V_S (say, 1V, in which case the peak output would be only ±2V), or to restrict the dynamic range of the signal to about 60dB.

The two amplifiers of the AD600 are used in cascade. The modest bandwidth of the unity-gain buffer U3A acts as a low pass filter, thus eliminating the risk of instability at the highest gains. The buffer also allows the use of a high-impedance coupling network (C1/R3) which introduces a high-pass corner at about 12Hz. An input attenuator of 10dB (× 0.316) is now provided by R1 + R2 operating in conjunction with the AD600's input resistance of 100Ω. The adjustment provides exact calibration of V_Z in critical applications, but R1 and R2 may be replaced by a fixed resistor of 215Ω if very close calibration is not needed, since the input resistance of the AD600 (and all the other key parameters of it and the AD636) are already laser-trimmed for accurate operation. This attenuator allows inputs as large as ±4V to be accepted, that is, signals with an rms value of 1V combined with a crest-factor of up to 4.

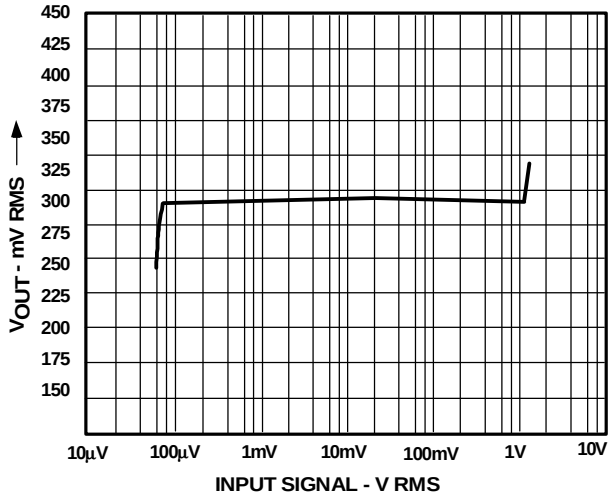
The output of A2 is AC-coupled via another 12Hz high-pass filter formed by C2 and the 6.7kΩ input resistance of the AD636. The averaging time-constant for the RMS/DC converter is determined by C4. The unbuffered output of the AD636 (at pin 8) is compared with a fixed voltage of +316mV set by the positive supply voltage of +6V and resistors R6 and R7. (V_Z is proportional to this voltage, and systems requiring greater calibration accuracy should replace the supply-dependent reference with a more stable source. However, V_S is independent of the supply voltages, being determined by the band-gap reference in the X-AMP.) Any difference in these voltages is integrated by the op-amp U3B, with a time-constant of 3ms formed by the parallel sum of R6/R7 and C3.

If the gain of the AD600 is too high, V_{OUT} will be greater than the "set-point" of 316mV, causing the output of U3B – that is, V_{LOG} – to ramp up (note that the integrator is non-inverting). A fraction of V_{LOG} is connected to the *inverting* gain-control inputs of the AD600, causing the gain to be reduced, as required, until V_{OUT} is equal to 316mV (DC), at which time the AC voltage at the output of A2 is forced to exactly 316mV (rms). This fraction is set by R4 and R5 such that a 15.625mV change in the control voltages of A1 and A2 – which would change the gain of the two cascaded amplifiers by 1 dB – requires a change of 100mV at V_{LOG}. Since A2 is forced to operate well below its limiting level, waveforms of high crest-factor can be tolerated throughout the amplifier.

To verify the operation, assume an input of 10mV rms is applied to the input, resulting in a voltage of 3.16mV rms at the input to A1 (due to the 10dB attenuator). If the system performs as claimed, V_{LOG} (and hence V_G) should be zero. This being the case, the gain of both A1 and A2 will be 20dB and the output of the AD600 will be 100 times (40dB) greater than its input, 316mV rms. This is the input required at the AD636 to balance the loop, confirming the basic operation. Note that unlike most AGC circuits, (which often have a high gain/temperature coefficient due to the internal "kT/q" scaling), the voltages and thus the output of this measurement system are very stable over temperature. This behavior arises directly from the exact exponential calibration of the ladder attenuator.

Typical results are shown for a sinewave input at 100kHz. Figure 3.10 shows that the output is held very close to the set-point of 316mV rms over an input range in excess of 80dB.

SIGNAL OUTPUT V_{OUT} VERSUS INPUT LEVEL

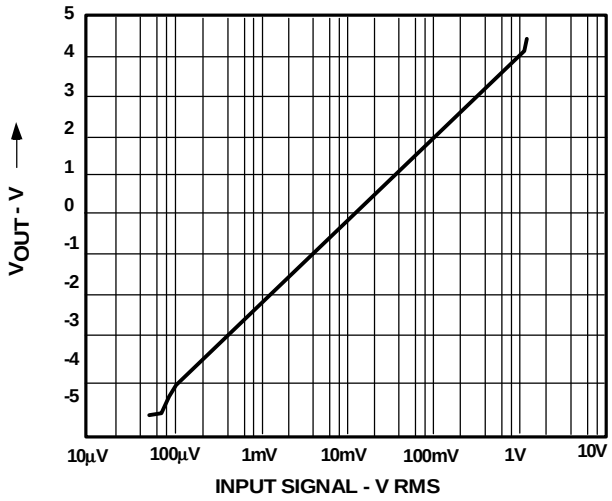


ANALOG DEVICES

3.10

Figure 3.11 shows the "decibel" output voltage, V_{LOG}, and Figure 3.12 shows that the *deviation* from the ideal output logarithmic output is within ±1 dB for the 80dB range from 80µV to 800mV.

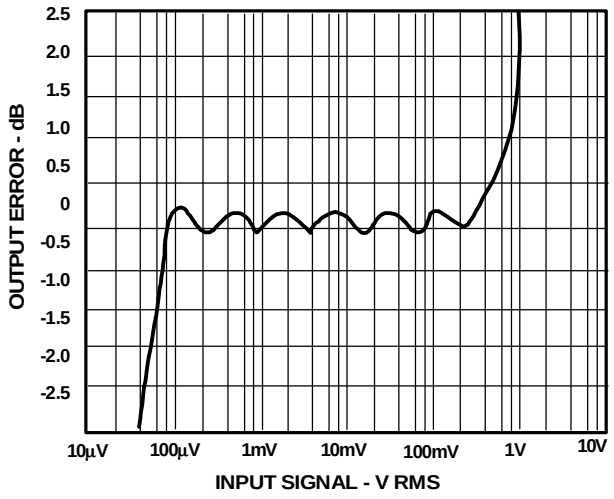
THE LOGARITHMIC OUTPUT V_{LOG} VERSUS INPUT SIGNAL LEVEL



ANALOG DEVICES

3.11

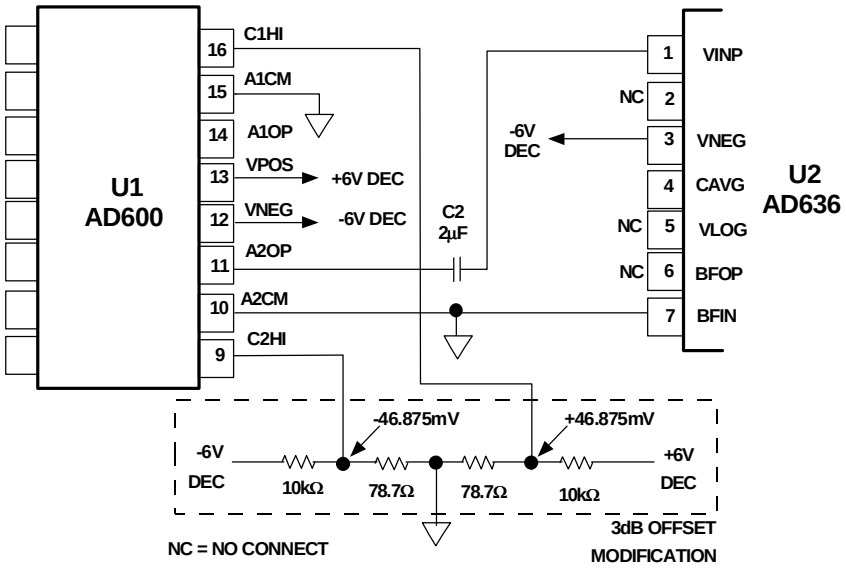
DEVIATION FROM THE IDEAL LOGARITHMIC OUTPUT



By suitable choice of the input attenuator, R1+R2, this could be centered to cover any range from 25µV to 250mV to, say, 1mV to 10V, with appropriate correction to the value of V_Z. (Note that V_S is not affected by the changes in the range). The gain ripple of ±0.2dB seen in this curve is the result of the finite interpolation error of the X-AMP. It occurs with a periodicity of 12dB – twice the separation between the tap points in each amplifier section.

This ripple can be canceled whenever the X-AMP stages are cascaded by introducing a 3dB offset between the two pairs of control voltages. A simple means to achieve this is shown in Figure 3.13: the voltages at C1HI and C2HI are "split" by ±46.875mV, or ±1.5dB. Alternatively, either one of these pins can be individually offset by 3dB, and a 1.5dB gain adjustment made at the input attenuator (R1+R2). The error curve shown in Figure 3.14 demonstrates that over the central portion of the range, the output voltage can be maintained very close to the ideal value. The penalty for this modification is higher errors at both ends of the range.

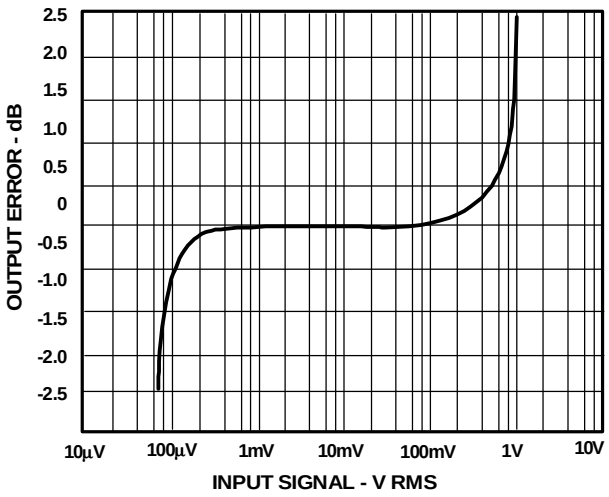
METHOD FOR CANCELING THE GAIN-CONTROL RIPPLE



ANALOG DEVICES

3.13

LOGARITHMIC ERROR USING THE PREVIOUS CIRCUIT MODIFICATION

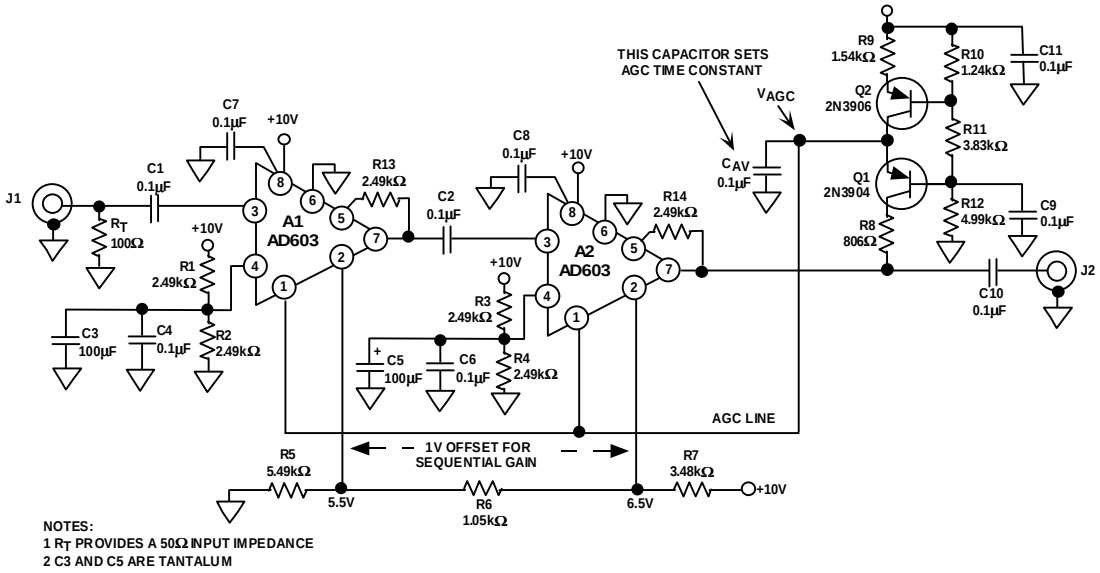


ANALOG DEVICES

3.14

Figure 3.15 shows the ease with which the AD603 (90MHz X-AMP) can be used as a high speed AGC amplifier. The circuit uses few parts, has a linear-in-dB gain, operates from a single supply, uses two cascaded amplifiers in sequential gain mode for maximum S/N ratio (see the data sheet for the AD600/AD602, or AD603 for a complete description of the methods for cascading X-AMPS), and external resistor programs each amplifier's gain. It also uses a simple temperature-compensated detector.

A 40MHz, 80dB, LOW-NOISE AGC AMPLIFIER USING THE AD603



ANALOG DEVICES

3.15

The circuit operates from a single +10V supply. Resistors R1, R2 and R3, R4 bias the common pins of A1 and A2 at 5V. This pin is a low impedance point and must have a low impedance path to ground, provided by the 100µF tantalum capacitor and the 0.1µF ceramic capacitors.

The cascaded amplifiers operate in sequential gain. The offset voltage between the pins 2 (GNEG) of A1 and A2 is 1.05V (42.14dB x 25mV/dB), provided by a voltage divider consisting of resistors R5, R6, and R7. Using standard values, the offset is not exact but is not critical for this application.

The gain of both A1 and A2 is programmed by resistors R13 and R14, respectively, to be about 42dB; thus the maximum gain of the circuit is twice that, or 84dB. The gain-control range can be shifted up by as much as 20dB by appropriate choices of R13 and R14.

The circuit operates as follows. A1 and A2 are cascaded. Capacitor C1 and the 100Ω of resistance at the input of A1 form a time-constant of 10µs. C2 blocks the small DC offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 16kHz, eliminating low frequency noise.

A half-wave detector is used based on Q1 and R8. The current into capacitor C_{AV} is the difference between the collector current of Q2 (biased to be 300µA at 27°C, 300K) and the collector current of Q1, which increases with the amplitude of the output signal. The automatic gain control voltage, V_{AGC}, is the time-integral of this error current. In order for V_{AGC} (and thus the gain) to remain insensitive to short-term amplitude fluctuations in the output signal, the rectified current in Q1 must,

on average, exactly balance the current in Q2. If the output of A2 is too small to do this, V_{AGC} will increase, causing the gain to increase, until Q1 conducts sufficiently.

Consider the case where R8 is zero and the output voltage V_{OUT} is a square wave at, say 455kHz, that is, well above the corner frequency of the control loop.

During the time V_{OUT} is negative with respect to the base voltage of Q1, Q1 conducts; when V_{OUT} is positive, it is cut off. Since the average collector current of Q1 is forced to be 300µA, and the square wave has a duty cycle of 1:1, Q1's collector current when conducting must be 600µA. With R8 omitted, the peak amplitude of V_{OUT} is forced to be just the V_{BE} of Q1 at 600µA, typically about 700mV, or $2V_{BE}$ peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically –1.7mV/°C. Although this may not be troublesome in some applications, the correct value of R8 will render the output stable with temperature.

To understand this, first note that the current in Q2 is made to be proportional to absolute temperature (PTAT). For the moment, continue to assume that the signal is a square wave.

When Q1 is conducting, V_{OUT} is now the sum of V_{BE} and a voltage which is PTAT and which can be chosen to have an equal but opposite TC to that of V_{BE}. This is actually nothing more than an application of the "bandgap voltage reference" principle. When R8 is chosen such that the sum of the voltage across it and the V_{BE} of Q1 is close to the bandgap voltage of about 1.2V, V_{OUT} will be stable over a wide range of temperatures, provided, of course, that Q1 and Q2 share the same thermal environment.

Since the average emitter current is 600µA during each half-cycle of the square wave, a resistor of 833Ω would add a PTAT voltage of 500mV at 300K, increasing by 1.66mV/°C. In practice, the optimum value will depend on the type of transistor used, and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the inexpensive 2N3904/2N3906 pair and sine wave signals, the recommended value is 806Ω.

This resistor also serves to lower the peak current in Q1 when more typical signals (usually sinusoidal) are involved, and the 1.8kHz lowpass filter it forms with C_{AV} helps to minimize distortion due to ripple in V_{AGC}. Note that the output amplitude under sine wave conditions will be higher than for a square wave, since the average value of the current for an ideal rectifier would be 0.637 times as large, causing the output amplitude to be 1.2V/0.637=1.88V, or 1.33V rms. In practice, the somewhat nonideal rectifier results in the sine wave output being regulated to about 1.4Vrms, or 3.6V p-p.

The bandwidth of the circuit exceeds 40MHz. At 10.7MHz, the AGC threshold is 100µV (–67dBm) and its maximum gain is 83dB, 20log(1.4V/100µV). The circuit holds its output at 1.4V rms for inputs as low as –67dBm to +15dBm (82dB), where the input signal exceeds the AD603's maximum input rating. For a +10dBm input at 10.7MHz, the second harmonic is 34dB down from the fundamental, and the third harmonic is 35dB down.

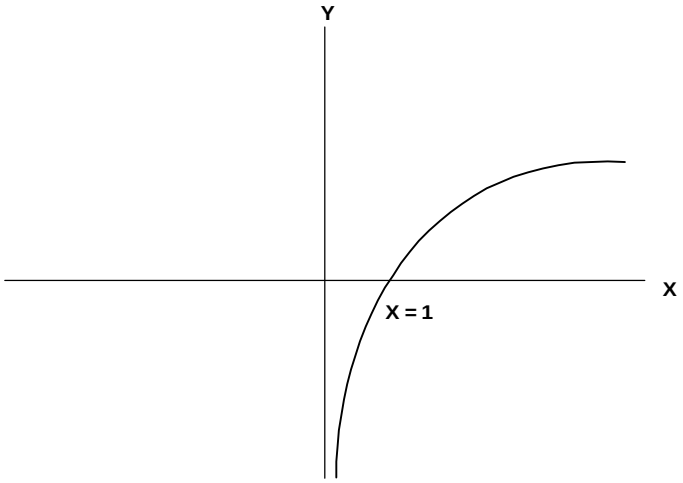
LOGARITHMIC AMPLIFIERS

The term "Logarithmic Amplifier" (generally abbreviated to "log amp") is something of a misnomer, and "Logarithmic Converter" would be a better description. The conversion of a signal to its equivalent logarithmic value involves a nonlinear operation, the consequences of which can be confusing if not fully understood. It is important to realize that many of the familiar concepts of linear circuits are irrelevant to log amps. For example, the incremental gain of an ideal log amp approaches infinity as the input approaches zero, and a change of offset at the output of a log amp is equivalent to a change of amplitude at its input - not a change of input offset.

For the purposes of simplicity in our initial discussions, we shall assume that both the input and the output of a log amp are voltages, although there is no particular reason why logarithmic current, transimpedance, or transconductance amplifiers should not also be designed.

If we consider the equation y = log(x) we find that every time x is multiplied by a constant A, y increases by another constant A1. Thus if log(K) = K1, then log(AK) = K1 + A1, log(A^2K) = K1 + 2A1, and log(K/A) = K1 – A1. This gives a graph as shown in Figure 3.16, where y is zero when x is unity, y approaches minus infinity as x approaches zero, and which has no values for x for which y is negative.

GRAPH OF Y = LOG(X)



On the whole, log amps do not behave in this way. Apart from the difficulties of arranging infinite negative output voltages, such a device would not, in fact, be very useful. A log amp must satisfy a transfer function of the form

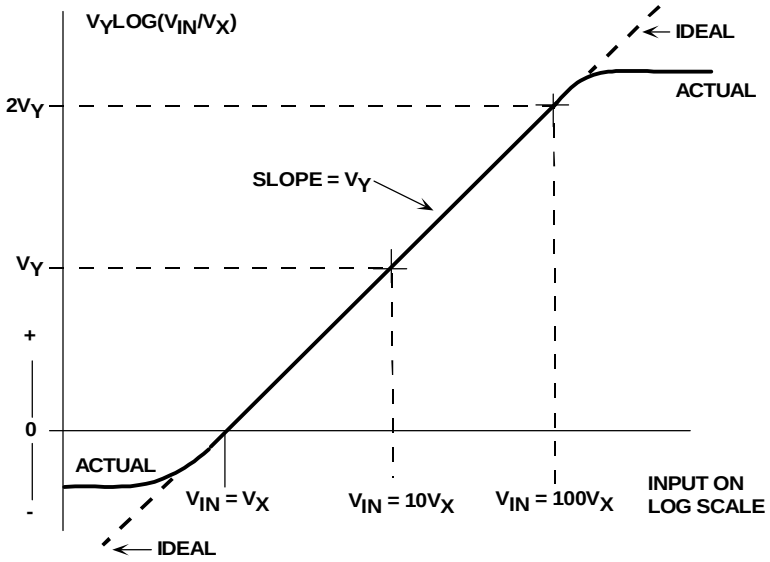
$V_{out} = V_y \log(V_{in}/V_x)$

over some range of input values which may vary from 100:1 (40dB) to over 1,000,000:1 (120dB).

With inputs very close to zero, log amps cease to behave logarithmically, and most then have a linear V_{in}/V_{out} law. This behavior is often lost in device noise. Noise often limits the dynamic range of a log amp. The constant, V_y,has the dimensions of voltage, because the output is a voltage. The input, V_{in}, is divided by a voltage, V_x, because the argument of a logarithm must be a simple dimensionless ratio.

A graph of the transfer characteristic of a log amp is shown in Figure 3.17. The scale of the horizontal axis (the input) is logarithmic, and the ideal transfer characteristic is a straight line. When $V_{in} = V_x$, the logarithm is zero (log 1 = 0). V_x is therefore known as the *intercept voltage* of the log amp because the graph crosses the horizontal axis at this value of V_{in}.

LOG AMP TRANSFER FUNCTION



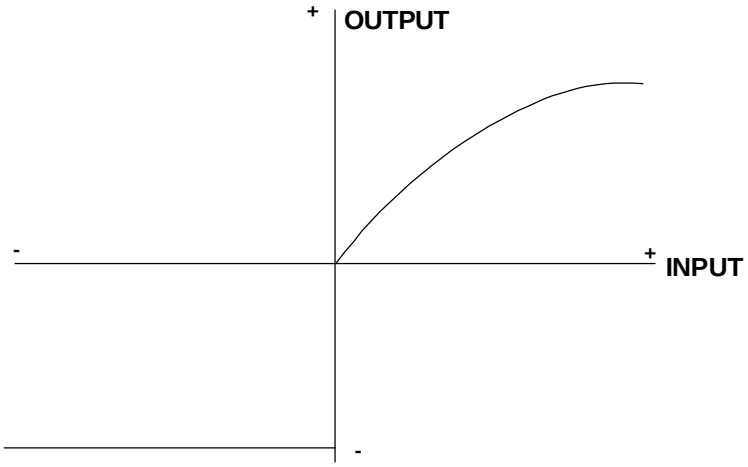
ANALOG DEVICES

3.17

The slope of the line is proportional to V_y. When setting scales, logarithms to the base 10 are most often used because this simplifies the relationship to decibel values: when $V_{in} = 10V_x$,the logarithm has the value of 1, so the output voltage is V_y. When $V_{in} = 100V_x$, the output is $2V_y$,and so forth. V_y can therefore be viewed either as the "slope voltage" or as the "volts per decade factor."

The logarithm function is indeterminate for negative values of x. Log amps can respond to negative inputs in three different ways: (1) They can give a fullscale negative output as shown in Figure 3.18. (2) They can give an output which is proportional to the log of the absolute value of the input and disregards its sign as shown in Figure 3.19. This type of log amp can be considered to be a full-wave detector with a logarithmic characteristic, and is often referred to as a *detecting* log amp. (3) They can give an output which is proportional to the log of the absolute value of the input and has the same sign as the input as shown in Figure 3.20. This type of log amp can be considered to be a video amp with a logarithmic characteristic, and may be known as a *logarithmic video* (*log video*) amplifier or, sometimes, a *true log amp* (although this type of log amp is rarely used in video-display-related applications).

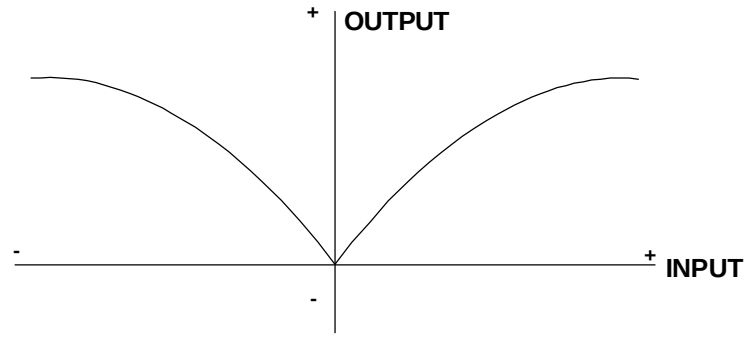
BASIC LOG AMP
(SATURATES WITH NEGATIVE INPUT)



ANALOG DEVICES

3.18

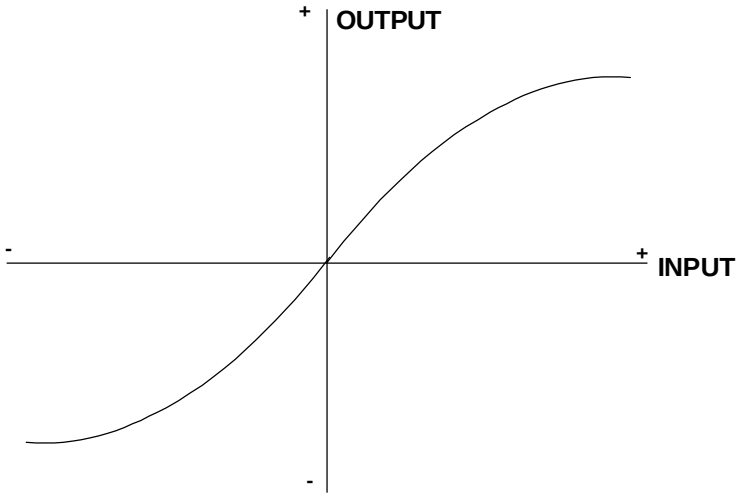
DETECTING LOG AMP
(OUTPUT POLARITY INDEPENDENT OF INPUT POLARITY)



ANALOG DEVICES

3.19

LOG VIDEO OR "TRUE LOG AMP" (SYMMETRICAL RESPONSE TO POSITIVE OR NEGATIVE SIGNALS)



ANALOG DEVICES

3.20

There are three basic architectures which may be used to produce log amps: the *basic diode log amp*, the *successive detection log amp*, and the *"true log amp"* which is based on cascaded semi-limiting amplifiers.

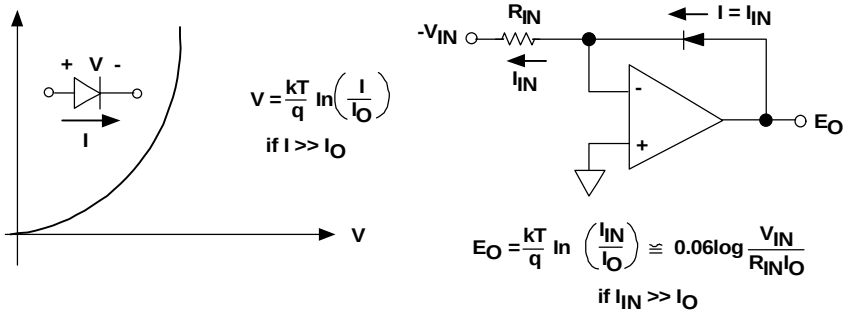
The voltage across a silicon diode is proportional to the logarithm of the current through it. If a diode is placed in the feedback path of an inverting op-amp, the output voltage will be proportional to the log of the input current as shown in Figure 3.21. In practice, the dynamic range of this configuration is limited to 40-60dB because of non-ideal diode characteristic, but if the diode is replaced with a diode-connected transistor as shown in Figure 3.22, the dynamic range can be extended to 120dB or more. This type of log amp has three disadvantages: (1) both the slope and intercept are temperature dependent; (2) it will only handle unipolar signals; and (3) its bandwidth is both limited and dependent on signal amplitude.

Where several such log amps are used on a single chip to produce an analog computer which performs both log and antilog operations, the temperature variation in the log operations is unimportant, since it is compensated by a similar variation in the antilogging. This makes possible the AD538, a monolithic analog computer which can multiply, divide, and raise to powers. Where actual logging is required, however, the AD538 and similar circuits require temperature compensation (Reference 7). The major disadvantage of this type of log amp for high frequency applications, though, is its limited frequency response - which cannot be overcome. However carefully the amplifier is designed, there will always be a residual feedback capacitance C_C (often known as Miller capacitance), from output to input which limits the high frequency response.

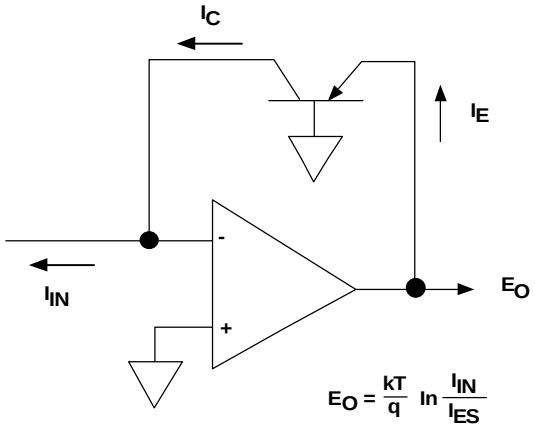
What makes this Miller capacitance particularly troublesome is that the impedance of the emitter-base junction is inversely proportional to the current flowing in it - so that if the log amp has a dynamic range of 1,000,000:1, then its bandwidth will also vary by 1,000,000:1. In practice, the variation is less because other considerations

limit the large signal bandwidth, but it is very difficult to make a log amp of this type with a small-signal bandwidth greater than a few hundred kHz.

THE DIODE / OP-AMP LOG AMP



TRANSISTOR / OP-AMP LOG AMP

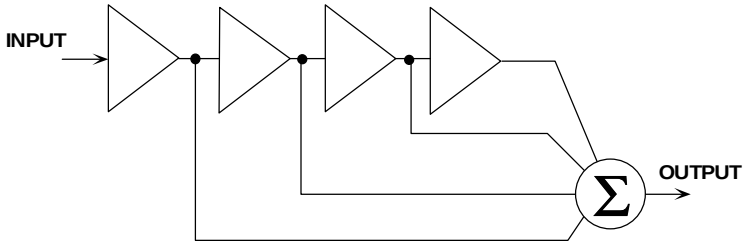


For high frequency applications, therefore, *detecting* and *true log* architectures are used. Although these differ in detail, the general principle behind their design is common to both: instead of one amplifier having a logarithmic characteristic, these designs use a number of similar cascaded linear stages having well-defined large signal behavior.

Consider N cascaded limiting amplifiers, the output of each driving a summing circuit as well as the next stage (Figure 3.23). If each amplifier has a gain of A dB,

the small signal gain of the strip is NA dB. If the input signal is small enough for the last stage not to limit, the output of the summing amplifier will be dominated by the output of the last stage.

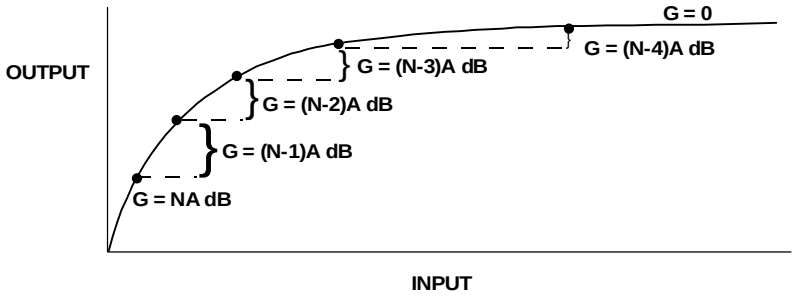
BASIC MULTI-STAGE LOG AMP ARCHITECTURE



As the input signal increases, the last stage will limit. It will now make a fixed contribution to the output of the summing amplifier, but the incremental gain to the summing amplifier will drop to (N-1)A dB. As the input continues to increase, this stage in turn will limit and make a fixed contribution to the output, and the incremental gain will drop to (N-2)A dB, and so forth - until the first stage limits, and the output ceases to change with increasing signal input.

The response curve is thus a set of straight lines as shown in Figure 3.24. The total of these lines, though, is a very good approximation to a logarithmic curve, and in practical cases, is an even better one, because few limiting amplifiers, especially high frequency ones, limit quite as abruptly as this model assumes.

BASIC MULTI-STAGE LOG AMP RESPONSE (UNIPOLAR CASE)

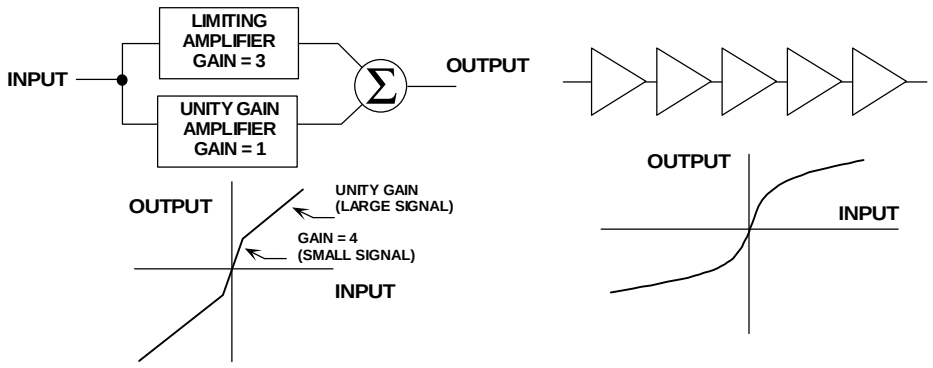


The choice of gain, A, will also affect the log linearity. If the gain is too high, the log approximation will be poor. If it is too low, too many stages will be required to achieve the desired dynamic range. Generally, gains of 10 to 12dB (3x to 4x) are chosen.

This is, of course, an ideal and very general model - it demonstrates the principle, but its practical implementation at very high frequencies is difficult. Assume that there is a delay in each limiting amplifier of t nanoseconds (this delay may also change when the amplifier limits but let's consider first order effects!). The signal which passes through all N stages will undergo delay of Nt nanoseconds, while the signal which only passes one stage will be delayed only t nanoseconds. This means that a small signal is delayed by Nt nanoseconds, while a large one is "smeared", and arrives spread over Nt nanoseconds. A nanosecond equals a foot at the speed of light, so such an effect represents a spread in position of Nt feet in the resolution of a radar system-which may be unacceptable in some systems (for most log amp applications this is not a problem).

A solution is to insert delays in the signal paths to the summing amplifier, but this can become complex. Another solution is to alter the architecture slightly so that instead of limiting gain stages, we have stages with small signal gain of A and large signal (incremental) gain of unity (0dB). We can model such stages as two parallel amplifiers, a limiting one with gain, and a unity gain buffer, which together feed a summing amplifier as shown in Figure 3.25.

STRUCTURE AND PERFORMANCE OF "TRUE" LOG AMP ELEMENT AND OF A LOG AMP FORMED BY SEVERAL SUCH ELEMENTS

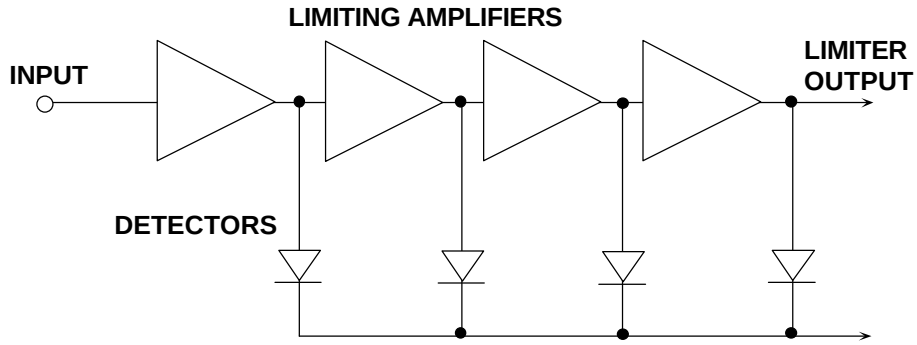


ANALOG DEVICES

3.25

Figure 3.25 shows that such stages, cascaded, form a log amp without the necessity of summing from individual stages. Both the multi-stage architectures described above are *video* log amplifiers, or *true log* amplifiers, but the most common type of high frequency log amplifier is the *successive detection* log amp architecture shown in Figure 3.26.

SUCCESSIVE DETECTION LOGARITHMIC AMPLIFIER WITH LOG AND LIMITER OUTPUTS



- **DETECTORS MAY BE FULL OR HALF WAVE**
- **SHOULD BE CURRENT OUTPUT DEVICES (NOT SIMPLE DIODES) SO THAT OUTPUTS MAY BE SUMMED WITHOUT ADDITIONAL SUMMING COMPONENTS BEING NECESSARY**

ANALOG DEVICES

3.26

The *successive detection* log amp consists of cascaded limiting stages as described above, but instead of summing their outputs directly, these outputs are applied to detectors, and the detector outputs are summed as shown in Figure 3.26. If the

detectors have current outputs, the summing process may involve no more than connecting all the detector outputs together.

Log amps using this architecture have two outputs: the log output and a limiting output. In many applications, the limiting output is not used, but in some (FM receivers with "S"-meters, for example), both are necessary. The limited output is especially useful in extracting the phase information from the input signal in polar demodulation techniques.

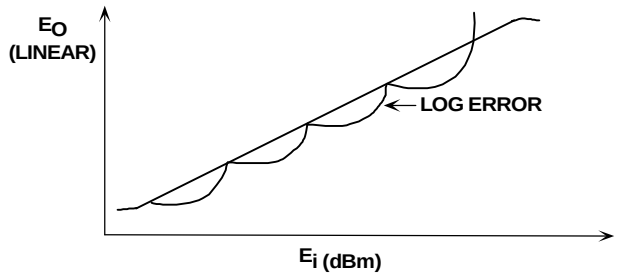
The log output of a successive detection log amplifier generally contains amplitude information, and the phase and frequency information is lost. This is not necessarily the case, however, if a half-wave detector is used, and attention is paid to equalizing the delays from the successive detectors - but the design of such log amps is demanding.

The specifications of log amps will include *noise, dynamic range, frequency response* (some of the amplifiers used as successive detection log amp stages have low frequency as well as high frequency cutoff), the *slope of the transfer characteristic* (which is expressed as V/dB or mA/dB depending on whether we are considering a voltage- or current-output device), the *intercept point* (the input level at which the output voltage or current is zero), and the *log linearity*. (See Figures 3.27 and 3.28)

KEY PARAMETERS OF LOG AMPS

- **NOISE: The Noise Referred to the Input (RTI) of the Log Amp. It May Be Expressed as a Noise Figure or as a Noise Spectral Density (Voltage, Current, or Both) or as a Noise Voltage, a Noise Current, or Both**
- **DYNAMIC RANGE: Range of Signal Over Which the Amplifier Behaves in a Logarithmic Manner (Expressed in dB)**
- **FREQUENCY RESPONSE: Range of Frequencies Over Which the Log Amp Functions Correctly**
- **SLOPE: Gradient of Transfer Characteristic in V/dB or mA/dB**
- **INTERCEPT POINT: Value of Input Signal at Which Output is Zero**
- **LOG LINEARITY: Deviation of Transfer Characteristic (Plotted on log/lin Axes) from a Straight Line (Expressed in dB)**

LOG LINEARITY



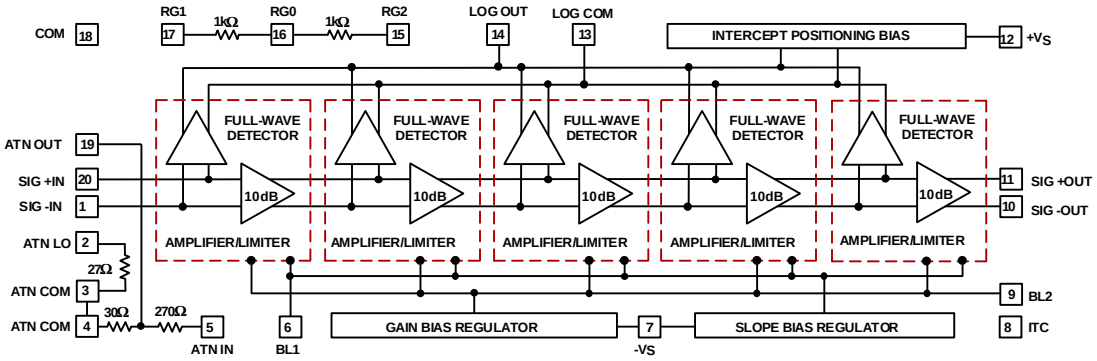
ANALOG DEVICES

3.28

In the past, it has been necessary to construct high performance, high frequency successive detection log amps (called log strips) using a number of individual monolithic limiting amplifiers such as the Plessey SL-1521-series (see Reference 16). Recent advances in IC processes, however, have allowed the complete log strip function to be integrated into a single chip, thereby eliminating the need for costly hybrid log strips.

The AD641 log amp contains five limiting stages (10dB per stage) and five full-wave detectors in a single IC package, and its logarithmic performance extends from dc to 250MHz. Furthermore, its amplifier and full-wave detector stages are balanced so that, with proper layout, instability from feedback via supply rails is unlikely. A block diagram of the AD641 is shown in Figure 3.29. Unlike many previous integrated circuit log amps, the AD641 is laser trimmed to high absolute accuracy of both slope and intercept, and is fully temperature compensated. Key features of the AD641 are summarized in Figure 3.30. The transfer function for the AD641 as well as the log linearity is shown in Figure 3.31.

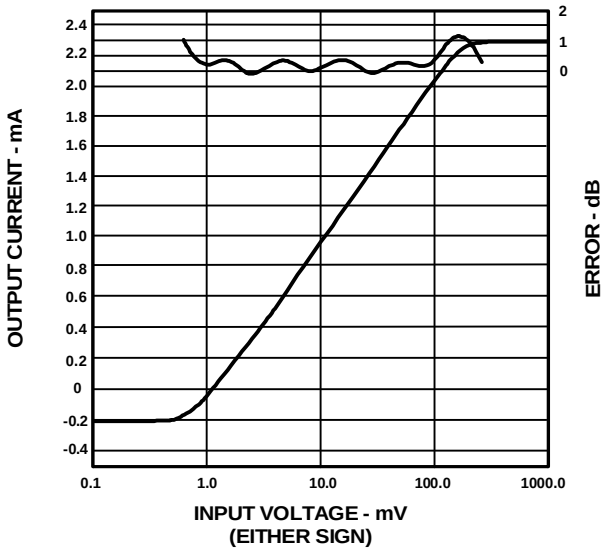
BLOCK DIAGRAM OF THE AD641 MONOLITHIC LOG AMP



AD641 KEY FEATURES

- 44dB Dynamic Range
- Bandwidth dc to 250MHz
- Laser-Trimmed Slope of 1mA/decade - Temperature Stable
- Laser-Trimmed Intercept of 1mV - Temperature Stable
- Less than 2dB Log Non-Linearity
- Limiter Output: ±1.6dB Gain Flatness, ±2° Phase Variation for -44dBm to 0dBm inputs @ 10.7MHz
- Balanced Circuitry for Stability
- Minimal External Component Requirement

DC LOGARITHMIC TRANSFER FUNCTION AND ERROR CURVE FOR SINGLE AD641



ANALOG DEVICES

3.31

Because of its high accuracy, the actual waveform driving the AD641 must be considered when calculating responses. When a waveform passes through a log function generator, the mean value of the resultant waveform changes. This does not affect the slope of the response, but the apparent intercept is modified according to Figure 3.32.

THE EFFECT OF WAVEFORM ON INTERCEPT POINT

INPUT WAVEFORM	PEAK OR RMS	INTERCEPT FACTOR	ERROR (RELATIVE TO A DC INPUT)
Square Wave	Either	1	0.00dB
Sine Wave	Peak	2	–6.02dB
Sine Wave	RMS	1.414 (√2)	–3.01dB
Triwave	Peak	2.718 (e)	–8.68dB
Triwave	RMS	1.569 (e/√3)	–3.91dB
Gaussian Noise	RMS	1.887	–5.52dB

ANALOG DEVICES

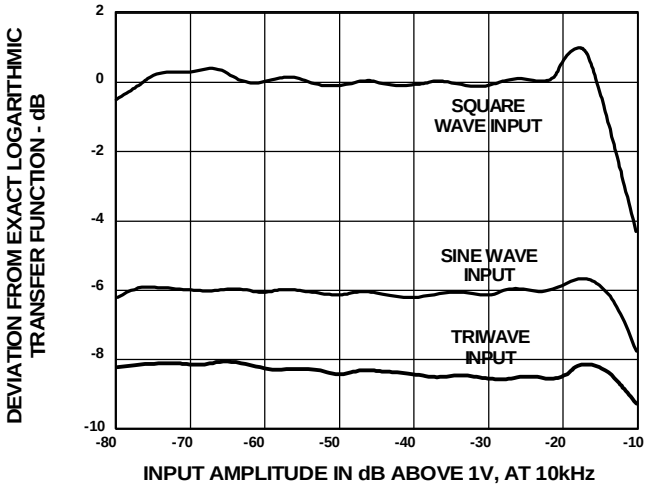
3.32

The AD641 is calibrated and laser trimmed to give its defined response to a DC level or a symmetrical 2kHz square wave. It is also specified to have an intercept of 2mV for a sinewave input (that is to say a 2kHz sinewave of amplitude 2mV peak [not

peak-to-peak] gives the same mean output signal as a DC or square wave signal of 1mV).

The waveform also affects the ripple or nonlinearity of the log response. This ripple is greatest for DC or square wave inputs because every value of the input voltage maps to a single location on the transfer function, and thus traces out the full nonlinearities of the log response. By contrast, a general time-varying signal has a continuum of values within each cycle of its waveform. The averaged output is thereby "smoothed" because the periodic deviations away from the ideal response, as the waveform "sweeps over" the transfer function, tend to cancel. As is clear in Figure 3.33, this smoothing effect is greatest for a triwave.

THE EFFECT OF WAVEFORM ON AD641 LOG LINEARITY



ANALOG DEVICES

3.33

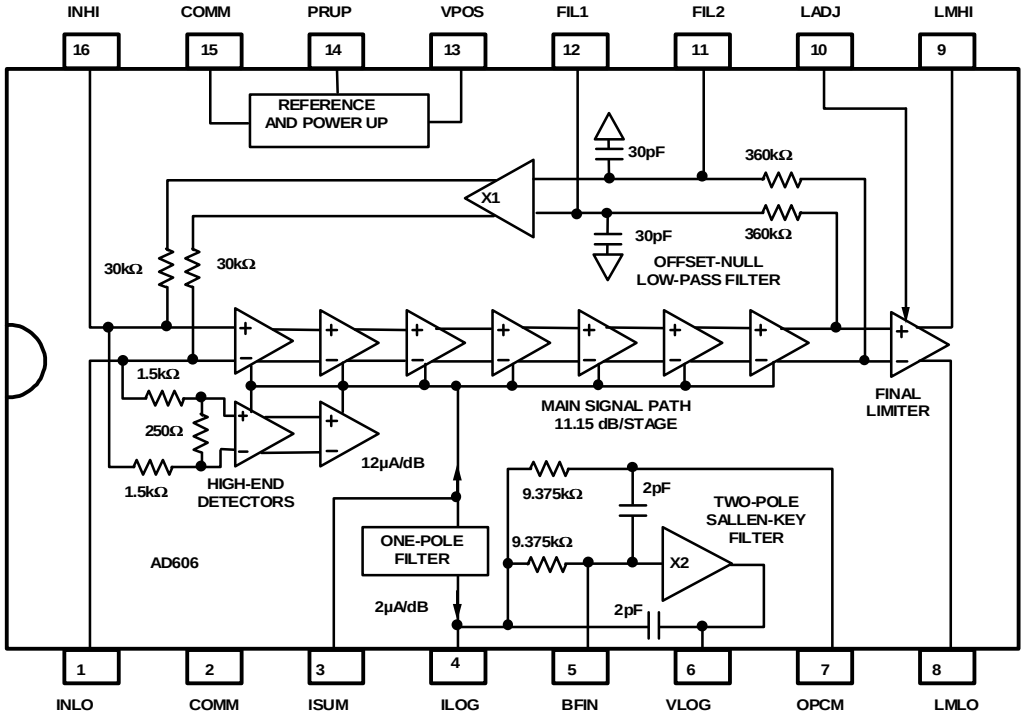
Each of the five stages in the AD641 has a gain of 10dB and a full-wave detected output. The transfer function for the device was shown in Figure 3.21 along with the error curve. Note the excellent log linearity over an input range of 1 to 100mV (40dB). Although well suited to RF applications, the AD641 is dc-coupled throughout. This allows it to be used in LF and VLF systems, including audio measurements, sonar, and other instrumentation applications requiring operation to low frequencies or even dc.

The limiter output of the AD641 has better than 1.6dB gain flatness (-44dBm to 0dBm @ 10.7MHz) and less than 2° phase variation, allowing it to be used as a polar demodulator

The AD606 is a complete monolithic 50MHz bandwidth log amp using 9 stages of successive detection, and is shown in Figure 3.34. Key specifications are summarized in Figure 3.35. Seven of the amplifier/detector stages handle inputs from –80dBm (32µV rms) up to about –14dBm (45mV rms). The noise floor is about –83dBm (18µV rms). Another two parallel stages receive the input attenuated by 22.3dB, and respond to inputs up to +10dBm (707mV rms). The gain of each stage is 11.15dB and is accurately stabilized over temperature by a precise biasing system.

The AD606 provides both logarithmic and limited outputs. The logarithmic output is from a three-pole post-demodulation lowpass filter and provides an output voltage of +0.1V DC to +4V DC. The logarithmic scaling is such that the output is +0.5V for a sinusoidal input of –75dBm, and +3.5V at an input of +5dBm. Over this range, the log linearity is typically within ±0.4dB.

AD606 50MHz, 80dB LOG AMP BLOCK DIAGRAM



ANALOG DEVICES

3.34

AD606 LOG AMP KEY FEATURES

- **Dynamic Range: –75dBm to +5dBm (80dB)**
- **Input Noise: < 1.5nV/√Hz**
- **Usable from 200Hz to Greater than 50MHz**
- **Slope: 37.5mV/dB Voltage Output**
- **On-Chip Lowpass Output Filter**
- **Limiter Output: ±1.6dB Gain Flatness, ±2° Phase Variation for -44dBm to 0dBm inputs @ 10.7MHz**
- **+5V Single-Supply, 65mW Power Consumption**

ANALOG DEVICES

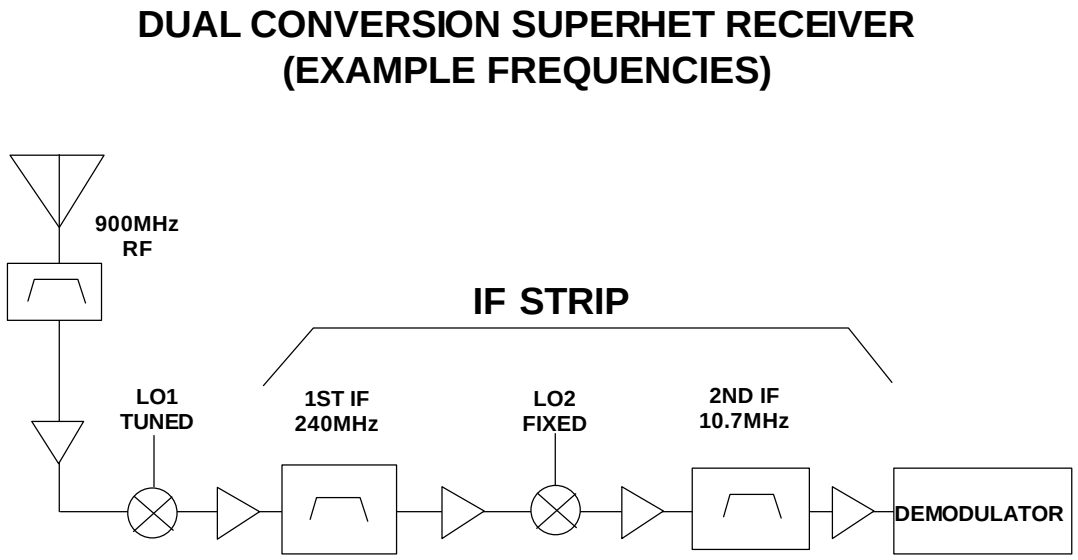
3.35

The AD606 can operate above and below these limits, with reduced linearity, to provide as much as 90dB of conversion range. A second lowpass filter automatically nulls the input offset of the first stage down to the submicrovolt level.

The AD606's limiter output provides a hard-limited signal output as a differential current of ±1.2mA from open-collector outputs. In a typical application, both of these outputs are loaded by 200Ω resistors to provide a voltage gain of more than 90dB from the input. This limiting amplifier has exceptionally low amplitude-to-phase conversion. The limiter output has ±1dB output flatness and ±3° phase stability over an 80dB range at 10.7MHz.

RECEIVER OVERVIEW
Walt Kester, Bob Clarke

We will now consider how the previously discussed building blocks can be used in designing a receiver. First, consider the analog superheterodyne receiver invented in 1917 by Major Edwin H. Armstrong (see Figure 3.36). This architecture represented a significant improvement over single-stage direct conversion (homodyne) receivers which had previously been constructed using tuned RF amplifiers, a single detector, and an audio gain stage. A significant advantage of the superheterodyne receiver is that it is much easier and more economical to have the gain and selectivity of a receiver at fixed intermediate frequencies (IF) than to have the gain and frequency-selective circuits "tune" over a band of frequencies.



ANALOG DEVICES **3.36**

The receiver shown is a dual conversion receiver with two intermediate frequency (IF) stages. The frequencies chosen are typical in digital mobile radio (DMR), but the principles apply to other systems as well. The 900MHz RF signal is mixed down to the first IF frequency of 240MHz. Tuning is accomplished by the first local oscillator (LO1). The LO1 frequency is chosen such that the output of the first mixer is at the first IF frequency, 240MHz. Choosing a relatively high first IF frequency eases the requirement on the image frequency rejection filter as will be discussed in the next section on mixers. The first IF is then mixed down to the second IF frequency of 10.7MHz, where it is demodulated (either using analog or digital techniques).

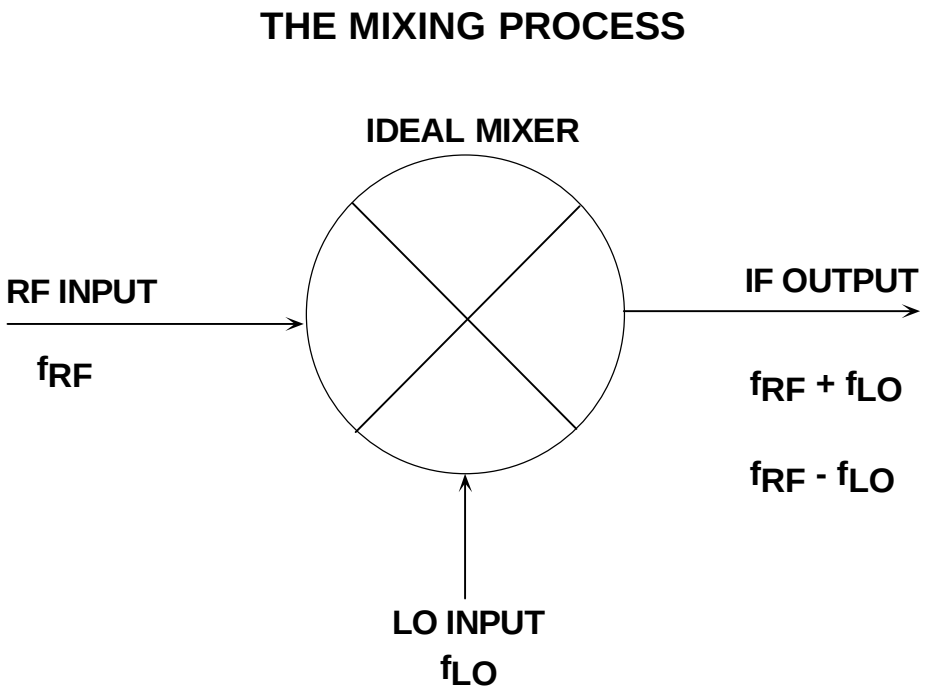
Because of the wide dynamic range of the RF signal, such a receiver requires the use of automatic gain control, voltage controlled amplifiers, and in some cases (depending on the type of demodulation), logarithmic amplifiers.

Receiver design is a complicated art, and there are many tradeoffs that can be made between IF frequencies, single-conversion vs. double-conversion or triple conversion, filter cost and complexity at each stage in the receiver, demodulation schemes, etc. There are many excellent references on the subject, and the purpose of this section is only to acquaint the design engineer with some of the building block ICs which can make receiver design much easier.

Before we look at further details of a receiver, the subject of *mixing* requires further discussion.

MULTIPLIERS, MODULATORS, AND MIXERS
Barrie Gilbert, Bob Clarke

An idealized mixer is shown in Figure 3.37. An RF (or IF) mixer (not to be confused with video and audio mixers) is an active or passive device that converts a signal from one frequency to another. It can either modulate or demodulate a signal. It has three signal connections, which are called *ports* in the language of radio engineers. These three ports are the radio frequency (RF) input, the local oscillator (LO) input, and the intermediate frequency (IF) output.



ANALOG DEVICES

3.37

A mixer takes an RF input signal at a frequency f_{RF}, mixes it with a LO signal at a frequency f_{LO}, and produces an IF output signal that consists of the sum and difference frequencies, $f_{RF} \pm f_{LO}$. The user provides a bandpass filter that follows the mixer and selects the sum ($f_{RF} + f_{LO}$) or difference ($f_{RF} - f_{LO}$) frequency.

Some points to note about mixers and their terminology:

• When the sum frequency is used as the IF, the mixer called an *upconverter*; when the difference is used, the mixer is called a *downconverter*. The former is often used in a transmit channel, the latter in a receive channel.

• In a receiver, when the LO frequency is below the RF, it is called *low-side injection* and the mixer *a low-side downconverter*; when the LO is above the RF, it is called *high-side injection*, and the mixer *a high-side downconverter*.

• Each of the outputs is only half the amplitude (one-quarter the power) of the individual inputs; thus, there is a loss of 6dB in this ideal linear mixer. (In a

practical multiplier, the conversion loss may be greater than 6dB, depending on the scaling parameters of the device. Here, we assume a *mathematical* multiplier, having no dimensional attributes.

A mixer can be implemented in several ways, using active or passive techniques. A brief review of the various classes of nonlinear elements that can be used for frequency translation may be helpful in setting the context. We can identify three subclasses of circuits, sharing certain similarities. All are in the class of signal multipliers, producing at their output a signal which is, in one way or another, the product of its two inputs. They are *multipliers*, *modulators*, and *mixers*.

An *analog multiplier* generally has two signal input ports, which can be called X and Y, and generates an output W that is the linear product of the voltages applied to these two ports. To retain dimensional consistency, the analog linear multiplication function must invoke the use of a reference voltage, which we can call U, thus W=XY/U. In some cases, U is actually a third input that can be used to implement analog division.

There are three functional categories of multipliers: In *single-quadrant* multipliers, X and Y must be unipolar; in *two-quadrant* multipliers, one of the inputs may be bipolar; in *four-quadrant* multipliers, both X and Y may be bipolar. Analog Devices produces a wide range of "linear" multipliers, including the AD534, AD538, AD539, AD633, AD734, AD834 and AD835, providing the highest available accuracy (±0.02% for the AD734) to the highest speed (more than 500MHz for the AD834).

Modulators (sometimes called *balanced-modulators*, *doubly-balanced modulators* or even on occasions *high level mixers*) can be viewed as *sign-changers*. The two inputs, X and Y, generate an output W, which is simply one of these inputs (say, Y) multiplied by just the sign of the other (say, X), that is W = Ysign(X). Therefore, no reference voltage is required. A good modulator exhibits very high linearity in its signal path, with precisely equal gain for positive and negative values of Y, and precisely equal gain for positive and negative values of X. Ideally, the amplitude of the X input needed to fully switch the output sign is very small, that is, the X-input exhibits a comparator-like behavior. In some cases, where this input may be a logic signal, a simpler X-channel can be used. A highly-linear mixer such as the AD831 is well-suited as a modulator.

A *mixer* is a modulator optimized for frequency-translation. Its place in the signal path is usually close to the antenna, where both the wanted and (often large) unwanted signals coexist at its signal input, usually called the *RF port*. Thus, the mixer must exhibit excellent linearity in the sense that its output (at the IF port) is expected to increase by the same number of dB as a test signal applied to the RF port, up to as high as level as possible. This attribute is defined both by the 1dB gain-compression and the 3rd-order intercept (later explained). The conversion process is driven by an input applied to the LO port.

Noise and matching characteristics are crucial to achieving acceptable levels of performance in a receiver's mixer. It is desirable to keep the LO power to a minimum to minimize cross-talk between the three ports, but this often conflicts with other requirements. The gain from the RF port to its IF port at specified RF and LO frequencies is called the *conversion gain* and in classical diode-bridge mixers is less than –4dB. *Active mixers* provide higher conversion gain, and better port-port

isolation, but often at the expense of noise and linearity. It is not usually possibly (nor even desirable) to describe mixer behavior using equations relating the instantaneous values of inputs and outputs; instead, we generally seek to characterize mixers in terms of their non-ideal cross-product terms at the output. In this class, Analog Devices has the AD831, and mixers are found embedded in the AD607, AD608 and other signal-processing ICs.

Thus far, we have seen that multipliers are linear in their response to the instantaneous value of both of their input voltages; modulators are linear in their response to one input, the other merely flipping the sign of this signal at regular intervals, with virtually zero transition time, and beyond that having ideally no other effect on the signal; mixers are a sort of RF half-breed, ideally being very linear on the RF input, and 'binary' in their switching function in response to the LO input, but in reality being nonideal in both respects; they are optimized for very low noise and minimal intermodulation distortion.

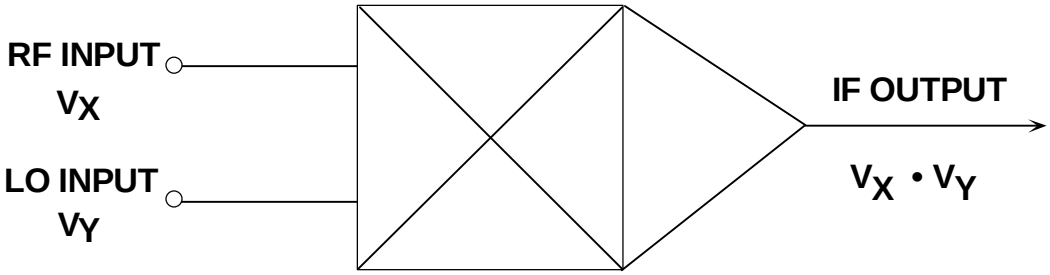
Mixing Using an Ideal Analog Multiplier

Figure 3.38 shows a greatly simplified RF mixer by assuming the use of an analog multiplier.

Ideally, the multiplier has no noise, no limit to the maximum signal amplitude, and no intermodulation between the various RF signals (that is, no spurious nonlinearities). Figure 3.39 shows the result of *mixing* (= multiplying) an RF input of $\sin\omega_{RF}t$ with (= by) a LO input of $\sin\omega_{LO}t$, where $\omega_{RF} = 2\pi\times11\text{MHz}$ and $\omega_{LO} = 2\pi\times10\text{MHz}$.

Clearly, to better understand mixer behavior, we will need to consider not only the time-domain waveforms, as shown here, but also the spectrum of the IF output. Figure 3.40 shows the output spectrum corresponding to the above IF waveform.

"MIXING" USING AN ANALOG MULTIPLIER

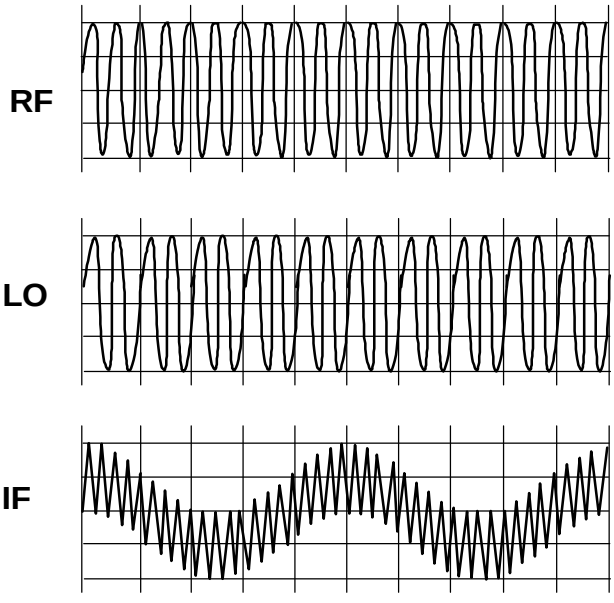


ANALOG MULTIPLIER, e.g., AD834

ANALOG DEVICES

3.38

INPUTS AND OUTPUTS FOR MULTIPLYING MIXER FOR f_{RF} = 11MHz, f_{LO} = 10MHz

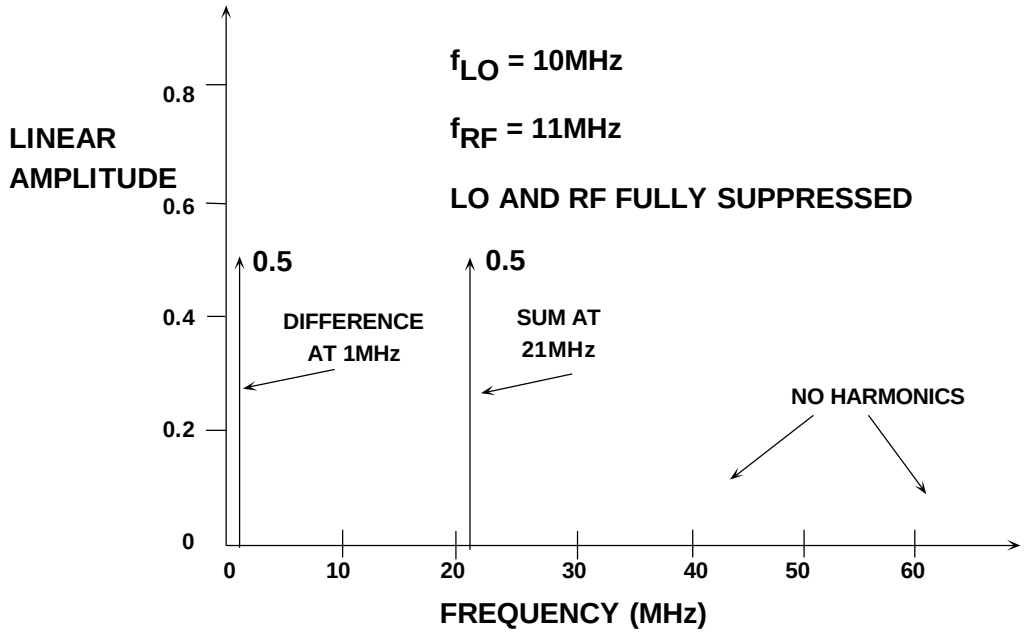


Horizontal: 200ns/div.

ANALOG DEVICES

3.39

OUTPUT SPECTRUM FOR MULTIPLYING MIXER FOR f_{RF} = 11MHz, f_{LO} = 10MHz



ANALOG DEVICES

3.40

There is no mystery so far. The mathematics are simple. Neglecting scaling issues (real signals are voltages; thus a practical multiplier needs an embedded voltage reference, ignored here) the relationship is:

$$\sin\omega_{RF}t \sin\omega_{LO}t = {}^1/_2 \{ \cos(\omega_{RF} + \omega_{LO})t + \cos(\omega_{RF} - \omega_{LO})t \} \qquad \text{Eq. 1}$$

The multiplier has thus transformed the RF input into two, equal-amplitude cosinusoidal components at its output (the IF port), one at the sum frequency, $\omega_{RF} + \omega_{LO}$, and the other at the difference frequency, $\omega_{RF} - \omega_{LO}$.

In practice, an analog multiplier would be a poor choice for a mixer because the two linear inputs bring with them a serious noise penalty.

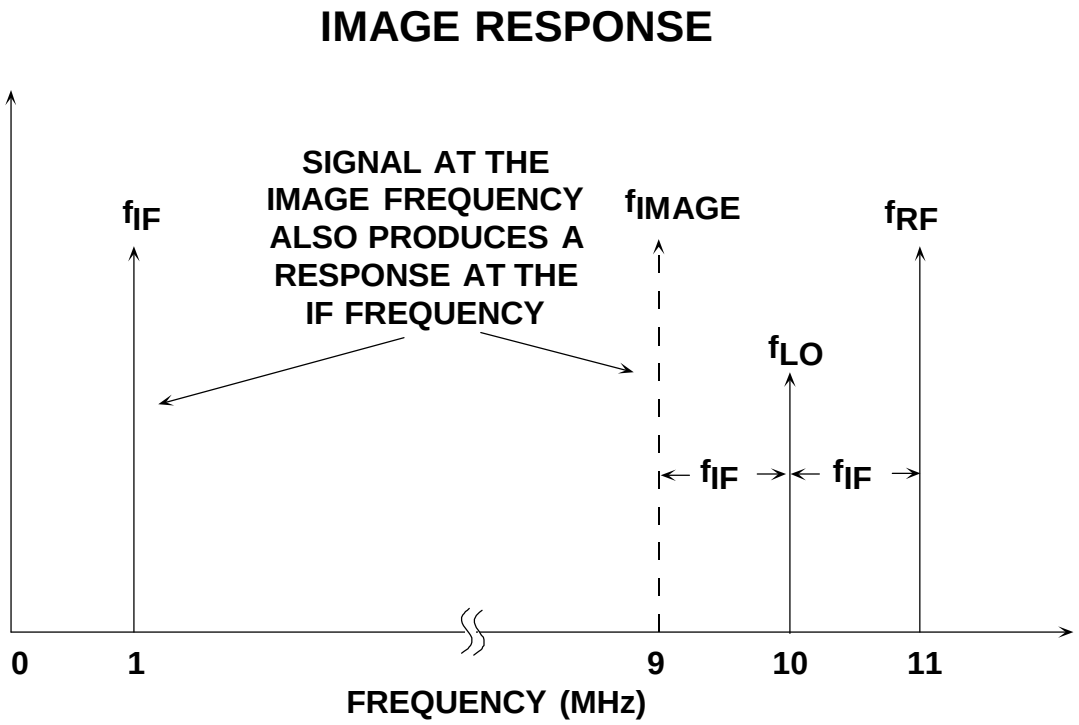
Image Response

A receiver using even this mathematically perfect mixer suffers a basic problem, that of *image response*. Consider the use of a low-side downconverter. The wanted output is found at the frequency $\omega_{IF} = \omega_{RF} - \omega_{LO}$. So we might suppose that the only component of the RF spectrum that finds its way through the mixer "sieve" to the narrow IF passband is the wanted component at ω_{RF}. But we could have just as easily written (1) as

$$\sin\omega_{RF}t \sin\omega_{LO}t = {}^1/_2 \{ \cos(\omega_{RF} + \omega_{LO})t + \cos(\omega_{LO} - \omega_{RF})t \} \qquad \text{Eq. 1a}$$

because the cosine function is symmetric about t = 0. So there is another spectral component at the RF input that falls in the IF passband, namely the one for which $\omega_{IF} = \omega_{LO} - \omega_{RF}$, in this case, the *image* frequency.

Consider the above example, where f_{LO} = 10MHz and f_{IF} = 1MHz; the wanted response is at the IF frequency, f_{IF} = 1MHz for f_{RF} = 11MHz. However, the mixer produces the same IF in response to the *image frequency*, f_{IMAGE} = 9MHz (see Figure 3.41).



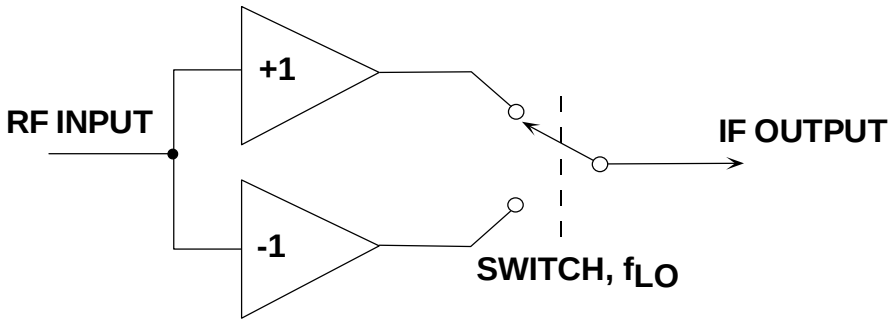
3.41

The most practical solution to this dilemma is to carefully choose the IF frequency to minimize the likelihood of image sensitivity and also include an image-reject filter at the RF input, just ahead of the mixer. Another approach is to use a special type of mixer circuit that does not respond to the image frequency. This approach requires circuitry which is considerably more complex, and for this reason has generally been unpopular, but it is becoming more practical in a modern IC implementation. It has the further disadvantage of higher power consumption, since two mixer cells operating in quadrature are required.

The Ideal Mixer

Ideally, to meet the low-noise, high-linearity objectives of a mixer we need some circuit that implements a polarity-switching function in response to the LO input. Thus, the mixer can be reduced to Figure 3.42, which shows the RF signal being split into in-phase (0°) and anti-phase (180°) components; a changeover switch, driven by the local oscillator (LO) signal, alternately selects the in-phase and antiphase signals. Thus reduced to essentials, the ideal mixer can be modeled as a sign-switcher.

AN IDEAL SWITCHING MIXER



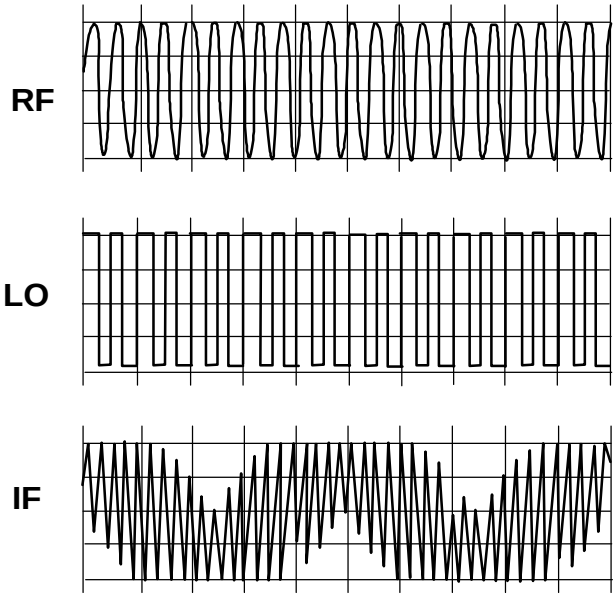
ANALOG DEVICES

3.42

In a perfect embodiment, this mixer would have no noise (the switch would have zero resistance), no limit to the maximum signal amplitude, and would develop no intermodulation between the various RF signals. Although simple in concept, the waveform at the intermediate frequency (IF) output can be very complex for even a small number of signals in the input spectrum. Figure 3.43 shows the result of *mixing* just a single input at 11MHz with an LO of 10MHz.

The *wanted* IF at the difference frequency of 1MHz is still visible in this waveform, and the 21MHz sum is also apparent. But the spectrum of this waveform is clearly more complex than that obtained using the analog multiplier. How are we to analyze this?

INPUTS AND OUTPUTS FOR IDEAL SWITCHING MIXER FOR f_{RF} = 11MHz, f_{LO} = 10MHz



ANALOG DEVICES

3.43

We still have a product, but now it is that of a sinusoid (the RF input) at ω_{RF} and a variable that can only have the values +1 or –1, that is, a unit square wave at ω_{LO}. The latter can be expressed as a Fourier series

$$S_{LO} = {}^{4}/_{\pi}\{ \sin\omega_{LO}t - {}^{1}/_{3}\sin3\omega_{LO}t + {}^{1}/_{5}\sin5\omega_{LO}t - \ldots.\} \qquad \text{Eq. 2}$$

Thus, the output of the switching mixer is its RF input, which we can simplify as $\sin\omega_{RF}t$, multiplied by the above expansion for the square wave, producing

$$S_{IF} = {}^{4}/_{\pi}\{ \sin\omega_{RF}t\sin\omega_{LO}t - {}^{1}/_{3}\sin\omega_{RF}t\sin3\omega_{LO}t + {}^{1}/_{5}\sin5\omega_{RF}t\sin5\omega_{LO}t - \ldots.\} \qquad \text{Eq. 3}$$

Now expanding each of the products, we obtain

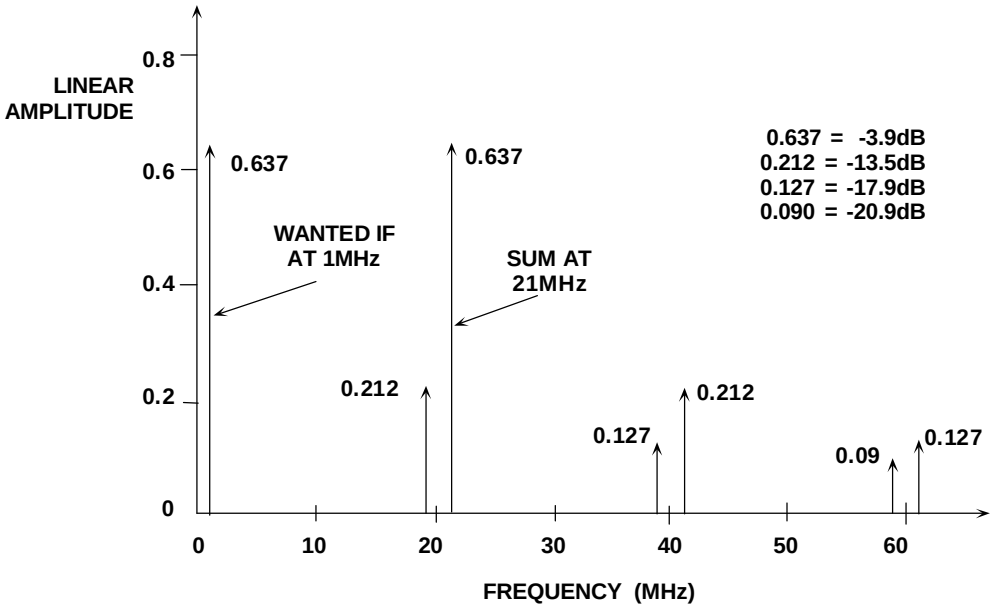
$$S_{IF} = {}^{2}/_{\pi}\{ \sin(\omega_{RF}+\omega_{LO})t + \sin(\omega_{RF}-\omega_{LO})t - {}^{1}/_{3}\sin(\omega_{RF}+3\omega_{LO})t - {}^{1}/_{3}\sin(\omega_{RF}-3\omega_{LO})t + {}^{1}/_{5}\sin(\omega_{RF}+5\omega_{LO})t + {}^{1}/_{5}\sin(\omega_{RF}-5\omega_{LO})t - \ldots\} \qquad \text{Eq. 4}$$

or simply

$$S_{IF} = {}^{2}/_{\pi}\{ \sin(\omega_{RF}+\omega_{LO})t + \sin(\omega_{RF}-\omega_{LO})t + \text{harmonics} \} \qquad \text{Eq. 5}$$

The most important of these harmonic components are sketched in Figure 3.44 for the particular case used to generate the waveform shown in Figure 3.43, that is, f_{RF} = 11MHz and f_{LO} = 10MHz. Because of the $2/\pi$ term, a mixer has a minimum 3.92 dB insertion loss (and noise figure) in the absence of any gain.

OUTPUT SPECTRUM FOR SWITCHING MIXER FOR f_{RF} = 11MHz AND f_{LO} = 10MHz



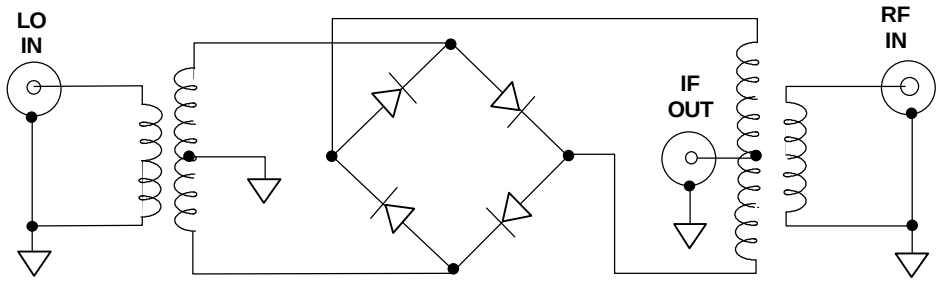
Note that the ideal (switching) mixer has exactly the same problem of image response to $\omega_{LO} - \omega_{RF}$ as the linear multiplying mixer. The image response is somewhat subtle, as it does not immediately show up in the output spectrum: it is a latent response, awaiting the occurrence of the "wrong" frequency in the input spectrum.

Diode-Ring Mixer

For many years, the most common mixer topology for high-performance applications has been the diode-ring mixer, one form of which is shown in Figure 3.45. The diodes, which may be silicon junction, silicon Schottky-barrier or gallium-arsenide types, provide the essential switching action. We do not need to analyze this circuit in great detail, but note in passing that the LO drive needs to be quite high—often a substantial fraction of one watt—in order to ensure that the diode conduction is strong enough to achieve low noise and to allow large signals to be converted without excessive spurious nonlinearity.

Because of the highly nonlinear nature of the diodes, the impedances at the three ports are poorly controlled, making matching difficult. Furthermore, there is considerable coupling between the three ports; this, and the high power needed at the LO port, make it very likely that there will be some component of the (highly-distorted) LO signal coupled back toward the antenna. Finally, it will be apparent that a passive mixer such as this cannot provide conversion gain; in the idealized scenario, there will be a conversion loss of $2/\pi$ [as Eq. 4 shows], or 3.92dB. A practical mixer will have higher losses, due to the resistances of the diodes and the losses in the transformers.

DIODE-RING MIXER



ANALOG DEVICES

3.45

Users of this type of mixer are accustomed to judging the signal handling capabilities by a "Level" rating. Thus, a Level-17 mixer needs +17dBm (50mW) of LO drive and can handle an RF input as high as +10dBm (±1V). A typical mixer in this class would be the Mini-Circuits LRMS-1H, covering 2-500MHz, having a nominal insertion loss of 6.25dB (8.5dB max), a worst-case LO-RF isolation of 20dB and a worst-case LO-IF isolation of 22dB (these figures for an LO frequency of 250-500MHz). The price of this component is approximately $10.00 in small quantities. Even the most expensive diode-ring mixers have similar drive power requirements, high losses and high coupling from the LO port.

FET Mixers

A modern alternative to the diode-ring mixer is one in which the diodes are replaced by FETs. The idea here is to reduce the distortion caused by the inherent nonlinearities of junction diodes, whose incremental resistance varies with the instantaneous signal current. To reduce this effect, the diodes are often driven to very high current levels. Indeed, some users of diode-ring mixers push them to extremes, operating at current levels close to those which will cause the diodes to fail by over-dissipation. Thus, in commenting about a certain minor variation to the diode-ring-mixer, we read:

"This helps the mixer to accept higher LO power without burning out the diodes!"

(From Wes Hayward, *Solid State Design for the Radio Amateur,* ARRL, 1986, Chapter 6, p.120)

To avoid "burning out the diodes", some mixers use two or four J-FETs in an analogous way to that shown in Figure 3.45. The idea is that the channel resistance

of a large FET driven into its triode region of conduction can be as low as the dynamic resistance of a diode, thus achieving similar conversion gain and noise levels. But this low resistance arises without any current flow in the channel and it is also more linear than that of the diodes when signal current does flow, thus resulting in lower intermodulation, and hence a larger overall dynamic range. MOS-FETs can also be used in a similar way.

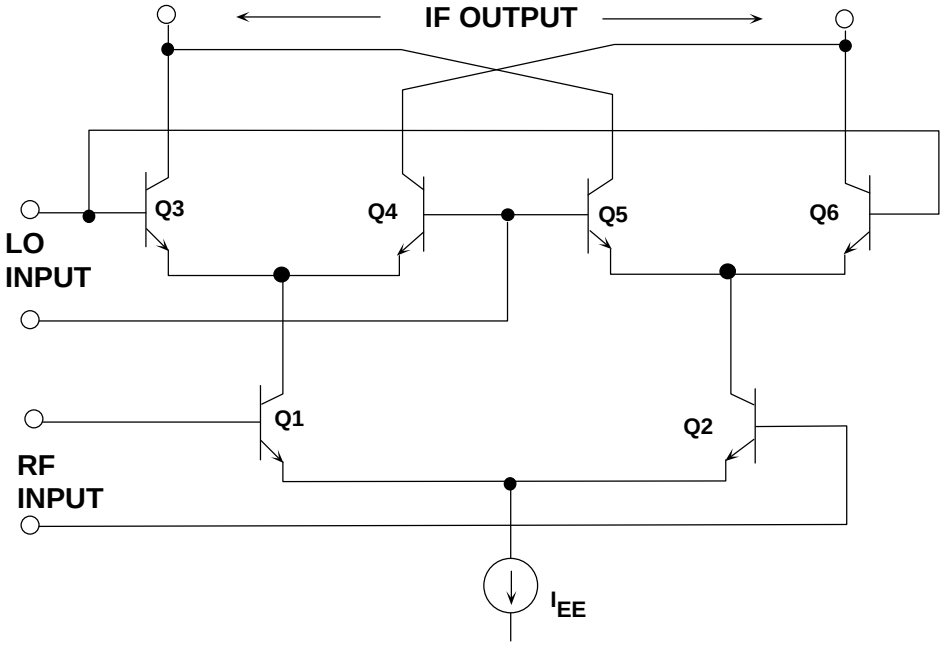
This style of FET-based mixers is very attractive for many high-performance applications. However, since the active devices are still used only as switches, they do not provide power gain, and have typical insertion losses of 6 to 8dB. Furthermore, the balance of these mixers is still critically dependent on such things as transistor matching and transformer winding accuracy, large LO drives (volts) are needed, and the overall matching requirements continue to be difficult to achieve over the full frequency range. Finally, of course, they are not directly amenable to monolithic integration.

Another popular circuit, widely used in many inexpensive receivers, is the dual-gate MOS-FET mixer. In this type of mixer, the RF signal is applied to one gate of the FET and the LO signal to the second gate. The multiplication process is not very well-defined, but in general terms relies on the fact that both the first and second gates influence the current in the channel. The structure can be modeled as two FETs, where the drain of the lower FET (having the RF input applied to it) is intimately connected to the source of the upper FET (having the LO input on its gate). The lower FET operates in its triode region, and thus exhibits a g_m that is a function of its drain voltage, controlled by the LO. Though not readily modeled to great accuracy, this mixer, like many others, can be pragmatically optimized to achieve useful performance, though not without the support of many associated passive components for biasing and matching.

Classic Active Mixer

The diode-ring mixer not only has certain performance limitations, but it is also not amenable to fabrication using integrated circuit technologies, at least in the form shown in Figure 3.45. In the mid 'sixties it was realized that the four diodes could be replaced by four transistors to perform essentially the same switching function. This formed the basis of the now-classical bipolar circuit shown in Figure 3.46, which is a minimal configuration for the fully-balanced version. Millions of such mixers have been made, including variants in CMOS and GaAs. We will limit our discussion to the BJT form, an example of which is the Motorola MC1496, which, although quite rudimentary in structure, has been a mainstay in semi-discrete receiver designs for about 25 years.

CLASSIC ACTIVE MIXER



ANALOG DEVICES

3.46

The *active mixer* is attractive for the following reasons:

- It can be monolithically integrated with other signal processing circuitry.

- It can provide conversion gain, whereas a diode-ring mixer always has an insertion loss. (Note: Active mixers may have gain. The analog Devices' AD831 active mixer, for example, amplifies the result in Eq. 5 by $\pi/2$ to provide unity gain from RF to IF.)

- It requires much less power to drive the LO port.

- It provides excellent isolation between the signal ports.

- Is far less sensitive to load-matching, requiring neither diplexer nor broadband termination.

Using appropriate design techniques it can provide trade-offs between third-order intercept (3OI or IP3) and the 1dB gain-compression point (P_{1dB}), on the one hand, and total power consumption (P_D) on the other. (That is, including the LO power, which in a passive mixer is "hidden" in the drive circuitry.)

Basic Operation of the Active Mixer

Unlike the diode-ring mixer, which performs the polarity-reversing switching function in the voltage domain, the active mixer performs the switching function in the current domain. Thus the active mixer core (transistors Q3 through Q6 in Figure 3.46) must be driven by current-mode signals. The voltage-to-current converter formed by Q1 and Q2 receives the voltage-mode RF signal at their base terminals and transforms it into a differential pair of currents at the their collectors.

A second point of difference between the active mixer and diode ring mixer, therefore, is that the active mixer responds only to magnitude of the input voltage, not to the input power; that is, the active mixer is not matched to the source. (The concept of matching is that both the current and the voltage at some port are used by the circuitry which forms that port). By altering the bias current, I_{EE}, the transconductance of the input pair Q1-Q2 can be set over a wide range. Using this capability, an active mixer can provide variable gain.

A third point of difference is that the output (at the collectors of Q3–Q6) is in the form of a current, and can be converted back to a voltage at some other impedance level to that used at the input, hence, can provide further gain. By combining both output currents (typically, using a transformer) this voltage gain can be doubled. Finally, it will be apparent that the isolation between the various ports, in particular, from the LO port to the RF port, is inherently much lower than can be achieved in the diode ring mixer, due to the reversed-biased junctions that exist between the ports.

Briefly stated, though, the operation is as follows. In the absence of any voltage difference between the bases of Q1 and Q2, the collector currents of these two transistors are essentially equal. Thus, a voltage applied to the LO input results in no change of output current. Should a small DC offset voltage be present at the RF input (due typically to mismatch in the emitter areas of Q1 and Q2), this will only result in a small feedthrough of the LO signal to the IF output, which will be blocked by the first IF filter.

Conversely, if an RF signal is applied to the RF port, but no voltage difference is applied to the LO input, the output currents will again be balanced. A small offset voltage (due now to emitter mismatches in Q3–Q6) may cause some RF signal feedthrough to the IF output; as before, this will be rejected by the IF filters. It is only when a signal is applied to both the RF and LO ports that a signal appears at the output; hence, the term doubly-balanced mixer.

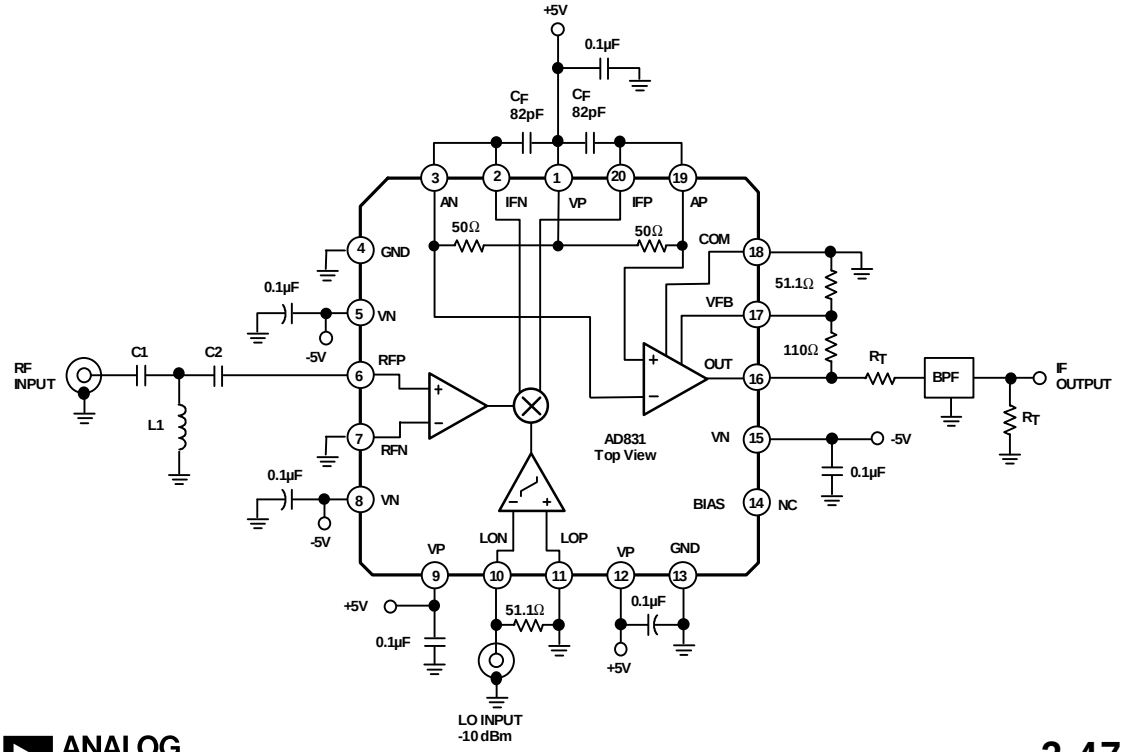
Active mixers can realize their gain in one other way: the matching networks used to transform a 50Ω source to the (usually) high input impedance of the mixer provides an impedance transformation and thus voltage gain due to the impedance step up. Thus, an active mixer that has loss when the input is terminated in a broadband 50Ω termination can have “gain” when an input matching network is used.

The AD831, 500MHz, Low Distortion Active Mixer

The AD831 is a low distortion, wide dynamic range, monolithic mixer for use in such applications as RF to IF down conversion in HF and VHF receivers, the second mixer in digital mobile radio base stations, direct-to-baseband conversion, quadrature modulation and demodulation, and doppler-frequency shift detection in ultrasound imaging applications. The mixer includes a local oscillator driver and a low-noise output amplifier. The AD831 provides a +24dBm third-order intercept point for –10dBm local oscillator power, thus improving system performance and reducing system cost, compared to passive mixers, by eliminating the need for a high power local oscillator driver and its associated shielding and isolation problems. A

simplified block diagram of the AD831 is shown in Figure 3.47, and key specifications in Figure 3.48.

AD831 500MHz LOW DISTORTION ACTIVE MIXER



ANALOG DEVICES

3.47

AD831 ACTIVE MIXER KEY SPECIFICATIONS

- **Doubly-Balanced Mixer, 10dB Noise Figure**
- **Low Distortion (IF = 10.7MHz, RF to 200MHz):**
  - **+24dBm Third Order Intercept**
  - **+10dBm 1dB Compression Point**
- **Low LO Drive Required: –10dBm**
- **Bandwidth:**
  - **500MHz RF and LO Input Bandwidths**
  - **250MHz Differential Current IF Output**
  - **DC to > 200MHz Single-Ended Voltage IF Output**

ANALOG DEVICES

3.48

Noise Figure

Noise Figure (NF) is a figure of merit used to determine how a device degrades the signal-to-noise ratio of its input. Note: in RF systems, the impedance is 50Ω unless otherwise stated. Mathematically, noise figure is defined as:

$$NF = 20\log_{10}\frac{S_I / N_I}{S_O / N_O},$$

where S_I/N_I is the input signal-to-noise ratio, and S_O/N_O is the output signal-to-noise ratio.

Typical noise figures for passive mixers with post amplifiers are 12 to 15dB. The NF of the AD831 is 10dB with a matched input, which is adequate for applications in which there is gain in front of the mixer.

Noise Figure is used in a "cascaded noise figure calculation", which gives the overall noise figure of a receiver. Basically, the noise figure of each stage is converted into a noise factor (F = antilog NF/10) and plugged into a spreadsheet containing the Friis Equation:

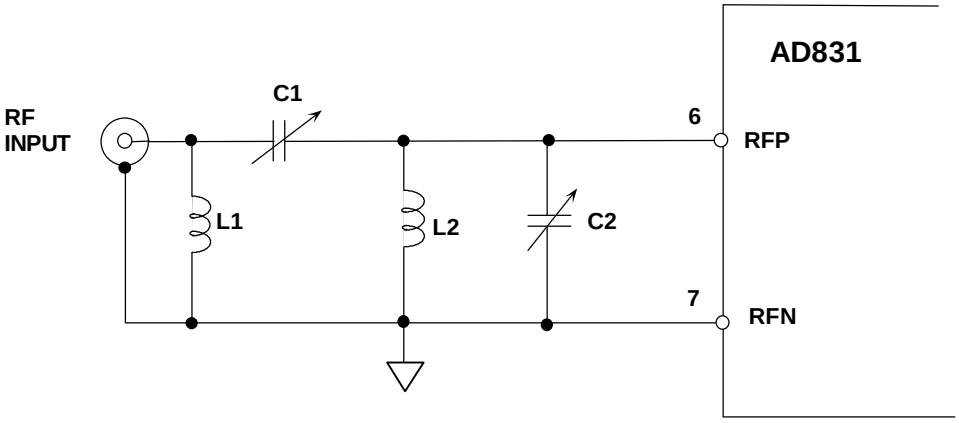
$$F_{RECEIVER} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \sum_{K=4}^{N} \frac{F_K - 1}{\prod_{J=1}^{K-1} G_J},$$

where F_N and G_N are the noise factor and gain, respectively, of the Nth stage in the receiver.

For a passive diode-ring mixer, the noise figure is the same as the insertion loss. For an active mixer, however, noise is added to the signal by the active devices in the signal path. The difference between the noise figure of a matched active mixer and an unmatched active mixer can be several dB due to the “voltage gain” of the impedance-matching network, which acts as a “noiseless” preamplifier (Figure 3.49). In the case of the AD831, the noise figure for the matched circuit is 10 dB (at 70MHz) and the unmatched circuit with its input terminated with a 50Ω resistor is 16dB.

The noise figure is 11.7dB at 220 MHz using the external matching network shown in Figure 3.49. The values shown are for 220 MHz and provide 10 dB of voltage gain.

AD831 ACTIVE MIXER WITH 220MHz EXTERNAL MATCHING NETWORK



L1: 100nH, COILCRAFT 1008CS-101
L2: 56nH, COILCRAFT 1008CS-560
C1, C2: 2-10pF CERAMIC VARIABLE

ANALOG DEVICES

3.49

Intermodulation Distortion

Even before the 'mixing' process in the core, the entire signal spectrum co-exists within the RF input stage. This part of the mixer is inevitably nonlinear, to a greater or lesser extent, and, with or without the LO input operative, generates a very large number of intermodulation products.

Thus, the key objectives in the design of a high-performance active mixer are to achieve a very linear RF input section, followed by a near-ideal polarity-switching stage, followed by a very linear IF output amplifier (if used) prior to the first filter.

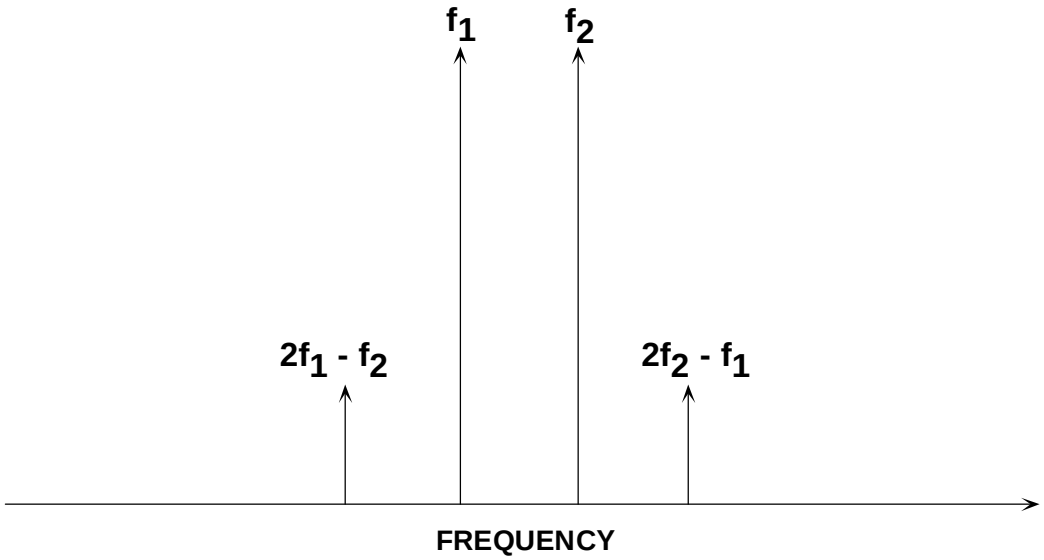
1dB Compression Point and Third-Order Intercept Point

For a single-sinusoid input to a system, a point will be reached as the input amplitude is increased at which the apparent gain becomes 1dB lower than that observed at lower input amplitudes. This is called the 1dB gain compression level, which we'll abbreviate P_{1dB}, and is usually quoted in dBm, or 'decibels above 1mW, that is, it is expressed as a power measurement. When using an active mixer with an input matching network, the gain of the input matching network must be taken into account when defining the system in terms of an active mixer's 1dB compression point, since the impedance transformation of the network increases the input voltage to mixer.

Another metric used in characterizing mixers is the third-order intercept, known as P_{3OI} or IP3. If two tones of frequency f_1 and f_2 (representing two adjacent channels in a communications system, for example) are applied to a non-linear system, there will be a large number of intermodulation products generated. The third-order

distortion products which fall at $2f_2$-f_1 and $2f_1$-f_2 are particularly troublesome, because they are close to the original frequencies (see Figure 3.50). If the two tones represent true signals, then the third-order IMD products can interfere with signals in the adjacent channels.

THIRD-ORDER INTERMODULATION DISTORTION



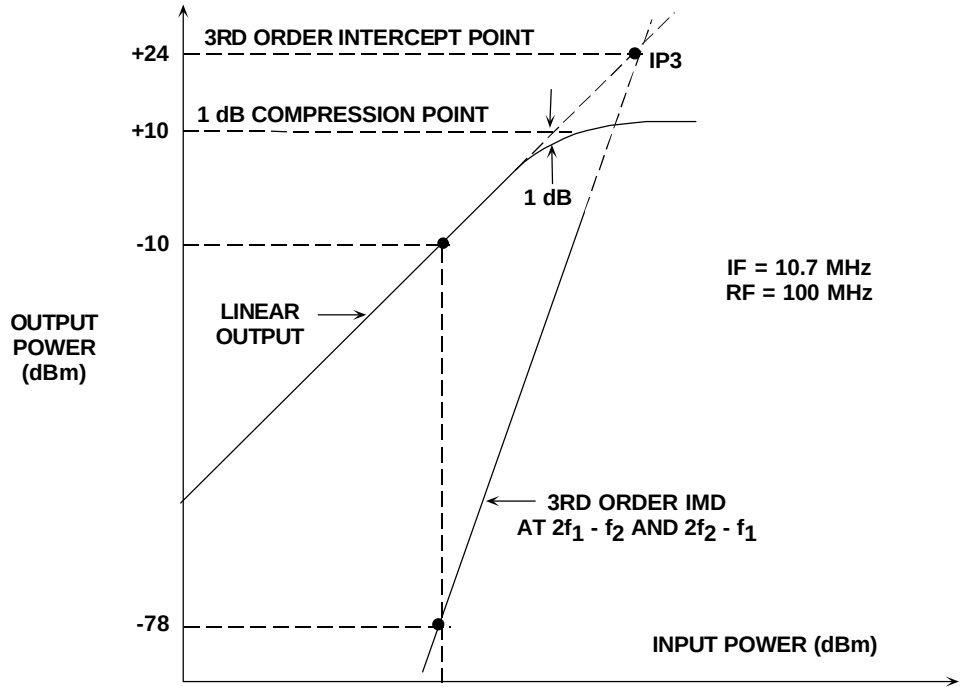
ANALOG DEVICES

3.50

Rather than measuring the third-order distortion products for a variety of signal amplitudes, the concept of third-order intercept can be used to extract the IMD information and is often used as a figure of merit for mixers and amplifiers in RF applications.

A plot (Figure 3.51) of the power levels at the output of the system for the fundamental of the output frequency and for its third harmonic, plotted versus the input power, will generally yield a pair of straight lines which eventually intersect (at the 3rd order intercept point, IP3).

THIRD-ORDER INTERCEPT USING DATA FOR AD831



ANALOG DEVICES

3.51

The problem with this metric is that it has meaning only for certain simple cases. In particular, the 3rd harmonic is assumed to increase at three times the rate of the fundamental. The appeal of P_{3OI} lies in the fact that it is easily measured, or at least, it is easy to obtain measurements. (The measurements are not hard to make, but it will be found that the apparent P_{3OI} is signal-dependent). Apply a low level signal, at some known level P_O (in dBm, see Figure 3.51), measure the output power at the fundamental, P_1 (in relative terms, dBc) and at the third harmonic, P_3 (also in dBc) and from simple geometry calculate

$$P_{3OI} = P_O + {}^1/_2 (P_1 - P_3) \qquad \text{Eq. 6}$$

The non-linearity in some classical circuits, such as the diode-ring mixer, approximates a cubic function, and the above relationship holds, but in practice, the P_{3OI} can be quite misleading, for several reasons. First, other circuits may not, in general, exhibit this type of non-linearity. This type of behavior could easily lead to apparent third-order intercept values which were impressively high (theoretically infinite, if 'measured' using signals of less than the critical amplitude).

A *spur chart* is a compilation of the $nf_1 \pm mf_2$ products that result from the mixing process. The spur chart is useful because it allows an engineer developing a frequency plan for a radio to identify possible problems due to spurious signals created in the mixer. However, the spur chart is also tedious to create; for n = m = 7, a chart requires 112 measurements.

The compilation of results is the spur chart (also called a "mixer table"). Details of making the spur chart measurements and results are given in the AD831 data sheet (see Reference 17).

Mixer Summary

Mixers are a special kind of analog multiplier optimized for use in frequency translation, having one linear input (that associated with the RF signal) and a second (that associated with the LO input) which alternates the phase of the first input by 0/180°. In integrating complete receivers in monolithic form, certain basic circuit forms have proven useful. So far, we have considered a classic form, a six-transistor circuit exemplified by the AD831. Compared to a diode-ring mixer, this circuit has several advantages, including much better isolation between ports, the ability to provide conversion gain (which may also be variable), the need for much lower LO drive levels, and the elimination of special matching networks.

Often cited as a disadvantage of the active mixer is it's poorer dynamic range: we have just begun to examine what defines this, beginning with a consideration of the linearity of the RF port, traditionally characterized by the 1dB gain-compression input power, P_{1dB}, and the third-order intercept, P_{3OI}. The second of these measures was shown to be meaningful only if the nonlinearity is essentially cubic in form, which may not always be true. In passing, we pointed out that while inputs and outputs are invariably characterized in terms of a power level of so-many-dBm, active mixers respond to instantaneous signal voltages at their inputs, which are usually not matched to their source, which can be confusing at times.

Now that we have examined each of the fundamental receiver building blocks, we are ready to look at receiver subsystems.

RECEIVER SUBSYSTEMS
Bob Clarke, Walt Kester

In order to design a communications receiver, a clear understanding of the modulation technique is essential. There are many types of modulation, ranging from simple amplitude modulation (AM), phase modulation (PM), and frequency modulation (FM) to multi-level quadrature-amplitude-modulation (QAM) where both amplitude and phase are modulated. Most modern modulation schemes make use of both signal amplitude and phase information. A complex signal can thus be represented in two ways as shown in the diagrams in Figure 3.52. The left-hand diagram represents the signal in rectangular coordinates as an inphase (I) and quadrature (Q) signal of the form:

$S(t) = I(t) + jQ(t)$.

The right hand diagram represents the same signal expressed in polar coordinates:

$S(t) = A(t)e^{j\emptyset(t)}$.

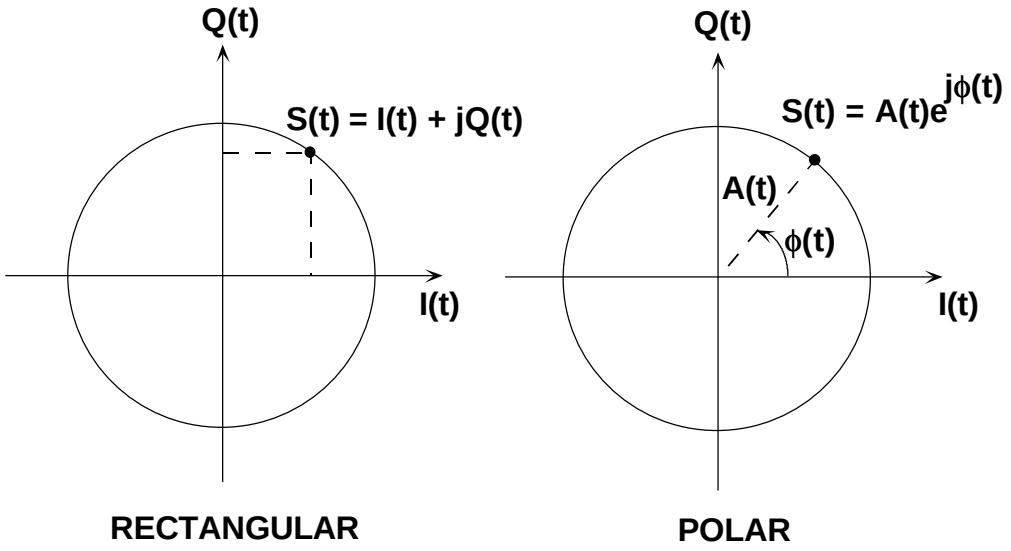
The conversions between the two coordinate systems are:

$S(t) = A(t)e^{j\emptyset(t)} = I(t) + jQ(t)$, where

$$A(t) = \sqrt{I(t)^2 + Q(t)^2},$$

$$\emptyset(t) = \arctan\left[\frac{Q(t)}{I(t)}\right].$$

RECTANGULAR AND POLAR REPRESENTATIONS OF AMPLITUDE AND PHASE MODULATED SIGNAL



RECTANGULAR **POLAR**

Note that the signals are identical, only their representation is different.

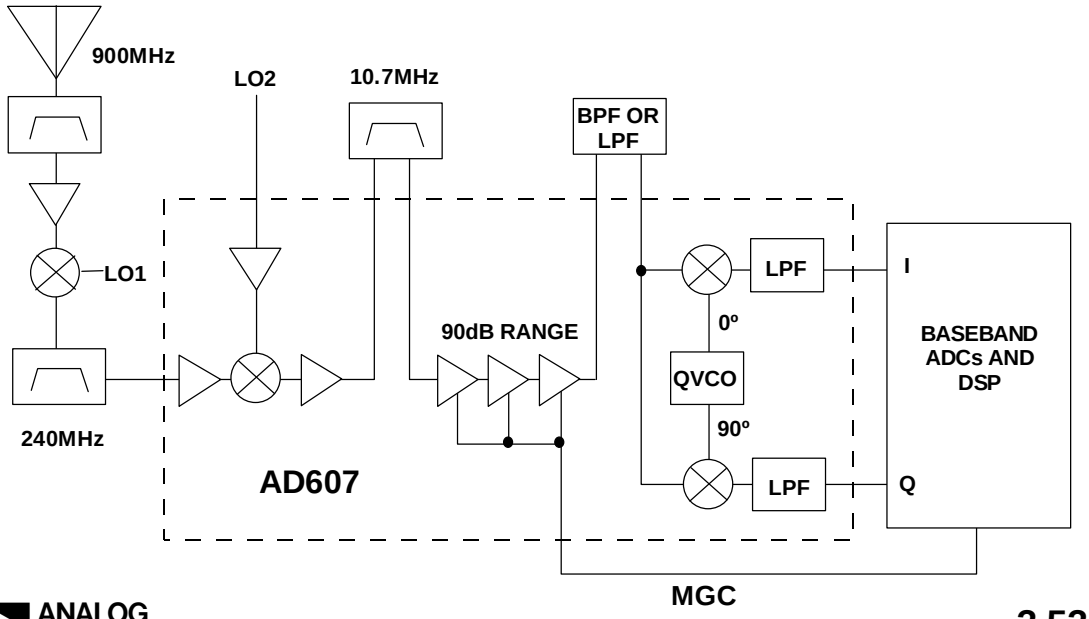
In the case of the I/Q (rectangular) representation, a linear IF strip is required. Variable gain is required because of the wide dynamic range, and amplitude and phase information must be preserved. This type of IF strip often incorporates an I/Q demodulator whose outputs drive baseband ADCs followed by a DSP. Linear IF amplifiers are used in these systems.

For the case of the polar representation, the signal amplitude is derived from the RSSI (log) output of a log/limiting amplifier and the phase information from the limited output. This type of IF strip operates at a high fixed gain, retains the phase information in the limited output, and often incorporates a phase demodulator.

In order to handle these two fundamental representations of modulation, ADI has developed two IF subsystems, the AD607 and the AD608. These are used in such applications as PHS, PCN, DECT, CT2, and GSM where the modulation mode is some form of phase-shift keying (PSK).

The chose of demodulation technique depends on the receiver architecture. The standard architecture in GSM and PHS uses a rectangular representation of the signal, that is S(t) = I(t) + jQ(t) and requires a linear IF amplifier stage such as that in the AD607. In this architecture, a baseband converter consisting of two signal inputs; each with individual low-pass filters, digitizes the I(t) and Q(t) outputs of the IF IC's quadrature demodulator. Further demodulation is performed digitally using a DSP. An equalizer in the DSP then determines the correct manual gain control (MGC) voltage (or digital signal) to change the IF gain to center the signal in the dynamic range of the baseband ADCs. The equalizer calculates the RSSI value as part of this process (see Figure 3.53).

RECEIVER BASED ON AD607 SUBSYSTEM USING INPHASE/QUADRATURE MODULATION

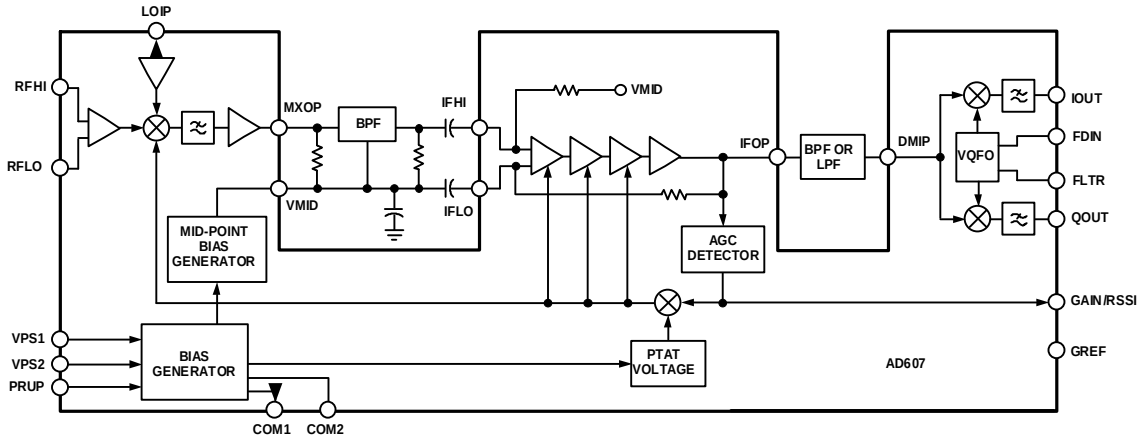


ANALOG DEVICES

3.53

A detailed block diagram of the AD607 Mixer/AGC/RSSI 3V receiver IF subsystem is shown in Figure 3.54. The RF input frequency can be as high as 500MHz, and the IF frequency from 400kHz to 12MHz. It consists of a mixer, linear IF amplifiers, I and Q demodulators, a phase-locked quadrature oscillator, AGC detector, and a biasing system with external power-down. Total power on +3V is 25mW.

AD607 FUNCTIONAL BLOCK DIAGRAM



ANALOG DEVICES

3.54

The AD607's low noise, high intercept mixer is a doubly-balanced Gilbert cell type. It has a nominal –15dBm input-referred 1dB compression point and a –8dBm input-referred third-order intercept. The mixer section also includes a local oscillator preamplifier, which lowers the required external LO drive to –16dBm.

The variable-gain mixer and the linear four-stage IF amplifier strip together provide a voltage controlled gain range of more than 90dB. The I and Q demodulators, each consisting of a multiplier followed by a 2-pole, 2MHz low-pass filter, are driven by a phase-locked loop providing inphase and quadrature clocks. An internal AGC detector is included, and the temperature stable gain control system provides an accurate RSSI capability.

The I and Q demodulators provide inphase and quadrature baseband outputs to interface with Analog Devices' AD7013 (IS54/IS136, TETRA, MSAT) and AD7015 (GSM) baseband converters.

Key specifications for the AD607 are summarized in Figure 3.55.

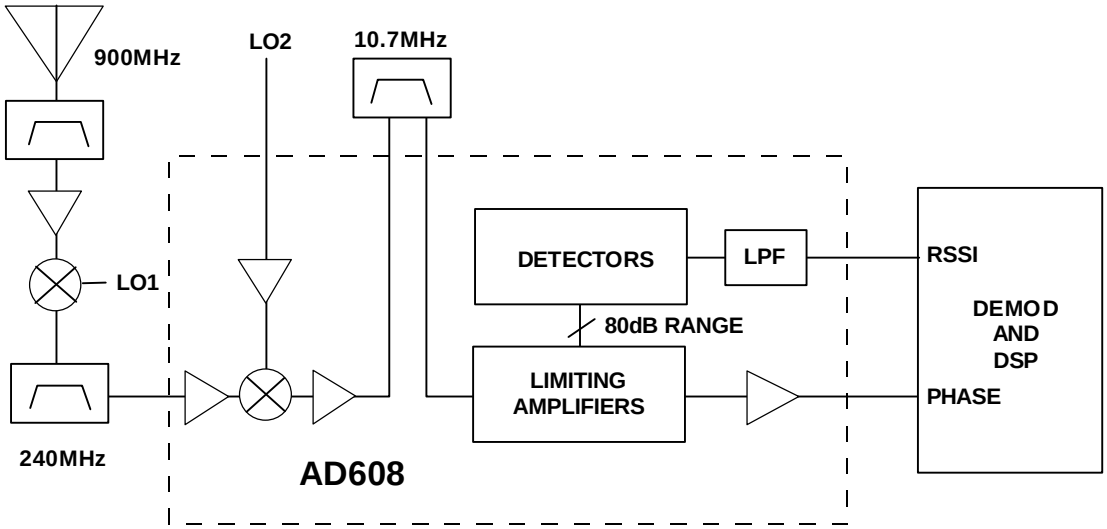
AD607 MIXER / AGC / RSSI 3V RECEIVER KEY FEATURES

- **Mixer:**
  - **–15dBm Input 1dB Compression Point**
  - **–8dBm Input Third Order Intercept Point**
  - **RF/LO Inputs to 500MHz**
  - **12dB Noise Figure, Matched Input**
  - **–16dBm LO Drive**
- **Linear IF Amplifier:**
  - **45MHz Bandwidth**
  - **Linear-in-dB Gain Control Over 90dB Gain Range**
  - **–15dBm Input 1dB Compression Point**
  - **+18dBm Output Third Order Intercept Point**
- **In-Phase and Quadrature Demodulators:**
  - **1.5MHz Output Bandwidth**
  - **Compatible with Baseband Converters (AD7013, AD7015)**
- **25mW Total Power @ Single +3V Supply**

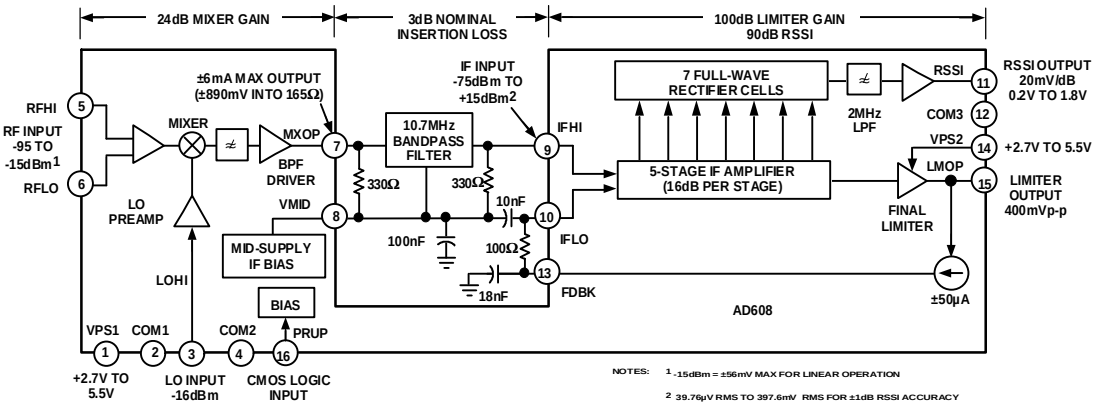
ANALOG DEVICES **3.55**

For cases where the signal is represented in polar form, the AD608 is the proper choice. The AD608 Mixer/Limiter/RSSI 3V Receiver IF Subsystem consists of a mixer followed by a logarithmic amplifier; the logarithmic amplifier has both limited output (phase information) and an RSSI output (amplitude information). This architecture is useful in polar demodulation applications as shown in Figure 3.56. A block diagram of the AD608 is shown in Figure 3.57, and key specifications in Figure 3.58.

RECEIVER BASED ON AD608 SUBSYSTEM USING POLAR DEMODULATION



AD608 FUNCTIONAL BLOCK DIAGRAM



ANALOG DEVICES

AD608 MIXER / LIMITER / RSSI 3V RECEIVER KEY FEATURES

- **Mixer:**
  - **–15dBm Input 1dB Compression Point**

- **–5dBm Input Third Order Intercept Point**
- **RF/LO Inputs to 500MHz**
- **12dB Noise Figure, Matched Input**
- **–16dBm LO Drive**

- **Logarithmic Amplifier / Limiter:**
  - **100dB Limiter Gain, 90dB RSSI**
  - **±1dB Log Linearity**
  - **±3° Phase Variation, –75dBm to +5dBm IF @ 10.7MHz**

- **21mW Total Power @ Single +3V Supply**

The log amp both measures the level of the signal (like the AD641 and AD606) and limits the signal. The RSSI or Received Signal Strength Indicator output is proportional to the log of the input signal. As a limiting amplifier, the AD608 removes any amplitude changes in the signal and keeps only the phase or frequency changes. These phase or frequency changes are proportional to the modulating signal and contain the intelligence in the signal. The AD608's limiting amplifier is a 5-stage log amp with more than 80dB of dynamic range.

In a typical mobile phone application, the RF signal (typically 900MHz or 1800MHz) is mixed down to the first IF (typically 240MHz), is filtered, and enters the AD608, where it is mixed down to a second IF at 10.7MHz, where it is amplified, limited, and measured. The limited output is demodulated by an external frequency or phase demodulator. The RSSI output is digitized by an ADC and used for active power control in the phone system.

As a practical note, the cutoff frequency of the log amp's internal low pass filter depends on what range of frequencies the log amp was designed for. In analog cellular systems, where the modulation mode is narrow-band FM, the IF is typically 450kHz. The low pass filters in the IF ICs designed for these standards have a fairly low cutoff frequency, and the filter's voltage output response provides a "slow" RSSI. In GSM (Global System for Mobile Communications) and PHS (Personal Handy System) applications, the IF is typically 10.7MHz or higher, and the filter's voltage output response provides a "fast" RSSI. The cutoff frequency of the low pass filter in the AD608 is 2MHz.

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