CHAPTER 6

APPLICATIONS

6.1 BASIC APPLICATIONS CIRCUITS

6.1.1 DAC as a Multiplier and Attenuator

It was pointed out in Section 1.3 that, in the current-steering mode, the CMOS DAC multiplies the digital input value by the analog input voltage at V_{REF} for any value of V_{REF} up to ±25 volts. This in itself is a powerful tool. Any applications requiring precision multiplication with minimal zero offset and very low distortion must consider the CMOS DAC as a candidate. CMOS DACs are widely used as audio frequency attenuators. The audio signal is applied to the V_{REF} input and the attenuation code is applied to the DAC; the output voltage is the product of the two—an attenuated version of the input.

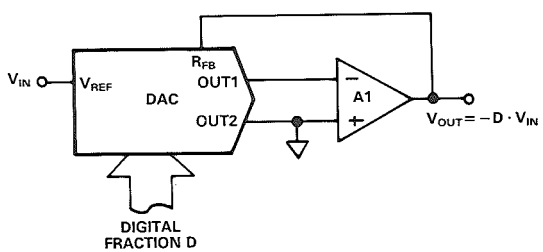


Figure 6.1.1 CMOS DAC as Multiplier or Attenuator

Conventional DACs provide a limited range of attenuation which is linear with code: an 8-bit DAC has a maximum attenuation range of 256:1 or 48dB, a 12-bit DAC gives 4096:1 or 72dB. To simplify the application of CMOS DACs as audio attenuators with logarithmic gain adjustment, three special purpose LOGDACs are available which are coded to give attenuation in equal decibel steps. See Section 6.8.

6.1.2 DAC as a Divider or Programmable Gain Element

If a CMOS DAC is connected as the feedback element of an op amp and R_{FB} is used as the input resistor, as shown in Figure 6.1.2, then the output voltage is inversely proportional to the digital input fraction D. For $D = 1-2^{-n}$ the output voltage is

$$V_{OUT} = -\frac{V_{IN}}{D} = -\frac{V_{IN}}{(1-2^{-n})}$$

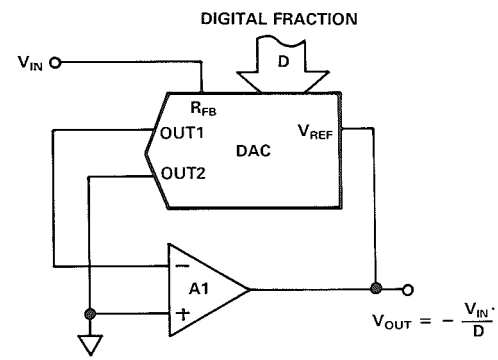


Figure 6.1.2 CMOS DAC as a Divider or Programmable Gain Element

As D is reduced, the output voltage increases. For small values of the digital fraction D, it is important to ensure that the amplifier does not saturate and also that the required accuracy is met. For example, an eight bit DAC driven with the binary code 10H (00010000), i.e., 16 decimal, in the circuit of Figure 6.1.2 should cause the output voltage to be sixteen times V_{IN}. However, if the DAC has a linearity specification of ± 1/2LSB then D can in fact have the weight anywhere in the range 15.5/256 to 16.5/256,

so that the possible output voltage will be in the range $15.5V_{IN}$ to $16.5V_{IN}$—an error of ±3% even though the DAC itself has a maximum error of 0.2%. The possible error in gain due to an E% linearity error in the DAC is approximately given by:

$$\text{Divider Gain Error} = \pm\frac{E}{D}\ \%$$

It can be seen that a programmable gain circuit with a gain of 16 specified to a maximum error of 1% requires a DAC with 0.06% absolute accuracy—i.e., an 11-bit DAC with ±3/4LSB linearity (AD7545KN would suffice).

DAC leakage current is also a potential error source in the divider circuit. The leakage current must be counterbalanced by an opposite current supplied from the op amp through the DAC. Since only a fraction D of the current into the V_{REF} terminal is routed to the OUT1 terminal, the output voltage has to change as follows:

$$\text{Output Error Voltage Due to DAC Leakage} = \frac{\text{Ilkg}\cdot R}{D}$$

where R is the DAC resistance at the V_{REF} terminal. For a DAC leakage current of 10nA, R = 10 kilohm and a gain (i.e., 1/D) of 16 the error voltage is 1.6mV. DAC leakage currents are normally less than 10nA up to 70°C.

6.1.3 Programmable Integrator Circuit

The circuit of Figure 6.1.3 shows a DAC connected as a programmable integrator. The output voltage is given by:

$$V_{OUT} = -\frac{1}{CR}\cdot D\int V_{IN}\ dt.$$

The integrator time constant is shortest when the DAC is at full scale and longest when the DAC is set to near zero code. The feedback resistor R_{FB} is not used in the integrator circuit and it is recommended that R_{FB} be tied to OUT1. The time constant of the integrator is proportional to C and R, the resistance of the DAC. It is normal to include a variable resistor R1 in series with the DAC to allow the full scale time constant to be trimmed to the appropriate value.

The temperature coefficients of the DAC, trim resistor and capacitor are unlikely to match so that the integrator time constant will vary somewhat with temperature. The dependance on the DAC resistance and its temperature coefficient can be removed by using the circuit of Figure 6.1.4 but the temperature coefficients of C and R1 remain critical for applications with wide temperature variations. Programmable integrators form the basis of a number of medium frequency function generators and graphics circuits—see Section 6.6.

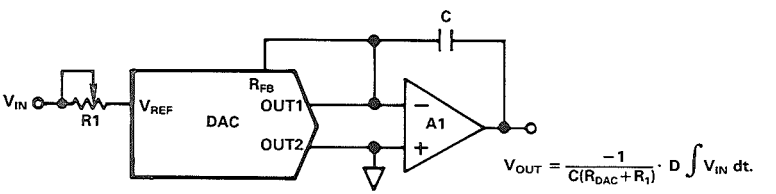


Figure 6.1.3 Programmable Integrator (Inverting)

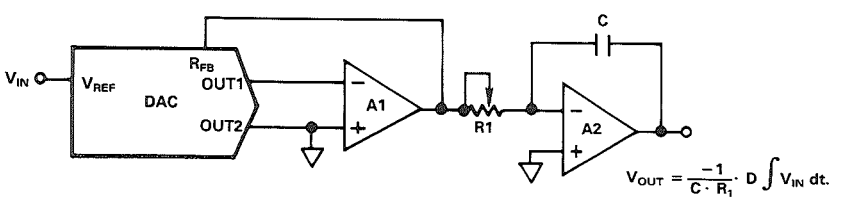
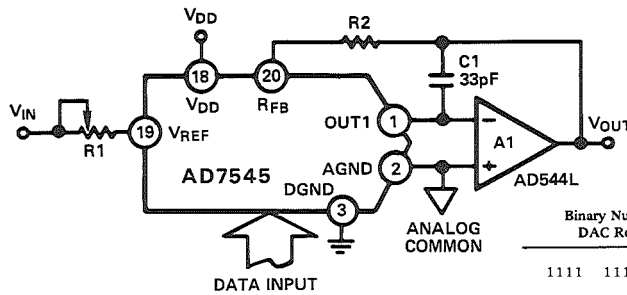


Figure 6.1.4 Programmable Integrator (Noninverting)

6.2 D/A CONVERTERS AND PROGRAMMABLE POWER SUPPLIES

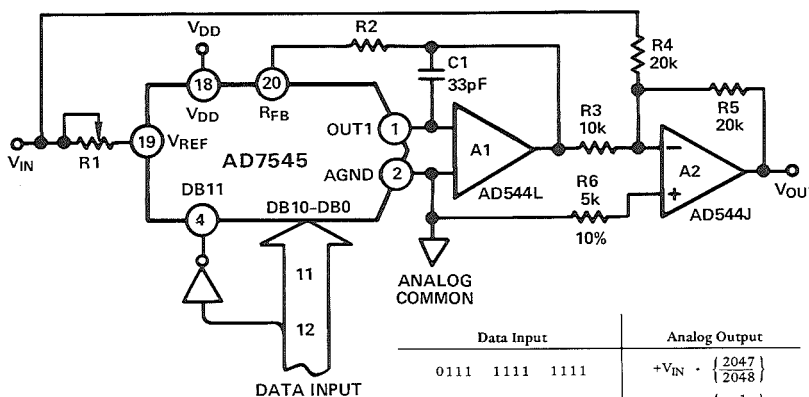
Figures 6.2.1, 6.2.2 and 6.2.3 show conventional circuits for using CMOS DACs. This type of circuit has been discussed at length in the text.



TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

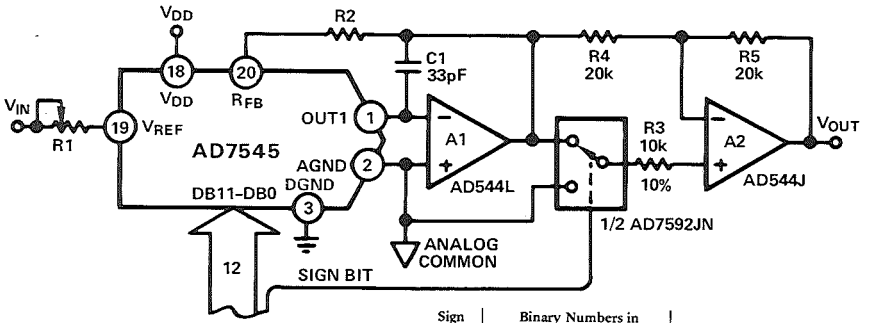
Binary Number in DAC Register	Analog Output
1111 1111 1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000 0000 0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000 0000 0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000 0000 0000	0 Volts

Figure 6.2.1 Low Cost 12-Bit Unipolar D/A Converter



Data Input	Analog Output
0111 1111 1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000 0000 0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000 0000 0000	0 Volts
1111 1111 1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000 0000 0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Figure 6.2.2 12-Bit Bipolar D/A Converter (2's Complement)



Sign Bit	Binary Numbers in DAC Register	Analog Output
0	1111 1111 1111	$+V_{IN} \cdot \{\frac{4095}{4096}\}$
0	0000 0000 0000	0 Volts
1	0000 0000 0000	0 Volts
1	1111 1111 1111	$-V_{IN} \cdot \{\frac{4095}{4096}\}$

Note: Sign bit of "0" connects R3 to GND.

Figure 6.2.3 12-Bit Plus Sign/D/A Converter

6.2.1 D/A Converter with Minimal Leakage Current

Figure 6.2.4 shows the AD7545 operated in the single-supply current-steering mode described in section 3.6. This type of circuit will operate correctly only when the ladder termination resistor is connected to OUT2/AGND as is the case for the AD7545. The P-well for the DAC switches is connected to DGND so that the P-well to N-channel switch diode (see Figure 2.2) is reverse biased by V_{IN}. This reverse bias minimizes leakage currents flowing from the P-well to the switches; it also drives the off-switch hard off due to the body-effect of the P-well (i.e., the well behaves like a second gate), which in turn reduces off-switch leakage. If V_{IN} is in the range 0 to +5V, the DAC linearity does not suffer unduly from the reverse bias of the P-well and 12-bit linearity is maintained up to quite high temperatures, with exceptionally low leakage currents. Certain aspects of this circuit design are the subject of a patent application.

6.2.2 Dual 8-Bit DAC—Single +5V Supply

Figure 6.2.5 gives the circuit for a low cost dual 8-bit DAC operating from a single +5V. This circuit is an effective way to provide a personal computer with two analog output channels to drive chart recorders, X-Y plotters etc. Care should be taken to minimize logic noise on the +5V and DGND lines to the D/A converter. A simple filter comprising R3, C1 and the ferrite bead cut down any noise. The circuit operates the two DACs in the voltage-switching mode with a

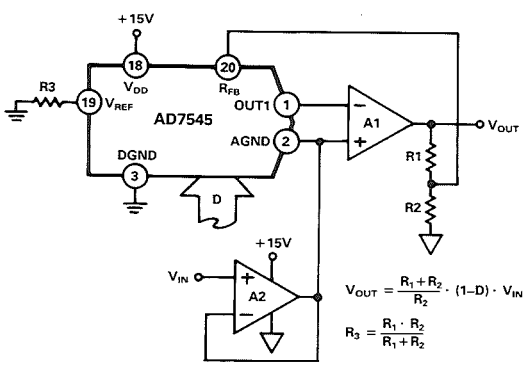


Figure 6.2.4 12-Bit D/A Converter for High Temperature Operation

+0.6V reference derived from an AD589 1.23V bandgap reference. The output voltage covers the range 0 to 2.54 volts in 10mV steps. If possible, gate the digital inputs as recommended in 5.3.1 (i.e., the DAC inputs are only active when the DAC is addressed). This helps minimize digital feedthrough spikes.

6.2.3 Low Cost 14-Bit Resolution D/A Converter

If the DAC can be calibrated to a voltmeter, then the circuit of Figure 6.2.6 may be used. The two eight-bit DACs are connected so that the reference voltage of DAC A is roughly 1/64 the reference voltage of DAC B. Resistor R2 should be less than one fifth the value of the DAC resistance. This minimizes the effect of changes in RDAC from one device to another.

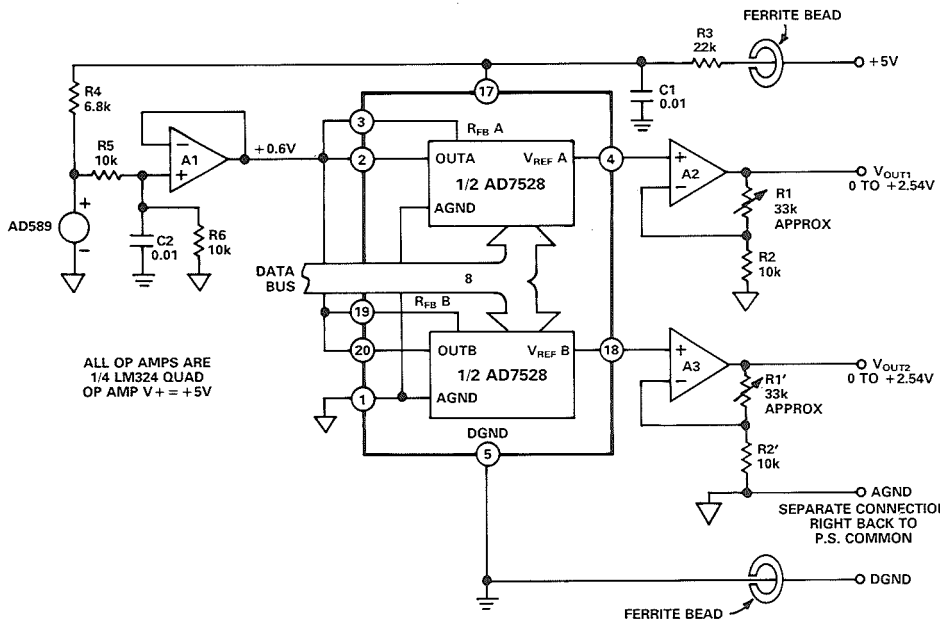


Figure 6.2.5 Dual DAC – Single 5V Supply

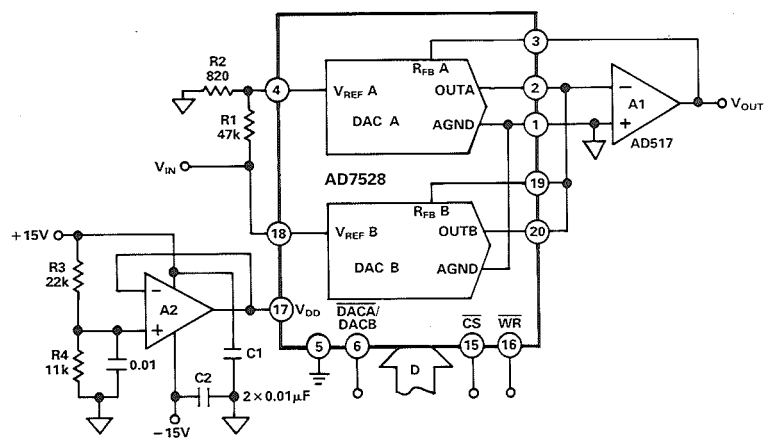


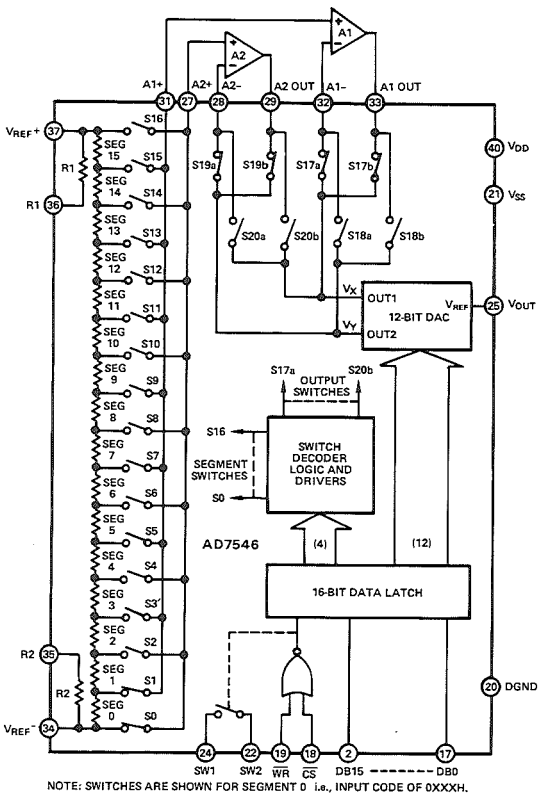
Figure 6.2.6 Low Cost 14-Bit Resolution D/A Converter

DAC B is used to provide a "coarse" setting of the output voltage and DAC A gives a fine adjustment upwards from DAC B setting. The total range covered by DAC A is equal to 4LSBs of the DAC B range. Clearly, DAC A and DAC B must be adjusted within a closed loop and this procedure is not always practical. Section 6.3.2 describes the application of this circuit to trim out the gain-error of a DAC.

In order to obtain satisfactory performance from this circuit, it is necessary to ensure that power lines and V_{IN} are noise free and stable. This is done by deriving the +5V for V_{DD} from the +15V via an op amp. The circuit operates satisfactorily over a wide temperature range, but it requires recalibration if the operating temperature changes because R1 and R2 temperature coefficients will not match those of the DAC. The input offset of amplifier A1 should be nulled to minimize DAC linearity errors due to amplifier input offset.

6.2.4 A 16-Bit D/A Converter[17]

Figure 6.2.7 shows the block diagram of the AD7546 16-bit resolution D/A converter (U.S. Patent No. 4338591). It consists of a 12-bit DAC, operated in the voltage-switching mode, and a tapped divider of 16 equal resistors to provide the voltages to OUT1 and OUT2 of the DAC. The 16 resistors divide the reference voltage into 16 equal segments and the voltage across a particular segment is applied to the DAC.



NOTE: SWITCHES ARE SHOWN FOR SEGMENT 0 i.e., INPUT CODE OF 0XXXH.

Figure 6.2.7 16-Bit D/A Converter

Since the segment voltage is only one sixteenth of the reference voltage, the potential difference between OUT1 and OUT2 is relatively small and nonlinearity errors due to unequal voltages across the NMOS DAC switches are minimized. A significant feature of the AD7546 is that it allows low cost FET input op amps to be used for the segment buffers and achieves a full 16-bit settling in 10μs. For the same resolution, an extended R-2R ladder would require op amps with excellent input offset and leakage current specifications; and it would have a much longer settling time because of the added switch capacitance at the OUT1 mode.

Since the AD7546 uses its DAC in the voltage-switching mode, it can readily be operated with a single supply. For further information on the AD7546 refer to the data sheet available from Analog Devices.

6.2.5 Simple Programmable Power Supply[6]

The circuit in Figure 6.2.8 shows a simple programmable power supply with programmable current limit. DAC A is used as a programmable voltage source and DAC B sets the current limits. R_{FB} A is not connected directly to the output but via a buffer amplifier, as shown, to eliminate any loading on the output which might cause a false value of I_{OUT}. The dual amplifier feedback of A1 and A3 oscillates with some amplifiers. The differential voltage across RS2 is amplified by A4 and fed to the feedback resistor of DAC B. The current in R_{FB} B is compared to a programmable current of opposite polarity flowing to DAC B. The net difference is applied to A2 which is connected as a "soft" comparator (Gain approx. 100). When over-current exists, the output of amplifier A1 is pulled to ground via RS1 and D1, RS1 limits the short circuit current. The output of amplifier A4 provides a useful indication of the current flowing. Figure 6.2.9 shows a similar circuit for bipolar operation,—i.e., 0 to ± 10V.

Section 6.3.5 shows how CMOS DACs can be used with the popular 723 voltage regulator to create a number of different power supply circuits.

6.3 CMOS DAC AS A CALIBRATION TRIMMER

CMOS DACs can be used to replace trim resistors in most circuits provided the designer makes allowance for this at an early stage. This approach is particularly suitable in self-calibrating type instruments; not only does it improve the instruments' performance but it also eliminates the requirement for trim resistors. This reduces production cost and test time. For example, the instrumentation amplifier shown in Figure 6.3.1 is particularly expensive to use in its basic form because it requires precisely matched resistors and two trim resistors. Additionally the calibration procedure is time consuming and can be a production line bottleneck. However, by replacing the trim-resistors with CMOS DACs the overall production cost and set-up time can be significantly reduced.

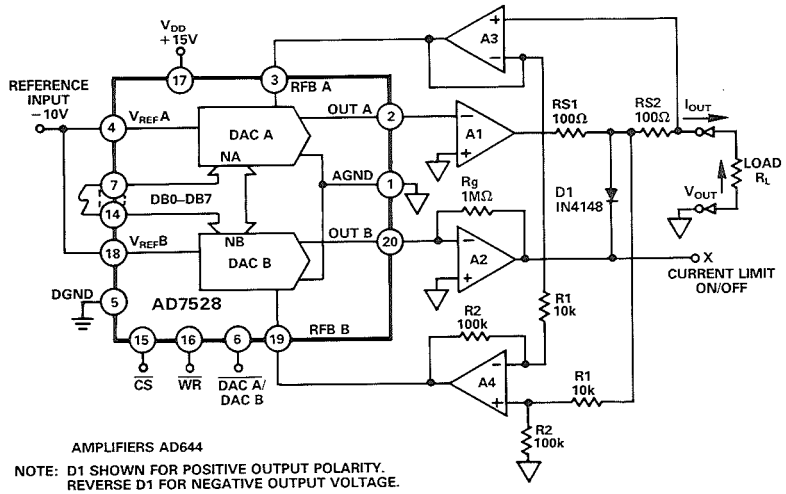


Figure 6.2.8 Programmable Voltage/Current Source V_{OUT} = 0 to +10V, I_{OUT} = 0 to +10mA

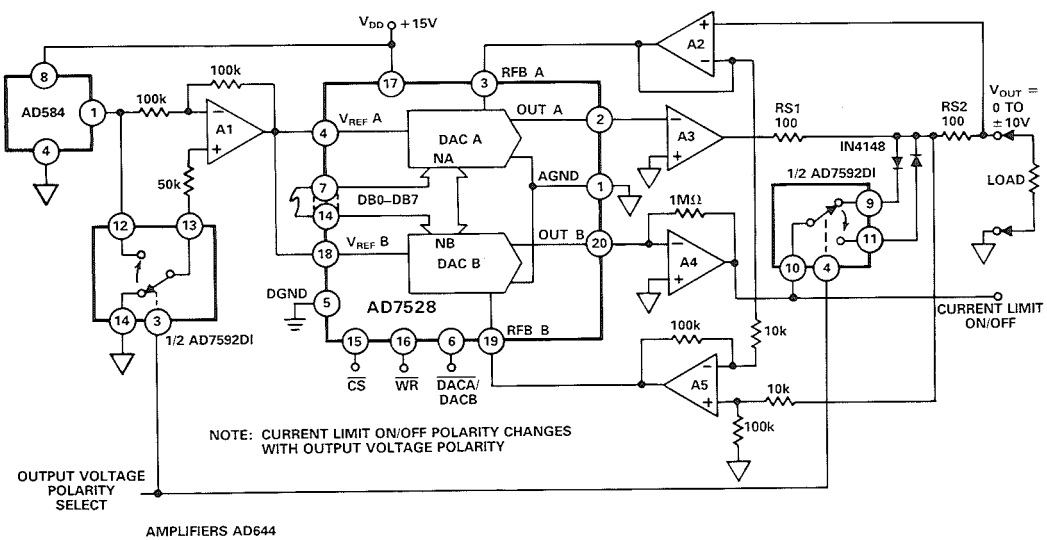
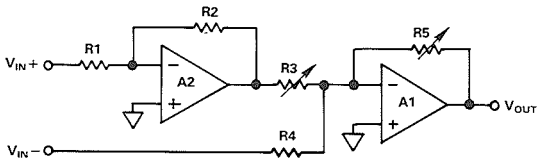


Figure 6.2.9 Programmable Voltage/Current Source with Bipolar Output



$$V_{OUT} = \frac{R_5}{R_3} \cdot \frac{R_2}{R_1} (V_{IN}+) - \frac{R_5}{R_4} (V_{IN}-)$$

Figure 6.3.1 Instrumentation Amplifier

6.3.1 Simple Potentiometer Connection

Figure 6.3.2 shows the simplest practical potentiometer connection and its equivalent circuit. The equivalent trim resistor has a maximum value equal to R3 and a minimum value approximately equal to:

$$\frac{R3}{1 + \frac{R3}{RDAC}}$$

The output voltage V_{OUT} is given by:

$$V_{OUT} = \frac{V1 \cdot R2}{R2 + \left\{\frac{RDAC \cdot R3}{RDAC + D \cdot R3}\right\}}$$

The feedback resistor of the DAC can often be used for R3, and since R3 = RDAC, the relationship simplifies to:

$$V_{OUT} = \frac{V1}{1 + \frac{RDAC}{R2} \cdot \left\{\frac{1}{1 + D}\right\}}$$

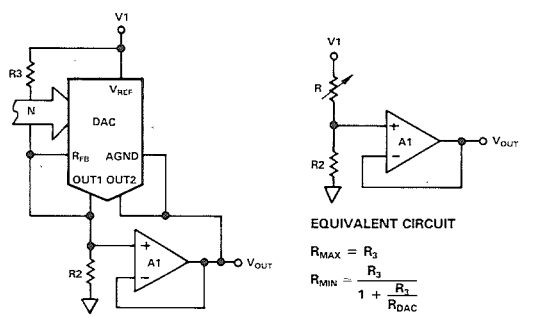


Figure 6.3.2 Simple Potentiometer Circuit

This type of circuit works provided the following constraints are observed:

i) The ladder termination resistor is connected to AGND or OUT2 (see Appendix A1).

ii) V_{DD} is at least 4V more positive than the maximum value of V_{OUT}. This is necessary to preserve DAC linearity.

iii) V1 is positive. Negative values of V1 will turn on internal diodes causing device destruction.

DAC types AD7528, AD7545, AD7240 and AD7548 are particularly suitable for this kind of application. If the AD7528 and AD7545 are operated with a V_{DD} other than +5V, their digital inputs are not TTL compatible. Note how the amplifier is used to bootstrap the potential at OUT2 to be equal to that at OUT1.

The specified resistance of the DAC generally covers quite a wide range; this results in some restriction on the application. Figure 6.3.3 shows an improvement which reduces the effect of variation in RDAC and also allows the trim to cover a narrower range with better resolution. For the equivalent circuit, the maximum value of the trim resistor is equal to R3 and the minimum value of the trim resistor is equal to R3 in parallel with (R1 + RDAC).

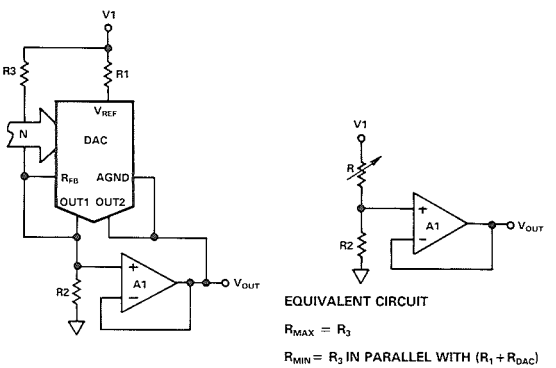


Figure 6.3.3 Potentiometer Circuit with Reduced Range and Improved Resolution

6.3.2 Dual DAC Trims Gain Error

Most CMOS DACs have a specified gain error of the order of 5% which is usually trimmed out by the use of an external trim resistor as described in Section 3.1. An alternative way of doing this is to use the AD7528 dual DAC to build a 14- bit DAC as described in Section 6.2.3. This 14-bit DAC then supplies the reference voltage to the main DAC in use. Figure 6.3.4 shows such a scheme for AD7545, although it could be used with any DAC. The AD7528 DAC combination covers a voltage range which can correct for any gain error in the AD7545. The input offset voltage of amplifier A1 must be nulled because DAC B operates with a very low value of V_{REF} and any input offset voltage may cause differential linearity errors in DAC B. To calibrate the circuit, full scale (all 1's) is applied to the AD7545 and the various codes are loaded to the AD7528 until the

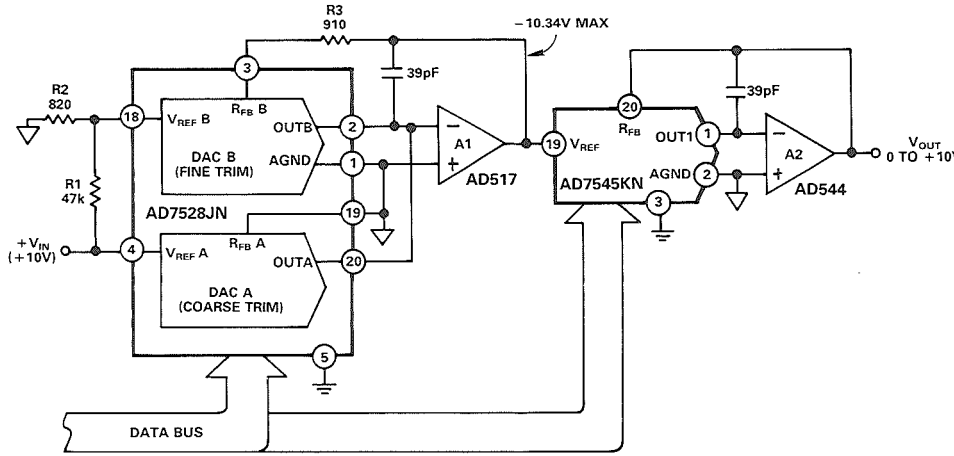


Figure 6.3.4 DAC Gain Error Trim Using AD7528 Dual DAC as Coarse/Fine Trim

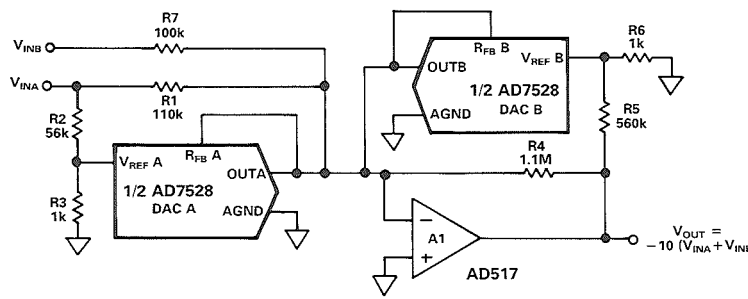


Figure 6.3.5 Precision Summing Amplifier

output voltage is correct. Once the system has been calibrated, the DAC output is determined by the AD7545; no further interaction with the AD7528 is required until the next recalibration.

6.3.3 Precision Gain Summing Amplifier

Precision gain amplifiers require the use of a trim resistor to set the appropriate gain at calibration time or entail the use of high cost precision resistors. The circuit of Figure 6.3.5 provides an alternative solution by using a dual DAC as shown. DAC A is adjusted to provide matching between the two inputs and DAC B is used to adjust the gain over a narrow range. The resistors R2, R3 and RDAC give rise to a small current in DAC A which is steered either to AGND or the amplifier summing junction. Similarly R5 and R6 feed back a small fraction of the output signal through DAC B. R3 and R6 should be about one fifth the maximum value of RDAC in order to make the circuit insensitive to different values of RDAC. For 5% resistance values, the circuit shown delivers 0.1% worst case channel to channel mismatch and 0.1% worst case gain error. Amplifier A1 should have very low input offset voltage because the two DACs operate with a low reference voltage.

6.3.4 Instrumentation Amplifier

Figure 6.3.1 shows a classic two amplifier instrumentation amplifier. It is useful in applications which have a high common-mode voltage at the inputs. Resistors R3 and R5 must be carefully trimmed to achieve good common-mode rejection and the correct gain. In a self-calibrating system, R3 and R5 are replaced by the AD7528 dual DAC circuit as shown in Figure 6.3.6. DAC A is then set by tying both inputs to the common voltage and adjusting the code to DAC A until the output is zero. DAC B code is adjusted to give the correct output for a known input voltage difference. The circuit shown will handle common-mode voltages up to 30V with a gain of 10 accurate to 0.1%.

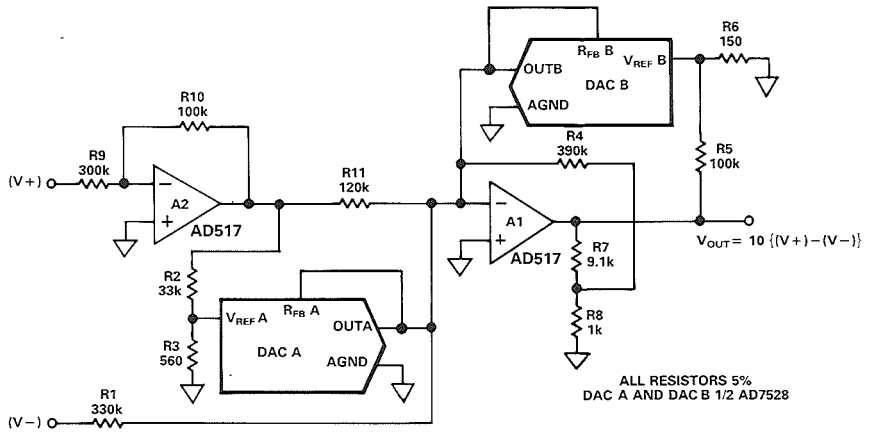


Figure 6.3.6 Instrumentation Amplifier with Digital Calibration for Common-Mode Rejection and Gain

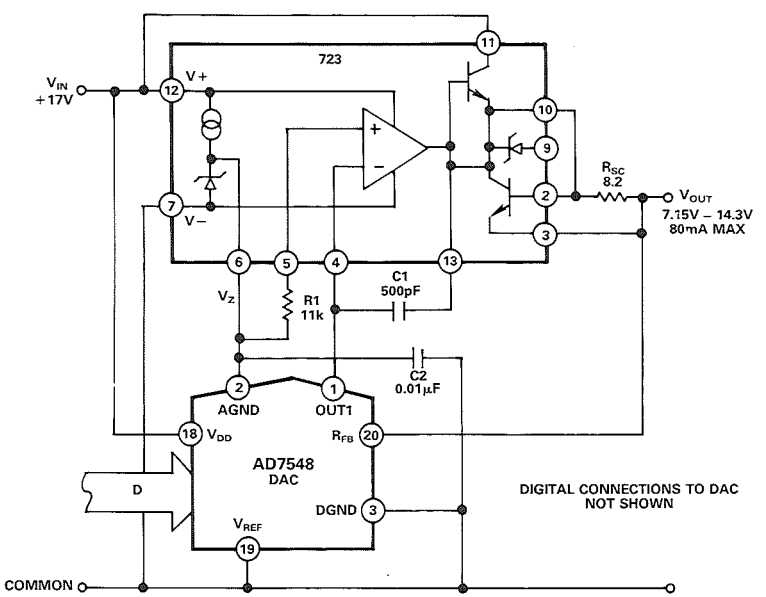


Figure 6.3.7 Simple 2 IC Programmable Power Supply

6.3.5 Programmable Power Supply Using 723 Voltage Regulator

Applications circuits for the 723 voltage regulator generally require a trim resistor to set the output voltage. For many of these circuits the trim resistor can be replaced by a CMOS DAC to form a digitally programmable power supply which can be programmed directly from an 8-bit bus. The circuit given here operates from a single supply and in its simplest form consists of just the 723 and a CMOS DAC with no additional active components.

Figure 6.3.7 shows a basic circuit which has an output programmable from 7.15 to 14.3 volts. The internal 7.15 reference voltage (V_{REF}) of the 723 drives the noninverting input of the 723 amplifier directly and fixes the AGND voltage of the DAC at 7.15 volts. The feedback resistor (R_{FB}) of the DAC and the DAC itself form a potential divider chain across the output and the 723 regulates to force the negative input of its amplifier to V_Z. The DAC is, therefore, operated with OUT1 and AGND at the same voltage (V_Z)—a necessary condition to ensure DAC

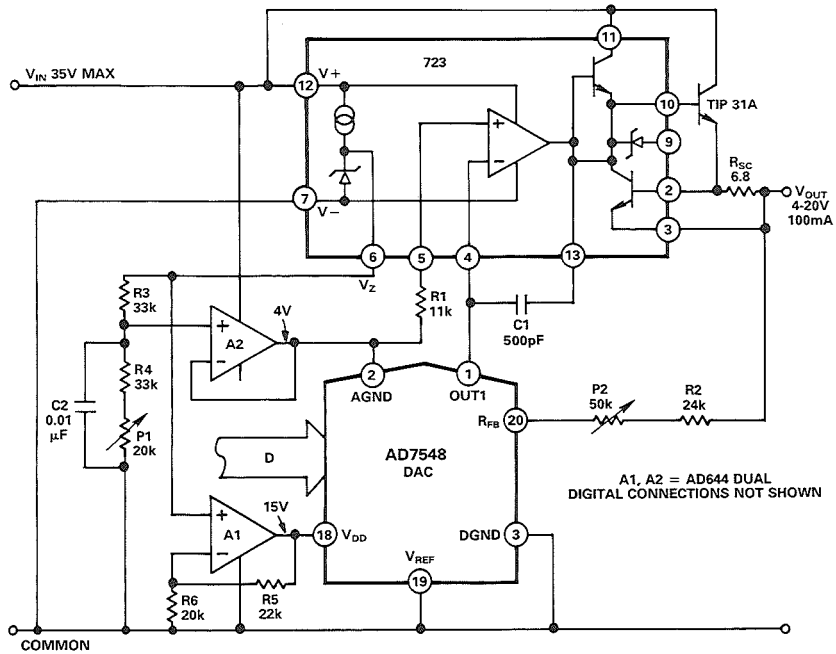


Figure 6.3.8 Inproved Programmable Power Supply

linearity. The input resistance of the DAC at the OUT1 node is equal to RDAC/D where D is the fractional binary input to the DAC and RDAC is the DAC input resistance. It is easily shown that:

$$V_{OUT} = V_Z(1 + D \cdot R_{FB}/RDAC)$$

and since R_{FB} usually matches RDAC to better than 0.5% this reduces to $V_{OUT} = V_Z(1 + D)$—a convenient transfer equation. The AD7548 is used because its inputs are TTL compatible and it interfaces directly to most microprocessor bus systems. Other DACs can be used in place of the AD7548 but the user should ensure that the AGND and DGND terminals are separately available and that logic inputs to the DAC are TTL compatible.

The maximum output current is determined by the power dissipation of the 723: the value of R_{SC} shown limits the current to the recommended value of 80mA for a plastic encapsulated device operated at an ambient temperature of 25°C without a heat-sink. Output current can be increased by heat sinking the 723 and/or using an external transistor as shown in Figure 6.3.8. The supply voltage to the AD7548 must be at least 5V greater than V_Z for the DAC to operate correctly and it should not exceed 17V. Resistor R1 minimizes errors due to different source impedances at the 723 amplifier inputs.

An alternative output voltage range of 3.6 to 7.15 volts can be achieved by connecting the potential divider chain between V_Z and ground, with the center tap going to the positive input of the amplifier: AGND, the output voltage V_{OUT} and the negative input of the amplifier are tied together. In this case the transfer equation is $V_{OUT} = V_Z/(1 + D)$.

In practice V_Z varies from one device to another and it is desirable to include provision for calibrating the power supply. Figure 6.3.8 shows a circuit which achieves this and incorporates a number of other improvements. It operates with any input voltage up to 35V and the output is programmable in the range 4.096 to 20.48 volts (i.e., 16mV/bit for 10-bit resolution). Output current is set to limit at 100mA. Other output currents can be accommodated by using different values of Rsc ($R_{SC} = 0.675/I_{SC}$ for $T_A = 25°C$) and by ensuring that the external transistor can handle the necessary power dissipation. Amplifier A1 buffers V_Z and provides the +15V supply to the DAC. Amplifier A2 generates an adjustable 4V reference voltage which drives the positive input of the 723 amplifier. A variable resistor P2 in series with R_{FB} sets full scale output. To calibrate the circuit D = 0 is applied to the DAC using the data override facility of the DAC and P1 adjusted for 4.096 volts out: then all 1's are applied to the DAC using the override and P2 adjusted for maximum output which

is (20.480 – 0.004) = 20.476 volts. The 723 amplifier has insufficient gain, and excessive input bias currents and offset voltage for the AD7548 to realize its full 12-bit monotonic range. In practice the circuit gives adequate performance for 10-bit resolution i.e. 16mV/bit.

6.4 PROGRAMMABLE CURRENT SOURCES

6.4.1 Basic Current Source Circuits

Programmable current sources form an important part of the analog circuit designers tool kit. They can be used as part of a larger circuit or can exist in their own right. Most of the circuits presented here are self explanatory—they establish a reference current programmed by a DAC, and then mirror the current until it flows in the right direction from the appropriate source. For eight-bit applications, the reference current can often be created by the DAC itself as shown in Figure 6.4.1. A fixed reference voltage is applied to the V_{REF} terminal of the DAC and the reference current created is the current flowing through the DAC itself. However, the D/A converter resistors exhibit an absolute temperature coefficient of the order of −300ppm/°C. For higher resolution or wide-temperature range applications, a more stable reference current is required. This can be achieved

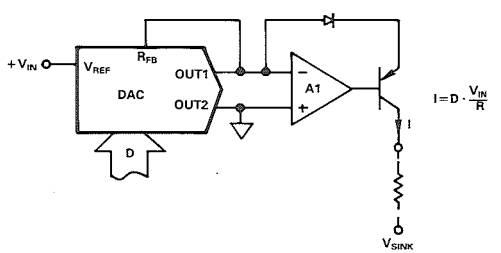


Figure 6.4.1 Simple Programmable Current Source to V_{SINK}

by establishing a precision voltage with the DAC, which in turn causes a reference current to flow through a precision resistor as shown, for example, in Figure 6.4.4.

In the circuits of Figures 6.4.2 and 6.4.3, the parallel combination of R1 and R_{FB} provides a sense resistor which feeds back a current through R_{FB} proportional to I.

$$I = D \cdot \frac{V_{IN}}{R1} \cdot \left\{ 1 + \frac{R1}{RDAC} \right\}_{\text{if RDAC} = R_{FB}}$$

If R1 is made small compared with R_{FB} then the output current will be relatively insensitive to different

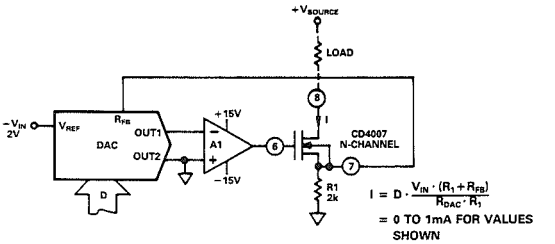


Figure 6.4.2 Programmable Current Sink from $+V_{SOURCE}$

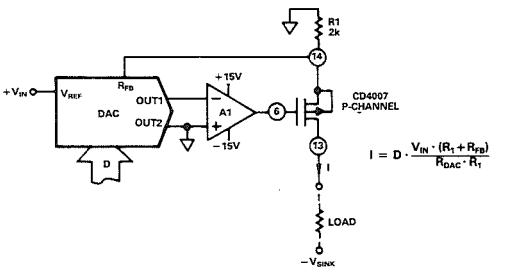


Figure 6.4.3 Programmable Current Source to $-V_{SINK}$

values of DAC resistance or the DAC resistance temperature coefficient.

The circuit of Figure 6.4.4 offers an even greater degree of insensitivity to DAC resistance. The DAC is operated as a programmable voltage source which sets a current through R1. This current is mirrored by Q1 and the same current creates a voltage drop across R3. Amplifier A2 and Q2 set up a proportional current I so that the voltages dropped across R3 and R4 are equal. In order to program right down to near zero levels of current, the input voltages of amplifier A2 must be capable of operating very close to V_{DD} and the output of A2 also must be able to swing near to V_{DD}. To achieve this, it is necessary to connect the positive supply point of the op amp to a voltage about 2.5V more positive than V_{DD}. Diodes D1 through D4 provide for this requirement.

The circuit of Figure 6.4.4 is insensitive to variations in V_{DD} because both R3 and R4 draw their current from the same node, and the output impedance of Q1 is very large due to the gain of amplifier A1. Resistor R2 protects Q1 from overload. Figure 6.4.5 shows a simple modification to the circuit for single supply operation. A further variation on the circuit of Figure 6.4.4 is shown in Figure 6.4.6. This provides a current source programmable in the range 0 to 1mA. NFET input op amps are used to reduce the effect of input bias currents and the bipolar transistors have

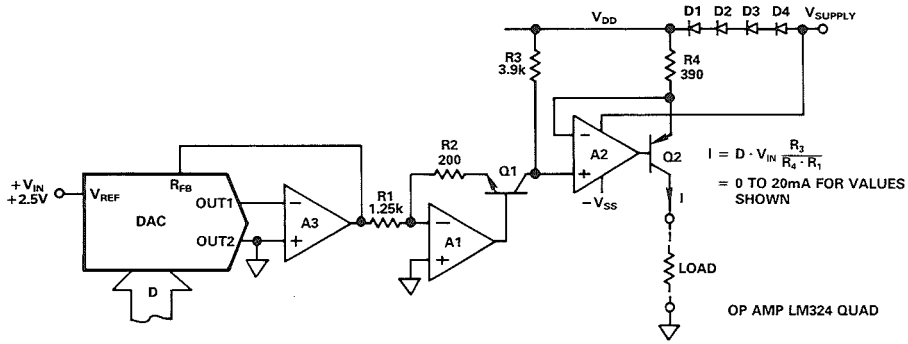


Figure 6.4.4 Programmable Current Source to AGND or $-V_{SINK}$

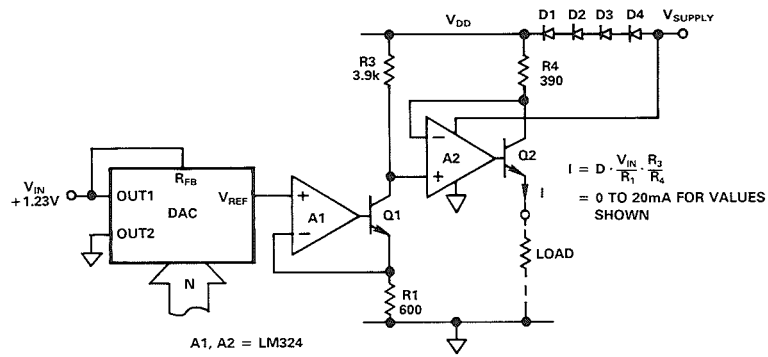


Figure 6.4.5 Single Supply Current Source to AGND

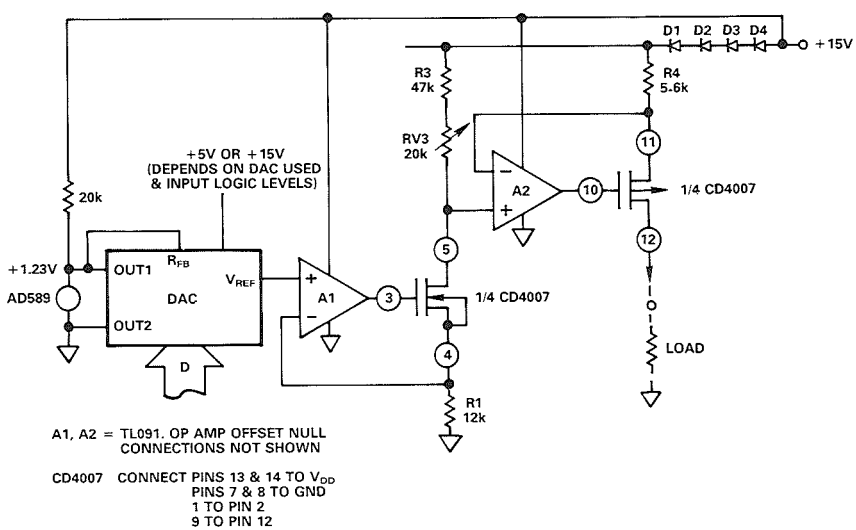


Figure 6.4.6 0 to 1mA Programmable Current Source – Single Supply

been replaced by MOS devices available on the CD4007 transistor array. It is important to null the input offset voltage of the amplifiers because the LSB bit weight of the DAC is only 5mV which is comparable to the typical input offset voltage of the TL091. The pin connections given for the CD4007 should be used to ensure correct operation of the device.

6.4.2 4-20mA Loop Circuits

Circuits of this class are used widely in the process control industry, particularly in the U.S.A. Analog values are transmitted from one point to another in a process plant as a current rather than a voltage to provide a greater degree of noise immunity. The effective 4mA offset on the scale can be used to power the remote receiver.

4-20mA loop circuits can be derived from any of the constant current-circuits described above. If the DAC is operated in the current-steering mode, the offset can be created by adding an offset current to the current from the OUT1 terminal of the DAC. If the DAC is operated in the voltage-switching mode, then the offset can be added by biasing OUT2 positive as described in Section 4.2.

Figure 6.4.7 shows the circuit of Figure 6.4.4 modified for 4-20mA loop applications. An additional current equal to $V_{IN}/4R$ is added to the summing junction of A1 via R8.

Figure 6.4.8 gives a simple 4-20mA loop circuit with the DAC operated in the voltage-switching mode. AGND is biased at approximately 300mV and OUT1 at 1.5V. The current in R1 is, therefore, $V_{OUT2}/R1$ for all zeroes code at the DAC and one bit less than $V_{OUT1}/R1$ for all ones applied to the DAC. The AD7545 and the op amps are operated from the +5V reference to improve system noise rejection. Since the DAC is CMOS, it draws very little supply current. Resistors R2, R3 and R6 improve the amplifiers' source capability (see Section 4.4.2) and R4 and R5 are used to set zero (4mA) and full-scale (20mA) respectively.

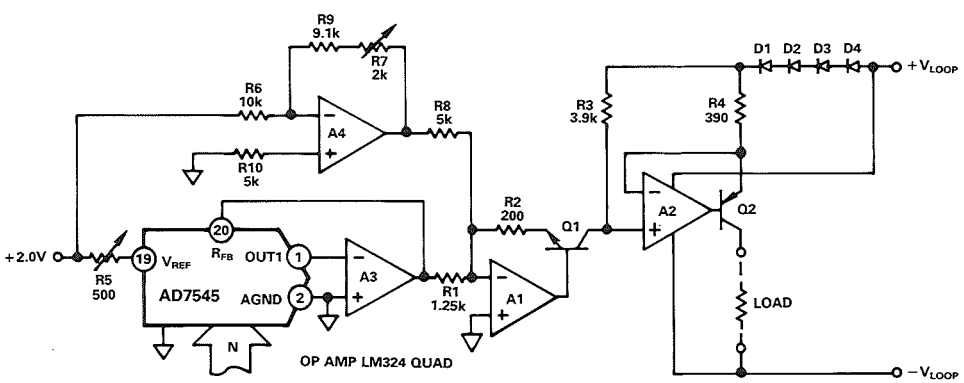


Figure 6.4.7 4-20mA Loop Circuit, Current-Steering Mode

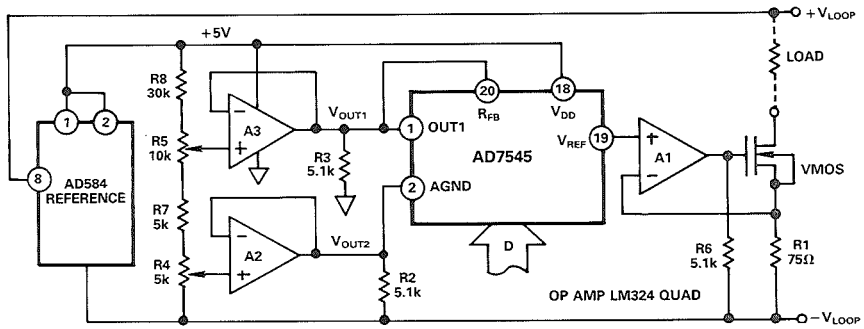


Figure 6.4.8 4-20mA Loop Circuit, Voltage-Switching DAC

6.5 LOW FREQUENCY FUNCTION GENERATION

6.5.1 Function Generation via DACs

Low frequency function generation is achieved by driving a DAC with a series of digital words representing the instantaneous values of the function to be synthesized. There is no limit to the lowest frequency that can be generated. The upper limit is determined by the settling time of the D/A converter circuit, the required resolution, permissible quantization noise etc.

Generally this method of function generation is used up to about 500Hz, although it can be extended up to about 20kHz if the DAC circuit is complemented with the appropriate filters, sample/hold etc. Digital audio systems use 14- and 16-bit D/A converters to reconstitute the analog audio signal.

Figure 6.5.1 shows the basic principle of a low frequency function generator. Since many functions are symmetric, it is normal to synthesize half a waveform and then invert it for the second half. For sinusoids, only the first quarter of the waveform need be synthesized and the remaining section can be derived using the relationships:

$$0 \le \theta < 90 \quad y = \sin\theta$$
$$90 \le \theta < 180 \quad y = \sin(180 - \theta)$$
$$180 \le \theta < 270 \quad y = -\sin\theta$$
$$270 \le \theta < 360 \quad y = -\sin(360 - \theta)$$

Figure 6.5.2 shows a block diagram of a sine-wave generator where the first quarter segment of the waveform is stored in ROM. The exclusive −OR is used to compute (180-θ) and (360-θ) and a sign magnitude coded DAC circuit is used to generate the appropriate polarity signal. In this type of function

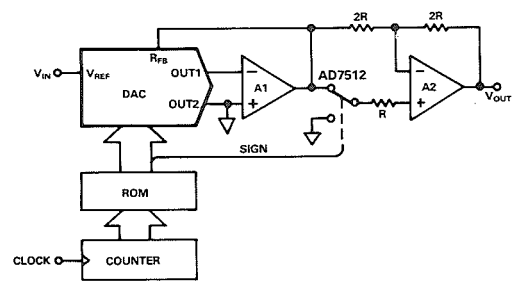


Figure 6.5.1 Basic DAC Based Low Frequency Function Generator

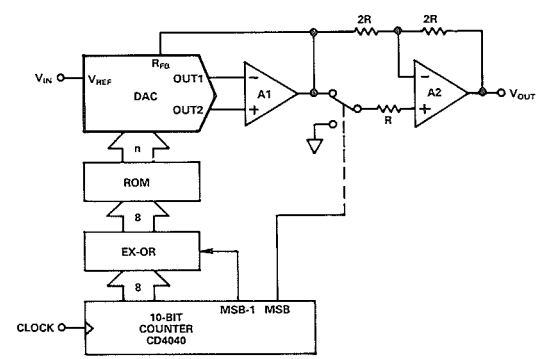


Figure 6.5.2 Block Diagram of Sinusoid Generator

generator, the amplitude of the output signal is easily controlled by varying V_{REF}.

Figure 6.5.3 shows a simple triangle waveform generator. The input clock frequency is applied to the CD4040 counter whose output drives the AD7524 DAC through exclusive −OR gates. The exclusive −OR inverts the binary code fed to the

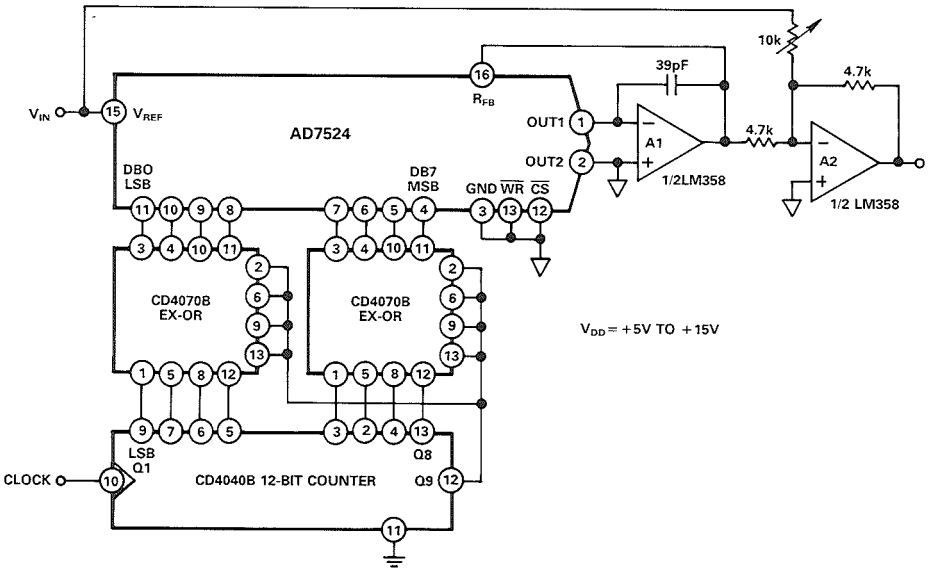


Figure 6.5.3 Simple Triangle Wave Generator

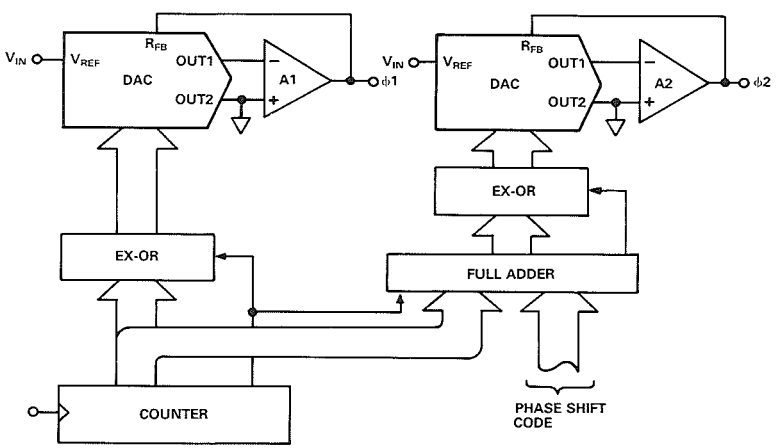


Figure 6.5.4 Two-Phase Triangle Wave Generator with Precision Phase Shift

DAC each half cycle. Consequently the binary number presented to the ROM counts up from 00000000 to 11111111 and then counts down from 11111111 to 00000000, thereby generating a well defined triangle waveform. Output amplitude is determined by V_{REF}, and the frequency is determined by the input clock frequency. Amplifier A2 shifts the dc level of the triangle to make it symmetrical about zero. Multi-phase waveforms can be generated by using an adder to add an offset to the binary code. Changing the offset code changes the phase between the waveforms and a very precise phase relationship between the waveforms can be achieved. Figure 6.5.4 shows the block diagram for a two phase waveform generator with adjustable phase relationship.

6.5.2 Triangle to Sine Conversion

There are various methods for converting a triangle waveform into other waveforms. A sinusoid can be approximated using the logarithmic relationship between V_{BE} and I_C of a bipolar transistor to smooth

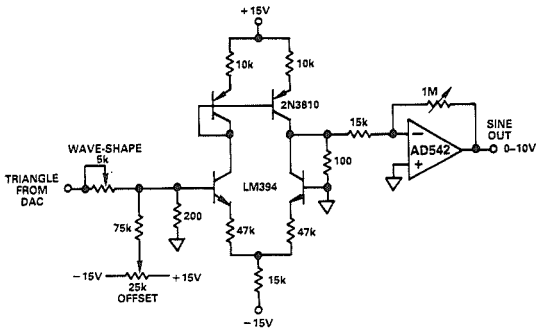


Figure 6.5.5 Triangle to Sine Wave Converter

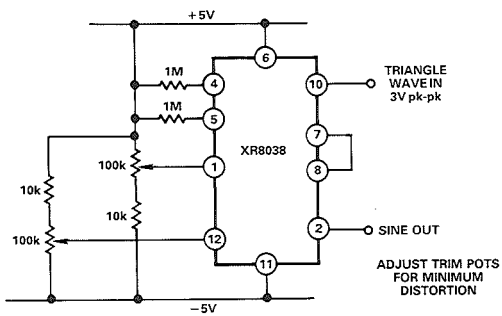


Figure 6.5.6 Monolithic Triangle to Sine Wave Generator

the triangular waveform. Figure 6.5.5 shows such a circuit described in References 7 and 8. A number of monolithic function generator circuits using this principle are also available (e.g., XR8038) and these can be used to convert a triangle wave into a sinusoid.[9] Figure 6.5.6 shows a sine wave generator which can be driven from the triangle-wave generator of Figure 6.5.3. An alternative method of obtaining a sine wave is to approximate it using the quadratic approximation.[10]

$$\sin\theta = 1.828.\theta + 0.828.\theta^2 \text{ for } 0 \leq \theta \leq \frac{\pi}{2}$$

Figure 6.5.7 shows a circuit to achieve this. DAC A and DAC B are driven from an up-down counter as shown. They form a pair of triangle wave generators as previously described. The reference voltage of DAC A is fixed, thus it delivers a simple triangle wave, i.e,. V_{OUT} A is proportional to D. This triangle wave is used as the reference voltage for DAC B so that DAC B behaves as a squaring circuit since both V_{REF} B and the digital inputs are determined by the digital value in the counter. DAC B output is, therefore, proportional to D^2. Amplifier A3 sums V_{OUT} A and V_{OUT} B in the proportion 1.828 : 0.828 and amplifier A4 delivers alternatively positive and negative half cycles. The circuit of Figure 6.5.7 can be used to synthesize sinusoids up to 2.5kHz with a distortion of −35dB. The values of R_A and R_B are critical to proper circuit operation and have a significant effect on wave-shape and distortion levels. Note how the circuit's oscillation rate is determined purely by the input clock frequency, consequently frequency changes are easily made. For amplitude modulation, the modulation voltage is applied to the V_{REF} terminal of DAC A. For more information on this circuit see Reference 10.

6.5.3 Interpolation Methods of Function Generation

Interpolation schemes are often used in vector scan C.R.T. systems where graphics are generated by drawing a series of straight lines on a long persistence C.R.T. Interpolation can also be used to generate any waveform by approximating the wave as a series of chords. The maximum fidelity and frequency of the output signal is determined by the number of chords used.

A simple interpolation scheme is shown in Figure 6.5.8. Two DACs are driven with triangular reference waveforms: the triangles are 180° out of phase. The DACs are alternately fed with the data word corresponding to the end value of the chord in question. In the example shown DAC P receives the first point Y1. Its triangle reference input ramps from zero to its maximum value at which point the output voltage corresponds to Y1. Y2 is now loaded to DAC Q and its reference voltage ramps from zero to maximum while Y1 reference is ramps down to zero. At the end of this period, the output voltage will be equal to Y2, since V_{REF} P = 0. DAC P is now loaded with value Y3 and the ramps are reversed. This process continues as long as required. Note that the digital fraction to each DAC is updated when its V_{REF} = 0, and therefore output glitches are minimized. For an X-Y graphics display two such systems are required, one per axis. Reference 11 gives a much more complete discussion of interpolation schemes.

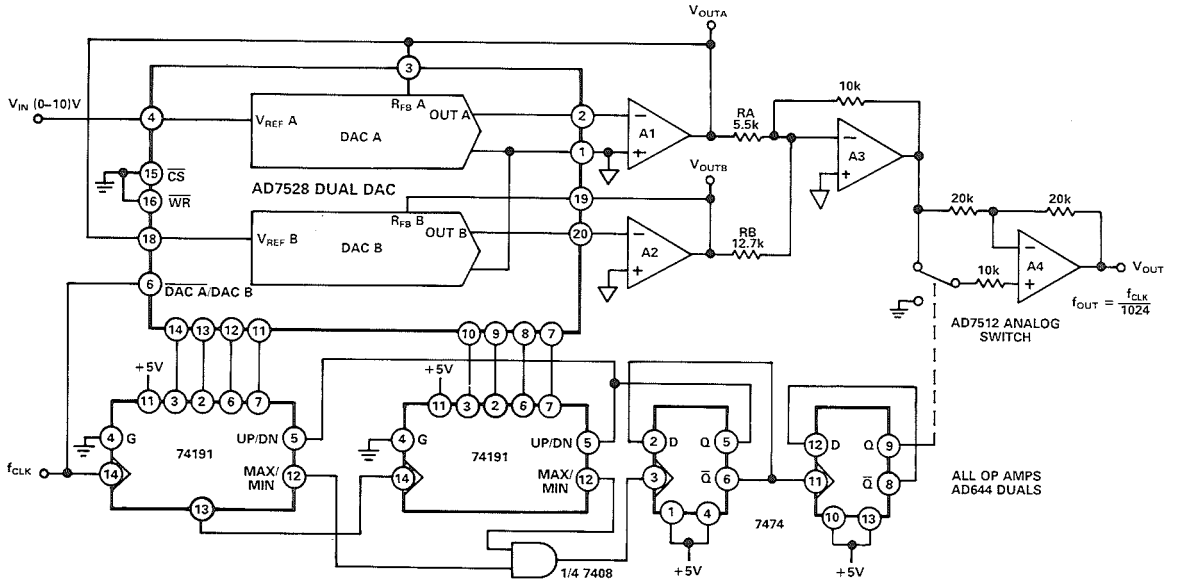


Figure 6.5.7 0-2.5kHz Low Frequency Sine Wave Generator Using Quadratic Approximation Method

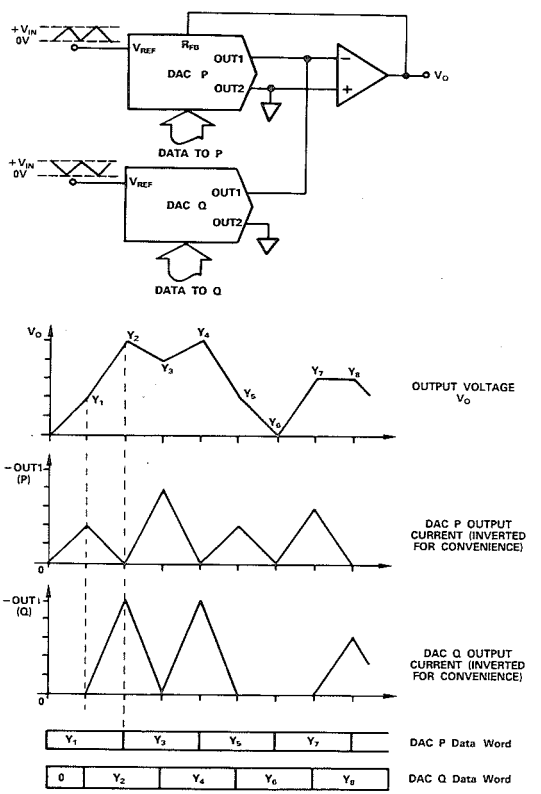


Figure 6.5.8 Simplified Interpolation Scheme for Function Generation

Figure 6.5.9 shows a simple stroke writing X-Y plotter drive for personal computers which demonstrates the interpolation system in use. The whole system operates from a single +5V supply. DAC 3 is used to generate the two triangle waveforms by operating it in the single supply current-steering mode with OUT1 and AGND biased at about +0.5V and with a nominal V_{REF} of 1.2V. Each triangle has exactly the same maximum and minimum values: R1 is used to compensate for amplifier offset mismatch and ensure that the maximum values of the triangle are the same (about 500mV). Resistor R2, which sets the gain of one of the curent to voltage converters, is used to trim the two minimum values to be the same (about 100mV). The triangle is generated by the microcomputer which alternately counts up and down between OOH and FFH and loads each value to DAC 3 as it does so. The peak triangle value of approximately 500mV is determined by the maximum voltage that can be applied to DAC 1 and DAC 2 before linearity is degraded. The minimum value of 100mV is determined by the current sink capability of output amplifiers A3 and A4 which have to sink current from DAC 1 and DAC 2, and must do this without any loss of linearity due to amplifier output impedance. Resistors R7 and R8 provide additional current sinking capability at the outputs of amplifiers A3 and A4 to assist the amplifier outputs to go down to +100mV. The outputs of each dual DAC are summed and amplified by the output amplifiers A1 and A2. Trim

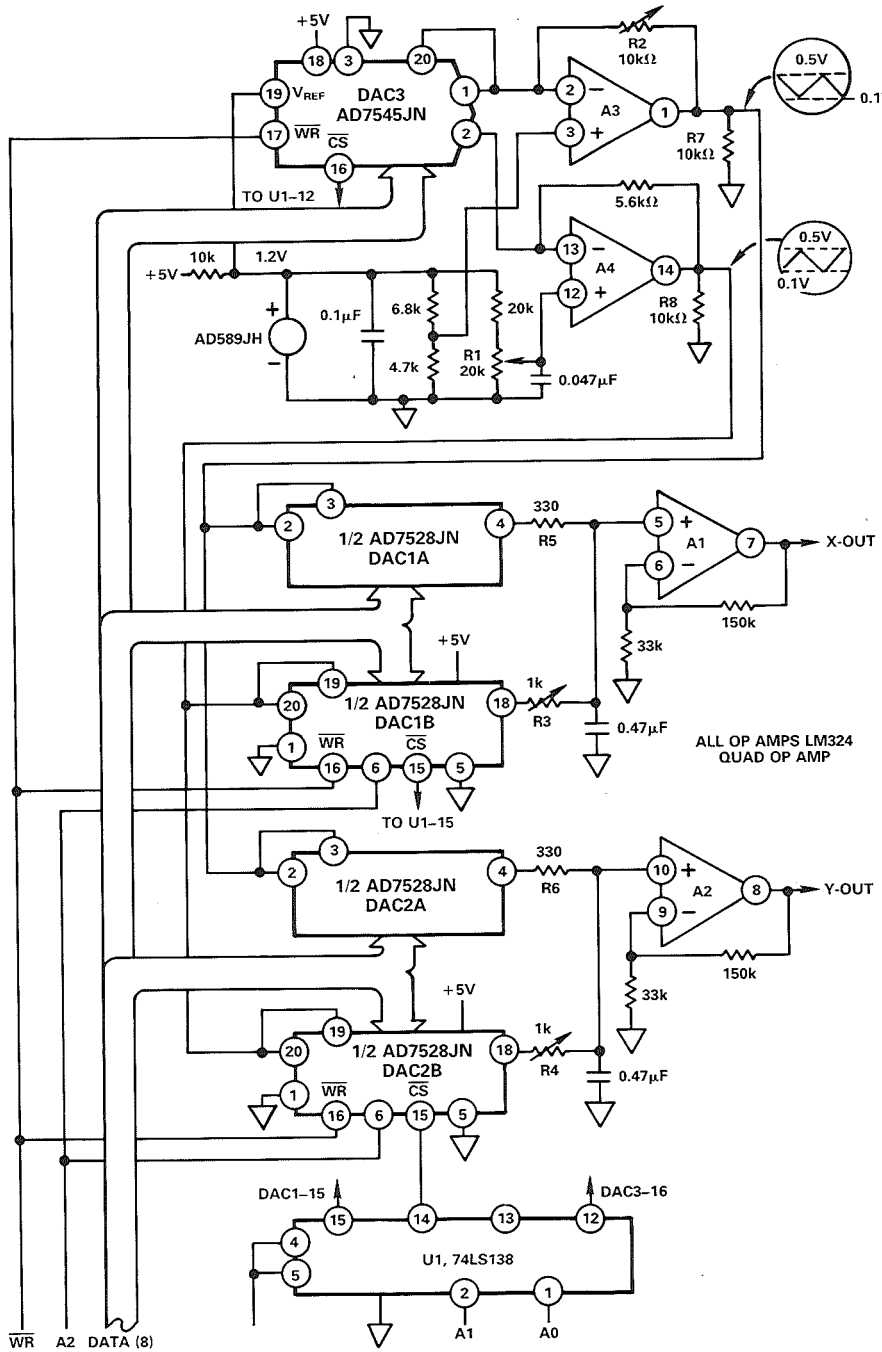


Figure 6.5.9 X-Y Plotter Interface Using +5V Supplies Only

resistors R3 and R4 can be used to match the output impedances of the DAC pairs. While the circuit in schematic form may look formidable, it in fact only uses five DIP packed I.C.'s and a bandgap reference type AD589JH. Note that the AD7545 is a 12-bit wide DAC but, in this application, the four LSBs are strapped low. Where possible, the +5V used by the circuit should be generated separately to reduce noise. Furthermore, the data, address and WR signals from the microprocessor should be gated as suggested in section 5.3.1 so that they only become active when the circuit is addressed.

6.6 MEDIUM FREQUENCY FUNCTION GENERATORS AND OSCILLATORS

6.6.1 Triangle/Square Wave Generator[28]

Figure 6.6.1 shows a basic triangle/square wave generator. A ramp is generated by the digitally controlled integrator : when the upper comparator trip point is reached, the opposite polarity reference is applied which causes the integrator to ramp in the opposite direction until it reaches the lower trigger point. The frequency of oscillation is determined by the fraction applied to the DAC, R, C and the value of the two trigger points. R is made up of R5 plus the DAC resistance: consequently, the oscillator frequency will change with DAC resistance. The circuit of Figure 6.6.2 overcomes this limitation by driving a constant current into the DAC. Amplifiers A3 and A4 form a constant current source which can be positive or negative depending upon the output of window comparator A2. The high frequency performance of this circuit is limited by the slew rate and settling time of amplifiers A2, A3 and A4, and for this reason should be high performance FET amplifiers such as AD544.

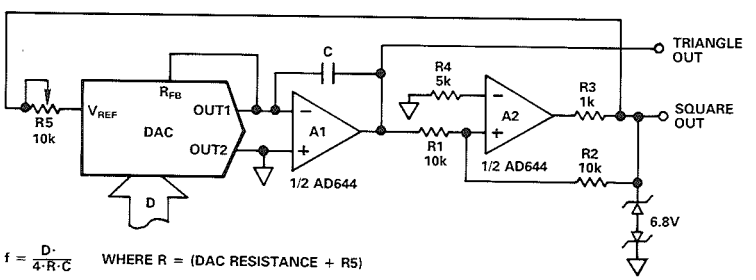


Figure 6.6.1 Programmable Triangle/Square Wave Generator

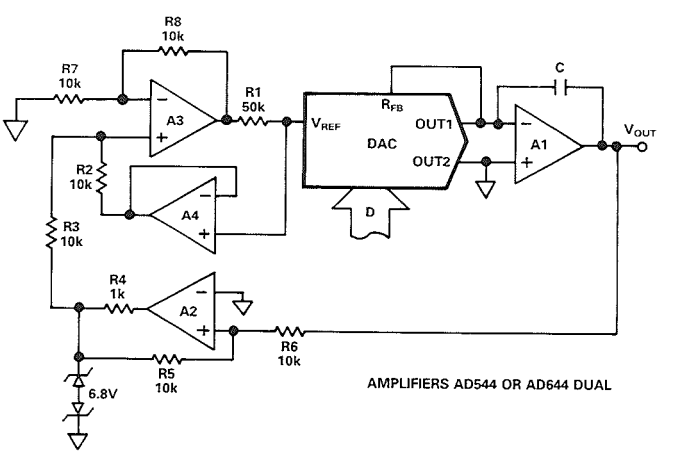


Figure 6.6.2 Improved Triangle Wave Generator

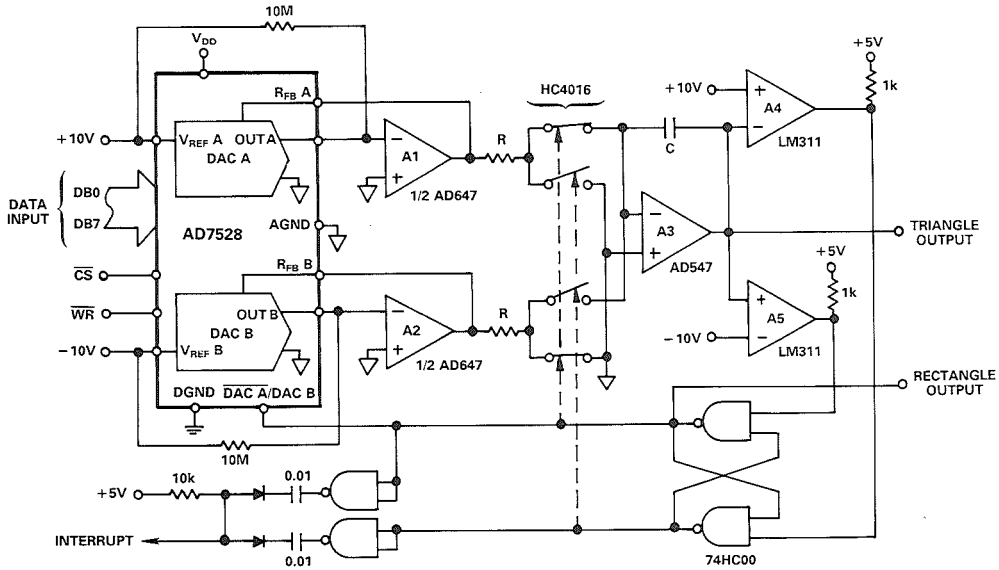


Figure 6.6.3 Triangle/Rectangle Generator with Individual Control of UP/DN Ramps and Mark/Space Ratio

6.6.2 Triangle/Rectangle Wave Generator with Programmable Waveform[10]

The circuit of Figure 6.6.3 overcomes the limitation imposed by amplifier slew rate as discussed above. It can be used to generate frequencies up to about 50kHz. Two DACs are used: DAC A controls the positive ramp and DAC B controls the negative ramp. DAC B is loaded while DAC A is driving the output positive, and vice versa. The flip-flop output automatically connects the "unused" DAC to the data bus for updating if necessary. The flip-flop provides a convenient interrupt to the processor at the start of each ramp. This type of triangle wave generator is useful in microprocessor controlled graphics systems. SW1 and SW2 are high speed CMOS switches such as HC4016. Spikes due to parasitic capacitance around the switches are minimized because the switched nodes are always at the same voltage (earth or virtual earth) and, therefore, a minimum amount of charging and discharging takes place. Each ramp period (i.e., half triangle) has a duration given by:

$$\text{Ramp period} = \frac{256RC}{D}$$

and ramps as short as 10μs (i.e., period frequency of 50kHz) can readily be generated by this method. The 10 megohm resistors provide 1/4LSB bias to each output so that in the event of all zeros being applied to either DAC, the circuit continues to oscillate.

6.6.3 State Variable Sine Wave Oscillators[10], [12]

A conventional state-variable sinusoidal oscillator is shown in Figure 6.6.4. The two integrators have been replaced by programmable integrators which may be conveniently constructed from an AD7528 dual 8-bit DAC. The frequency of oscillation is given by:

$$f = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\cdot\sqrt{\frac{1}{C1\cdot R1\cdot C2\cdot R2}}$$

where R1 and R2 are the effective resistances of DACs 1 & 2 respectively.

Since both DACs of the AD7528 are constructed on the same die, their resistance matches extremely well (typically 0.5%) and if C1 = C2 and R5 = R6, the frequency of oscillation is given by:

$$f = \frac{D}{2\pi\cdot R\cdot C}$$

where R is the resistance of the DAC. The circuit can be calibrated for a particular frequency/code ratio by adjusting R5. With the values shown, the output frequency varies from 0 to 15kHz in steps of approximately 60Hz/bit, with an amplitude of about 10V p-p. Total harmonic distortion measures −53dB at 1kHz and −43dB at 14kHz.

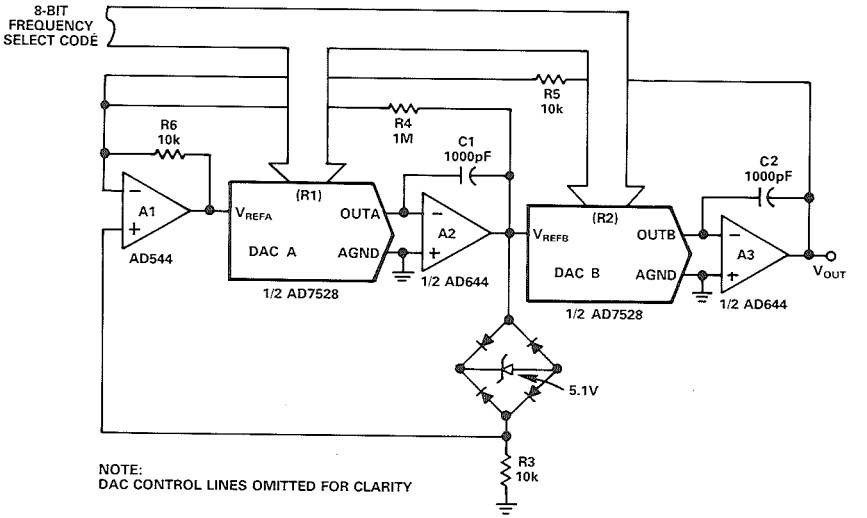


Figure 6.6.4 0-15kHz State-Variable Sine Oscillator

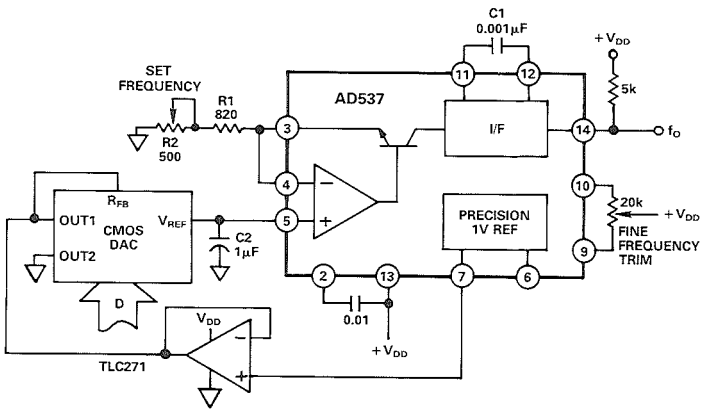


Figure 6.6.5 0-100kHz Programmable Oscillator for Single +5V to +15V Supplies

6.6.4 Digitally Programmable Oscillators and Frequency Modulators

D/A converters are often used to provide the control input to a voltage (or current) controlled oscillator. This technique is not limited to medium frequency applications and can be extended to quite high frequencies—for example, control of varactor diodes.

Figure 6.6.5 shows an AD537 Voltage/Frequency converter controlled by a CMOS DAC connected in the voltage-switching mode. This particular circuit is attractive because it operates from a single positive supply in the range +5V to +15V and exhibits excellent stability and independence from supply variations. The internal bandgap reference of the AD537, available on pin 7 of the device, is used to supply the 1 Volt reference to the DAC. The internal op amp of the AD537 is used to buffer the output of the CMOS DAC. Capacitor C2 in conjunction with the constant output resistance of the DAC forms a simple low pass filter which reduces the AD537 sensitivity to stray noise. The circuit, as shown, covers the range 0 to 100kHz: if C1 is changed to 0.01µF, the frequency range will be 0 to 10kHz. Any CMOS DAC can be used, but if a supply voltage other than +5V is applied and TTL compatible inputs are required then the user should select a DAC which has internal TTL to CMOS level shifters—see Appendix 1. Suitable DACs are AD7524 and AD7545 for +5V only operation and AD7240 or AD7548 for +10V to +15V operation.

The popular 555 timer/oscillator can also be controlled by a CMOS DAC. In its simplest form, the

DAC output voltage is applied to the control voltage pin of the 555. However, this gives a limited range of frequencies and Figure 6.6.6 shows one method of achieving wider control by using the DAC to program a constant current source for the capacitor charging circuit. The voltage-switching DAC supplies a voltage which determines the current in the constant current circuit. This current is mirrored by transistor pair Q1, Q2 to supply the charging current for the 555's timing capacitor. The accuracy of this circuit is limited by the performance of the current mirror and the response time of the comparator in the 555 timer. To improve the linearity of the relationship between digital fraction and oscillator frequency, the circuit of Figure 6.6.7 is recommended. A resistor is inserted between pins 6 and 7 of the 555 timer to increase the capacitor discharge time. Consequently, the comparator response time becomes

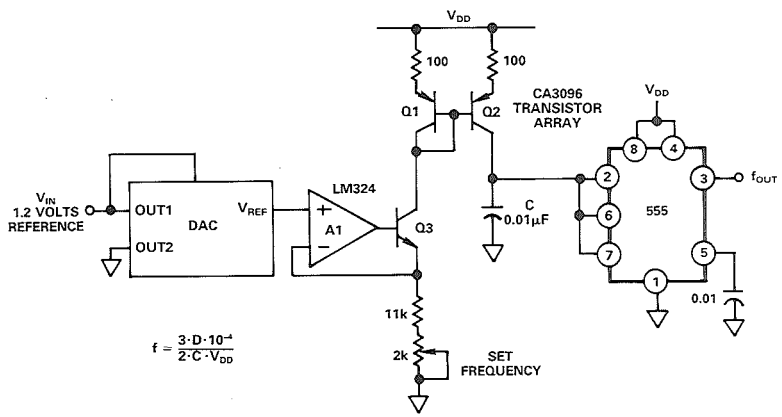


Figure 6.6.6 Single Programmable Osciilator Using 555 Timer

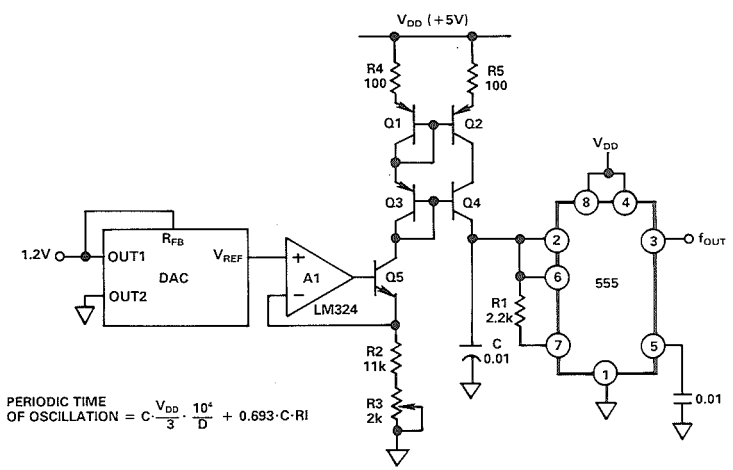


Figure 6.6.7 Programmable Oscillator with Improved Linearity

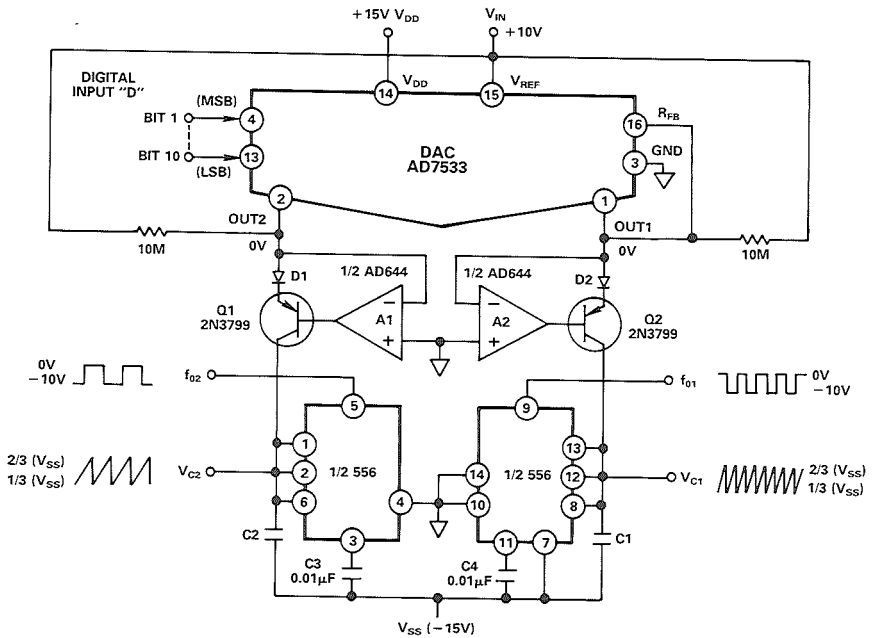


Figure 6.6.8 Programmable Oscillator with Complementary Output Frequencies

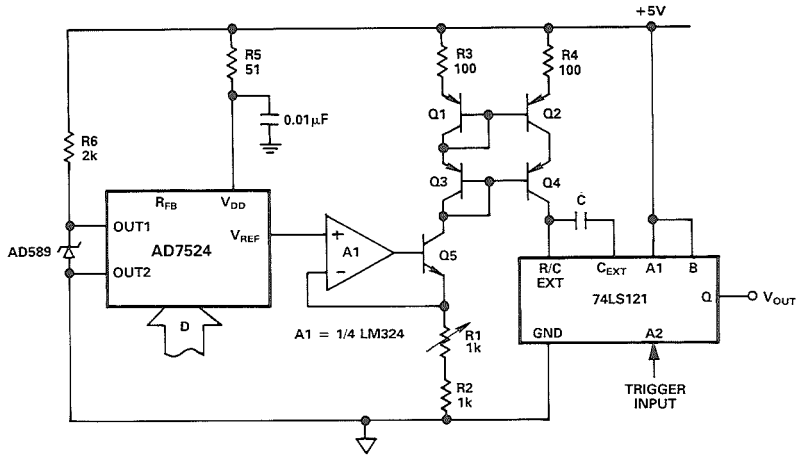
insignificant in the overall transfer function. The resistor does, however, introduce an additional term into the transfer equation of the circuit. The circuit shown covers the range from 20Hz to 5kHz with an accuracy of ± 10Hz.

Figure 6.6.8 shows a novel method of driving a dual 556 timer from one DAC[13]. OUT1 and OUT2 are driven into current mirror circuits consisting of A2, Q2 and A1, Q1. These current mirrors provide the capacitor charging current for the 556 timers which are operated with VCC at ground and their ground at $-V_{SS}$ (−15V). Since the sum of the currents from OUT1 and OUT2 is always a constant, the sum of the frequencies from the two oscillators must also be constant. Thus, as one frequency is increased, the other is decreased.

In all of the applications described above, the oscillator frequency is determined by the code to the DAC and the reference voltage. Frequency modulation from a digital data source is achieved by using the appropriate digital words. Frequency modulation from an analog source is done by adding the analog signal to the reference voltage. Where the DAC is operated in the voltage-switching mode, it is important to ensure that the composite input voltage of reference voltage plus modulation can never go negative, even under overload conditions. If there is any possibility of this happening, OUT1 should be connected to ground by a reverse biased Schottky diode (type HP-5082-2811) to prevent internal diodes from being turned on and damaging the DAC.

6.6.5 Programmable One-Shots and Pulse Generators[14]

The principles described above for controlling oscillators are equally applicable to pulse generators and one shots. In the circuit of Figure 6.6.9 a programmable current programs the pulse width of a 74121 type one shot. Full scale on the DAC produces the shortest pulse and small binary numbers give the longest available pulse. For a given capacitor the useful range of pulses is about 50:1 for an eight bit DAC. With small binary codes the pulse is long and any linearity error of the DAC represents a significant error in pulse width: therefore the circuit has poor accuracy in this region. Calibrate the circuit with the DAC at about half scale: this gives a pulse width long enough to be accurately measured and a binary code large enough to make any DAC linearity error relatively insignificant. For greater accuracy or a wider range of pulse widths use a higher resolution DAC (e.g. AD7545 12 bit DAC).



CμF	APPROX. RANGE OF PULSE WIDTHS
0.001	3μs TO 1ms
0.01	30μs TO 10ms
0.1	300μs TO 100ms

Q1, Q2 and Q3, Q4 CAN BE ANY SMALL DUAL PNP TRANSISTORS OR PART OF TRANSISTOR ARRAY, e.g., CA3096.

Q5 CAN BE ANY SMALL SIGNAL NPN DEVICE, e.g., PART OF CA3096.

Figure 6.6.9 One-Shot with Programmable Pulse Width

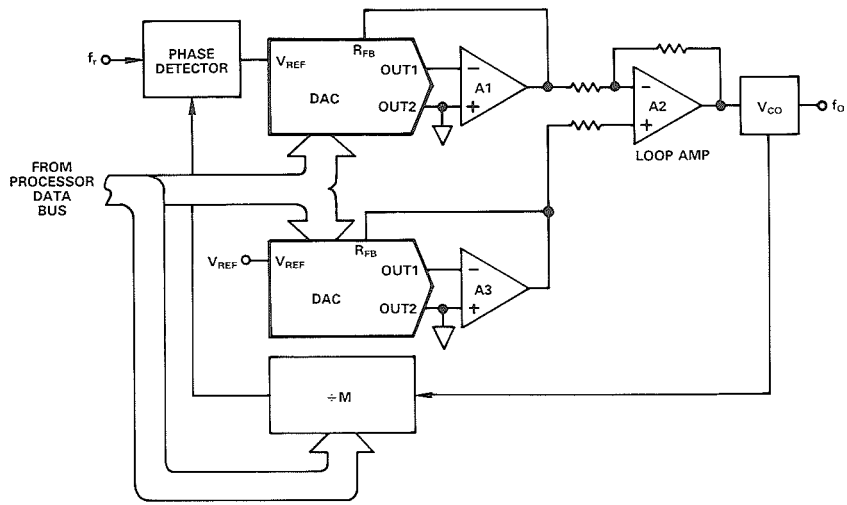


Figure 6.6.10 Phase-Lock Loop Stabilization Using Dual DAC

6.6.6 Phased Locked Loop Stabilization[15]

Phase locked loops allow a high frequency waveform to be synthesized and locked to a lower frequency oscillator. A reference frequency fr is applied to a phase sensitive detector, amplifier and voltage controlled oscillator. The output frequency is a multiple M of fr (i.e., f_o = M·fr) and this is divided by a digital counter for feedback to the phase sensitive detector as shown in Figure 6.6.10. For a given design, large changes in M, 2:1 or greater, during operation can cause severe problems in maintaining transient response, loop bandwith and overall stability. One solution is to compensate for these changes by using a multiplying DAC as a programmable gain (attenuator) element. When M is changed, under computer control, the loop gain is also modified by changing the digital word in the DAC. Since a phase-locked loop is an ac coupled system, it is necessary to cancel out the dc gain of the CMOS DAC attenuator circuit by a second DAC which subtracts the dc offset. Both

DACs should match and track one another so as to reduce any dc error drift—an AD7528 dual DAC is ideal for this task. Figure 6.6.10 shows a block diagram of a phase locked loop system using the dual DAC method of loop gain compensation. This scheme has several advantages over others which generally rely on transconductance amplifiers. Such amplifiers use current mirrors requiring precision resistors and many offset adjustments which cause major delays and expense on the production line. The DAC approach eliminates these problems by inherently possessing the needed accuracy. For more information on this method, the reader is referred to Reference 15.

6.7. DIGITALLY CONTROLLED FILTERS

6.7.1 Simple Low Pass Filters[24]

Multiplying D/A converters can be used to construct active filters with complete control of gain, centre frequency and Q-Factor. The advantage of multiplying DAC filters over other types is that they have very low noise and distortion. The resolution of the filter characteristics is determined by the resolution of the D/A converters.

Figures 6.7.1, 6.7.2 and 6.7.3 show three different methods of realizing simple first order low-pass filters. These illustrate the principle considerations for active filter design with multiplying DACs. Figure 6.7.1 shows the simplest form of a low-pass filter. The cut-off radial frequency is given by:

$$\omega = \frac{R1}{(R1 + R2)} \cdot \frac{D}{(C \cdot RDAC)}$$

Where D is the fractional binary number applied to the DAC.

Note that ω is determined by the value of RDAC which varies from device to device. This problem is avoided in the circuit of Figure 6.7.2 by using the DAC as a programmable gain element. It will be seen that the cut-off frequency is independent of RDAC. If it is required to have a proportional adjustment of a filter time constant rather than its cut-off frequency, the circuit of Figure 6.7.2 can be re-arranged with the DAC connected in the divider configuration as shown in Figure 6.7.3. The time constant of the circuit is given by:

$$\tau = \frac{R2 \cdot R4 \cdot D \cdot C}{R3}$$

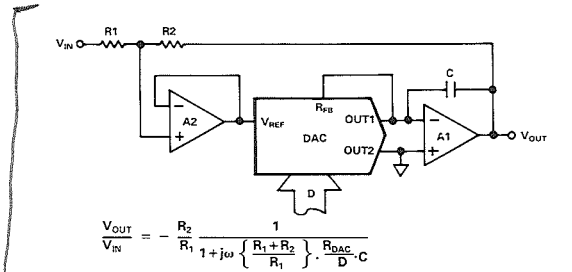


Figure 6.7.1 Simple Low Pass Filter

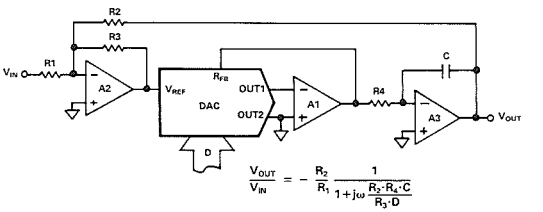


Figure 6.7.2 Low Pass Filter Independent of Value of DAC Resistance R_{DAC}

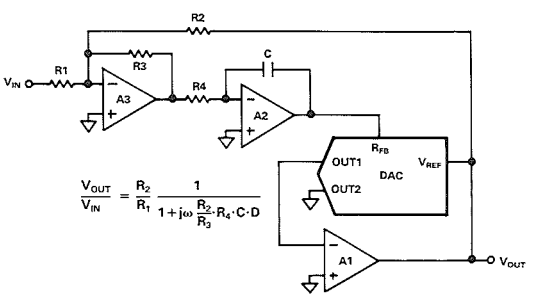


Figure 6.7.3 Low Pass Filter with Digitally Programmable Time Constant

Note that the divider follows the integrator in order to permit the divider to have high gain (at short time constants) without causing the circuit to limit.

6.7.2 State Variable Filters[16]

Most programmable filter circuits using multiplying DACs are based on the state variable technique. They can give high-pass, low-pass and band-pass from the same circuit. A complete analysis of state-variable filter design is beyond the scope of this text, but the following text will serve as an introduction.

Figure 6.7.4 shows one form of a second-order state-variable filter which is particularly suitable for use

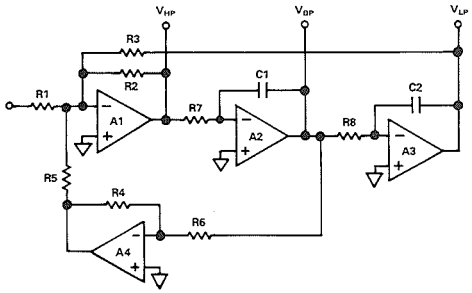


Figure 6.7.4 Second Order State Variable Filter with High Pass, Low Pass and Band Pass Outputs

with multiplying DACs because each amplifier operates with its summing node at virtual earth. Therefore, any one of the resistors could, if required, be replaced by a multiplying DAC operated in the current-switching mode. The transfer functions to the three outputs are as follows:

$$\text{High Pass } V_{HP} = \left\{ \frac{-\frac{R2}{R1} \cdot S^2}{S^2 + \frac{R4}{R6} \cdot \frac{R2}{R5} \omega_1 \cdot S + \frac{R2}{R3} \cdot \omega_1 \cdot \omega_2} \right\}$$

$$\text{Low Pass } V_{LP} = \left\{ \frac{-\frac{R2}{R1} \cdot \omega_1 \cdot \omega_2}{S^2 + \frac{R4}{R6} \cdot \frac{R2}{R5} \cdot \omega_1 \cdot S + \frac{R2}{R3} \cdot \omega_1 \cdot \omega_2} \right\}$$

$$\text{Band Pass } V_{BP} = \left\{ \frac{\omega_1 \cdot \frac{R2}{R1} \cdot S}{S^2 + \frac{R4}{R6} \cdot \frac{R2}{R5} \cdot \omega_1 \cdot S + \frac{R2}{R3} \cdot \omega_1 \cdot \omega_2} \right\}$$

where $\omega_1 = \frac{1}{C1 \cdot R7}$, $\omega_2 = \frac{1}{C2 \cdot R8}$

and S is the Laplace Operator

The high-pass and low-pass outputs can be considered simultaneously. If R2 = R3 = R5 and R4 = 2R6 and $\omega_1 = \omega_2 = \omega_0$ then the two equations become:

$$V_{HP} = \frac{-\frac{R2}{R1} \cdot S^2}{(S + \omega_0)^2}$$

$$V_{LP} = \frac{-\frac{R2}{R1} \cdot \omega_0^2}{(S + \omega_0)^2}$$

The pass-band gain is set by the ratio R2/R1 and the cut off frequency is determined by (R7·C1) = (R8·C2). Figure 6.7.5 shows a practical realization of this circuit using multiplying DACs. C1 is made equal to C2 and the AD7528 dual 8-bit DAC is used for DAC 1 and DAC 2 which control ω_1 and ω_2 respectively. If the fractional binary value D is applied to both DAC 1 and DAC 2, the transfer function for the two outputs is:

$$V_{HP} = \frac{-R2}{R1} \cdot \frac{S^2}{(S + \omega_0 \cdot D)^2}$$

$$V_{LP} = \frac{-R2}{R1} \cdot \frac{D^2 \cdot \omega_0^2}{(S + \omega_0 \cdot D)^2}$$

Note that the pass-band gain for both outputs is independent of the value of D, and that the cut-off frequency is directly proportional to D. The gain of the filter can be made variable by replacing R1 with another multiplying DAC, in which case the pass-band gain becomes (−D·R2)/RDAC where D is the fractional binary value applied to the DAC replacing R1. Figure 6.7.6 gives the measured frequency response for the high and low-pass outputs of the circuit of Figure 6.7.5.

If R2 = R3 = R5, the band-pass transfer function becomes:

$$V_{BP} = \left\{ \frac{\omega_1 \cdot \frac{R2}{R1} \cdot S}{S^2 + \frac{R4}{R6} \cdot \omega_1 \cdot S + \cdot \omega_1 \cdot \omega_2} \right\}$$

$$\omega_0 = \sqrt{\omega_1 \cdot \omega_2} = \omega_1, \omega_2 \text{ if } C1 \cdot R7 = C2 \cdot R8$$

$$\text{Q factor} = \frac{R6}{R4}$$

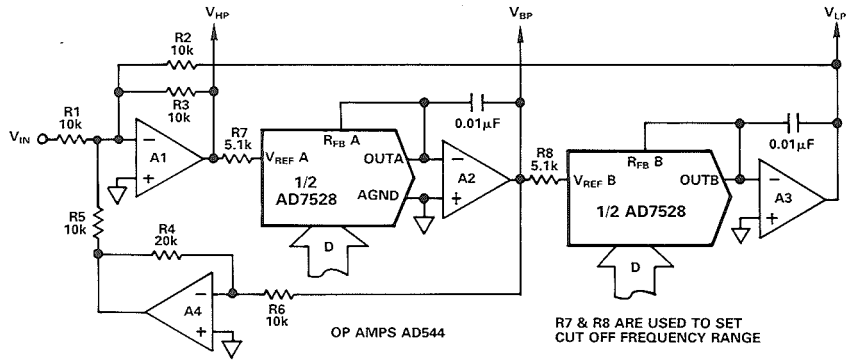


Figure 6.7.5 Practical State Variable Filter with Digital Control of Cut Off Frequencies

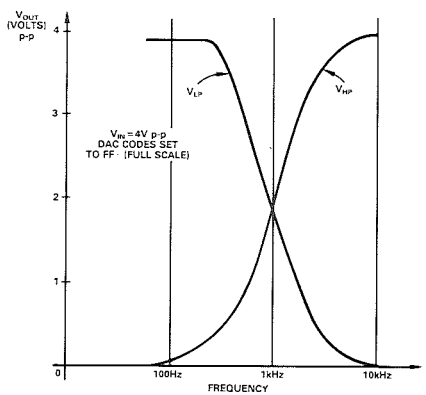


Figure 6.7.6 High and Low Pass Frequency Response for Figure 6.7.5 Circuit

Thus if R1, R6, R7 and R8 are replaced with multiplying DACs, it is possible to construct the state variable filter, shown in Figure 6.7.7 which has control of:

a) Pass band gain – vary D1
b) Q-factor – vary D6 (and D1 for constant gain)
c) Centre frequency – vary D7 and D8 simultaneously.

Changing the Q-factor, via D6 changes the pass-band gain. To hold the pass-band gain constant, DACs 1 and 6 should be changed in proportion to each other. Figure 6.7.8 shows the effect of changing only D6 for the circuit of Figure 6.7.7 with all other DACs set to full scale.

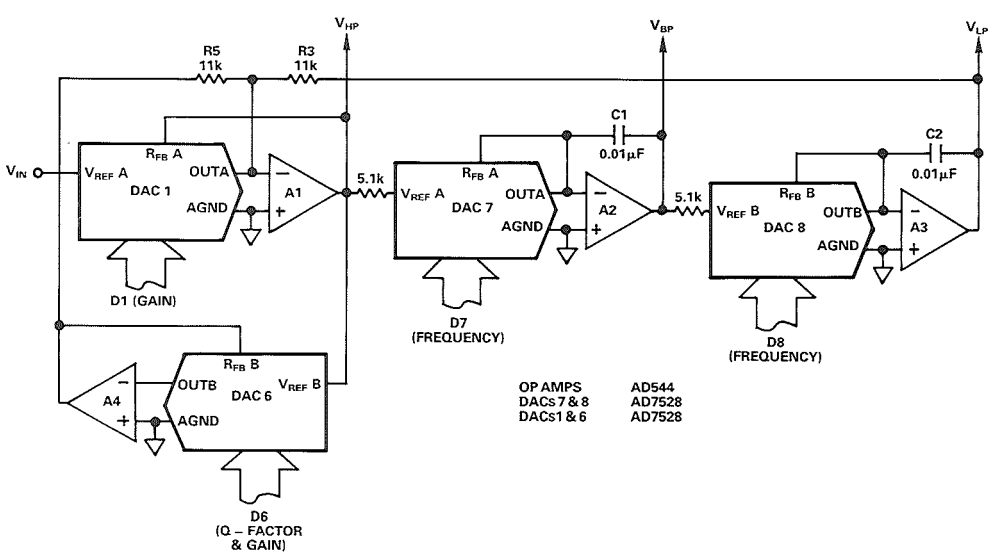


Figure 6.7.7 State Variable Filter with Digital Control of Gain, Frequency, Q-Factor

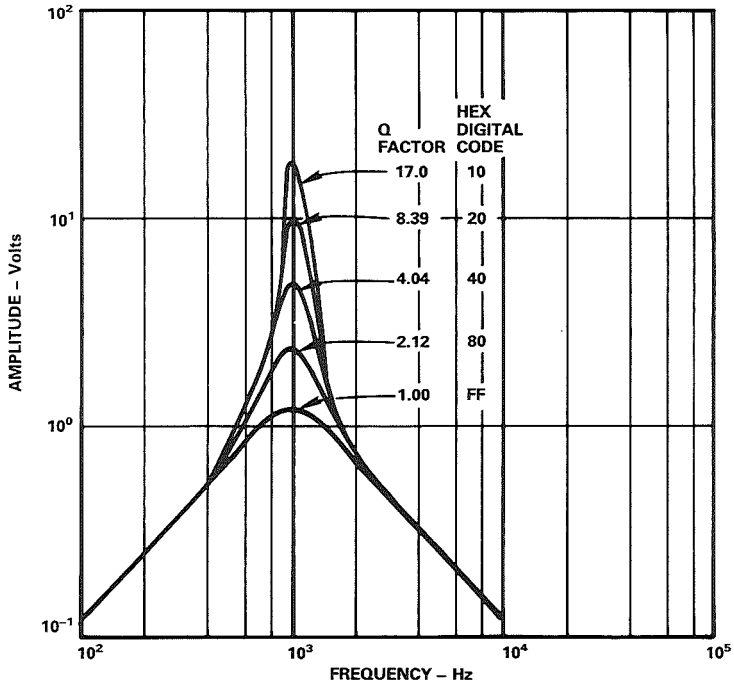


Figure 6.7.8 Effect of Changing D6 in Figure 6.7.7

6.8 AUDIO APPLICATIONS OF CMOS DACs

6.8.1 Audio Attenuators (Volume Control)

It was pointed out in Section 2.3.8 that CMOS DACs are particularly suited to audio applications because they create very little distortion or noise. They make excellent audio attenuators but conventional binary coded DACs deliver linear attenuation rather than the exponential relationship of the human ear. To overcome this, three CMOS DACs are now available which deliver a logarithmic relationship between digital fraction and output signal level. These "LOGDACs" are:

1) AD7111 0 to 88.5dB in 0.375dB steps
2) AD7118 0 to 88.5dB in 1.5 dB steps
3) AD7115 0 to 20dB in 0.1dB steps

Figure 6.8.1 shows the AD7111 connected as an audio attenuator and Figure 6.8.2 shows the AD7115 coupled with a second attenuator to provide precision attenuation accurate to ±0.05dB in the range 0 to 80dB. JFET input amplifiers such as AD542/544 are excellent low noise audio amplifiers in their own right and coupled with a LOGDAC make a formidable team.

6.8.2 Audio Balance and Panners[28]

Eight-bit binary coded DACs such as AD7528JN can give up to 30dB attenuation range to an accuracy of ± 1dB. This is insufficient for use as volume controls but is adequate for stereo balance applications as shown in Figure 6.8.3. The two channels are

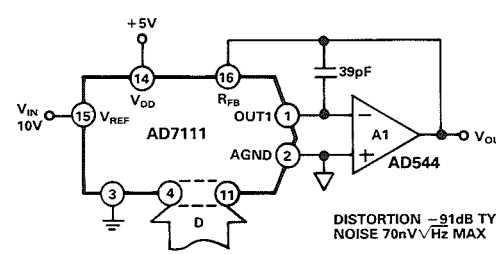
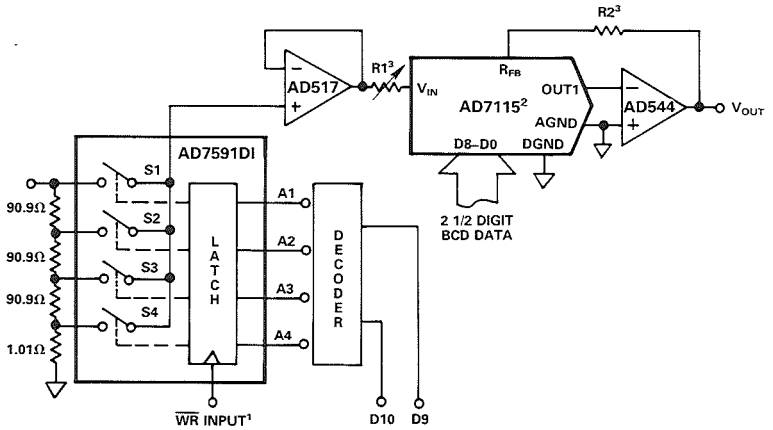


Figure 6.8.1 0.375dB Step Attenuator to −88.5dB



[1]THIS AD7591DI PIN SHOULD BE TIED LOW IF THE DATA LATCH FACILITY IS NOT REQUIRED.
[2]CONTROL INPUTS OMITTED FOR CLARITY.
[3]R1 AND R2 MAY BE OMITTED IF GAIN ERROR TRIM IS NOT REQUIRED.

Figure 6.8.2 0.1dB Step Attenuator to −80dB

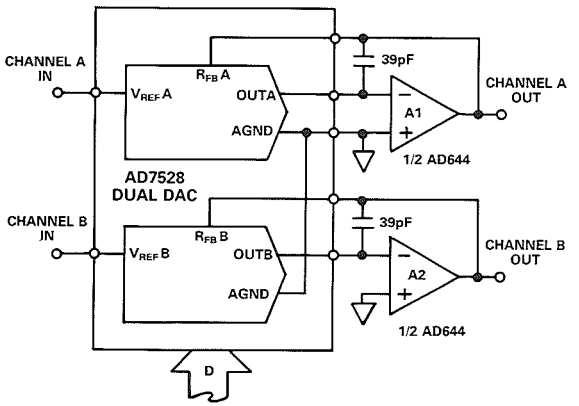


Figure 6.8.3 Dual 8-Bit DAC as Stereo Balance Control

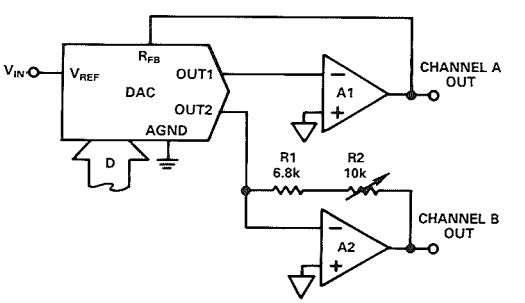


Figure 6.8.4 Digitally Programmed Audio Panner

applied to DACs A and B and the appropriate attenuation levels determined by the digital values loaded to each DAC. If OUTA and OUTB are fed into a single op amp, the circuit functions as a digitally controlled mixer.

Figure 6.8.4 illustrates a simple audio panner used to steer a single signal between two output channels. Since the currents at OUT1 and OUT2 are complementary, the proportion of the signal in each of the output channels is determined by the code applied to the DAC. This circuit works best when the ladder termination resistor is not tied to OUT2 (e.g., AD7533) so that both channels have a "mute" position.

6.9 MICROPROCESSOR INTERFACES

6.9.1 AD7545 to 8-Bit Data Bus Systems

The circuit of Figure 6.9.1 shows the general principles for connecting the AD7545 to an 8-bit data bus. The 74LS244 buffers the data bus; its outputs are enabled when the DAC address appears on the address bus. The first byte sent to the DAC is loaded to the 74LS373 octal latch and, when the second byte is sent to the DAC, it is combined with the first byte to create a 16-bit word. The DAC is connected to this 16-bit bus: the connections shown are for right-hand justified data. $\overline{CS}$ and $\overline{WR}$ inputs to the DAC are also gated, being active only when the DAC is loaded. Pull-up resistors at the output of the 74LS244 buffer

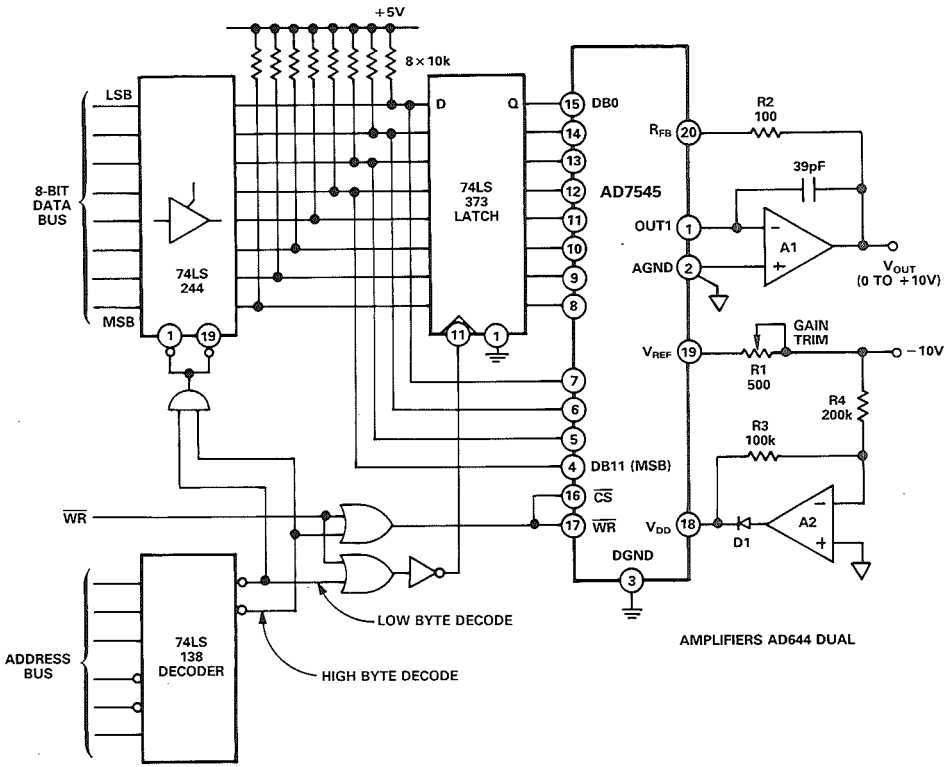


Figure 6.9.1 AD7545 to 8-Bit Data Bus Interface

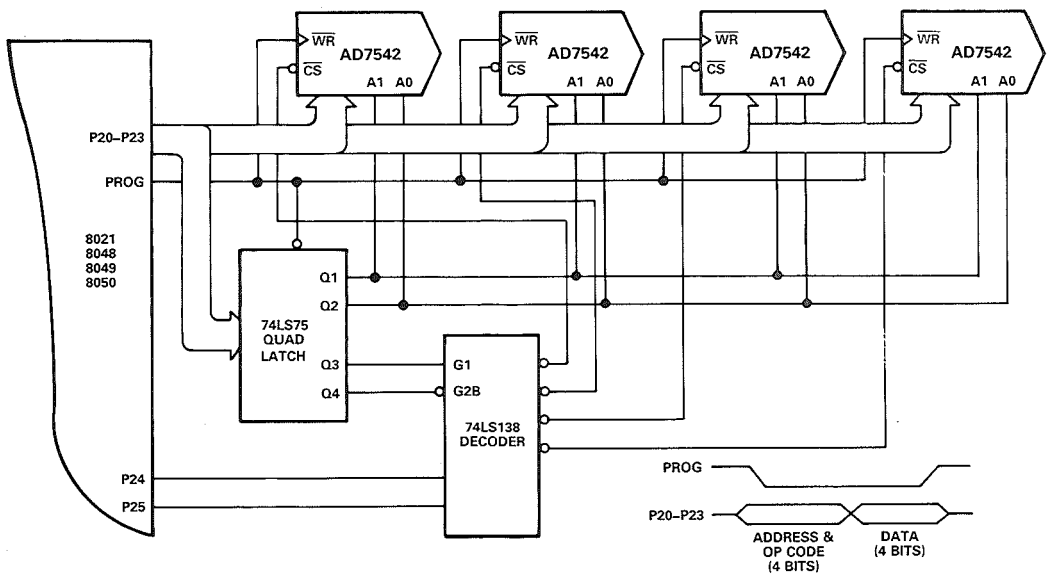


Figure 6.9.2 MCS48 Microcontroller to AD7542 Interface

ensure that the inputs to the DAC do not float at an ill defined level when the DAC is not being addressed. This method of connecting 12-bit DACs to an 8-bit data bus is most cost effective when more than two DACs exist on the same circuit board. In other applications, the AD7548 is preferred because it incorporates the octal latch on-chip. To reduce noise injection from the logic circuits, the +5V supply for the DAC is derived from the −10V reference via A2. Diode D1 prevents excessive current being drawn from the DAC in the event of A2 output going negative during power-up or for any other reason (e.g., power supply failure). For further information on reducing extraneous noise and general microprocessor interface techniques, the reader is referred to Chapter 5.

6.9.2 MCS48 Microcontroller to AD7542 Interface[29], [30]

The four-bit input data bus for the AD7542 makes it ideal for connecting to the four-bit expander port of the MCS48 family of microcontrollers as shown in Figure 6.9.2. P20 through P23 provide the four-bit data bus which carries both the DAC register address and the data as shown in the timing diagram. When PROG goes low, the register address and the op code are latched into the 7475 quad latch. The two least significant bits give the register address and the two most significant bits define the op code which is primarily intended for the 8243 expander. In this particular case, the AD7542 is only required to respond to the "WRITE" command. The "WRITE" op code is used to enable the 74LS138 decoder inputs G1 and G2B as shown. Data is latched into the AD7542 when PROG goes high: the particular DAC being selected with the address from bits P24 and P25, via the decoder.

The instruction set for the MCS48 family includes some special instructions which make it particularly easy and effective to communciate with the DACs via the four-bit expander port as shown. Although the MCS51 family of microcontrollers does not have the same four-bit expander port capability, it is a simple matter to emulate these facilities using an MCS51 device: The INTEL Microcontroller User's Handbook gives further details.

6.9.3 AD7542 to 8-Bit Data Bus Systems[23]

The AD7542 uses 4-bit "nibbles" to input data in conjunction with two address lines which determine whether the data is the low, middle or high 4- bits of the 12-bit word required for the DAC. Software difficulties arise when, as is usually the case, the data is stored as a conventional 16-bit value in two registers or consecutive memory bytes. If the four data inputs are connected to the four least significant bits of the data bus, then the lower and higher nibbles can be loaded to the DAC by a straightforward write instruction. But to load the middle nibble, the data must be shifted down four places before being written to the DAC. The circuit shown in Figure 6.9.3 eliminates the need for this shift by selecting the relevant four-bits of the 8-bit bus according to the sense of the address select lines. It allows the LOW byte of data to be loaded to the first two addresses with the lower and middle nibbles going to their respective registers. The addition of the 74LS157 data selector between the DAC and the data bus also serves to isolate the digital inputs to the DAC from the data bus except when the DAC is being addressed and thus reduces crosstalk between the bus and the analog output signal. The OR gates on the address and $\overline{WR}$ lines serve a similar function.

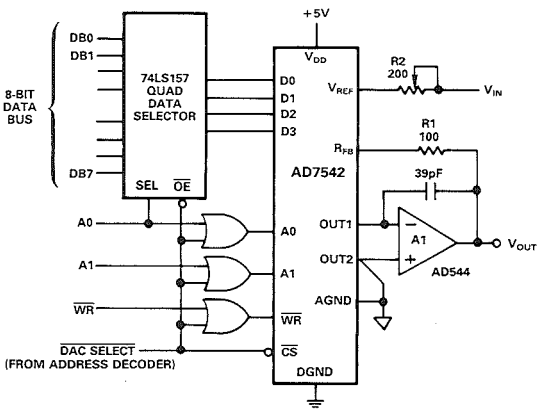


Figure 6.9.3 AD7542 to 8-Bit Data Bus Systems

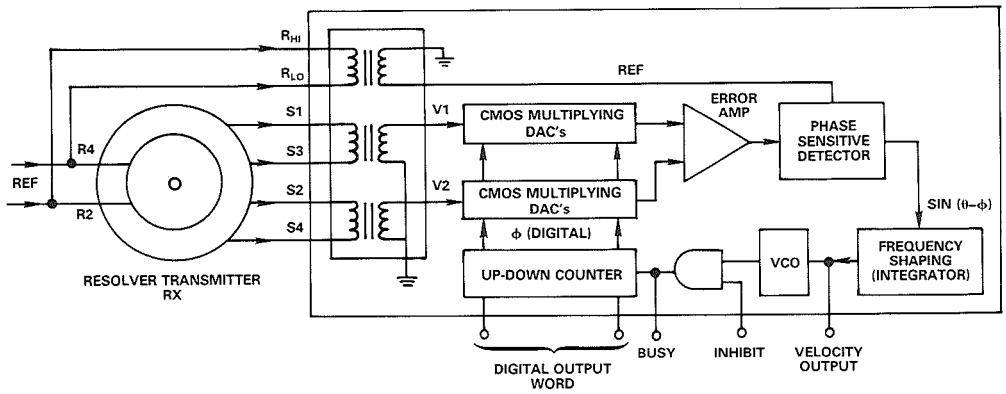


Figure 6.10.1 A Tracking Resolver-to-Digital Converter

6.10 MISCELLANEOUS SYSTEMS APPLICATIONS

6.10.1 Resolver-to-Digital Converter[18]

Resolvers and synchros indicate angular position. A rotor is excited with a reference voltage V sin ωt (usually 60 or 400Hz) and the stator has two windings at 90° to each other, so that the output of one stator winding is V sin ωt·sin θ and the other V sin ωt·cos θ. These two outputs are applied to the V_{REF} inputs of CMOS D/A converters whose digital input words are proportional to the sine and cosine of some angle θ as shown in Figure 6.10.1.

The output of the cosine multiplier is given by

$$V \sin \omega t \cdot \sin \theta \cos \phi$$

and the output of the sine multiplier is given by

$$V \sin \omega \cdot \cos \theta \sin \phi$$

These signals are subtracted by the error amplifier to give the error signal which is:

$$V \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$
$$= V \sin \omega t (\sin \theta - \phi)$$

This error signal is demodulated by the phase sensitive detector which utilizes the system reference voltage and a dc error signal proportional to sin (θ − ϕ) is produced. The dc error signal is fed back via an integrator and V.C.O. to drive the up-down counter until the error signal is nulled. The contents of the up-down counter give a binary representation of the angular position. In this application, it is the ability of the CMOS DAC to multiply an analog value by a digital word that makes the system feasible. For more information on resolver (and synchro) to digital conversion, the reader is referred to reference 18 from which this section is extracted.

6.10.2 Co-Ordinate Conversion

The circuit described here (taken from Reference 19) takes analog co-ordinates in the X-Y cartesian system and adds an angle of rotation to produce new co-ordinates. The basic principles of co-ordinate conversion as described here are used in some resolver to digital converters. A servo loop, such as that described above, is used to determine that angle of rotation which causes the inputs to match a set of reference co-ordinates. As shown in the schematic (Figure 6.10.2), the analog voltage pair (x_{in}, y_{in}) represents the vector r $\angle\theta$ where $r^2 = x^2 + y^2$ and tangent θ = y/x. The two inputs x_{in}, y_{in}—together with $-x_{in}$, $-y_{in}$ obtained from inverting amplifiers A1 and A2—are applied to the CD4052 dual analog multiplexer, which is controlled by the two most significant bits of the binary-coded rotation angle Φ. Each dual multiplexer output signal passes through a unity-gain amplifier, A3 or A4, and then through a tandem of inverting amplifiers (A5, A7, or A6, A8) to the final output.

Each tandem of inverting amplifiers is coupled with an AD7533 multiplying digital to analog converter to make a four-quadrant multiplier: A5 and A7 are coupled with DAC 1 and A6 and A8 are coupled with DAC 2. The digital input to both converters is provided by the remaining bits of Φ. The analog input to DAC 1 is the average of the signals from A4 and A8, and the analog input to DAC 2 is the average of the signals from A3 and A7. The output currents from the cross-fed D/A converters feed the summing junctions of A5 through A8, where they add to the inputs that have been selected by the multiplexer, thus producing the output voltages x_{out}, y_{out}.

All resistances in the circuit are 30 kilohms so it is convenient to use dual in-line packages, like

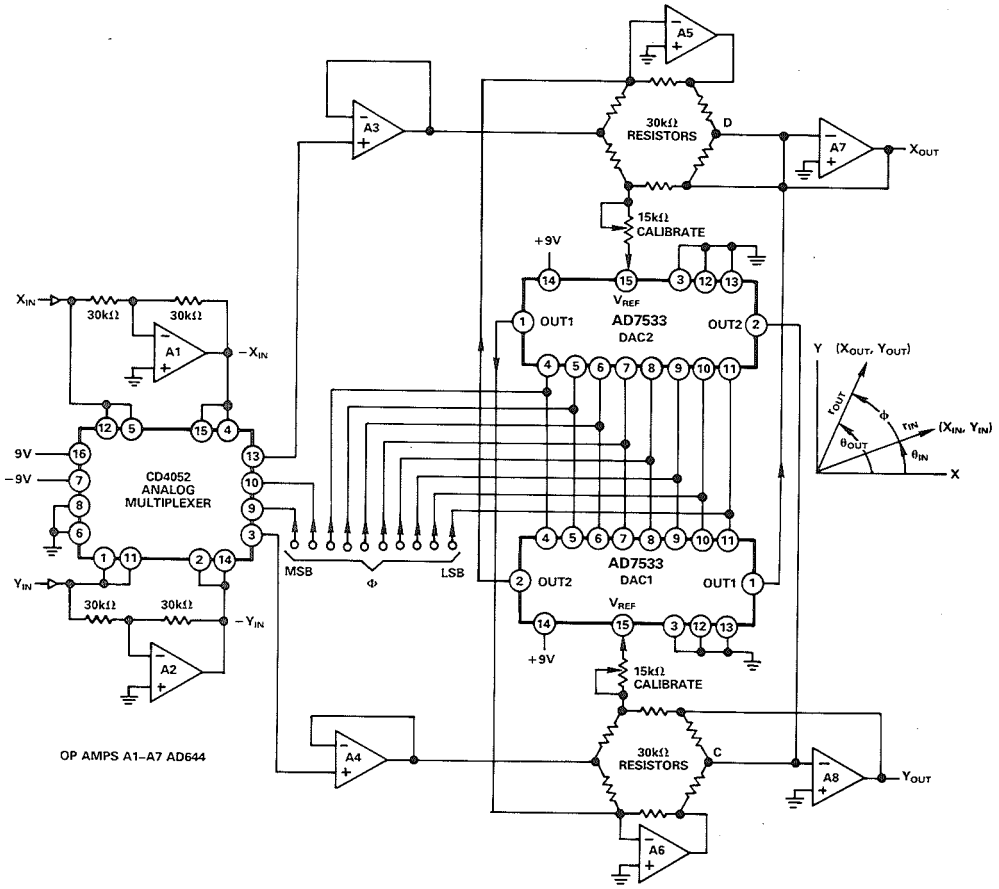


Figure 6.10.2 Co-Ordinate Rotator

Beckman's 698-3, with eight resistors per DIP. Another DIP, Bourn's 7102, could replace the two 15-k trimmers needed to raise the effective input impedance of each AD7533 to $15(2)^{1/2}$ kilohms, the value required in this design.

Regardless of the value of Φ

$$x^2_{out} + y^2_{out} = x^2_{in} = y^2_{in}.$$

In other words, the output vector's magnitude is always equal to that of the input vector. However, the relationship between the input and output vectors is given by $\theta_{out} = \theta_{in} + \Phi'$, where tan $(\Phi'/2)$ is equal to $(2^{1/2} - 1)$. $(\Phi - 45°)/45°$ and Φ is between 0° and 90°. The difference between Φ and Φ– 45° vanishes for Φ = 0°, 45° and 90° and is always less than 1° for other values of Φ in the first quadrant. Note that the error and its variation with angle recur in the other three quadrants. The 45° offset in Φ is due to the bipolar operation of the AD7533 converter. The offset may be corrected by simply adding 45° to the digital equivalent number at the Φ input lines. The remaining error will be small enough to go unnoticed on most graphical displays. To calibrate the vector rotator, x_{in} is set to some constant voltage and set $y_{in} = 0$. Then the trimmers are adjusted to make $x_{out} + y_{out} = 0$ when $\Phi = 0°$ and $x_{out} - y_{out} = 0$ when $\Phi = 90°$.

With the addition of a clock and a counter to make $\Phi = \omega t$, the vector rotator becomes a sine-cosine generator. For example, for a 5-volt-root-mean-square output, x_{in} and y_{in} is set to 5V dc; then $x_{out} = 5(2)^{1/2} \cos \omega t$ and $y_{out} = 5(2)^{1/2} \sin \omega t$.

Because of the functional error in the angle as given by the formula for tan $(\Phi'/2)$, either output will contain third and fifth harmonics each having a magnitude 0.8% that of the fundamental. Total harmonic distortion, therefore, is 1.1%.

This circuit has been used in the design of a low cost electronic compass—see Reference 20.

6.10.3 Using CMOS DACs in an AGC System[22]

In an automatic gain control system, an input signal is attenuated (or amplified) so that its average output level remains constant (Figure 6.10.3). The D/A converter is used here as a variable gain (attenuation) element that adjusts the output signal relative to the input level.

A feedback loop consisting of a detector, comparator, and up-down counter continuously adjusts the contents of the counter, and hence the gain, so that the signal level at the output of the detector remains constant and equal to V_{REF}. The negative feedback action of the loop ensures that the average output voltage of the automatic gain-control system remains constant.

Whenever the input signal level is outside the dynamic range of the programmable gain (attenuation) element of the gain-control system, there should be a stable, well-defined input/output relationship. However, if a simple up-down counter is used, an out-of-range signal causes it to count up continuously—once the counter reaches full scale (all 1's) it increments to the next value (all 0's), which is the zero end of the scale, and this produces a saw-tooth amplitude-modulated output that is determined by the count rate of the automatic gain-control system. To prevent this, the up-down counter should have end-stop logic.

The component values for the circuit depend on the bandwidth of the input signal and the response time of the automatic gain-control loop. The values shown apply for signals in the frequency range of 100Hz to 10kHz. Resistor R2 determines the I/O relationship when overranging occurs (all 0's in the counter), and R3 D2 and R4 D3 limit the outputs of comparators A3 and A4 to positive signals only.

Amplifier A2 and its associated components form the detector, R5 limits the maximum current available from A2 to charge C2, R6 and C2 provide an output voltage droop that is less than the required regulation accuracy of the system, and D1 is the detector diode. The AD584 voltage reference—in conjunction with R7, R8 and R9—determines the upper and lower limits of the output signal level when the automatic gain control is regulated.

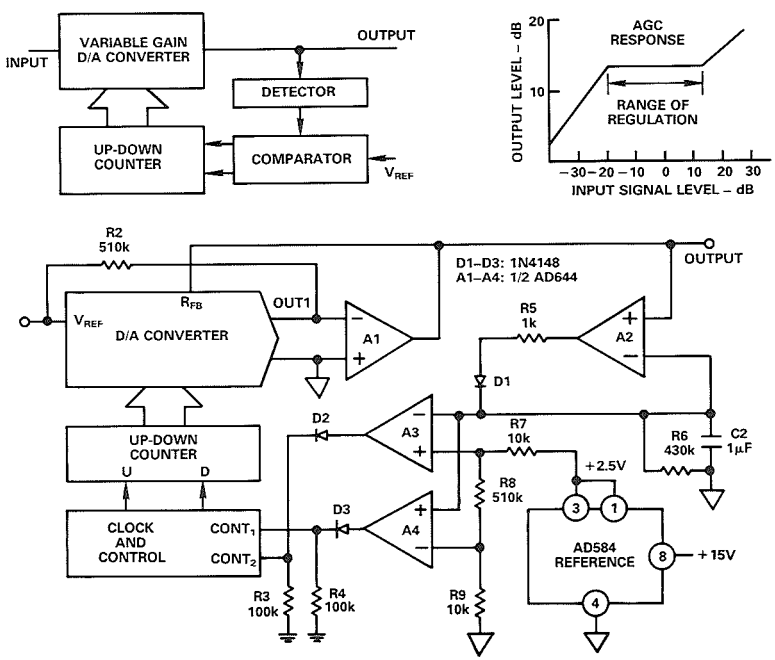


Figure 6.10.3 AGC System

APPENDIX KEY FEATURES AND CONNECTIONS FOR ANALOG DEVICES CMOS DACs

	No. of Pins	DGND	Logic P-Well	DAC Switch P-Well	AGND	OUT2	OUT1
LOGDACs(TM)[2]							
AD7111 (0.375dB Steps)	16	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
AD7115 (0.1dB Steps)	18	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
AD7118 (1.5dB Steps)	14	Pin 8 (DGND)	Pin 8 (DGND)	Pin 1 (AGND)	Pin 1 (AGND)	Pin 1 (AGND)	Pin 14
8-BIT DAC[2]							
AD7524	16	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 2	Pin 1
AD7528 Dual 8-Bit DAC	20	Pin 5 (DGND)	Pin 5 (DGND)	Pin 1 (AGND)	Pin 1 (AGND)	Pin 1 (AGND)	Pins 2 & 20
AD7226 Quad 8-Bit DAC	20	Note 4	Note 4	Note 4	Note 4	Note 4	Note 4
10-BIT DACs[2]							
AD7522	28	Pin 28 (DGND)	Pin 28 (DGND)	Pin 8 (AGND)	Pin 8 (AGND)	Pin 7	Pin 5
AD7533	16	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 2	Pin 1
12-BIT DACs[2]							
AD7240	18	Pin 3 (DGND)	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
AD7541A	18	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 3 (GND)	Pin 2	Pin 1
AD7542	16	Pin 12 (DGND)	Pin 12 (DGND)	Pin 3 (AGND)	Pin 3 (AGND)	Pin 2	Pin 1
AD7543	16	Pin 12 (DGND)	Pin 12 (DGND)	Pin 3 (AGND)	Pin 3 (AGND)	Pin 2	Pin 1
AD7545	20	Pin 3 (DGND)	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
AD7548	20	Pin 3 (DGND)	Pin 3 (DGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 2 (AGND)	Pin 1
16-BIT DACs							
AD7546	40	Note 5	Note 5	Note 5	Note 5	Note 5	Note 5

NOTES
[1]Operating a DAC at a voltage other than that for which it is specified may impair its performance – consult factory.
[2]All DACs are specfied in the current steering mode of operation except where stated otherwise.
[3]AD7522 and AD7524 purchased after 1982 do not require protection Schottky diodes.
[4]Not a conventional CMOS multiplying DAC – consult data sheet.
[5]Not a conventional CMOS multiplying DAC – see Section 6.2.4.

This Appendix is not a product specification and is for design guidance only. Consult product data sheet for full information.

Ladder Termination Connections	RDAC Min/Max kΩ	Protection Schottky Required	Specified Operating Voltage(s)	Operating Voltage Range[1]	Operating Voltage Range for TTL Compatibility	Description of Logic Structure and Other Comments
AGND (Pin 2)	9/15	No	+5	+5	+5	8-Bit Latched Data
AGND (Pin 2)	7/18	No	+5	+5	+5	2 1/2 Digit Latched BCD
AGND (Pin 1)	9/17	No	+5 & +15	+5 to +15	+5	6-Bit, No Latches
GND (Pin 3)	5/20	Note 3	+5 & +15	+5 to +15	+5	8-Bit, with Data Latches Can Be Made Transparent
AGND (Pin 1)	8/15	No	+5 & +15	+5 to +15	+5	Data Latches for Each DAC
Note 4	Note 4	Note 4	+15	11.4 to 16.5	11.4 to +16.5	Includes Output Amplifiers and Data Latches
Pin 2	5/20	Note 3	V_{DD} = +15 V_{CC} = +5	+12 to +15	+12 to +15 V_{CC} = +5	Double Buffered
GND (Pin 3)	5/20	No	+15	+7 to +15	+7 to +15	No Latches
						Specified in Voltage Switching Mode
AGND (Pin 2)	7/15	No	+15	+7 to +15	+7 to +15	No Latches
GND (Pin 3)	7/18	No	+15	+7 to +15	+7 to +15	No Latches
AGND (Pin 3)	8/25	No	+5	+5	+5	3 × 4-Bit Nibble Load
AGND (Pin 3)	8/25	No	+5	+5	+5	12-Bit Serial-In
AGND (Pin 2)	7/25	No	+5 & +15	+5 to +15	+5	12-Bit Parallel in with Data Latches
AGND (Pin 2)	7/20	No	+5, +12 & +15	+5 to +15	+5 to +15	8-Bit + 4-Bit (i.e., Two Byte) Load Double Buffered
Note 5	Note 5	Note 5	+15	+15	+15	16-Bit Parallel in with Data Latches