CHAPTER 4

SINGLE SUPPLY OPERATION FOR CMOS DACs USING THE VOLTAGE-SWITCHING MODE

4.1 SINGLE SUPPLY UNIPOLAR DAC

CMOS DACs are traditionally used in a current-steering mode. The current in the R-2R ladder is steered either to OUT2 or to OUT1, both of which are at ground potential. D/A converters can also be realized by connecting the DAC, as shown in Figure 4.1. This mode of operation is known as voltage-switching. It is particularly useful where single supply operation is required for CMOS DACs. Figure 4.2 shows a CMOS D/A converter operated in the voltage-switching mode. The reference voltage V_{IN} is applied to OUT1, OUT2 is connected to AGND, and the output voltage is available at the V_{REF} terminal. This book indicates the voltage-switching mode

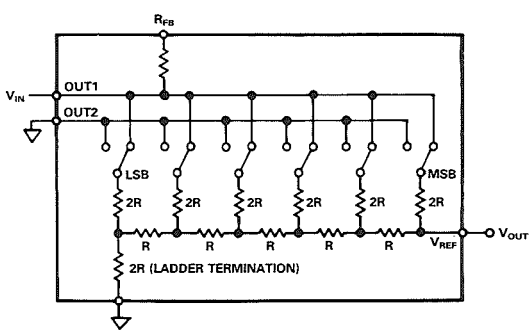

Figure 4.1 Voltage-Switching DAC Using R-2R Ladder

of operation by drawing the DAC symbol as a simple rectangle as shown in Figure 4.2. There are several points to note about this mode of operation:

a) A positive reference voltage gives a positive output voltage—hence, single supply operation is possible.

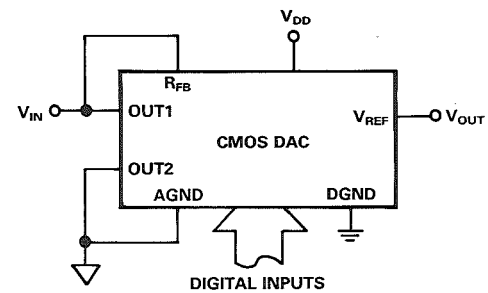

Figure 4.2 Single Supply D/A Converter Using Voltage-Switching Mode

b) The output is a voltage (not a current) at a constant impedance equal to the ladder resistance.

c) The reference voltage input (V_{IN}) no longer sees a constant input impedance, but one which varies with code. Hence, buffering the V_{IN} source is an absolute necessity.

d) V_{IN} is limited to low voltages (about 2.5V max. for V_{DD} = +15V) because the switches in the DAC no longer have the same source-drain voltages. As a result their on-resistance differs. This degrades the integral linearity of the DAC.

e) Output spikes due to digital to analog glitch impulses (2.3.7) in the DAC are reduced. Both switched nodes OUT1 and OUT2, are connected to low impedance points V_{IN} and AGND, and parasitic capacitances are charged from these two points.

f) The circuit has no significant gain error drift as long as the current load at the DAC output is small (i.e., use output buffer amplifier).

g) The feedback resistor R_{FB} is not required in the circuit. To minimize stray capacitance effects, tie R_{FB} to OUT1, or use it as a bias resistor for the reference circuit.

In the voltage-switching mode, the full-range multiplying capability of the CMOS DAC is lost. V_{IN} must not go more than 0.3 volts negative with respect to OUT2 or an internal diode will turn on and a heavy current may flow which will damage the device. Furthermore, the maximum permissible value of V_{IN} without substantial degradation of accuracy is determined by several factors. Figures 4.3 and 4.4 show the effect of variation of V_{DD} and V_{IN} for the AD7240, a 12-bit D/A converter designed and specified for use in the voltage-switching mode. In general, a 12-bit DAC requires a greater difference between V_{DD} and V_{IN} (max) than an 8-bit DAC does in order to preserve linearity.

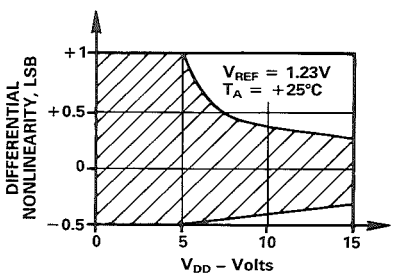

Figure 4.3 Differential Nonlinearity vs. V_{DD} (Shaded Area Shows Typical Range of DNL vs. Supply Voltage)

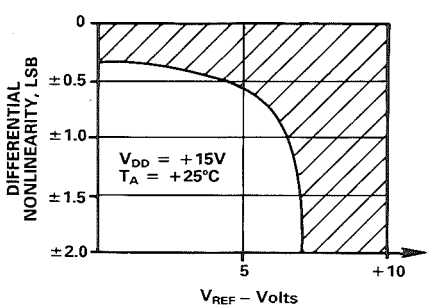

Figure 4.4 Differential Nonlinearity vs. Reference Voltage (Shaded Area Shows Range of Values of DNL That Typical Occur for K and J Grades)

4.2 SINGLE SUPPLY DAC WITH OFFSET SCALE (VOLTAGE-SWITCHING)

In some applications (for example in 4-20mA circuits) a DAC is required to have zero code input correspond to an output value other than zero, i.e., a zero code point offset from ground. This can be achieved by the voltage-switching circuit of Figure 4.5. OUT2 is driven by the lower offset voltage, and OUT1 is driven by the full scale output voltage. If the ladder termination resistor is connected to AGND, then the output voltage for digital input code D is given by:

$$V_{OUT} = D\cdot(V1–V2) + (1–2^{-n})\cdot V2$$

when D = 0, $V_{OUT} = V2\cdot(1–2^{-n})$

when D = $1–2^{-n}$, $V_{OUT} = V1$

If the ladder termination resistor is connected to OUT2, the output voltage is given by:

$$V_{OUT} = D\cdot(V1–V2) + V2$$

when D = 0, $V_{OUT} = V2$

when D = $1–2^{-n}$, $V_{OUT} = V1\cdot(1–2^{-n}) + 2^{-n}\cdot V2$

Thus the end points are V2 and approximately V1. Note that the connection of the ladder termination resistor has a slight dc effect on the transfer function. Practical realizations of the circuit of Figure 4.5 require that DGND and OUT2 be available as separate pins on the D/A converter. The outputs of amplifiers A1 and A2 should never go negative with respect to OUT2 or parasitic transistor action may damage the DAC. Usually A1 and A2 are operated on the same single supply (V_{DD}) as the DAC.

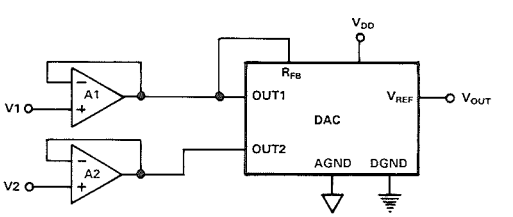

Figure 4.5 Single Supply D/A Converter with Scale Offset from Zero (Voltage-Switching)

4.3 OP AMPS FOR VOLTAGE-SWITCHING DAC CIRCUITS

The output op amp for a voltage-switching DAC circuit buffers the output of the DAC and usually provides some gain, since the input reference voltage, V_{IN}, is usually smaller than the required output voltage span. The output voltage for the circuit of Figure 4.6 is given by:

$$V_{OUT} = D \cdot V_{IN} \cdot G \cdot \frac{1}{1+\frac{G}{A}}$$

$$\text{where } G = \frac{R1+R2}{R1}$$

the nominal gain of the output buffer amplifier. The error due to finite op amp gain A is approximately given by:

$$\text{Absolute Full Scale Error} \approx \frac{-G^2}{A}$$

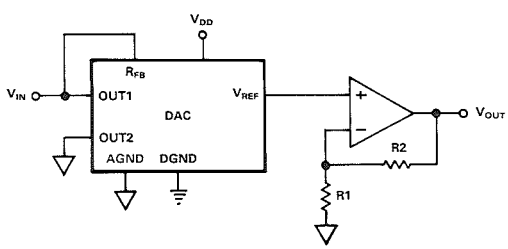

Figure 4.6 Voltage-Switching D/A Converter

Such errors are primarily gain errors which may be corrected by minor gain adjustment. In many voltage-switching circuits, it is convenient to operate with V_{IN} = 1.23V (a low-cost bandgap reference such as AD589) and G = 8.13 for a 0 to 10V output range from the DAC. The input bias current and the input offset voltage of the op amp produce an offset at the voltage output. However, unlike the current-steering circuit, these two parameters are not code dependent and do not affect DAC linearity because the voltage-switching DAC has a constant output impedance.

The common-mode rejection of the op amp is important in voltage-switching circuits, since it produces a code dependent error at the voltage output of the circuit. Unfortunately, most manufacturers do not specify common-mode performance very well because it is a difficult parameter to define and measure. Most op amps have adequate common-mode rejection for use at 8- and 10-bit resolution but for 12 bits the required performance can outstrip that of some popular op amps. For example, a common-mode rejection ratio of 85dB at 1V input is often quoted as an op amp's performance; it results in an error of 0.23LSB for 12-bit resolution.

Provided the DAC switches are driven from true wideband low impedance sources (V_{IN} and AGND), they settle quickly. Consequently, the slew-rate and settling time of a voltage-switching DAC circuit is determined largely by the output op amp. To obtain minimum settling time, it is important to minimize capacitance at the V_{REF} node (voltage output node in this application) of the DAC. This is done by using low input capacitance buffer amplifiers and careful board design.

4.4 OP AMP INPUT STAGES FOR SINGLE SUPPLY

Most single-supply circuits include ground as part of the analog signal range, which in turn requires that the op amps common-mode input range should include its "negative supply". This restricts the available op amps to those that use either PNP transistors, PMOS devices or N-channel JFET's for the input differential pair.

The choice of single supply op amps currently available is quite small. Typical devices are the LM324 PNP input bipolar quad op amp, the CA3130 PMOS input BIMOS op amp family and the TL091 NFET family. The input stage determines most of the op amp's input characteristics. Bipolar inputs have the lowest untrimmed input offset voltage; PMOS inputs have the highest input impedance but also the highest offset voltage while JFETs usually provide the lowest noise.

The output stage of an op amp determines the maximum output voltage swing. CMOS outputs such as those used in the CA3130 can swing to both supply rails unloaded, although their output resistance is fairly high. The output swing available from bipolar output stages such as that used on the LM324 is typically from the negative supply rail (ground) to within 1.5V of the positive supply rail. The current sink capability of the LM324's output stage when V_{OUT} is close to ground is limited but it can be improved by connecting a shunt resistor from V_{OUT} to ground (see Figure 4.7). A more recent bipolar op amp design, the LM10 allows the output to swing to within 15mV of either supply rail. Figure 4.8 shows the performance of the LM10, TL091, LM324 and CA3130 under various load conditions, when operated on a single +5V supply. Be aware of the fact that at low supply voltages op amp settling time and slew rate are seriously impaired.

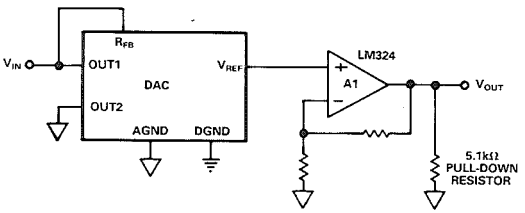

Figure 4.7 Method of Improving LM324 Output Drive Near Ground

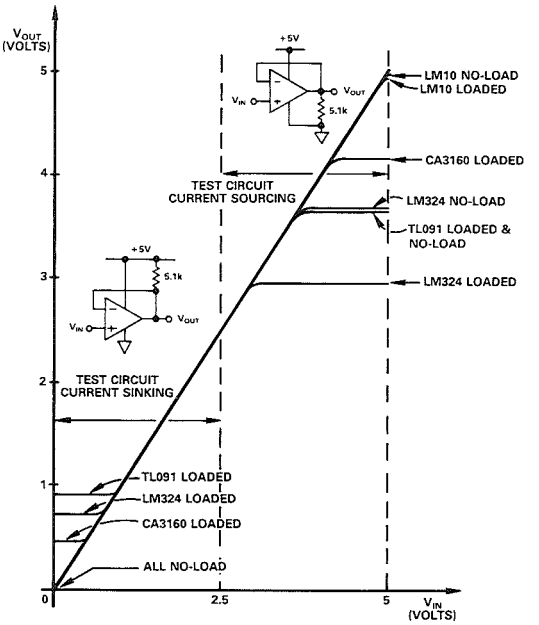

Figure 4.8 Single-Supply Op Amp Performance V_{CC}+5V