CHAPTER 2

INSIDE CMOS DACs

2.1 INTRODUCTION

CMOS DACs are fabricated with a CMOS plus thin-film resistor process. The thin-film is used for the R-2R ladder and CMOS provides the N-channel current steering switches and the interface logic. Thin-film resistors are preferred to diffused resistors for a number of reasons:

a) They match one another better and track better with temperature so that more-accurate D/A converters can be made.

b) Thin-film resistors do not have any parasitic diodes to the substrate or surrounding circuit (diffused resistors do); therefore voltages on the resistors can safely exceed the supply voltages without forward biasing any junctions. Furthermore since there are no diodes and the resistors are insulated from the silicon no leakage takes place from the resistors.

c) Thin-film resistors can be laser trimmed to adjust their final in-circuit value. This allows more accurate converters to be made than would otherwise be possible.

d) Diffused resistors exhibit a voltage dependent resistance. This makes them unsuitable for variable reference circuits, and causes harmonic distortion in attenuator type applications.

Different manufacturers use different processes for the CMOS used in D/A converters. Some adapt a fairly standard metal gate process; Analog Devices uses polysilicon gate processes. The polysilicon gate technique is preferred because it gives two levels of interconnect (compared with the single level of metal gate) and therefore produces denser and smaller circuits. Also it makes it possible to design circuits which are virtually free from the latch-up problems (see Section 2-5) that plague many CMOS devices.

2.2 THE BASIC DESIGN OF CMOS DACs

The NMOS switches used in the D/A converter have a finite on resistance. If all the switches shown in Figure 2.1 were made the same physical size (i.e., equal on-resistance), then the voltage dropped across each

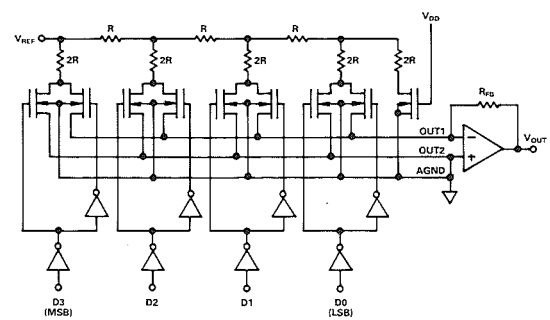


Figure 2.1 Simple CMOS D/A Converter

switch would be proportional to the current in each 2R leg of the R-2R ladder. For example, if V_{REF} = 10V, R = 10 kilohms and the switch on-resistance is 20 ohms then the voltage across the MSB (most significant bit) switch would be 10mV, the voltage across the next most significant switch would be 5mV and so on. This results in each 2R leg of the R-2R ladder having a different voltage at its "lower end". As a result, the D/A converter linearity would be adversely affected. To prevent this from happening the NMOS switches are "scaled" so that the nominal on-resistance of the MSB switch is 20 ohms, the next-significant one is 40 ohms, the next is 80 ohms, etc. all the way down the ladder. For a ten-bit device the least significant bit switch has a nominal

on-resistance of roughly 2 kilohms. All switches therefore have voltage drops of about 10mV for a 10V reference, and each 2R resistor has the same voltage at its "lower end"—thus DAC linearity is unaffected. The resistance of the switches varies with temperature but since the switches are scaled, the voltages across the switches will always match and the D/A converter linearity will be maintained.

The voltage across each switch is chosen to be roughly 10mV (proportional to the reference) because diodes exist from the switch to the P-well containing the switches—see Figure 2.2. With a negative reference voltage the voltage across the switch is negative and the diode is therefore slightly forward biased. However the voltage is designed to be small enough that this does not result in any significant current flowing from the P-well to the R-2R ladder (see section on leakage current).

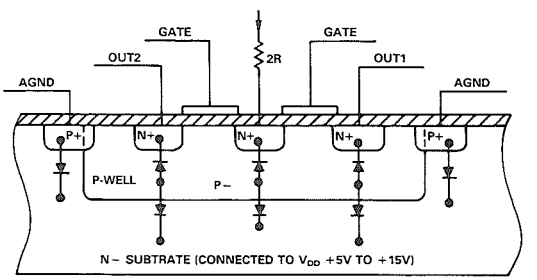


Figure 2.2 Simplified Cross Section through N-Channel DAC Switch Showing Diodes

The P-well containing the N-MOS switches is usually connected to Analog Ground (AGND). If there are sufficient pins available in the package AGND and OUT2 are brought out separately for improved applications flexibility. However, in many cases the number of pins available for analog connections to the DAC are severely limited and OUT2 is often connected internally to AGND and brought out on a single pin. The P-well for the N-MOS switches behaves as an extra gate to the NMOS switches and variations in the P-well voltage can change the on-resistance of the switches, which in turn can cause variations in the output of the D/A converter.

It is, therefore, important to minimize any noise at this node. Some converters use just a single P-well for all N-channel devices, others use separate P-wells for the D/A switches and the supporting interface logic. In this latter case the P-well for the interface logic is connected to digital ground—DGND.

There are three options for connecting the ladder termination resistor:

1) It can be brought out as a separate pin—this is not normally done because a pin is not available.
2) It can be connected internally to AGND (or DGND).
3) It can be connected internally to OUT2.

In designs prior to 1980, the ladder termination resistor is connected to AGND but in more recent circuits the resistor is connected to OUT2 as this is advantageous in some applications. See Appendix 1 for the connections used in various CMOS DACs.

The thin-film resistors used in the R-2R ladder all have the same physical shape: to improve matching 2R is realized by connecting two resistors of value R in series. The resistors are usually designed for a nominal value of 10 or 11 kilohm with a typical manufacturing tolerance of -5, $+10$ kilohms. Matching between resistors on a given die is of the order of 0.1% which is sufficient for a 10-bit converter. Higher-resolution converters require better matching between resistors; it is achieved by means of laser trimming. A very narrow laser beam is used to evaporate portions of the resistors in order to make them match better. Laser trimming for monolithic CMOS DACs is carried out at the wafer stage, because it is easier and more cost-effective to do the trim prior to separating the wafer into individual dice than to trim after assembly (as is done with hybrids). The trimming process is usually termed L.W.T. for Laser Wafer Trimming.

The switches used in the D/A converter constitute a small extra resistor in series with the 2R leg. Figure 2.3 shows an approximate equivalent circuit for a DAC with all inputs at logic "1"; all the input current is steered to OUT1 with the exception of the ladder

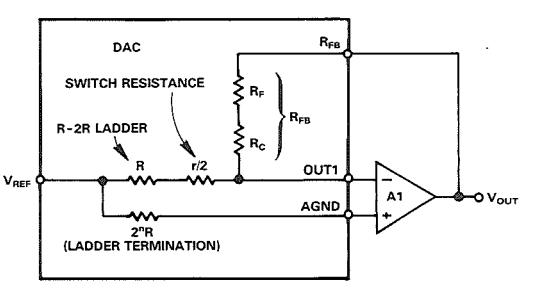


Figure 2.3 Approximate dc Equivalent Circuit of DAC at Full Scale

termination current (which will be neglected here). "r/2" represents the effective on-resistance for all the switches, where r is the on-resistance for the most significant switch. For the circuit to have the correct full-scale value, the equivalent feedback resistor RFB should be equal (R + r/2). To ensure that the performance is held over temperature R_F should equal R and have the same temperature coefficient as the resistors in the R-2R ladder, and RC should equal r/2 and have the same temperature coefficient as the DAC switches. It is a simple matter to achieve this requirement for R_F because the feedback resistor is normally made the same value as the other resistors but the requirement for RC = r/2 is more difficult to achieve. It can be realized by a permanently on switch twice the physical size of the MSB switch; however this significantly increases the die size and cost and also more than doubles the output capacitance which in turn increases the settling time of the DAC. An alternative procedure is to insert a special resistor of value r/2 in series with the feedback resistor R_F. The RC resistor is fabricated from a material whose temperature coefficient matches that of DAC switch. Using either of these methods the "gain error temperature coefficient" of the DAC can be made less than 5ppm/°C.

2.3 CMOS DAC PARAMETERS

2.3.1 Output Leakage Current (ILKG)

Ideally, with all digital inputs at "0", no current should flow out of the OUT1 terminal. In practice the small current that flows is known as the output leakage current. Similarly with all digital inputs at a logic "1", i.e., full scale, no current should flow out of the OUT2 terminal (provided that the ladder termination resistor is not connected to OUT2) but again a leakage current does flow in practice. The leakage current at each terminal comes from two sources, leakage across the source-drain of the "off switch" (ILKGSD), and substrate to P-well leakage (ILKGSS). This is shown in Figure 2.4. Both leakage currents are temperature dependent, roughly doubling for every 10°C temperature rise. ILKGSS will always flow from the substrate out of the OUT1 and OUT2 terminals but the direction and magnitude of ILKGSD will be determined by the reference voltage (analog input). A positive reference voltage gives an ILKGSD which flows out of OUT1 and adds to the effect of ILKGSS; a negative reference voltage gives an ILKGSD which flows into OUT1 and subtracts from the substrate leakage. If the reference voltage is ac, ILKGSD will be ac, setting a lower limit to feedthrough voltage (see 2.3.6). The worst case leakage current arises at the highest operating temperature with a positive reference voltage. For this reason a CMOS D/A converter should always be specified with a positive reference voltage (+10V is normally used). ILKGSS and ILKGSD are usually approximately equal although their relationship depends upon the geometry of the D/A converter under consideration and the various processing steps used in fabrication. In an applications circuit the effect of the leakage currents is to introduce a shift in the D/A transfer function, shown in Figure 2.5, which usually becomes significant at temperatures above 100°C.

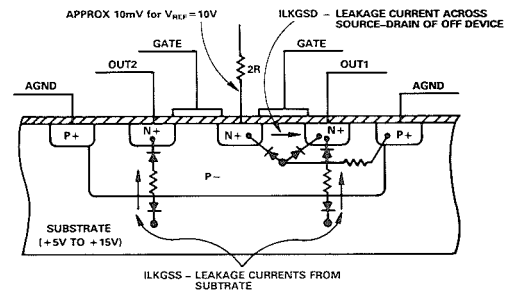
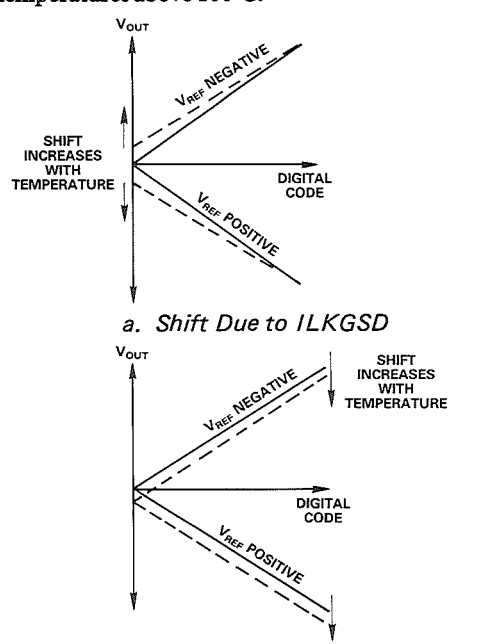


Figure 2.4 Cross-Section through DAC Switch Pair Showing Leakge Paths to OUT1 and OUT2



a. Shift Due to ILKGSD

b. Shift Due to ILKGSS

Figure 2.5 Effect of Leakage Currents on DAC Transfer Function

2.3.2 Gain Error

For an ideal D/A converter the maximum output voltage is given by:

$$V_{max} = -V_{REF} \cdot (1-2^{-n})$$

In practice the feedback resistor R_{FB} is usually not exactly equal to the ladder resistance R and as a result V_{max} deviates from its correct value. The amount of this deviation is known as gain error and is usually expressed as a percentage or in LSB equivalent units.

$$\text{Gain Error \%} = \frac{V_{max\,actual} - V_{max\,theoretical}}{V_{max\,theoretical}} \times 100$$

The gain error for laser trimmed DACs is usually less than that for non-trimmed devices because laser trim is used to adjust the gain error. As pointed out in the previous section the N-channel DAC switches have a temperature sensitive on-resistance which is compensated for by a matching device in series with the feedback resistor. This reduces the variation of gain error with temperature but does not eliminate it. Gain error temperature coefficient is usually defined as:

$$\text{Gain Error T.C. (ppm/°C)} = \frac{\text{Gain Error at } T_{max} - \text{Gain Error at } T_{min}}{(T_{max} - T_{min})}$$

T_{max} and T_{min} are the two temperatures at which measurements are performed for a given temperature range.

It is very difficult to distinguish between gain error shifts due to temperature coefficient mismatch between the feedback resistor and the DAC, and apparent gain error shifts due to variation in leakage current. As a result the specified gain error for a D/A converter is usually taken to include any effects due to leakage currents. A gain error temperature coefficient of 5ppm/°C results in a 0.5mV shift in full scale output for V_{REF} = 10V and a 10°C temperature change.

2.3.3 Power Supply Rejection Ratio

Gain error is also affected by variations in the supply voltage because a change in V_{DD} changes the gate drive to the DAC switches, causing a variation in switch resistance which in turn results in a small change in the output voltage. Power supply rejection ratio is normally quoted in terms of % change in output per % change in V_{DD} for full scale output of the DAC.

$$\text{Power Supply Rejection Ratio} = \frac{(V_{OUT2} - V_{OUT1}) \cdot V_{DD1}}{(V_{DD2} - V_{DD1}) \cdot V_{OUT1}}$$

V_{OUT1} is the full scale output voltage for $V_{DD} = V_{DD1}$.

V_{OUT2} is the full scale output voltage for $V_{DD} = V_{DD2}$.

A power supply rejection ratio of 0.01%/% results in a full scale output voltage change of 5mV for V_{REF} = 10V and a 5% change in supply voltage.

2.3.4 Output Capacitance

The output capacitance of a CMOS D/A converter may be measured using the circuit of Figure 2.6. The frequency is varied to find the −3dB point and the

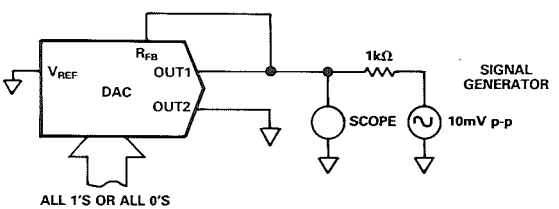


Figure 2.6 Circuit for Measuring Output Capacitance of DAC

capacitance may then be calculated. The output capacitance, which results from the relatively large N-channel devices used for the DAC switches, changes with the digital fraction applied to the D/A converter. The capacitance is a maximum when all the switches to the pin being tested are on and is a minimum when all the switches are off. The output capacitance of a CMOS DAC has a major influence on the settling time of the overall circuit.

2.3.5 Settling Time and Propagation Delays of CMOS DACs

Settling time is defined as the time required for the output of the D/A converter to settle to within 1/2LSB of its final value for a given digital input stimulus—usually zero to full scale. However this apparently straightforward definition hides a multitude of problems. The output current settling time of a CMOS DAC to two equivalent time constants (86%) is measured using an oscilloscope as shown in Figure 2.7 and then this is extrapolated to give a settling time to 1/2LSB assuming single pole exponential response. This provides a basis for comparing different CMOS DACs but is of little practical use because most applications use an output op amp to realize the voltage output. Since the response of the

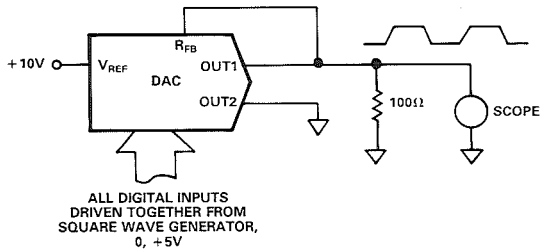


Figure 2.7 Test Circuit for Current Settling Time

output op amp plays a major part in the overall settling time there have been some attempts to quote output voltage settling time using a specified op amp. However, this approach has its own difficulty because different applications use different op amps.

Another factor which complicates the picture is that the definition of settling time given above encompasses both digital propagation delays and analog time constants. Recognizing this, the dependency on the type of op amp used, and the inherent errors in measuring and extrapolating time constants, a useful specification "Propagation Delay" is sometimes employed. Propagation Delay, primarily a measure of the internal digital delays of the DAC, is the time measured from the digital input changing to the output current reaching 90% of the final value. Knowing this, the output capacitance of the DAC (which interacts with the DAC resistance to further delay the response) and the response time of the output op amp, the user is better able to predict the final performance of the circuit.

2.3.6 Multiplying Feedthrough Error

When the D/A converter is operating with an ac signal as its reference some of the input signal may appear on the output even with all 0's presented to the DAC inputs. This is known as Multiplying Feedthrough Error; it arises as a result of stray capacitance, particularly DAC switch capacitance and inter-pin capacitance. Excessive multiplying feedthrough error is usually the result of poor circuit board layout (see Section 5.3.2). Some CMOS DACs have been designed to give very low feedthrough error (notably the AD7111 audio attenuator DAC).

2.3.7 Digital-to-Analog Glitch Impulse

A digital input change results in a change of voltage applied to some of the DAC switch gates. This voltage change is coupled across the stray capacitance shown in Figure 2.8 and appears as an impulse on either the OUT1 or OUT2 line. Digital glitch impulse is usually specified as the area of the resulting spike in either pA-s or nV-s with a specified output amplifier. It is measured with the reference input V_{REF} connected to analog ground and for a zero to full scale output transition. The glitch impulse is proportional to the D/A converter supply voltage and sometimes can be reduced by operating the converter at a lower supply voltage. Excessive digital-to-analog glitch impulse in an applications circuit can often be traced to poor circuit layout or residual solder flux—see Section 5.3.2.

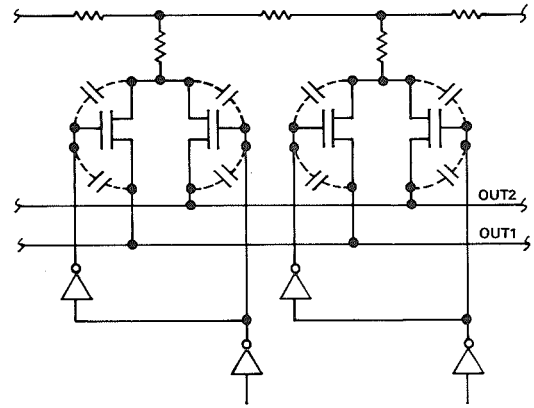


Figure 2.8 Capacitive Coupling from Gate Drive to OUT1 and OUT2

2.3.8 Distortion and Noise

When used as digitally controlled attenuators CMOS DACs exhibit very low distortion—in fact the distortion is primarily determined by the output op amp rather than the DAC itself. CMOS DACs have low distortion because the converter functions as a resistive attenuator using thin-film resistors which have low noise and very low voltage coefficient. The active devices in the DAC, i.e., the DAC switches, have only a very small fraction of the V_{REF} voltage across them; therefore any distortion introduced by the switches is proportionally reduced. The distortion introduced by a CMOS DAC (including the output op amp) is typically −90dB, and the output voltage noise density is about $70nV/\sqrt{Hz}$. It is common to quote the distortion and noise of CMOS D/A converters with a specified op amp. The audio attenuator DACs produced by Analog Devices have been specifically designed for use in applications requiring low noise and distortion.

2.3.9 Supply Voltage (V_{DD})

It is not practical to production test DAC performance for all possible values of supply voltage and as

a result DACs are usually specified and tested at a single value of V_{DD}. DACs can be operated at other supply voltages but this may adversely affect their linearity. Appendix 1 gives the specified operating voltages (i.e., the voltages at which the DACs are tested) for Analog Devices DACs and also their permissible operating range of V_{DD}. Analog Devices (or any other manufacturer) does not guarantee DAC performance at any voltage, other than that for which it is specified. As a general rule, the higher the supply voltage, the better the DAC performance (don't exceed maximum ratings) but there are exceptions to this—see for example Section 2.3.7 above. If the application requires the DAC to operate at a value of V_{DD} other than that for which it is specified, consult the local Analog Devices office for advice. It is often useful to test all DACs at incoming inspection to ensure that they meet their required performance at the application supply voltage.

2.4 EQUIVALENT CIRCUIT OF A CMOS DAC[2]

Figure 2.9 shows an equivalent circuit for a CMOS DAC. C_O is the output capacitance of the DAC switches, and R_S is the output resistance seen between OUT1 and OUT2 with V_{REF} at ground. Both C_O and R_S are code dependent. Full Scale (i.e., 111....111) gives a value for R_S of about 0.75R, and zero gives an almost infinite output resistance. C_O the capacitance from OUT1 to ground, varies approximately linearly with digital fraction from its minimum value at "all zeros" to its maximum value at "all ones".

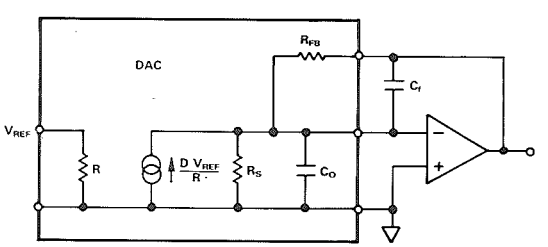


Figure 2.9 Equivalent Circuit of DAC

2.4.1 Feedback Capacitor Selection

The output capacitance of the DAC, C_O, introduces a pole into the open loop response which can cause ringing or instability in the closed loop applications circuit. To compensate for this an external feedback capacitor C_f is usually connected in parallel with R_{FB} as shown in Figure 2.9. Too small a value of C_f can produce ringing at the output, while too large a value can adversely affect the settling time. C_f is best chosen according to the equation

$$C_f = 2 \cdot \sqrt{\frac{C_O}{2\pi \cdot R_{FB}} \cdot \frac{1}{GBW}}$$

where GBW is the small signal unity gain-bandwidth product of the op amp in use. For a typical output capacitance of 100pF, an R_{FB} of 11 kilohm and GBW $= 2.10^6$, $C_f = 53$pF. Since C_O varies with code (typically 50pF to 200pF), it is not possible to fix a precise value for C_f; and for most DACs a value of 39pF or 47pF is adequate.

2.4.2 Noise Gain of CMOS DACs

The output resistance of a CMOS DAC at OUT1 varies with code. Consequently the feedback circuit of a CMOS DAC exhibits a code-dependent gain for op amp offset voltage. This variable gain is sometimes referred to as the "noise-gain" of the circuit and is shown in Figure 2.10 for an 8-bit DAC. The noise-gain introduces differential linearity errors (i.e., an error between adjacent codes) which, if the amplifier

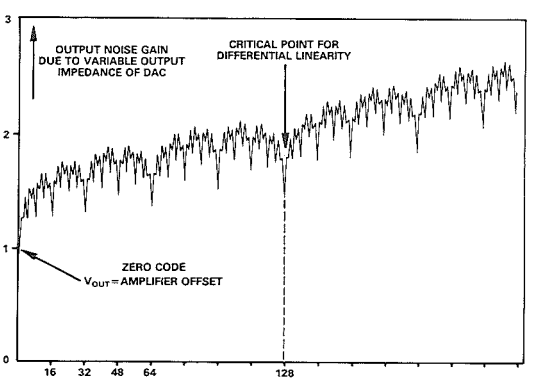


Figure 2.10 DAC Noise Gain vs. Code for 8-Bit DAC

input offset voltage is too large, can result in the DAC becoming non-monotonic. To minimize errors due to the variability of the noise-gain, amplifiers with low offset voltage and low bias currents are used. JFET input amplifiers with laser trimmed offset, such as AD542, AD544, and AD547, are commonly used as DAC output amplifiers—see Section 3.2.

2.5 LATCH-UP IN CMOS

Most CMOS devices contain parasitic SCRs (Silicon Controlled Rectifier)— see Figure 2.11. In normal operation these SCRs are unimportant; however, if an output or input of a CMOS circuit is taken more negative than the most negative supply voltage, the

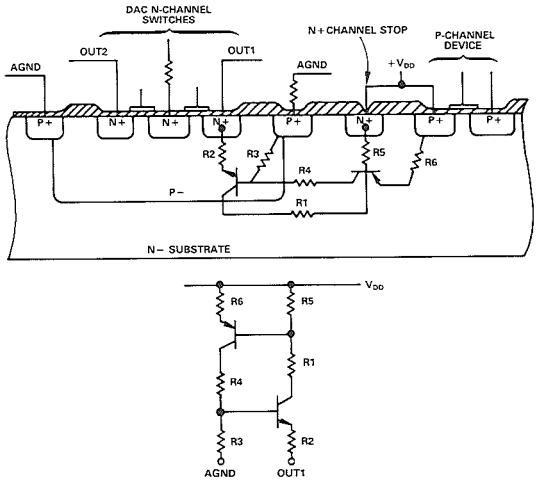


Figure 2.11 Cross Section through CMOS DAC Showing Parasitic NPN and PNP Devices Forming SCR

SCR can be turned on and will remain on until the device is destroyed or the power supply switched off. Negative transient inputs to CMOS devices can occur during power-up as a result of excessive voltage drops in ground lines, or due to transmission line effects in high speed logic systems. In particular some amplifiers exhibit low impedance at their inputs during power-up or power-down sequencing, and as a result the OUT1 or OUT2 lines can go negative. The traditional solution to this problem has been to clamp the OUT1 and OUT2 lines to ground using external Schottky diodes; however, all modern CMOS DACs from Analog Devices use a design technique which reduces the gain of the internal SCR to such a low level that SCR action cannot take place without excessive misuse. Consequently, external Schottky diodes are not required for these DACs. See Appendix 1 for a list of DACs requiring Schottky diodes.

2.6 PROTECTING CMOS AGAINST MISUSE

The digital inputs of Analog Devices' CMOS DACs are diode protected against static electricity using diodes as shown in Figure 2.12. In operation, however, if the digital input goes outside either V_{DD} or GND, the diode turns on and excessive current can flow. If the current exceeds 35mA, metal lines on the chip may fuse open. Close attention should be given to ground management, as substantial negative transients at digital inputs can arise if the ground system is inadequate. In general, "power should be

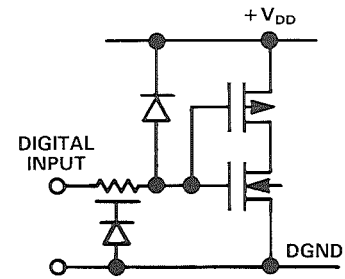


Figure 2.12 Digital Input Circuit Showing Protection Diodes

OFF" when CMOS devices are plugged into working circuits.

2.6.1 Electrostatic Discharge (ESD)[25], [26]

CMOS devices present a very high impedance at their inputs and outputs when not in use. If a high voltage, such as static electricity, is applied to an input or output terminal (usually inadvertently) it is possible, despite the input protection diode, for this voltage to rupture the gate-oxide of some of the MOS devices and destroy the circuit. To prevent such accidents happening, the following five steps should be observed during transportation, storage and system assembly:

1. Keep unused CMOS devices in the black conductive foam or conductive tubes in which they were shipped.
2. Ground the operator who is inserting the devices to the system power ground or bench with a conductive plastic wrist strap.
3. The bench work surface should be made of conductive material and should be connected to ground.
4. Before removing CMOS devices from their foam or tubes, ground the foam to discharge any static that may have built up.
5. After the circuit has been inserted into a circuit board, keep the board grounded or protected whenever it is carried around. Be~are of nylon or similar non-conductive plastic circuit board carriers.

ESD is one of the most common causes of circuit failure during the manufacturing process. It can affect MOS and bipolar devices. For further information see References 25 and 26.