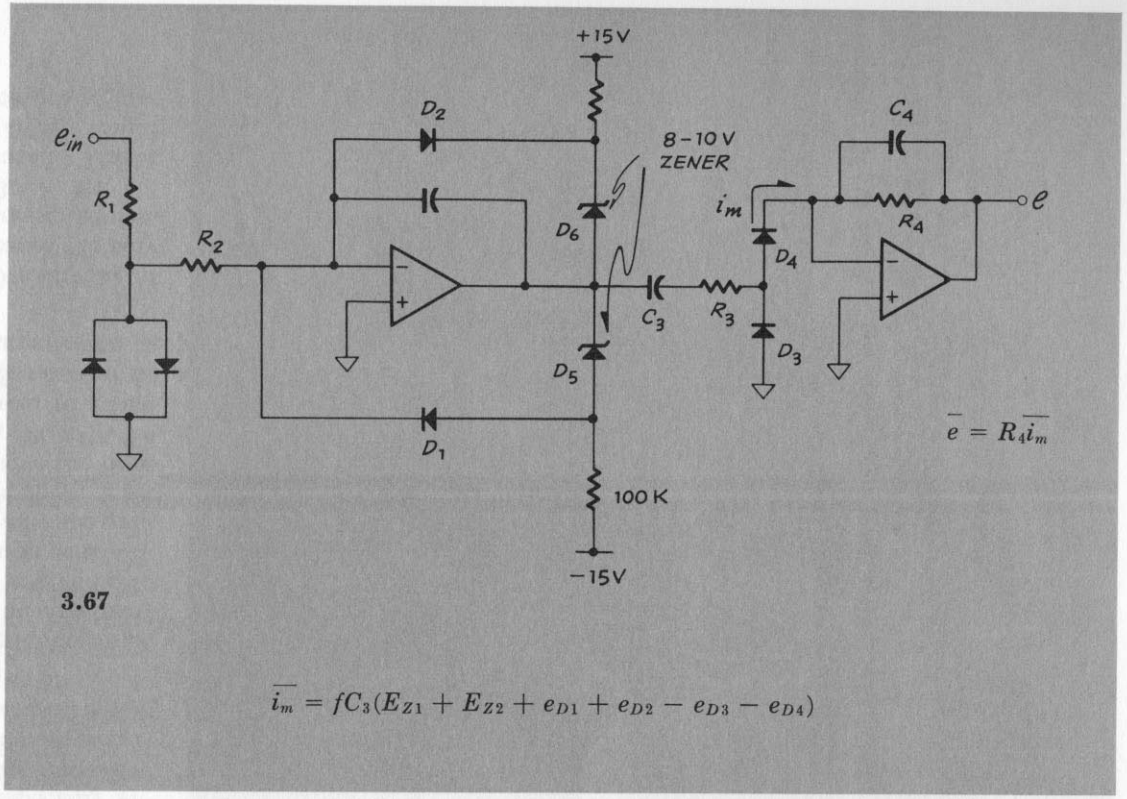
III.67 LOW FREQUENCY METER-CONVERTER. This circuit is a low-frequency version of the preceding one (III.66). The bounded open-looped amplifier to the left produces a trapezoid of very steep sides (for low frequencies) and an amplitude of 16–20 volts. This waveform then produces "spikes" or pulses of current through C_3R_3 (proportioned as in III.66) and these are "averaged" by C_4 in the modified current-to-voltage transducer, which then drives a meter or other load. e is proportional to frequency *only*, for a given set of component values, as shown in the equations on the diagram.

The feedback capacitor shown connected around the main amplifier is of critical importance and must not be made too small, lest overshoot and effective distortion occur.



3.67

$$\overline{i_m} = fC_3(E_{Z1} + E_{Z2} + e_{D1} + e_{D2} - e_{D3} - e_{D4})$$

III.67
I.25
I.27
II.18
II.39
to
II.43
III.54
III.66

III.68 DERIVATIVE dy/dx FROM TIME DERIVATIVES. If e_x and e_y are *increasing* functions of time, so that their time-derivatives are positive,* they will drive input currents into each of the logarithmic-response amplifiers to the left of the Subtractor. The output of each amplifier will, then, be proportional to the log of its input current—i.e., to the log of the time-derivative of the corresponding input voltage.

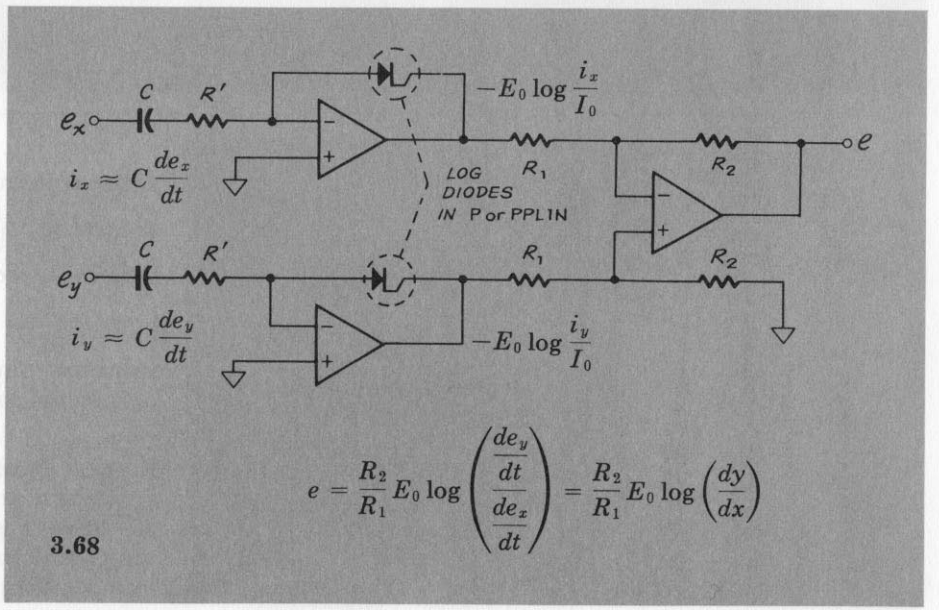
The Subtractor stage produces an output proportional to the *difference* of the logarithms, or proportional to the logarithm of their *ratio*, as indicated.

An anti-log circuit (see II.23) might be tacked on, at this point, to produce a signal of the form:

$$e' = K\left(\frac{dy}{dx}\right) \qquad (3\text{-}26)$$

R' is proportioned: (1) to achieve stability (see II.18, et al); (2) to prevent excessive capacitive loading of the input; and (3) to be as small as possible, yet still satisfy (1) and (2).

*Both i_x and i_y must be positive (or both negative if the log diodes are reversed), since the logarithm of a negative quantity is not real.



3.68

$$e = \frac{R_2}{R_1}E_0 \log\left(\frac{\frac{de_y}{dt}}{\frac{de_x}{dt}}\right) = \frac{R_2}{R_1}E_0 \log\left(\frac{dy}{dx}\right)$$

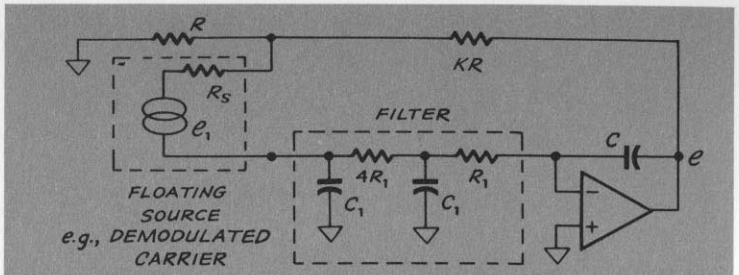
III.68
II.22
to
II.32

III.69 DEMODULATOR-AMPLIFIER. This circuit provides gain, impedance-buffering, and effective carrier filtering with reasonably fast envelope response for almost any kind of demodulator that can "float." The demodulator impedance (R_s) should be low enough to preserve the filter dynamics. This circuit permits one to insert a correcting bias (or an arbitrary "set point") of appropriate polarity in series with the positive-input return to ground of the (differential) amplifier, without influencing the gain . . . a useful feature.

Note that the source impedance does not affect the low-frequency gain $(1 + K)$ but does make the amplifier current offset more significant.

The circuit has the further advantage of providing an independent gain control, in the fórm of an adjustment of the feedback resistor (or the feedback divider ratio) thus making it possible to adjust both the sensitivity and the intial zero independently.

The filter characteristic has been chosen to provide a minimally-overshooting transient step response, low phase shift $\left(\phi \approx \frac{10}{3} R_1 C_1 \omega\right)$ at low frequencies and high attenuation at high frequencies $\left(\left|\frac{e}{e_1}\right| \approx \frac{9(1+K)}{20(R_1C_1\omega)^3}\right)$. It is near optimum in these regards for an attenuation of 1000 at the carrier frequency.



If: $R_1 = R_s + \left(\frac{K}{1+K}\right)R \qquad C = \frac{5}{9}\left(\frac{1}{1+K}\right)C_1$

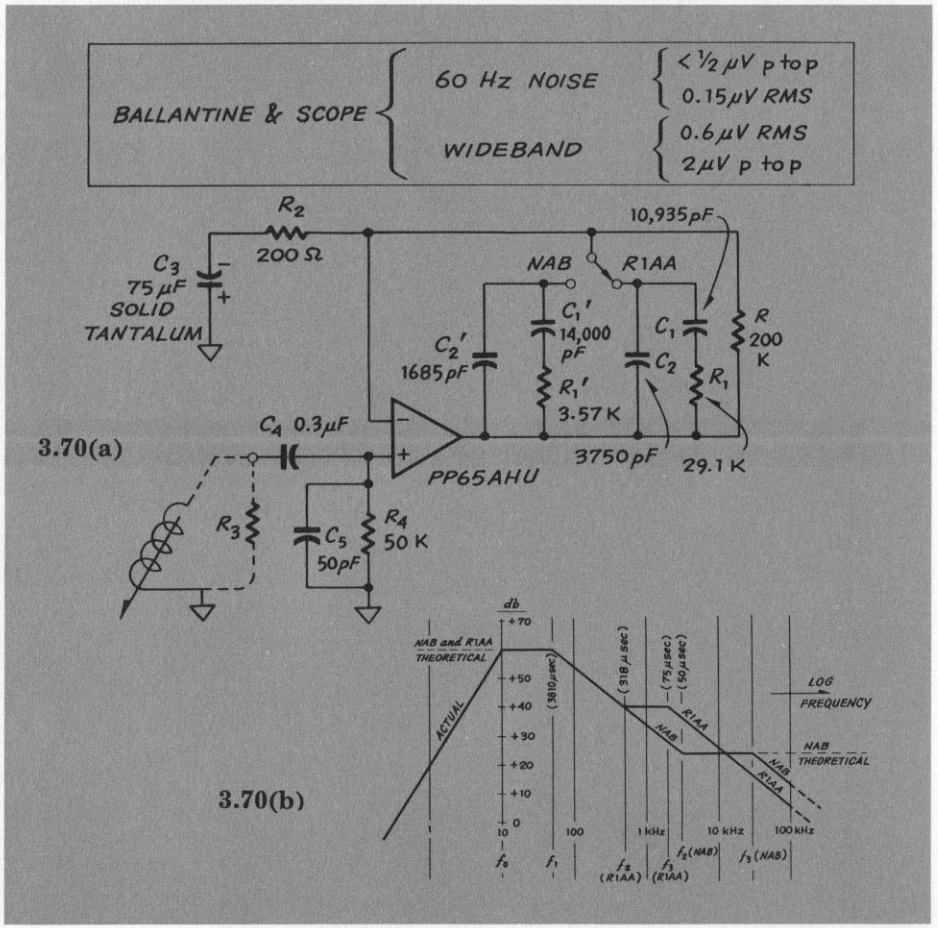
Then: $e = \dfrac{1+K}{1 + \frac{10}{3}R_1C_1p + \frac{50}{9}(R_1C_1p)^2 + \frac{20}{9}(R_1C_1p)^3}\, e_1$

III.69
I.7
I.18
I.19
I.20
II.1
II.2
II.3

III.70 PHONO & TAPE PREAMPLIFIERS. This circuit will be recognized as a form of follower with gain (see II.2), three features of which are important to this application. First, the amplifier's input resistance is well over 50 megohms, shunted by less than 20 pF. Second, the noise will be very low, especially important at low frequencies, where the input is smallest. Third, the frequency response is determined by the feedback network alone, and not by the amplifier; thus the calculated network values will be accurate to within a small fraction of a db.

Two standard equalization curves are shown—the RIAA for phonograph records, and the NAB for tape recordings. They require that the gain of the equalizing preamplifier begin "rolling off" at some frequency, f_1, at 6 db per octave up to another frequency, f_2. From f_2 to a higher frequency, f_3, the gain is constant. Above f_3, the gain rolls off again, indefinitely, for RIAA. For NAB, the gain should be constant above f_2, indefinitely; however, to minimize noise, most audio equipment manufacturers arbitrarily roll off the response above the limit of hearing . . . beginning, say, at 30 kHz, as is shown here for f_3 (NAB). To minimize low-frequency noise, especially transients, it is advisable to reject "DC" and low-frequency signals below some arbitrary cut-off frequency, f_0, here selected to be 10.6 Hz. Two time constants, R_2C_3 and R_4C_4, combine to provide a 12 db per octave attenuation below f_0.

The tantalum capacitor C_3 will always charge to about 10 to 100 millivolts of DC in the polarity shown (if the amplifier is properly zeroed) because the tiny amplifier input current (DC) flows through R_4 from ground. Low noise requires relatively low input-circuit impedance—hence the choice of 0.3 μF for C_4, which, with R_4 = 50 kΩ, provides the desired low-frequency cutoff. Direct coupling can be employed by eliminating the R_4C_4 filter, and the circuit would then present essentially "infinite" impedance; however, most pick-ups *require* a resistive load of about 50 kΩ (some as low as 5 kΩ), hence R_3.



III.70
I.40
I.41
I.42
II.2
III.35

III.71 NEGATIVE-IMPEDANCE/ADMITTANCE CIRCUITS. The circuits shown here exhibit, between the input terminal and signal ground, a negative impedance (or admittance)* in that a positive-going signal results in a negative current flow. Such a condition, produced as it is by positive feedback, will immediately suggest to the battle-scarred circuit designer the possibility of at least conditional instability, if not outright oscillation. Indeed, either of these circuits can run the gamut of instabilities from sinusoidal ringing to flipping and flopping from one bound to the other. Circuit (a), used to create negative impedance (Z_n) tends to be stable for small values of source impedance $|Z_s|$ and is, therefore, said to be "short-circuit stable." Circuit (b), used to create negative *admittance* (Y_n) tends to be stable for *large* values of $|Z_s|$, and is, therefore, said to be "open-circuit stable."

*The reason for making this distinction in nomenclature will be apparent in a very few lines.

A necessary condition for stability for each circuit may be stated more rigorously as:

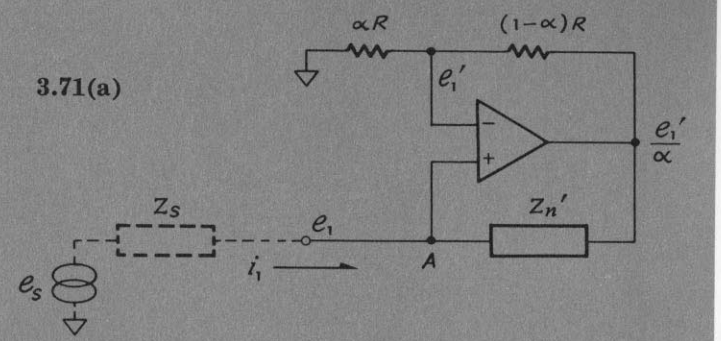
- Circuit (a), $\left|1 + \frac{Z_n}{Z_s}\right| > \frac{1}{\alpha} = 1 - \frac{Z_n'}{Z_n}$
- Circuit (b), $\left|1 + \frac{Z_n}{Z_s}\right| < \frac{1}{\alpha} = 1 - Y_n Z_n'$

(3-27)

for all values of frequency. However, even when (3-27) is satisfied, one cannot be certain of stability—in other words, the condition stated is not sufficient.

We have already seen one very useful application of these circuits, in III.37, which discussed the creation of a negative capacitance across the input-to-ground terminals, to neutralize input capacitance. It is apparent from the equations developed on the drawings that these circuits can develop negative resistance, capacitance, inductance, or combinations thereof, provided only that the stability requirements be respected.

3.71(a)



$e_1 = e_1'$ (assuming infinite amplifier gain)

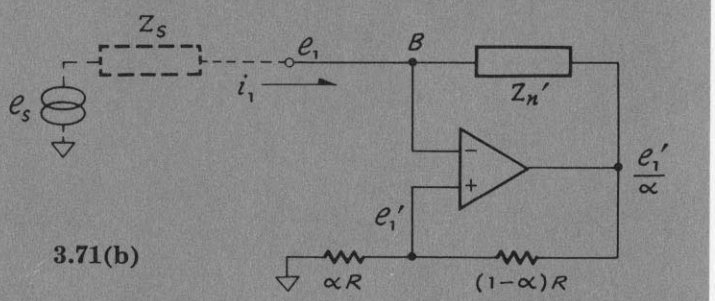
$$i_i = \left(e_1 - \frac{e_1'}{\alpha}\right)\frac{1}{Z_n'}$$

$$= -\frac{e_1}{Z_n'}\left(\frac{1}{\alpha} - 1\right)$$

$$Z_n = \frac{e_1}{i_1} = -\left(\frac{Z_n'}{\frac{1}{\alpha} - 1}\right)$$

Negative Impedance, $Z_n < 0$.

3.71(b)

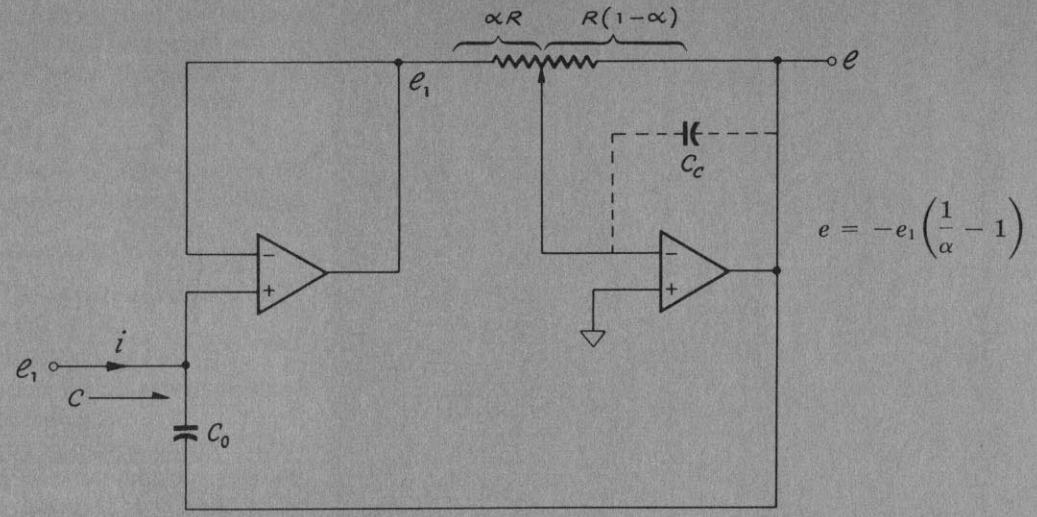


$$Y_n = \frac{i_1}{e_1} = -\frac{\left(\frac{1}{\alpha} - 1\right)}{Z_n'}$$

Negative Admittance, $Y_n < 0$

III.72 CAPACITANCE MULTIPLIER. This circuit allows the synthesis of a capacitor or other impedance (between the input terminal and ground) that may be adjusted over a wide range by rotating the potentiometer shown, so as to adjust the gain of the inverter stage. The first stage is a simple follower, the only function of which is to isolate the capacitance created by this circuit from the loading represented by αR. Indeed, if we have no objection to creating a "lossy" capacitor, and if αR need never be adjusted near zero, the follower could well be omitted . . . but this circumstance is, unfortunately, rare. It will be noted that the capacitance created is inversely proportional to the rotation of the potentiometer, and it will further be noted that, since α may be varied between 0 and 1, the input capacitance is always larger than, or at least equal to C_0. The principal limitation in applying this circuit to the construction of mammoth capacitors from tiny ones is that the ratio of e to e_1 is almost exactly the same as the ratio of C to C_0, so that the larger the multiplication of capacitance achieved, the smaller is the maximum input signal that may be tolerated, for a given amplifier output-voltage rating.

Other limitations include: signal frequency, which must not exceed the value at which the finite-gain error factor intrudes upon the simple response relationship given here; Q, which is the function of the phase shift in the amplifiers, since such phase shift introduces a loss component, and noise components, which are magnified by the ratio of C to C_0.



$$\frac{d(e_1 - e)}{dt} = \frac{i}{C_0} = \frac{1}{\alpha}\left(\frac{de_1}{dt}\right) \qquad \text{Thus: } C = \frac{i}{\frac{de_1}{dt}} = \frac{1}{\alpha} C_0$$

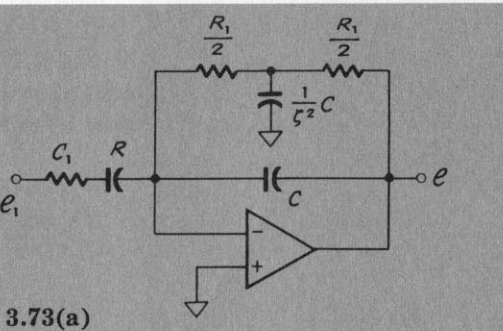
3.72

III.72
II.1
II.2
II.3
II.4
II.5
III.6
III.37
III.71

III.73 HIGH FIDELITY AC INTEGRATOR. In this circuit, the conventional frequency response characteristic of an AC integrator (see II.11) is extended as shown providing accurate integration at lower frequencies, without loss of stability. This characteristic is accomplished by paralleling the integrating capacitor with a Tee network designed to roll off at approximately the same frequency as that at which the stabilizing Resistor and Capacitor, (R_c and C_0 in II.11) would normally begin to limit the low-frequency response.

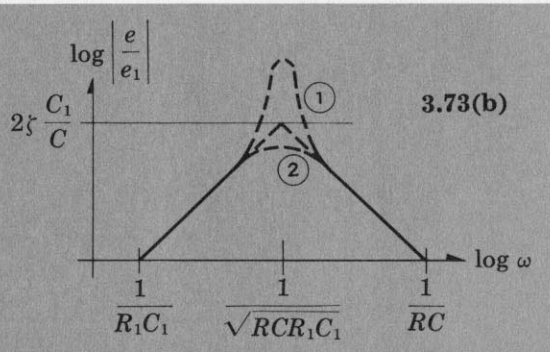
The same technique (with the R's and C's playing reverse roles) permits extended high frequency performance of a differentiator, while maintaining the noise-rejection capabilities at still higher frequencies. Both circuits are useful as second-order band pass filters, for ζ (the damping ratio) not much smaller than 0.5.

This circuit has applications in instrumentation, e.g., the conversion of acceleration to velocity, velocity to position (or vice versa), etc.



3.73(a)

$$e = -\frac{e_1}{\frac{1}{R_1 C_1 p} + \frac{C}{C_1} + RCp} \qquad \zeta = \tfrac{1}{2}\sqrt{\frac{R_1 C}{RC_1}}$$



3.73(b)

Dashed lines ① and ② indicate typical underdamped and overdamped responses.

Peak amplitude is $\frac{C_1}{C}$

III.73
I.26
I.40
to
I.43
II.10
II.11
II.12
III.57

III.74 PRECISION PEAK-READER/MEMORY. This circuit will be recognized as a simpler variant of that of III.50, using only two amplifiers instead of three, at some (small) sacrifice of accuracy. The left-hand amplifier is used in a switching circuit of the type described in II.40. It responds only to negative input signals, being diode-bounded against positive inputs. Negative inputs are permitted to charge C, through R, D_1 and D_2. The voltage across C is the input signal for the second amplifier, which is connected as a unity-gain follower having *two* feedback paths:

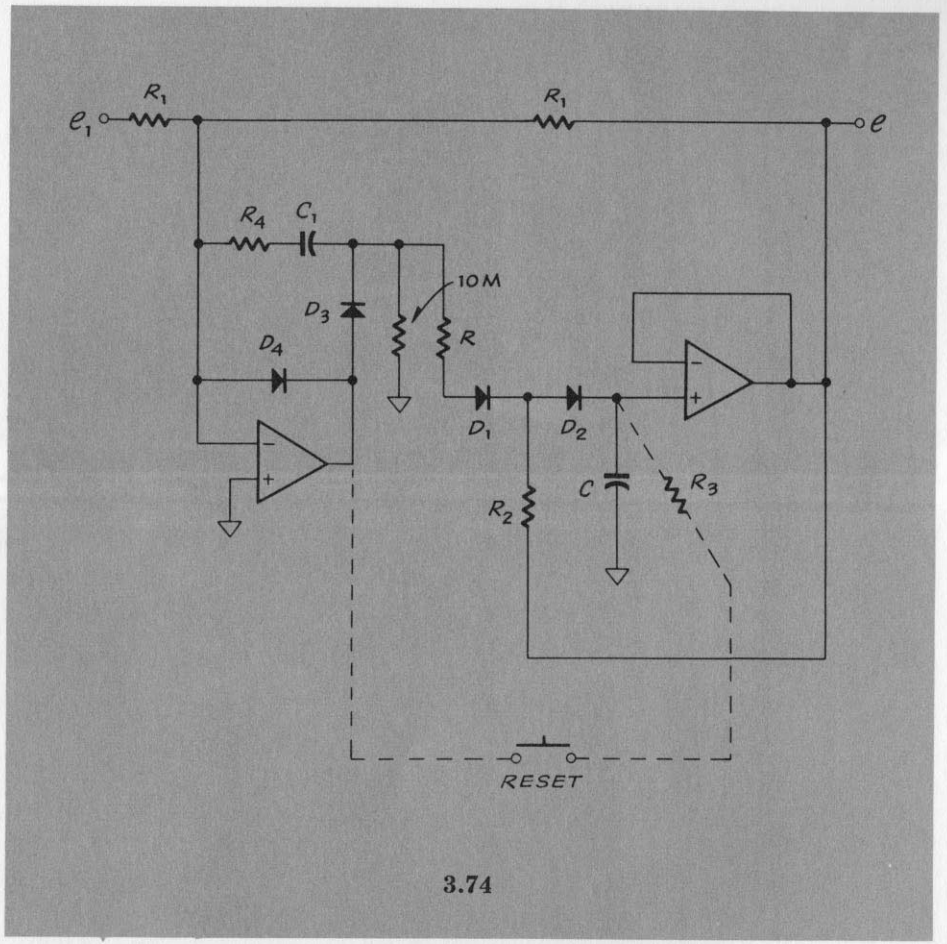
(1) feedback through R_1, which creates, in effect, a unity-gain inverter, in combination with the input resistor, R_1. (The normal inverter summing-point equilibrium is achieved, however, *only* when and if C is charged fully to the instantaneous values of e_1; otherwise, some current must flow through C_1 and R_4.)

(2) feedback through R_2, which assists D_1 and D_2 in disconnecting C from any discharge path whenever the input voltage is the same as or less than the highest peak to which C has been charged since the last resetting. (Leakage in C itself, or through the reset push-button insulation, is not nullified by this expedient, however.)

The 10 M resistor provides a path for the leakage in D_1. The reset push-button restores C to the potential of the output of the switching amplifier, thus nullifying the error due to diode drop, particularly if R_3 is made about equal to R. Initial conditions other than zero may be achieved by the method shown in III.49.

For good tracking RC should be *very* short compared to the fastest rate of change of e_1; preferably an order of magnitude shorter. By reversing all of the diodes, the circuit can be made to track positive peaks, instead of negative. Note that the circuit inverts; that is,

e (a positive voltage) $= -E_p$ (highest negative peak of e_1 since reset) (3-28)



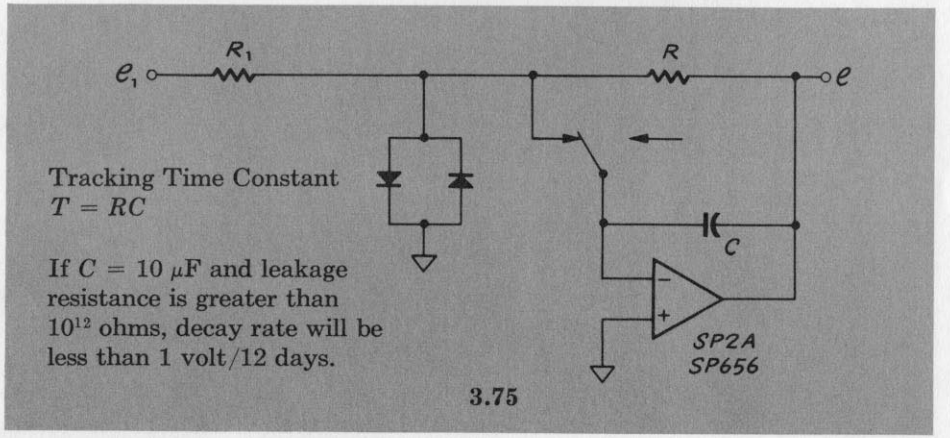
3.74

III.74
II.39
II.40
II.49
II.50
II.51
III.49
to
III.53
III.75
III.76

III.75 TRACK-HOLD LONG-TERM MEMORY. When the input to this circuit varies, the output "tracks" it, provided that the rate of change of output required does not exceed the limitations imposed by the tracking time constant, RC. (See II.46–48.)

When the relay contacts are open, the "Hold" Performance of the circuit depends almost entirely on the leakage in C, and only slightly upon the amplifier input current. The performance quoted in our exemplary diagram, while impressive, is not unusual for the best (Philbrick) amplifiers, polystyrene capacitors, and heads-up circuit construction.

There is the matter of resetting, which is automatically accomplished (back to "Track") by closing the relay contacts. The diodes are provided principally to keep the resistive summing point near ground potential during "Hold," whatever the range of input variation, thus tending to minimize voltage drop and hence leakage across the switch.



3.75

III.75
II.39
II.40
II.49
II.50
II.51
III.49
to
III.53
III.74
III.76

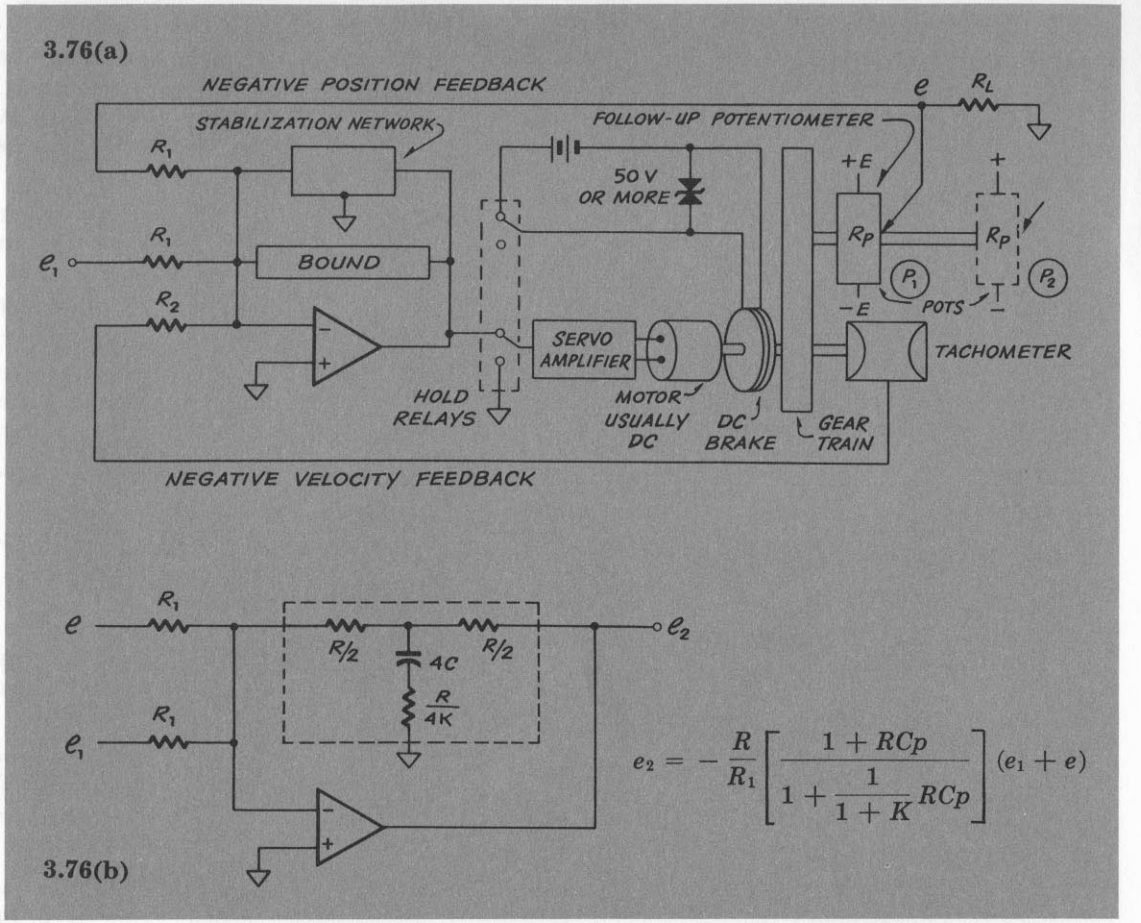
pages 98 & 99

III.76 PERMANENT TRACK-HOLD MEMORY. This circuit, with the exception of the hold relays and brake, is representative of a servo-driven (computing) potentiometer of the kind used for multiplication, function generation, or trigonometric resolution. Tachometer (velocity or rate) feedback is incorporated to aid stabilization; although a tachometer may not be necessary if the ~~output~~ input, e_1, is sufficiently noise-free to be differentiated to obtain a rate signal, as in (b).

The input must not change so rapidly that the output, e, is unable to follow it; therefore the time delay associated with relay operation and brake actuation should be small. The brake must be capable of rapidly dissipating the kinetic energy of the rotating parts. The zener clipping diodes in the brake solenoid circuit are used to reduce the magnetic field rapidly (by dissipating its energy) whenever the hold relay is opened. If the brake is spring loaded, it will always maintain the most-recently-servoed shaft position, even when the power is off. Note that the clamping accuracy of the brake is enhanced by the use of an anti-backlash gear train.

An additional follower-amplifier is needed if the output (e) must drive a varying or heavy load (R_L) since the potentiometer is loaded with the parallel resistance of R_1 and R_L. If any other potentiometers are mounted on the same shaft as P_1, they should have the same resistance and electrical load as does the follow-up potentiometer, in order that their output voltages be proportional to e_1.

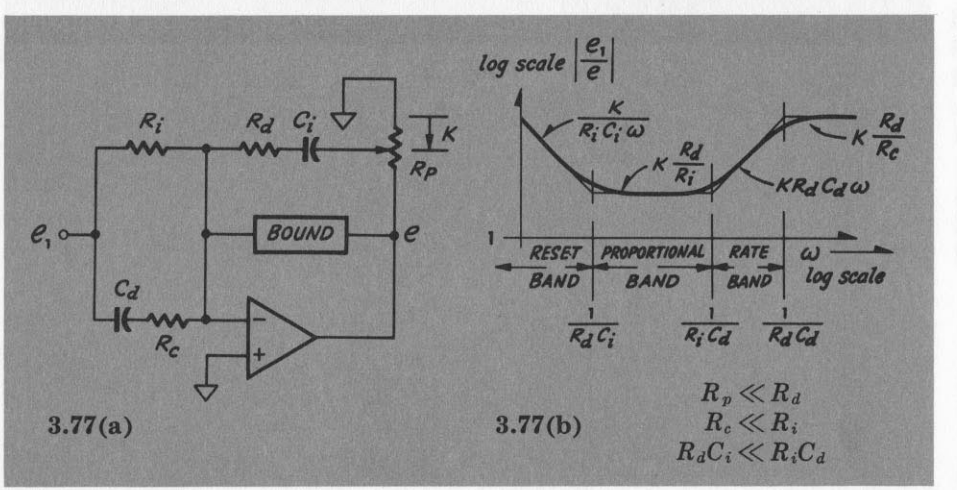
One may have to interchange the voltages (E and $-E$), for net negative feed-back around the "position" loop.



III.76
II.1
to
II.4
II.41
III.49
to
III.53
III.74
III.75

III.77 SIMPLE ONE-AMPLIFIER CONTROLLER WITH INDEPENDENT ADJUSTMENTS. This controller circuit provides standard three-term proportional-derivative-integral control capability in a compact adjustable one-amplifier form convenient for many laboratory applications. Particularly useful is the ability of the bounding circuit (see I.25), to prevent "integrator wind-up" during periods of large error. As the sign of the error (input, e_1) reverses, the output comes out of the bound immediately and begins to control the process.

In essence, this circuit is a combination of the augmenting differentiator of II.20, and the augmenting integrator of II.11.

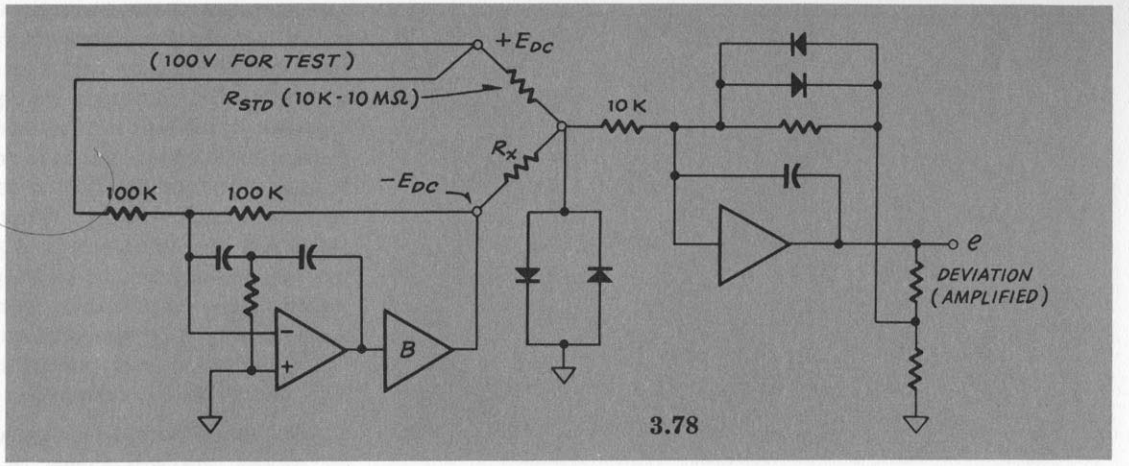


III.77
I.40
to
I.43
II.10
to
II.21
II.44
II.45

III.78 PRECISION COMPARATOR. The unity-gain-inverter circuit in the lower left of the drawing accepts the $+E_{DC}$ test voltage, and creates its exact mirror image ($-E_{DC}$) to drive the lower end of R_x, the unknown. If $R_x = R_{STD}$, and if the inverter feedback divider is perfect, then the input to the null-deviation detector circuit will be at zero, exactly. The output, e, of the detector will also be zero.

The detector output is bounded (to protect its meter load and avoid saturation) and its input is diode-clamped against such unnatural conditions as removal of R_x. For *small* deviations, this detector circuit is fairly linear, and may be calibrated for percent of deviation, or ohms of deviation.

The null (match) point is unaffected by variations in E_{DC}, because of the "mirror-image" behavior of the inverter, but the calibration sensitivity is still directly proportional to E_{DC}.

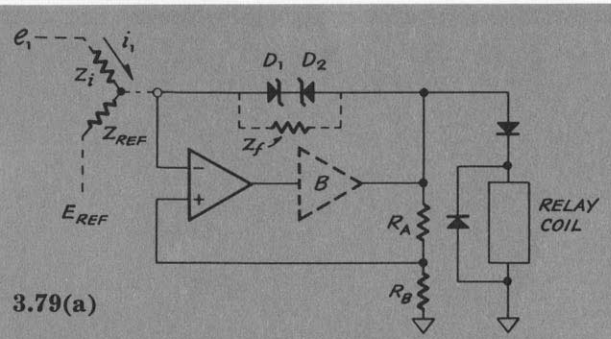


3.78

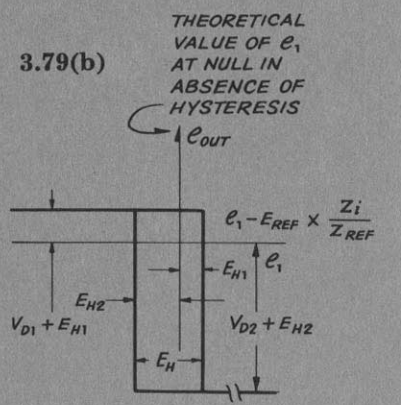
III.78
I.25
II.1
to
II.4
II.30
II.41
III.43
to
III.48
III.58

III.79 METERLESS "METER RELAY." This circuit simulates a meter relay—that is, a moving coil relay in which the pointer of the meter in some way carries a contact, or has the ability to cause contact closure when its deflection reaches a specified value, in either direction around a center-zero position. Let us begin our analysis by mentally grounding the positive input terminal of the amplifier, instead of connecting it to the output divider R_A, R_B. Now the circuit will compare the potential at the junction of Z_1 and Z_{REF} with ground, and any appreciable deviation, however small, will cause the output to bound at the voltage of the back-to-back zeners used as the feedback elements in order to maintain the summing point at zero. This swing to the bound condition will certainly cause the relay to operate. If the input signal range is small compared to noise (in e_1, e_n, or i_i) the output of the amplifier will swing wildly, which will in turn cause the relay to "chatter."

If, however, we now restore the positive input terminal to its proper tap on R_A, R_B, the positive feedback that results produces a "hysteresis" action quite similar to that produced by magnetically aided meter relay contacts—that is, once the circuit crosses the threshold, the positive feedback forces it the rest of the way, and holds it in the bound state until such time as the input signal comes back well beyond the forward threshold. By adjusting the positive feedback divider, the width of this hysteresis region may be varied. Note that the diodes in series with the relay are often not necessary, and should be omitted if bi-directional action is desired. Note also that the input signal need not be a voltage source, but may be a pure current source. The booster may not be required if the amplifier has sufficient current capacity to drive the relay. Figure (b) shows a typical hysteresis of the kind we have described. Useful design equations are given under the schematic.



3.79(a)



Z_f = Effective value of impedance when zener diodes are non-conducting

factor K by which the normal gain, $\Delta e/\Delta e_i$, is modified by feedback (+ for positive):

$$K = \frac{1}{1 - \underbrace{\left(\frac{R_B}{R_A + R_B}\right)\left(1 + \frac{Z_f}{Z_i} + \frac{Z_f}{Z_{REF}}\right)}}$$

when this term $\geqq +1$ denominator goes through zero and hysteresis will occur

$$\frac{\Delta e}{\Delta e_i} = -\frac{Z_f}{Z_i} \times K\left[\underbrace{\frac{1}{1 - \frac{K}{A}\left(1 + \frac{Z_f}{Z_i} + \frac{Z_f}{Z_{REF}}\right)}}\right]$$

error factor usually $<0.01\%$ when $K = 1$

Referred to signal, e_i, the total width in volts of the hysteresis loop, E_H, is:

$$E_H = (V_{Z1} + V_{Z2}) \times \frac{R_B}{R_A} \times \left(1 + \frac{Z_i}{Z_{REF}}\right)$$

III.79
I.25
I.27
I.44
I.45
II.1
to
II.4

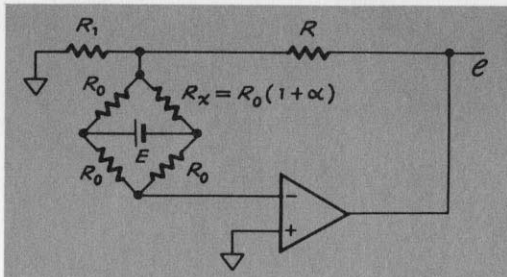
pages 100 & 101

III.80 BRIDGE AMPLIFIERS. Because of their inherent symmetry and self-duality, bridges are fascinating subjects for study. Here are four (out of many) popular approaches to the use of Operational Amplifiers with resistance bridges.

All but (d) are primarily used as small-signal (nulling) bridges, because of their nonlinearity in response to large deviations. Circuit (a) is the most convenient, because it may be used with a single-ended (possibly chopper-stabilized) amplifier, the sensitivity is independent of bridge impedance level (permitting indifference to common-mode bridge temperature variations), and the readout is proportional to the true voltage difference developed across the bridge—*but* the bridge-excitation supply must float . . . often a significant limitation. Circuits (b) and (c) are "galvanometric" bridges, in which the opposing corners are maintained at equal potential by the amplifier, which reads out the voltage required to establish the balancing differential current. If an accurately-tapped, stable power supply is available, (c) is better; otherwise (b) serves well, but one must choose an amplifier type insensitive to the potentially-large common-mode level. Bridge (b) could be read out potentiometrically by the use of circuit III.39, with consequent first-order independence of impedance level, for both scaling and common-mode rejection.

Bridge (d) is inherently linear, even for very large deviations; and it is used with a grounded supply—two major virtues. A further advantage of (d) is that its output is independent of bridge impedance level, as is that of (a). However, because (d) does not provide amplification, the measurement of small resistance changes may be difficult, unless another amplifier is added to increase sensitivity. Also, it is a 5-terminal "interrupted" bridge—one corner has been opened. This circuit configuration may not be realizable using a conventional bridge as the base for constructing circuit (d).

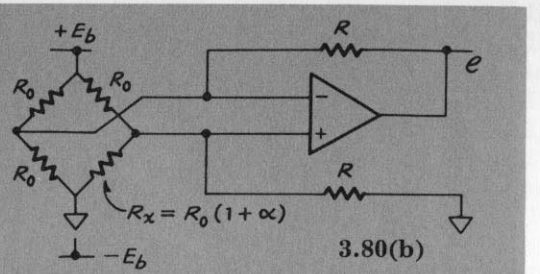
III.80



3.80(a) FLOATING SUPPLY

$$e = \left(1 + \frac{R}{R_1}\right) \frac{\alpha}{4\left(1 + \frac{\alpha}{2}\right)} E$$

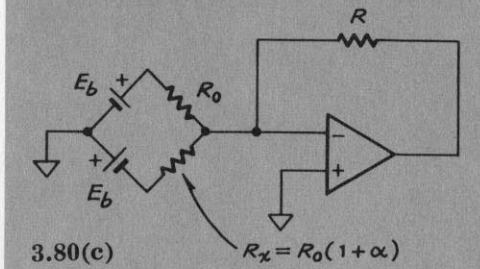
$$\left(\text{Linear for } \frac{\alpha}{2} \ll 1\right)$$



3.80(b)

GROUNDED OR FLOATING SUPPLY, NOT NECESSARILY BALANCED

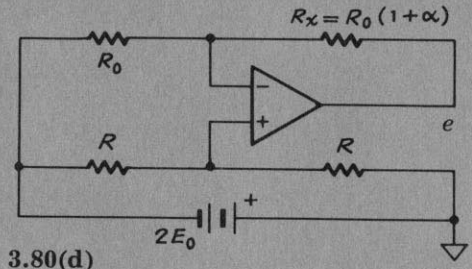
$$e = \frac{R}{R_0} \frac{\alpha}{1+\alpha} \frac{E}{1 + \frac{R_0}{2R}} \frac{1}{2} \quad \text{(Linear for } \alpha \ll 1\text{)}$$



3.80(c)

GROUNDED BALANCED SUPPLY

$$e = \frac{R}{R_0} \frac{\alpha}{1+\alpha} E \quad \text{(Linear for } \alpha \ll 1\text{)}$$



3.80(d)

5-TERMINAL BRIDGE, GROUNDED SUPPLY LINEAR DEVIATION

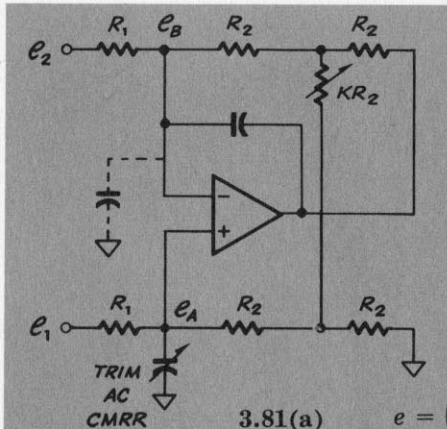
$$e = \alpha E_0 \quad \text{(No linear approximation)}$$

III.81 ADJUSTABLE-GAIN DIFFERENCE AMPLIFIER. By using differential form of the Tee network (I.26), the gain of the difference amplifier (II.5) may be widely ranged by adjusting only a single resistor—KR_2 in (a). The common-mode rejection of the circuit is independent of this resistor; indeed, if the same (common-mode) voltage is applied to each input, and if all the resistors are symmetrically matched, the output will be zero.

Since the effect of K on gain is far from linear, gain variation with the rotation of a (linear) rheostat is also nonlinear (b). Linearity can be improved by putting a fixed resistor in series with the rheostat. This expedient will increase the gain at the minimum setting, for a given resistor ratio. An alternative is to use a multi-position switch to select discrete values of KR_2, and thus specific calibrated gains (b).

The trimming capacitor shown from the positive input to ground may be necessary to ensure good common-mode rejection over a substantial range of frequencies. This capacitor should be adjusted to compensate for the net effect of all of the capacitances at the negative summing point. If the common-mode voltage varies substantially, an amplifier having a small and linear common-mode error should be used, so that trimming one of the R_1 resistors will provide almost perfect rejection. A CMRR greater than 10^6 can be achieved at low and moderate frequencies with (a), if the inputs are driven from low impedance sources.

III.81



3.81(a)

$1+\frac{1}{K}$	K
1	∞
2	1
5	1/4
10	1/9
20	1/19
50	1/49
100	1/99

3.81(b)

$$e = \left(1 + \frac{1}{K}\right) \frac{2R_2}{R_1} (e_1 - e_2)$$