III.9 CONSTANT-CURRENT REGULATOR. In this circuit, a unipolar derivative of the Howland circuit, a follower with gain is used to add or subtract a correcting current to or from (larger) unregulated current derived directly from the power supply through R_3. It must be appreciated that this circuit depends for its accuracy on the stability of the +15 volt supply with respect to signal ground . . . as well as the accuracy and stability of R_3,* and the accuracy and stability of the other resistors in the feedback networks.

Let us deal first with the diodes connected across the amplifier input terminals. They function merely as input signal clamps, preventing excessive input voltage in the event that the load is disconnected or suddenly becomes a very high impedance.

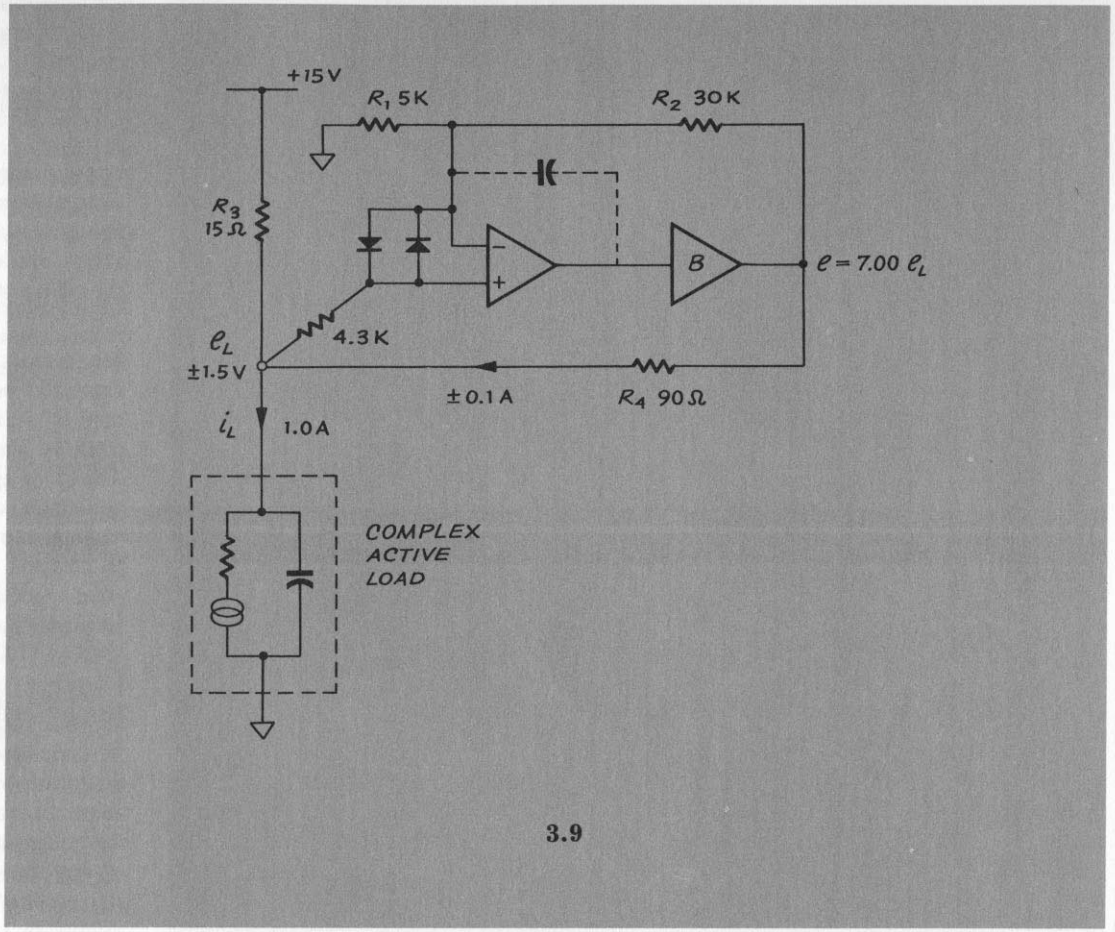
If $R_2 = aR_1$, and $R_4 = aR_3$, then it can be shown that in the ideal case the load current is simply given by $i_L = 15/R_3$.

The sources of error, beyond the resistor contributions and the power supply stability mentioned above are as follows: Input current to the amplifier; Voltage offset and drift; and CME and finite-gain error factors.

The booster current ratings should be selected to match the requirements of the load, and the output voltage capability of the booster must be such that it can furnish that current through R_4, when R_4 is made equal to aR_3.

The 4.3 kΩ resistor shown in series with the positive input terminal in our example, is so proportioned (with respect to R_1 and R_2) as to reduce the effect of current offset. It also prevents excessive current in the clamping diodes.

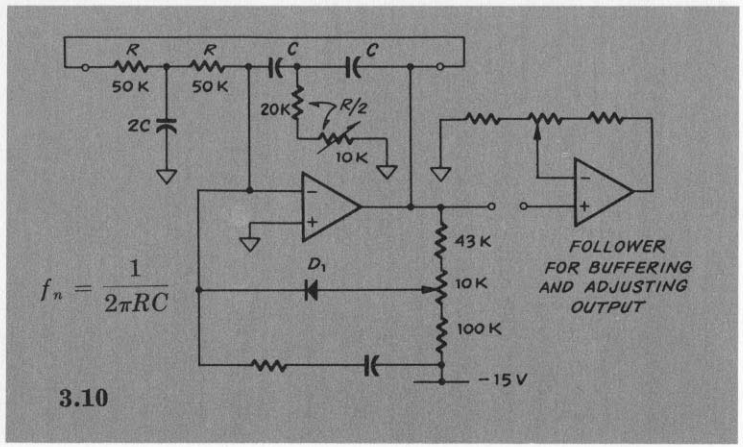
*Establishing high accuracy and holding high stability in a 15Ω 15-watt resistor may not be as easy as it sounds. Extreme derating helps, of course.



3.9

III.9
I.34
I.46
II.1
II.2
II.3
II.4
II.5
III.3
III.4
III.5
III.6
III.7
III.8

III. 10 SINE WAVE OSCILLATOR—TWIN-TEE. This circuit is almost identical to the double integrator of II.14. At some frequency, when $R/2$ is exactly 25 kΩ, the phase shift around the feedback loop is exactly 180°, so that the total phase shift, including the amplifier's sign inversion, is 360°, and the circuit is zero damped. A small increase in $R/2$ will encourage oscillatory buildup. (Note that the accuracy of frequency and zero-ness of damping are encouraged if f is well within the amplifier bandwidth—see I.17 and I.41.) Without the damping network at the lower right of the diagram, sustained oscillations would build up between the extremes of saturation of amplifier—producing a distorted output. Beyond a selected threshold, a damping path through the biased diode, D_1, maintains a stable, sinusoidal oscillation at a selected, adjustable value of peak-to-peak output. Adjusting the threshold will adjust the output. The voltage at which the damping circuit limits the amplitude is a direct function of power supply voltage, and is temperature-dependent because the diode forward voltage drop is. The series RC circuit from summing point to power supply can be proportioned for rapid startup yet minimal interference with normal operation. The output impedance of this circuit is, unfortunately, high near f_n; therefore, this circuit would benefit from the addition of a follower or inside-the-loop booster. The follower choice allows adjustable output, as shown.

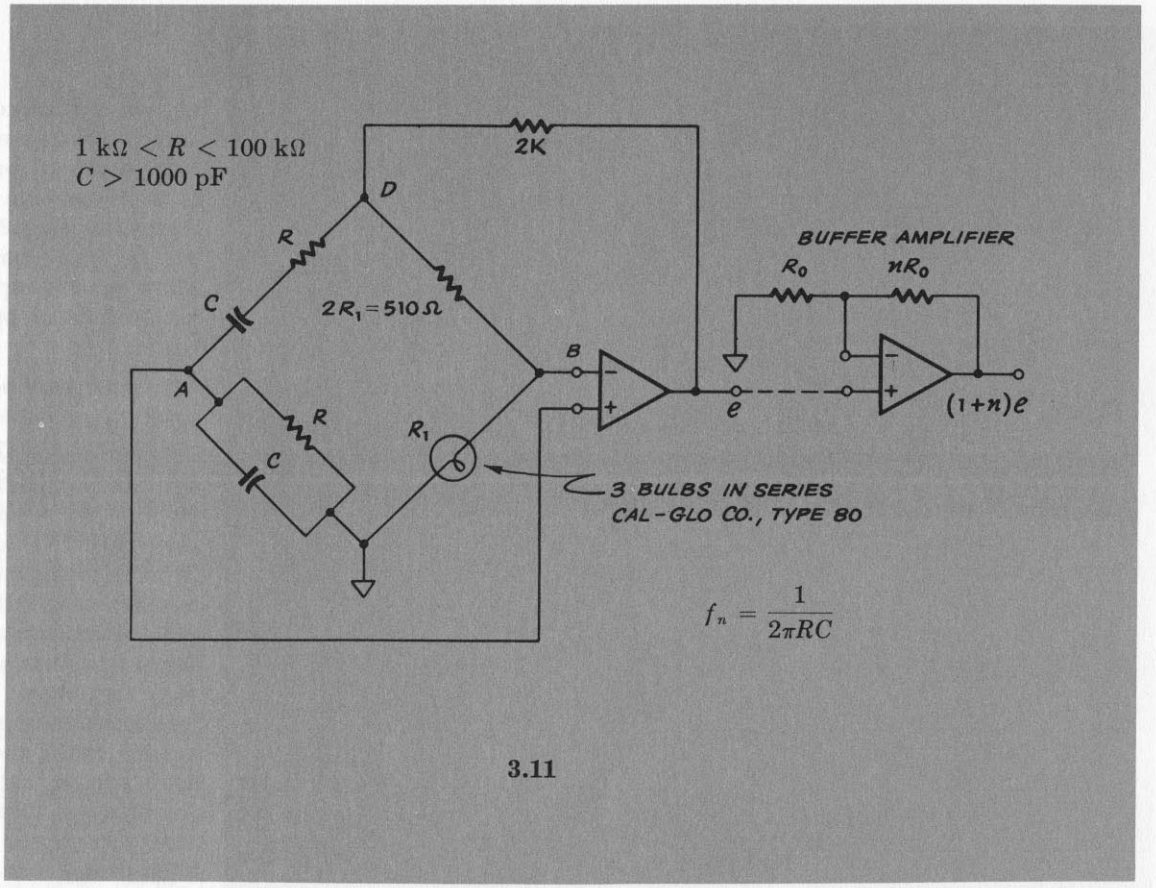


3.10

III.10
I.7
I.17
I.18
I.26
I.40
to
I.43
II.12
III.11
to
III.14

III.11 SINE WAVE OSCILLATOR (Wien Bridge). At the frequency f_n, the voltage at A is ⅓ of that at D, and in phase with it. The voltage at B is approximately the same, varying from slightly more than to slightly less than that at A, as the average power dissipated in R_1 decreases. This variation at point B acts to regulate (without distorting) the output amplitude, which amplitude can be adjusted by setting R_2 appropriately. At balance, there is no net feedback; hence the output impedance is high equalling that of the open-loop amplifier. As noted in III.10, an adjustable-gain buffering amplifier could be used as a convenient way to adjust the output amplitude.

R_1 actually consists of three incandescent lamps in series, operated below their visible-illumination current level. Because the regulating action of these lamps is primarily a thermal effect, the output amplitude of this circuit is inherently temperature-sensitive and it must be temperature-compensated (III.14) or oven-stabilized, if amplitude stability against ambient temperature is required. Over reasonable ranges, neither the amplitude nor the frequency of oscillation are affected by power supply variations.



3.11

III.11
I.7
I.17
I.18
I.26
I.40
to
I.43
II.12
II.21
III.10
III.12
III.13
III.14

III.12 TWO-PHASE OSCILLATORS. Circuit (a) cascades a non-inverting integrator with a bounding inverting integrator, in a feedback loop represented by the differential equations:

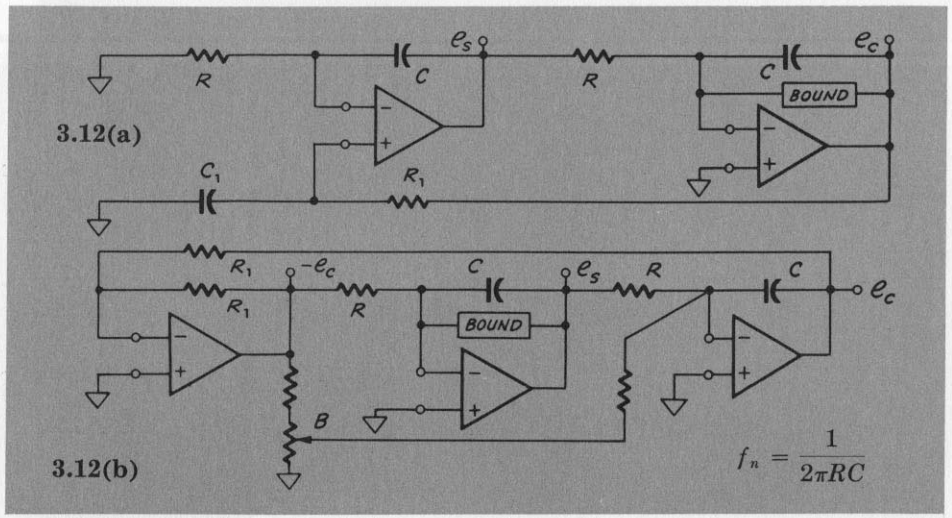
$$RC\frac{de_s}{dt} = e_c \qquad RC\frac{de_c}{dt} = -e_s \tag{3-3}$$

The time constant R_1C_1 is deliberately made slightly larger than RC, so that the circuit is slightly unstable; the bound stabilizes the amplitude without greatly distorting the waveform of e_c.* Note, the two outputs are 90° out of phase.

$$e_s = E\sin\frac{t}{RC} \qquad e_c = E\cos\frac{t}{RC} \tag{3-4}$$

Circuit (b) is similar, but employs inverting amplifiers only, thus enhancing its usefulness in very slow, very fast, and computor-bound applications, . . . advantages implicit in the wider choice of available single-ended amplifiers. Positive feedback is provided at B to cause the oscillations to build up until bounded.

*Because of the integration that operates upon e_c, e_s will be nearly a perfect sinusoid.



3.12(a)

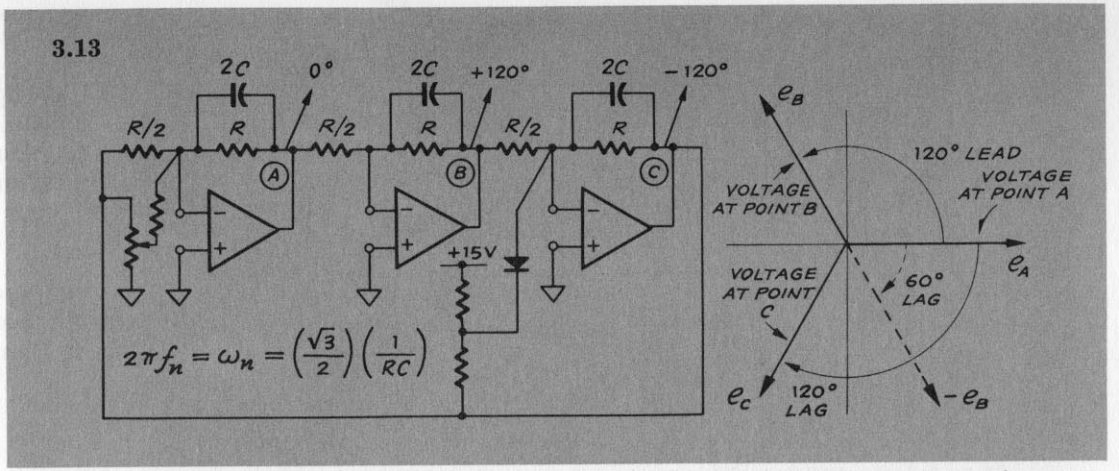
3.12(b)

III.12
I.7
I.17
I.18
I.26
I.40
to
I.43
II.12
II.21
III.10
III.11
III.13
III.14

pages 68 & 69

III.13 3-PHASE OSCILLATOR. This circuit produces three signals at the same frequency (f) but phase-shifted 120° apart, one from the other. The total phase shift around the loop, at f, is 360°, each of the three identical "unit lags" contributing an *effective* 120° by combining its 60° lag and the normal polarity inversion of the amplifier, as shown in the vector diagram.

Note that the biased-diode amplitude-limiter circuit used previously in III.10 and III.12 is also employed here, as is an adjustment to permit setting the loop phase-shift just to the point of oscillation.

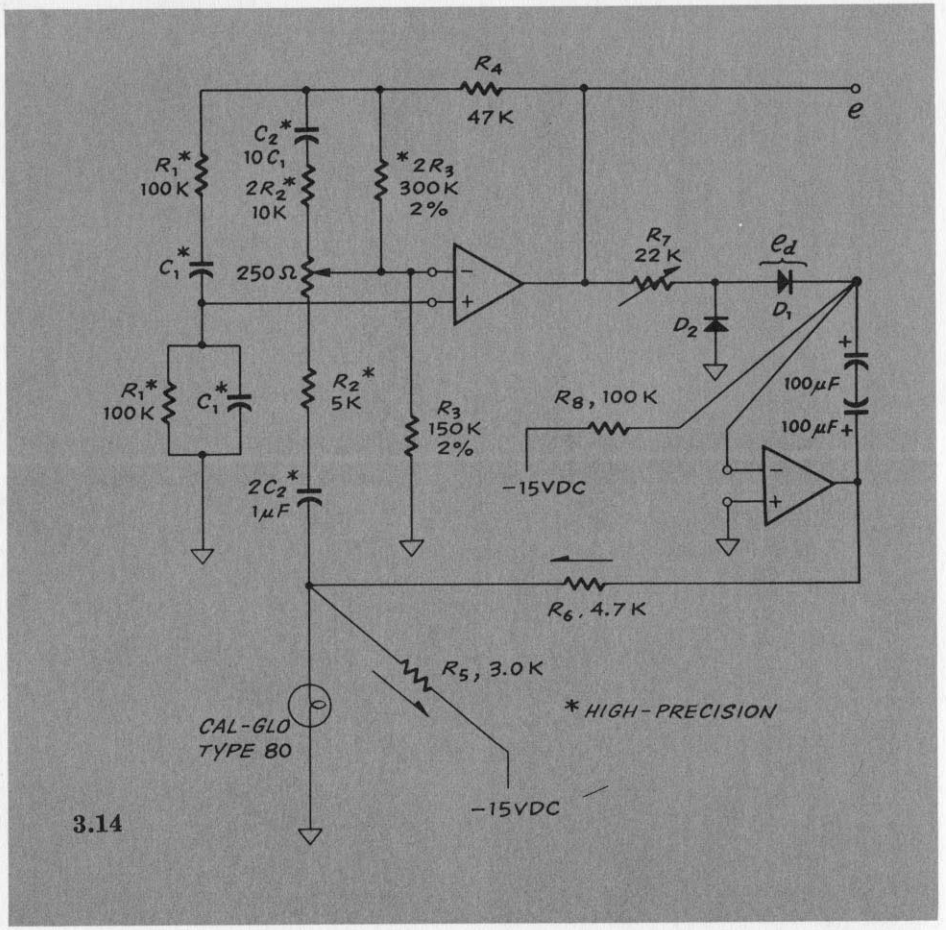


III.13
I.7
I.17
I.18
I.26
I.40
to
I.43
II.12
II.21
III.10
III.11
III.12
III.14

III.14 WIEN BRIDGE OSCILLATOR—AMPLITUDE-CONTROLLED. Very precise and stable control of the amplitude of a sine-wave Wien-bridge oscillator is achieved by the circuit shown here. The amplifier to the left oscillates when the positive feedback fraction of the output terminal exceeds the negative feedback fraction. The magnitude of the negative feedback signal is dependent upon a voltage divider, one element of which is an incandescent lamp. As the effective (RMS) current through the lamp increases, its resistance increases, increasing the negative feedback, reducing the amplitude of oscillation. The current in the lamp is derived from three sources: the current through R_6 (DC) the current through R_5 (DC from the −15 volt supply) and the current through C_2, R_2, etc. divider (AC at the oscillator frequency).

An integrator circuit drives R_6. The input to this integrator is a half-wave-rectified current derived from the output sine-wave through R_7 and D_1. (D_2 clips the negative half-cycle.) By so proportioning R_7 and R_8 that the average net input current at the summing point of the integrator is effectively zero when the output amplitude is at the desired value, and by adjusting the time constant of the integrator to filter the rectified sine-wave effectively, the output voltage of the integrator will be essentially DC, and will be essentially zero when, and only when, the output amplitude is correct.

If the output amplitude should fall, the integrator output would swing positive, driving a positive current through R_6, reducing the net current through the lamp, since this current would furnish some of the current demanded by R_5. If the output amplitude should rise, the integrator output would go negative, increasing the current through the lamp. Both actions will be seen to operate so as to regulate the sine-wave output. Since the gain of the integrator is quite high, it permits only a very small variation in the output amplitude. To avoid low-frequency oscillation, or "hunting," the integrator time constant must be somewhat longer than the lamp time constant.

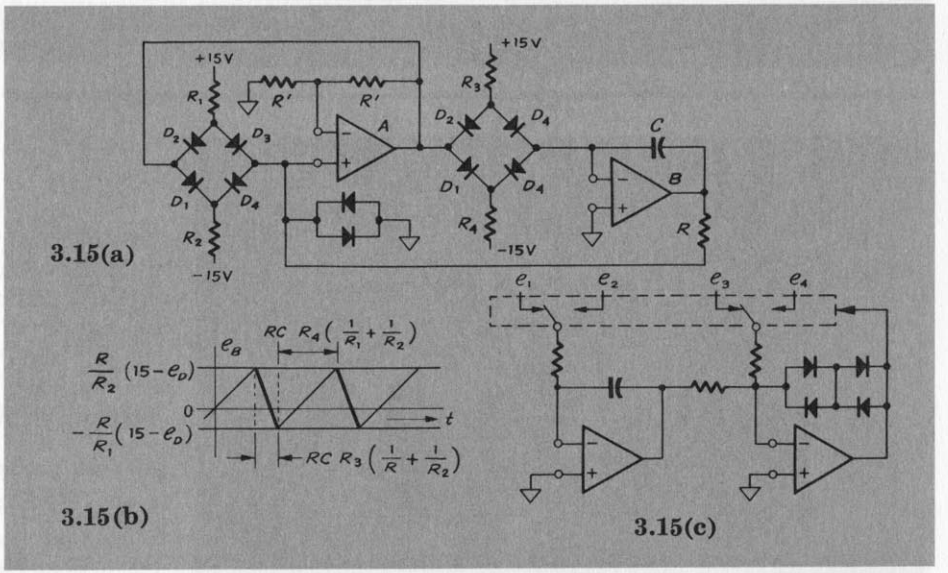


III.14
I.7
I.17
I.18
I.26
I.40
I.41
I.42
I.43
II.12
II.21
III.10
III.11
III.12
III.13

III.15 PRECISE TRIANGULAR-WAVE GENERATOR. The output of amplifier A switches between ±1 volt (approximately) levels determined by the two diodes clamping the positive input to ground. Amplifier A drives two current gates (diode bridges) so arranged that when e_A is positive, D_1 and D_3 conduct, while D_2 and D_4 block. This circuit condition connects +15 V through R_3 to the summing point of amplifier B, an integrator. The output of B is, in this mode, a negative-going ramp, the magnitude of which continues to increase until it is large enough to drive the input of amplifier A negative, causing the output of A to flip. (The switching speed can be extremely high, if amplifier A is fast.)

After amplifier A flips, the behavior of the circuit is reversed throughout: −15 V is connected, through R_4, to the summing point of integrator B; the output of B is a positive-going ramp, continuing until it drives the input of A positive, causing the output of A to flop back to the state it had at the start of this description.

This circuit can perform well at frequencies ranging from 10^{-3} Hz to 10^{6} Hz, depending upon the choice of amplifier, diode, and impedance levels.



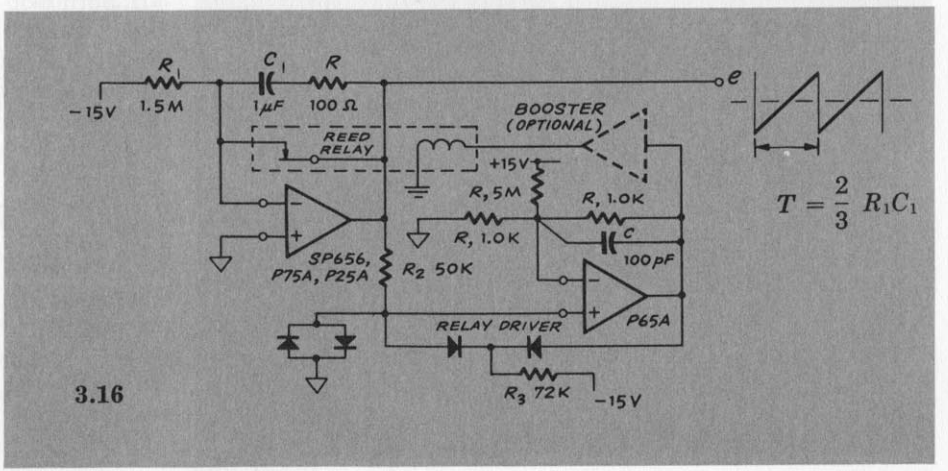
3.15(a)

3.15(b)

3.15(c)

III.15
I.25
I.27
II.10
II.11
II.12
II.39
II.41
II.43

III.16 PRECISE SAW-TOOTH GENERATOR, LOW FREQUENCY. The input signal to the integrator is the −15 V reference. When the output voltage has reached +10 volts, the current through R_2 balances the current through R_3, the voltage at the positive input of the relay driver becomes positive, and the relay driver switches its output from (about) −1 volt to (about) +1 volt, driving the reed relay to reset the integrator. (If a Philbrick SPREL is used, no booster is necessary, as it requires only a +1 volt or −1 volt logic level to activate a high-reliability reed relay.) When e has arrived at zero, the relay driver senses this (because R_3 has been effectively disconnected) and its output switches back to −1 volt, removing the excitation from the reed relay reconnecting R_3, and starting the cycle again.



3.16

III.16
I.24
I.25
II.10
II.11
II.12
II.41

pages 70 & 71

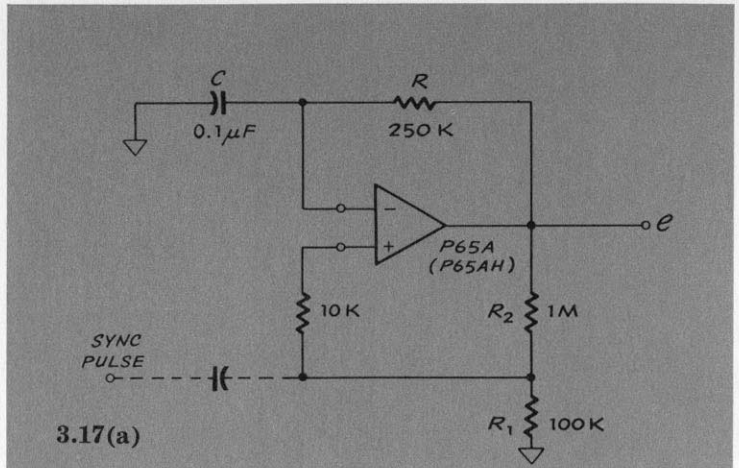
III.17 ASTABLE (FREE RUNNING) MULTIVIBRATOR. This circuit has two metastable states, in one of which the output is at positive saturation, and in the other of which the output is at negative saturation. The circuit regularly shifts from one to the other of these two states; hence, the output is a square wave, the period of which is determined by the values of R and C, and by the feedback ratio established by the output divider that drives the positive input terminal.

Assume that the amplifier saturates symmetrically at ± 12 volts output, and let us begin our analysis by assuming that the circuit has been in its positive-output state long enough for the capacitor C to have charged sufficiently so that the potential at the negative input terminal has just approached the potential of the positive input terminal. At (or immediately after) the instant at which they become equal in potential, the circuit will switch, very rapidly, from its positive-output state to its negative-output state.

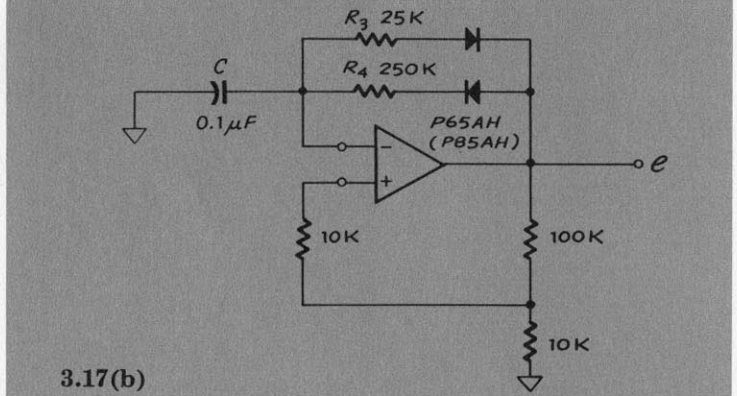
In the new state, the positive input terminal is held at a potential of about -1.1 volt. The negative input terminal is still connected to the capacitor C, which has had no opportunity to change its voltage, and is still charged to $+1.1$ volts, because the switching action occurs essentially instantaneously. The circuit remains locked, therefore, in the negative-output state for the period of time that is required for C to discharge and re-charge to approximately -1.1 volts, through R. This time interval, obviously, is dependent on the product of R and C: The fact that the voltage across C must change by a total of 2.2 volts is determined, of course, by the 1 : 11 ratio of the output divider . . . if the divider had had a different ratio, the voltage difference through which the potential of the negative terminal would have had to swing would have been different, also. The exact expression for the operating frequency is:

$$f = \frac{1}{2RC \ln\left(1 + 2\frac{R_1}{R_2}\right)} \qquad (3\text{-}5)$$

Note that if, during the time that C is charging to the new value required for the circuit to switch states, a large enough pulse (of the opposite polarity to the output) is fed into the synchronizing terminal, the circuit will immediately change state. The frequency is essentially independent of loading or power supply voltage.



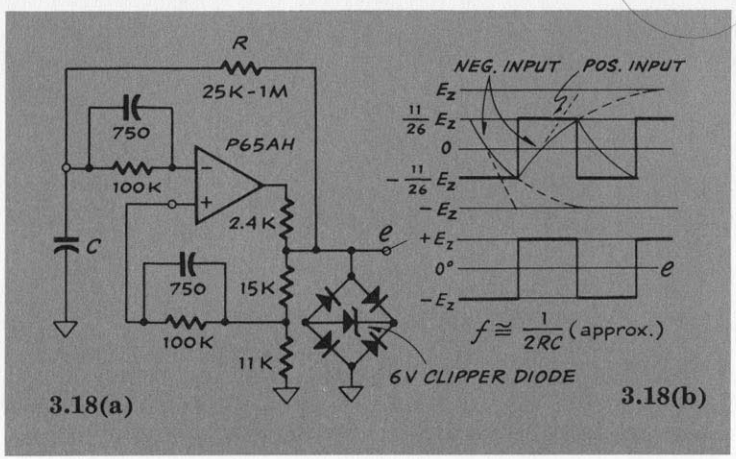
3.17(a)



3.17(b)

III.17
II.1
to
II.4
III.18
to
III.21

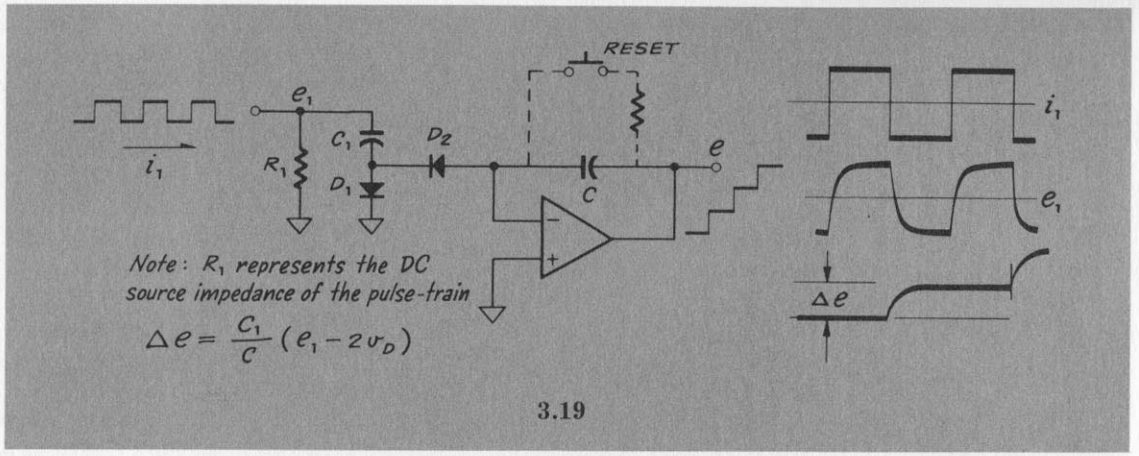
III.18 SIMPLE SQUARE WAVE GENERATOR. The output of this circuit is limited by a pair of back-to-back zener diodes which, beyond their avalanche voltage limits, exhibit such low impedance compared to the output impedance of the circuit that they ensure generation of a clean, flat-topped wave by "clipping" the output below the amplitude at which overshoot, ringing, or rounding can occur. The positive input terminal of the amplifier is connected to an output divider that provides positive feedback. Suppose that the output is at $+E_Z$. The positive input terminal will be at about $+{}^{11}\!/_{26}E_Z$. Capacitor C will be charged via R until the voltage at the negative input exceeds $+{}^{11}\!/_{26}E_Z$. Because of the amplifier's high gain, the output e will "flip" to $-E_Z$. The positive input will be at $-{}^{11}\!/_{26}E_Z$, maintaining the saturated condition. The capacitor C will start to charge exponentially in the negative direction (from $+{}^{11}\!/_{26}E_Z$ to $-E_Z$), and the output will flip once again when the output crosses $-{}^{11}\!/_{26}E_Z$ starting the cycle again. The positive feedback aids in driving the circuit more rapidly to saturation; the 2.4 kΩ resistor limits the amplifier current during clipping to within 2 mA.



3.18(a) 3.18(b)

III.18
II.1
II.2
II.3
II.4
III.17
III.19
III.20
III.21

III.19 STAIRCASE GENERATOR. This circuit must be driven from a current source. Each positive upstep charges C_1 through D_1. The corresponding negative downstep discharges C_1 (in parallel with the source resistance, if DC coupled) through R_1 and D_2, drawing current from the summing point. This current must, of course, come from the capacitor C. Thus, a series of current pulses are drawn through C, and the voltage across C (the output voltage, e) increases by the time-integral of each of those current pulses. If the R_1C_1 time constant is short compared to the pulse-to-pulse spacing, the output wave form will resemble a staircase, as shown. The circuit may be reset by means of a pushbutton . . . or if manual reset is not practical, by means of a relay operated from the generator output, at some critical value of time or output voltage—the last desired "step."



3.19

III.19
II.1
to
II.4
II.10

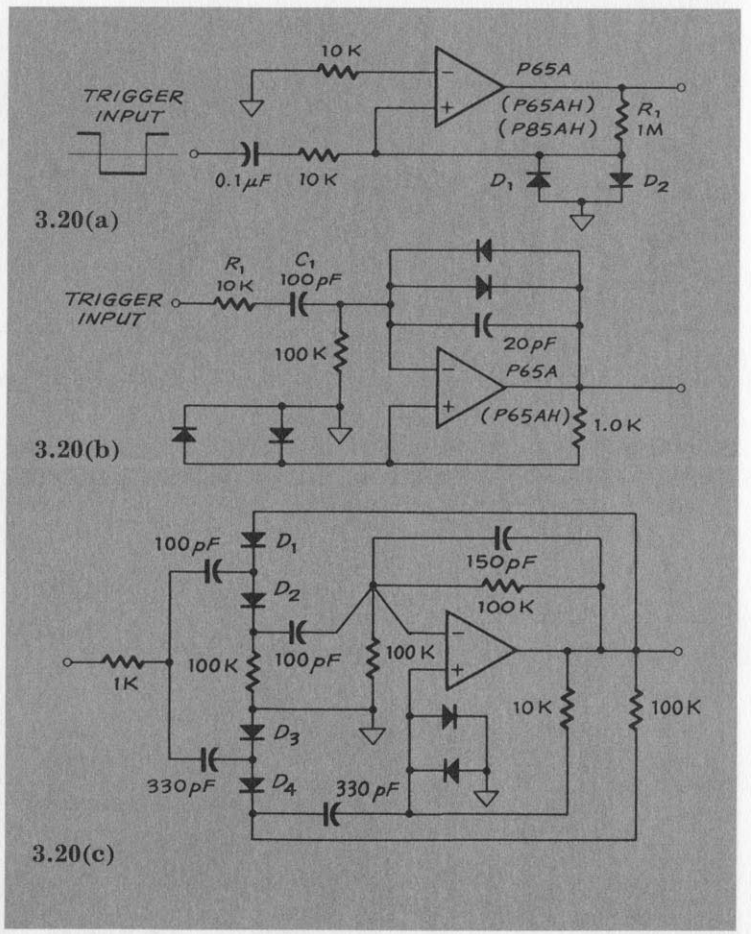
III.20 BISTABLE MULTIVIBRATOR. These circuits are different forms of bistable multivibrators, frequently miscalled "flip-flops." Each has two stable states, in either one of which it will remain indefinitely, unless and until a step or pulse signal of appropriate polarity is fed to the input, to change its state.

In the basic (saturating) circuit of (a), the output is saturated at either its positive or its negative limit (typically ±12 V) because of the positive feedback to the positive input through R_1. A small step of opposite polarity applied to the trigger input will reverse the polarity of the voltage at the positive input. Within a millisecond the output will switch to its other limit, and the positive feedback via R_1 will keep it there, until a step of the opposite polarity is applied to the trigger input. Square waves, pulses, sine-waves, from 1.0 V to 20 Vp-p, and from very low frequency to a few hundred cycles per second will activate the circuit.

The circuit shown in figure 3.20(b) uses diode bounding to prevent saturation. Its two stable output states are +1 V and −1 V. It is more sensitive than the circuit in 3.20(a), and will respond faster, even to smaller input signals. With the values shown, square waves, etc., as small as 0.1 Vp-p, and as fast as 20 kHz will reliably switch the state of the circuit. If the existing trigger signal is substantially larger than 0.2 Vp-p, R_1 may be increased and C_1 decreased, to minimize the loading on the trigger signal source.

The circuit in figure 3.20(c) is a special kind of bi-stable device that changes state only every other cycle of input, and thus can be used as a frequency divider or scale of two counter. The diode steering networks $D1$–4 insure that negative-going steps are steered alternately to the positive and negative inputs. With the values shown, square waves of 1 to 4 Vp-p, and from very low frequencies to 10 kHz will actuate the circuit.* Of course, any number of (c) circuits may be cascaded, to achieve (binary) frequency division or counting with moduli of 2, 4, 8, 16, or more.

*with outputs up to 5 kHz.



3.20(a)
3.20(b)
3.20(c)

III.20
III.17
III.18
III.21

pages 72 & 73

III.21 MONOSTABLE MULTIVIBRATOR. A monostable multivibrator has only one stable state. However, immediately following the introduction of a trigger pulse, it will change state and stay in the new "metastable" state for a predetermined period, and then return to its stable state.

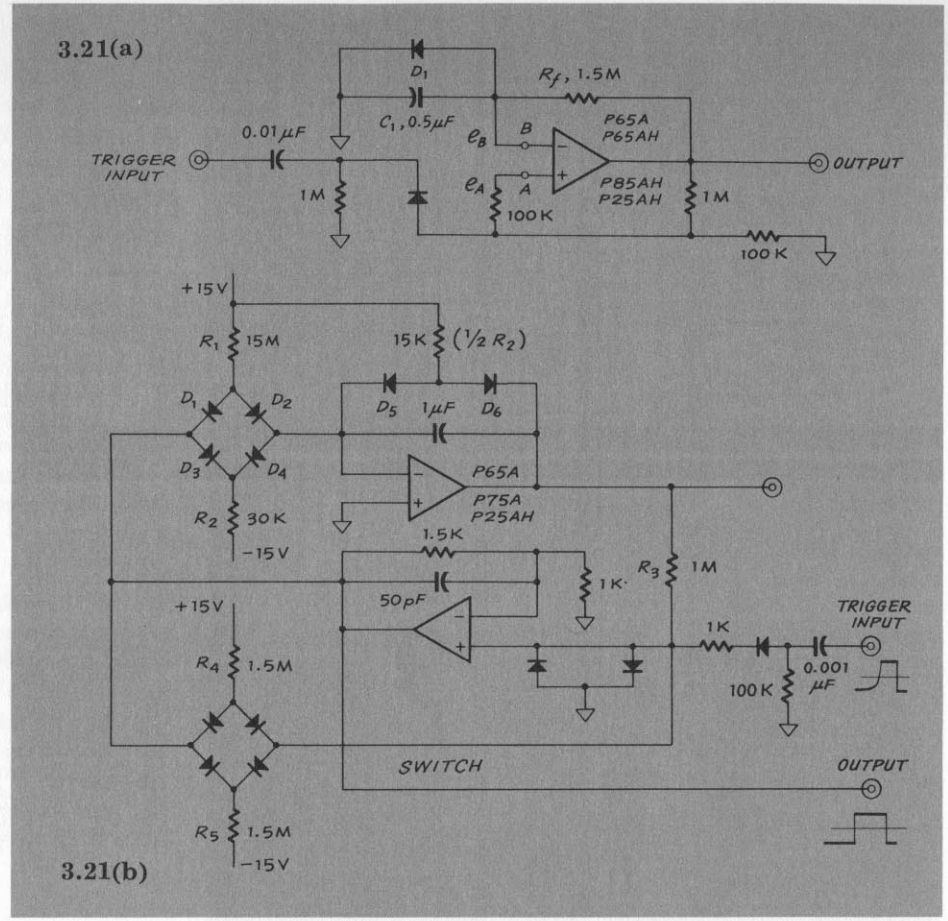
In circuit (a), the output states are plus and minus saturation (+12 V and −12 V, typically). When a negative step is applied to the trigger input (3 to 8 volts, typically) the output switches from its stable state at +12 V to −12 V, and R_f begins to charge C_1 toward −12 V. When the voltage on C_1 reaches a point at which $|e_B| > |e_A|$, the amplifier output voltage switches back to +12 V, and will remain there until the circuit is triggered again. Meanwhile, the voltage on C_1 starts to charge back up from −1 V to +12 volts, but is clamped at about +0.6 V, by D_1. Values of C_1 from 1000 pF to 10 μF and of R_f from 10 kΩ to 2 MΩ are suitable (for smaller values of R or C, a fast amplifier is recommended). With the values shown, the temporary state lasts about 1 second.

To obtain more predictable and "nearer-ideal" behavior, circuit 3.21 (b) is recommended. As in the nonsaturating flip-flop of 3.17(b), diode bounds are used to prevent saturation and improve response speed, trigger sensitivity, and stability. The circuit is a variation of the triangular-wave generator of III.15. In the stable state, the switch output is at about −1 VDC, and about 0.5 mA flows through D_4 and D_5. The integrator's output is bounded at about 0 V by D_5.

If a step signal of sufficient magnitude is applied to the trigger input, the output of the switch will go very quickly to +1 volt. Current then flows through R_1 and D_2, and the output of the integrator begins to ramp downward linearly. When it reaches −10 volts, the current through R_4 balances that through R_3, and the switch flips back to its permanent state of −1 V. This connects R_2, through D_4 resetting the integrator. Since R_2 can be much smaller than R_1, the reset can be accomplished quickly. Using the formula

$$\tau = 0.7R_1C \qquad (3\text{-}6)$$

for the component values shown, the output will be at +1.0 volt for 10 seconds. Substituting the value of R_2 for R_1 in equation (3.6) gives the formula for the reset time—in this example, only 20 milliseconds.



III.22 ACTIVE FILTERS. Operational Amplifiers can greatly simplify the design of high-performance signal filters, because they eliminate the need for inductors and for impedance matching. Furthermore, use of active filters can result in reduction of weight, size, and cost. Filters designed to satisfy sophisticated mathematical criteria can be realized without resort to "equalization" or trimming.

We shall, in the six sections that follow, attempt to summarize a two-part article published in *The Lightning Empiricist*, Vol. 13, 1 & 2, 3 & 4. Our necessarily brief considerations will include Operational Amplifier circuits for low-pass, high-pass, band-pass, and band-reject filters. Procedures for cascading quadratic filter stages will be presented, so that high-order "mathematically-designed" filters, in this case the Butterworth, may be synthesized.

In section III.28, we present (in highly-concentrated form) filter-design tables and a design example, all from the second part of the article, in which all these matters are examined in a less compressed, more detailed manner.