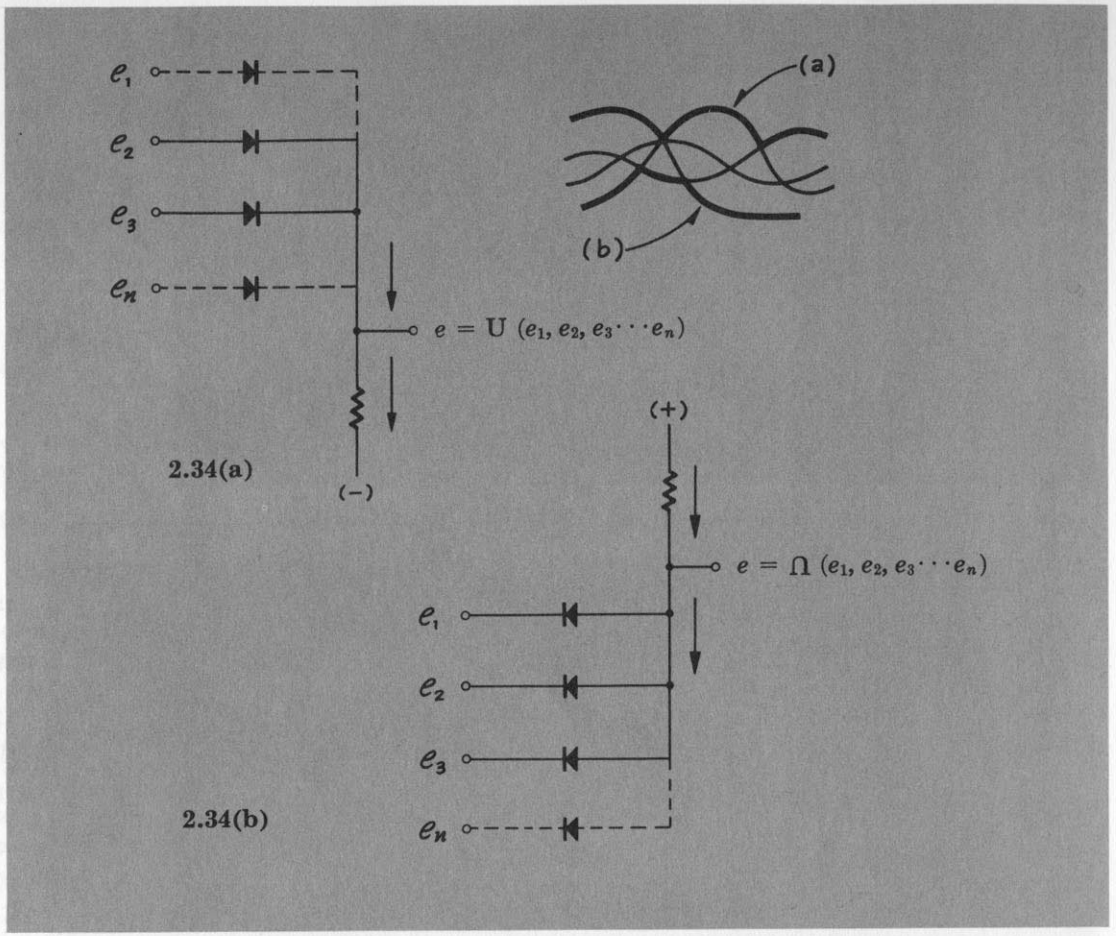
II.34 ELEMENTARY SELECTOR CIRCUITS. In circuit (a), the output voltage will always be at a potential equal to the highest of the input voltages, minus the diode drop. Thus, (except at near equality) only one diode can conduct at any instant, and at least one *must* conduct, assuming that the negative supply is lower in potential than any of the inputs may ever be. The resistor is proportioned to provide sufficient current to maintain adequate speed at the lowest voltage, yet limit the diode current to a specified maximum value for the *highest* voltage anticipated. For fast switching circuits, it is best to design for as much diode current as can comfortably be allotted to the Selector Circuit, so that stray capacitance effects are minimized.

The output of circuit (b) is always equal to the lowest input voltage, *plus* the diode drop. Once again, we assume that no input voltage can be higher than the positive supply, and we advocate designing for the highest comfortable diode current.

To achieve compensation that is independent of signal amplitude, even when the largest signal is very close to the return supply in magnitude, we recommend constant-current sources instead of resistors—see III.9.

The Upper Selector can be thought of as presenting at its output the most positive (or least negative) of its input voltages. As shown in 2.34(b) it presents to its output the "upper envelope" of all the input signals. Similarly, the lower selector presents to its output the most negative (or least positive) of its inputs, i.e., the "lower envelope" of all the input signals.



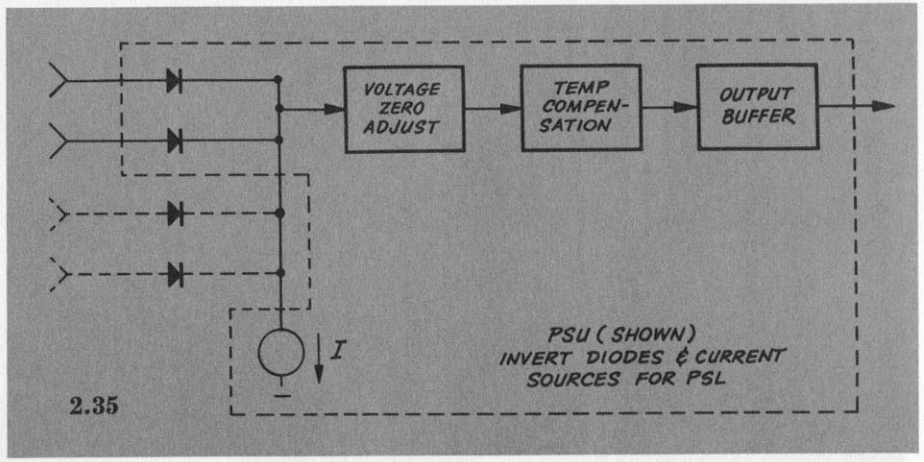
2.34(a)

2.34(b)

II.34
I.32
II.35
to
II.44
III.8
III.58
III.74
III.79
III.81

II.35 COMPENSATED SELECTOR. Although Selection is simple enough in concept, Selector circuits require certain refinements if their performance is to approach the ideal described in II.34.

These features are incorporated in Philbrick standard Upper and Lower Selectors, designated the PSU and PSL respectively. As shown here, a constant-current source (I) draws current from one or the other of a pair of diodes. The diodes are carefully matched at the current level established by the source. (If Selection among more than two voltage variables is required, the user may connect additional diodes of a recommended type to the selection node.) A voltage adjustment is included in the PSU/PSL design, enabling the user to establish zero output for zero input. This is done by grounding one input, leaving the other(s) open, and adjusting for zero output. The temperature compensation provided in the PSU/PSL design achieves thermometric insensitivity comparable to that of wirewound resistors. Finally, an output buffer amplifier aids error-free cascading of Selectors and provides adequate output-current capability for driving computor amplifier inputs.

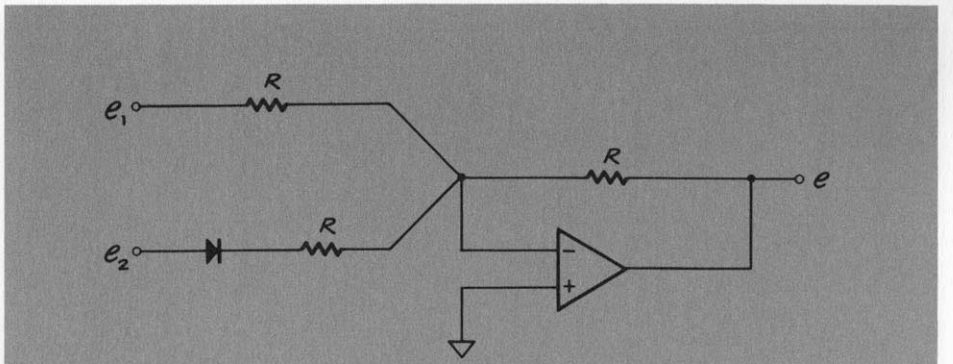


2.35

II.35
I.32
II.34
II.36
to
II.44
III.8
III.58
III.74
III.79
III.81

II.36 SIMPLE DUAL-MODE CIRCUIT. The only difference between this circuit and the inverting adder of II.3 is the diode in series with e_2. The basic rules must still be followed, of course, so that the sum of the input currents must equal the feedback current, and the summing point must be very close to ground—removed only by the residual null voltage. If both inputs are positive, the output is simply the negative of the sum of the two (ignoring the diode drop). On the other hand, if e_2 is negative, or if both are negative, the output is simply equal to the negative of e_1. This circuit, therefore, has two modes of operation, the choice of which depends upon the polarity of e_2 with respect to ground—with $e_2 > 0$, the circuit is an inverting adder; and, with $e_2 < 0$, it is merely a unity-gain inverter with respect to e_1 only.

In particular, if e_2 and e_1 are identical, the gain will be different for positive or negative input. Accuracy can be improved through use of a Selector circuit (see II.34, II.35), to reduce or eliminate the effect of diode drop.

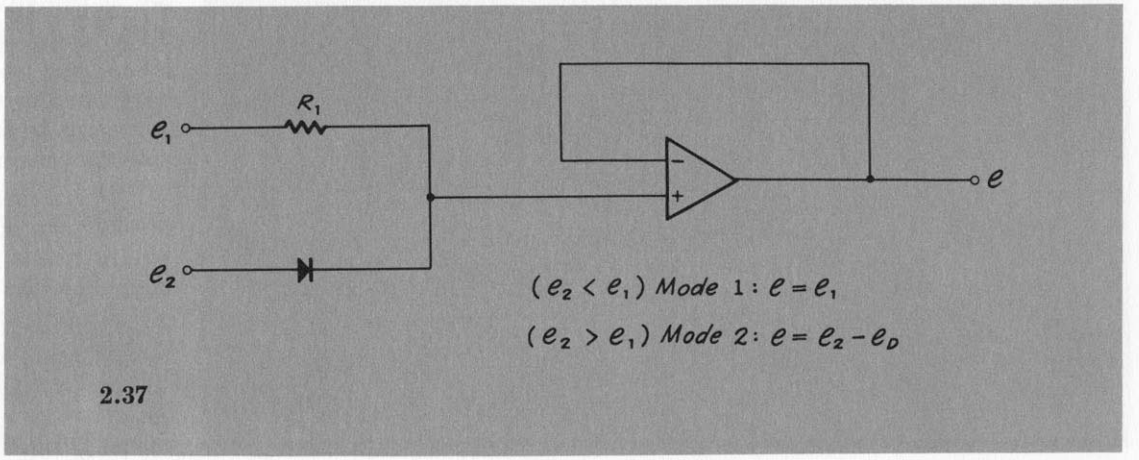


2.36

II.36
II.34
II.35
II.37
to
II.44
III.50
III.63
III.74
III.75
III.81

II.37 SIMPLE DUAL MODE CIRCUIT (Non-Inverting). This circuit will be recognized as a simple follower having two inputs. If e_2 is more positive than e_1, the output is equal to e_2, ignoring the diode voltage drop.

When e_2 is negative with respect to e_1, the output is equal to e_1, and the specific value of e_2 has no effect on the output, provided that it is sufficiently negative to render the diode leakage current negligible. (The path for this leakage current, by the way is mostly through R_1.) The accuracy and speed can both be improved by use of a Selector circuit.



2.37

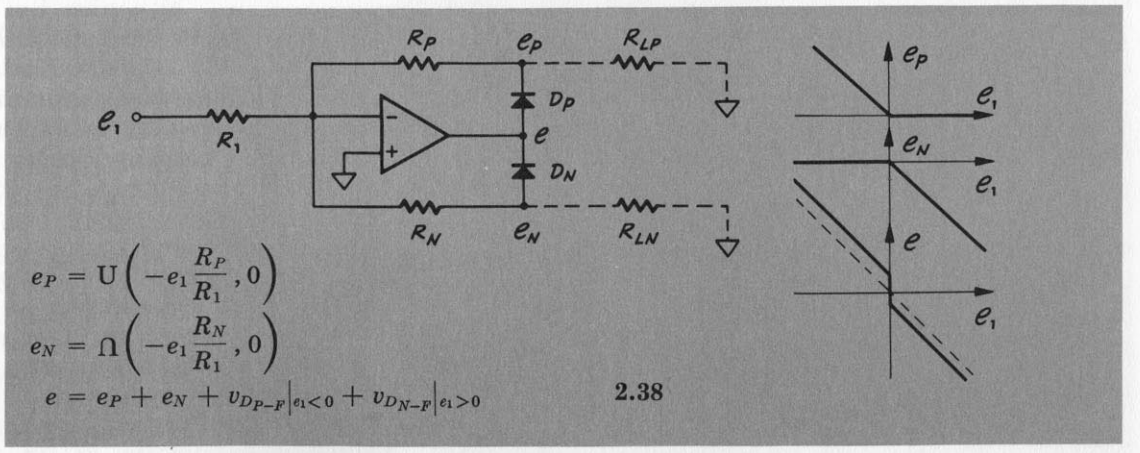
II.37
II.34
II.35
II.37
to
II.44
III.50
III.63
III.74
III.75
III.81

II.38 SIGNAL POLARITY SEPARATOR. This circuit is important for low voltage applications because it provides precisely-scaled selection of the input, e_1, with respect to ground potential, at the outputs e_P and e_N.

When D_P is not conducting, e_P is nearly zero, assuming resistive loads returned to ground (or to the virtual ground of a single-ended amplifier). The departure of e_P from zero will depend upon the reverse current of diode D_P through R_P in parallel with R_{LP}. This error can be made small and virtually constant by making R_N zero.

When D_P is conducting, the error at e_P is the forward voltage across D_P *divided by the amplifier gain*. Hence, precise selection may be accomplished, even when e_1 is in the millivolt range.

As an added feature at the selection point ($e_1 = 0$) the output e undergoes a sharp transition which may be differentiated and used as a logic signal for commanding gates or relays.



2.38

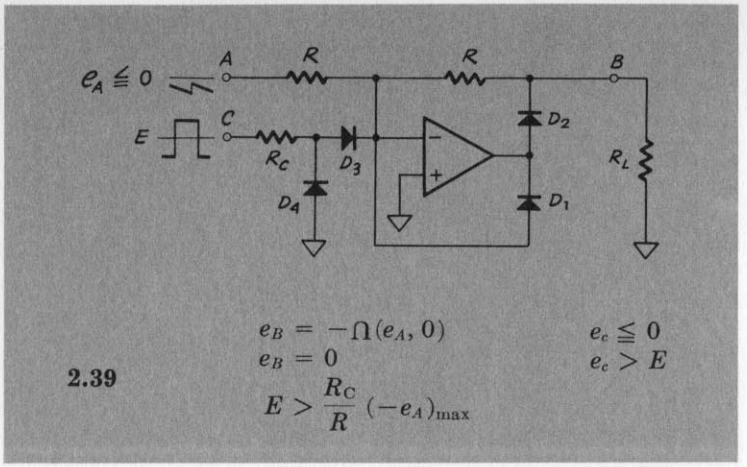
II.38
I.25
I.32
II.34
to
II.37
II.39
to
II.44

pages 56 & 57

II.39 PRECISION GATE. When this gate is "closed" it functions as a normal unity-gain inverter between terminals A & B, for *negative* input signals. Positive input signals result in no output, because they would tend to swing the amplifier output terminal negative, which is prevented by the cooperative bounding action of D_1 and D_2. When the gate is "open," terminal A is isolated from terminal B.

The gate is swung open and shut by application of a signal to terminal C. Assuming that the resistor (R_C) in series with terminal C is small compared to R, a positive signal of any appreciable magnitude applied to C will cause the circuit to clamp in the condition in which D_1 bounds it, and D_2 disconnects the amplifier from terminal B. If terminal C is open-circuited, or returned to ground, or if a negative signal is applied to terminal C, the gate is closed, and the A-to-B circuit acts like a normal unity gain inverter . . . but as mentioned above, only for negative input signals applied to A. Positive input signals applied to A will open the gate, just as if they had been applied to terminal C. Note that the "closed resistance" of this switch approaches zero, to the extent that the inverter performance approaches the ideal. When the switch is open, the isolation is nearly as perfect, being somewhat dependent upon the leakage in D_2.

As in II.38, loads must be resistive and grounded.



2.39

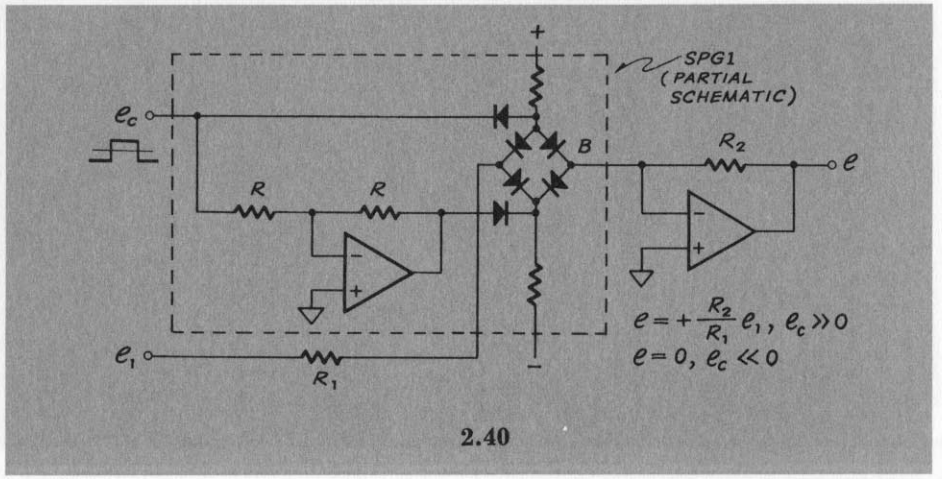
II.39
I.25
I.32
II.34
to
II.38
II.40
to
II.44
III.50
III.58
III.74
III.75
III.79
III.81

II.40 ELECTRONIC SWITCH. In this circuit, e_1 is gated to point B when, and only when $e_c \geqq 1$ volt. The unity-gain inverter produces $-e_c$ at the lower end of the diode bridge when $+e_c$ is applied as shown; and, provided the magnitude of e_c is of the order of 2 volts or more, the bridge becomes conducting from e_1 to B. Negative values of e_c ($e_c \leqq -1$ V) render the bridge non-conducting.

An application to which this circuit is ideally suited, and often applied, is the resetting or clamping of integrators. In such applications the corner of the bridge nearest "e_1" is connected to the output of the integrator, and the opposite corner is connected (as shown in our diagram) to the summing point.

The reader who prides himself on commercial awareness will not be at all surprised to learn that Philbrick makes available a module, called the SPG1, in which not one, but *two* of these splendid circuits, are economically presented, in a neat and painless package.*

*The SPG1 contains two complete diode bridges, and a driver stage; a single logic signal "inhibits" one bridge, "enables" the other, or vice versa, according to the signal polarity. The two bridges may be used, for example, instead of the relay circuit of II.50, for setting arbitrary initial conditions.

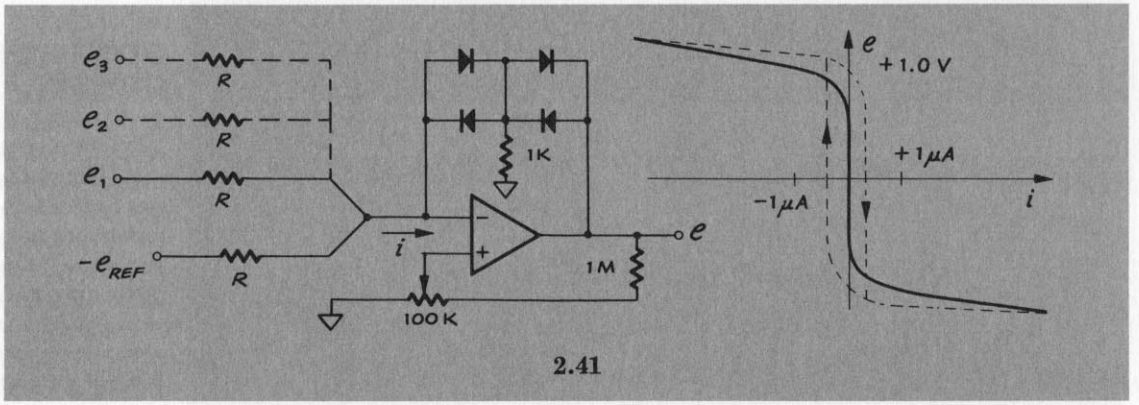


2.40

II.40
I.25
I.32
II.34
to
II.44
III.50
III.58
III.74
III.75
III.79
III.81

II.41 PRECISION COMPARATOR. This circuit indicates whether a voltage is greater than or less than a desired reference voltage. It does so by sensing the direction of the current, i, flowing between the input network and the amplifier summing point, and bounding the output accordingly. Since the circuit is current-sensitive, it can just as easily compare the sum of several voltages against a reference, or for that matter, against the sum of several references. Note that the reference voltage, although it need not be constant, does need to be inverted before being presented to the comparator. The output is approximately logarithmic, providing a graded null.

For very *slowly* changing voltages, "snap action" can be added by means of positive feedback, at the small price of introducing a finite amount of hysteresis. The amount of hysteresis is controlled by the potentiometer connected to the positive input (which should be grounded if snap action is not required).

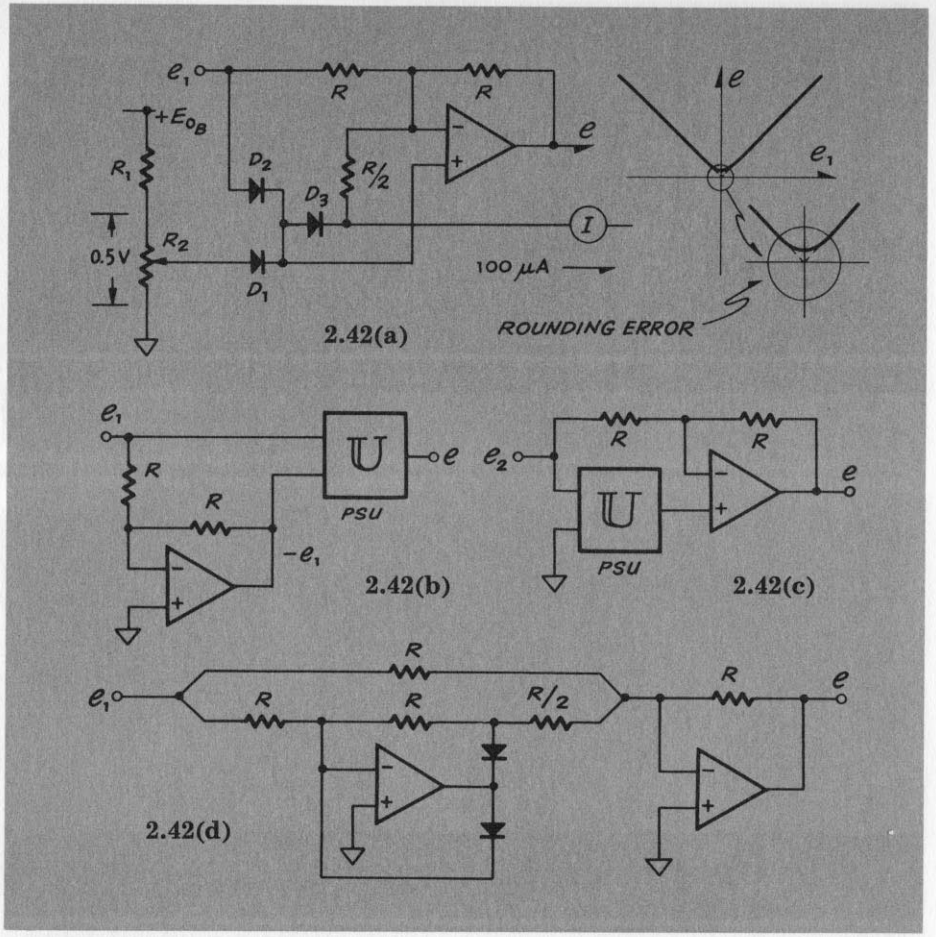


2.41

II.41
I.25
I.27
I.32
II.34
to
II.44
III.39
III.40
III.43
III.44
III.45
III.58

II.42 SIMPLE ABSOLUTE-VALUE, PRECISION ABSOLUTE-VALUE CIRCUIT. With negative input, the positive terminal of the amplifier in (a) is as close to ground potential as one can adjust the low-resistance potentiometer. Hence, negative-polarity signals find their way from e_1 to e through a unity-gain inverter. Positive-going signals have three paths. One is via the unity-gain inverter. Another is via the drop of D_2 to the positive input, whence a gain of $(+4)$ is realized for $(e_1 - V_{D2})$. The third is via D_2 and D_3 in series with $R/2$, whence a gain of (-2) is obtained for $(e_1 - V_{D2} - V_{D3})$. The sum of these terms is simply e_1, if $V_{D2} = V_{D3}$ at the suggested current. The output is, thus, a positive-going signal, equal in magnitude to the input, but of positive polarity, *regardless* of the input polarity. (If, for example, e_1 were to be a sine wave, e would be the positive full-wave-rectified version of it.) If all diode and supply polarities were reversed, one would obtain the *negative* absolute value. The Philbrick PSU Upper Selector is used to obtain the absolute value in 2.42(b) and 2.42(c). In the PSU, a zero adjustment, for diode-difference compensation, is incorporated within the unit. In (b), the Selector is presented with the input voltage and its negative, and presents the greater of them at the output. A (single-ended) amplifier is required to invert the input, if its negative is not already available in the system. In (c), the PSU selects accurately between the input and ground, presenting the greater of them to the positive input. When the input is negative, inverter action takes place, because the positive input is at ground potential; when the input is positive, follower action occurs. A good differential amplifier is needed in (c), but all the advantages of a feedback amplifier are gained, including the possibility of inserting a booster in the loop for high current capability.

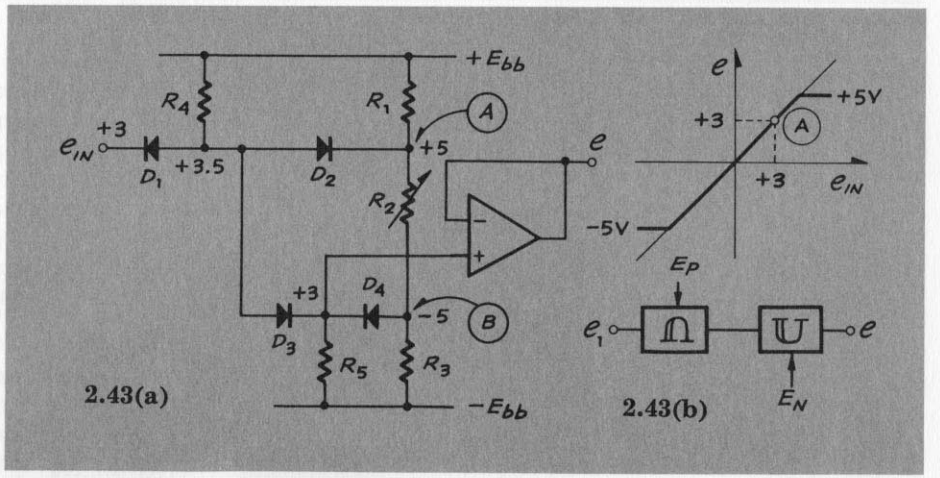
By placing the diodes within the feedback loop, the circuit of 2.42(d) renders them effectively "ideal." When e_1 goes negative, the output of the first amplifier jumps positive by one diode drop, shutting off the upper diode and bounding the amplifier through the (conducting) lower diode. The second amplifier simply inverts the (negative) e_1. When e_1 is positive, both amplifiers invert and the output is: $e = 2e_1 - e_1 = +e_1$, by virtue of the gain of 2 in the lower branch.



II.42
I.25
I.32
II.34
to
II.41
II.43
II.44
III.52
III.53
III.54
III.63
III.64
III.65
III.81

II.43 CLIPPER. This circuit has, in the Ideal Case, linear and unity-gain response between two sharply-defined limits, above and below which its output is constant at the limit value; thus it behaves as a "clipper," without saturation of the amplifier or other undesirable side effects. The curve illustrates its Ideal behavior for symmetrical limits of ± 5 V. R_2 adjusts both limits simultaneously.

For convenience in analyzing circuit performance, we have annotated the schematic with typical voltage values, representing the prevailing conditions for a +3 V input (point A on the curve). Under these conditions, D_1 and D_3 are conducting, and D_2 and D_4 are not. Above $e_{in} = 5$ V, D_2 conducts, clamping the output at +5 V. Below $e_{in} = -5$ V, D_4 conducts, clamping the output at -5 V. For good accuracy, the forward drop of D_1 should match that of D_3 . . . a condition that could be encouraged by replacing R_4 and R_5 by constant-current sources (cf: II.35 and III.8), particularly if the signal excursion approaches E_{bb} in magnitude. When in lower bounds, diode drop in D_4 is not compensated. N.B. Selector units PSL & PSU will provide bounds having accuracy, temperature and diode-difference compensation, and low output impedance—*sans* amplifier!



II.43
I.25
I.32
II.34
to
II.42
II.44
III.8
III.15
III.58
III.66
III.67

II.44 DEAD ZONE. This circuit establishes a region of almost complete insensitivity to small values of input.

$$-E\frac{R_2}{R_1} < e < E\frac{R_4}{R_3} \qquad (2\text{-}59)$$

In that region, both D_1 and D_2 are reverse-biased. D_3 and D_4 limit the reverse bias, and hence block both the leakage current and any stray capacitive coupling from the input terminal to the amplifier.

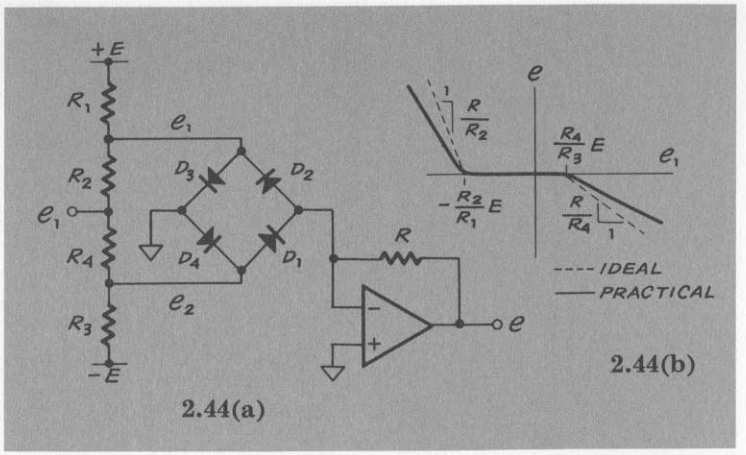
When e_1 becomes sufficiently large, D_1 or D_2 conducts. The output voltage is approximately:

$$e = -\frac{R}{R_2}\left(e_1 + \frac{R_2}{R_1}E\right), e_1 \text{ neg.} \qquad (2\text{-}60)$$

$$e = -\frac{R}{R_4}\left(e_1 - \frac{R_4}{R_3}E\right), e_1 \text{ pos.} \qquad (2\text{-}61)$$

In both expressions, diode offset has been neglected. Its principal effect is to cause significant rounding at the corners of the response characteristic, as shown. Practical values for R_3 and R_1 may be larger than the equations would indicate.

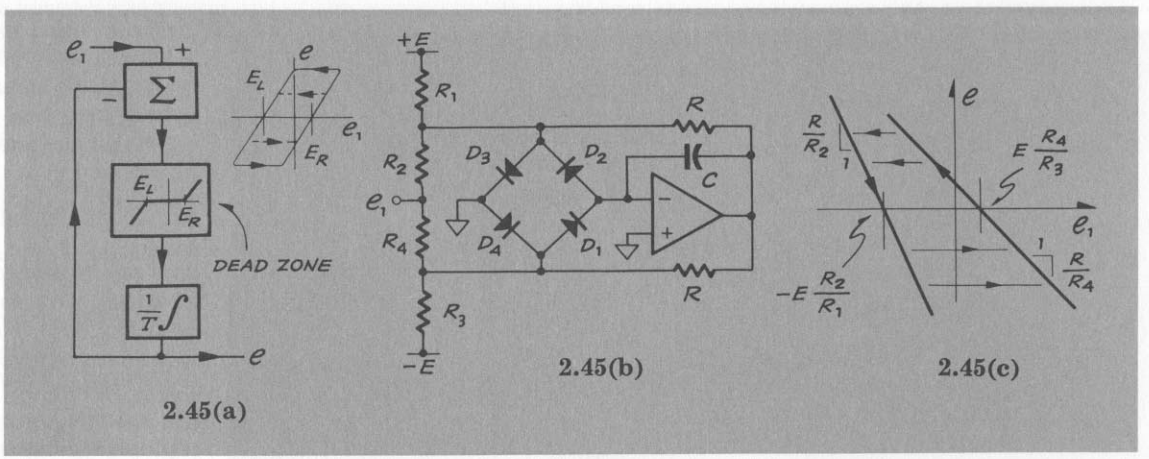
Further, these offsets are temperature-dependent (2–3 mV/°C referred to input), a source of uncertainty in the intercepts of the characteristic. D_1 and D_2 may each be replaced by an "ideal diode" (or polarity separator) circuit like that of II.38, virtually eliminating the effect of diode offsets. The dashed resistor—when used—permits symmetrical adjustment of the thresholds by means of a single adjustable element.



II.44
I.32
II.34
to
II.43
III.58
III.77
III.79

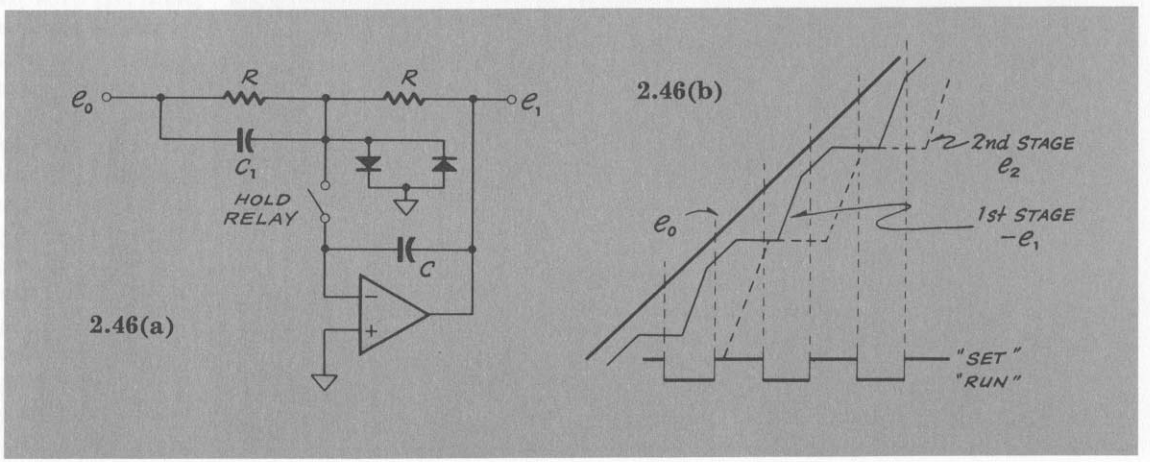
II.45 BACKLASH SIMULATION. Backlash (often called hysteresis) may be simulated by applying a circuit having the dead-zone characteristic described in II.44 to a feedback loop like the one shown in (a). Circuit (b) is a practical realization of 2.44(a), providing the required summing and integrating capabilities.

When the input is changing, and the output is beyond the transition region the output lags the input in a manner determined by the time constant RC. (To minimize this lag, minimize RC.) When the output is in the transition region (diodes D_1 and D_2 both reverse-biased) the output drifts at a rate equal to the net leakage current into the summing point divided by C. Hence, the diodes, the amplifier, and the capacitor should be chosen for minimum leakage. The choice of C must therefore reflect a compromise between tracking speed and holding accuracy.



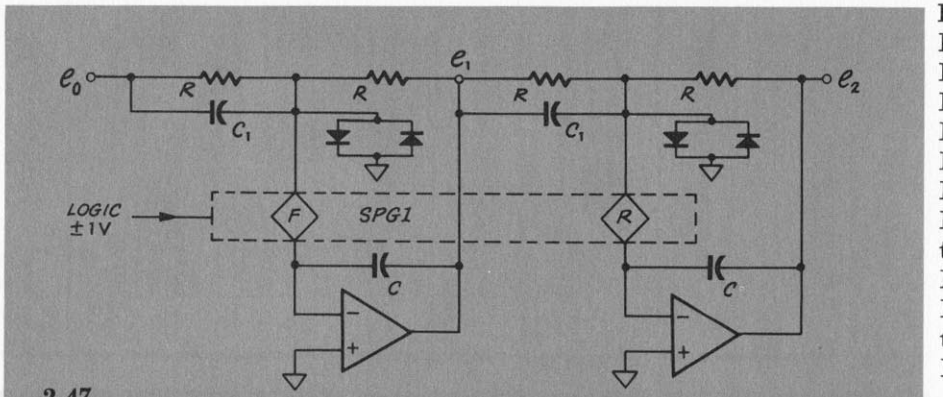
II.45
III.77

II.46 TRACK AND HOLD MEMORY (Relay Switching). The Philbrick SPREL set-hold relay pair is an excellent way of equipping an integrator with Track-and-Hold capability, using circuit (a). Choose C to achieve the hold accuracy required (see II.10 and II.11). R must be low enough in resistance so that RC is a small enough time constant to permit accurate tracking of the fastest-changing signal expected. The capacitor C_1 can be chosen so that the ratio of the feedback time constant to the input time constant is the same as the ratio of the closed-to-open switching times of the relay. The second relay in the SPREL operates in a complementary manner to the first and, can be used in a second-stage track-hold circuit, by driving the logic input appropriately. (Two stages of Track-Hold are often required so that the second can hold the previous result while the first is taking a new sample.) The ramp response typical of (a) is shown in (b).



II.46
I.33
I.34
I.36
II.47
III.53
III.56
III.57
III.74
III.75
III.76

II.47 TRACK-HOLD MEMORY (Electronic Switching). The Philbrick SPG1 (see II.40) can be used to replace the SPREL circuit of II.46. In the circuit shown here, which embodies two stages, as suggested in II.46 C_1 must equal C, since the diode switch operates virtually instantaneously . . . at least in comparison with the RC time constants. The major disadvantage of this circuit is the required long recovery (sampling) time, while the output relaxes exponentially (following the RC feedback time constant) from the value it had in the previous Hold state to the value it must have in the Track state. This problem can be largely eliminated by using the circuit of II.48. Leakage in the Hold mode may be a problem, particularly at high temperatures. The Waveforms that would describe the behavior of 2.47 are similar to those in Figure 2.46(b), except that there is no relay-operating-time delay.

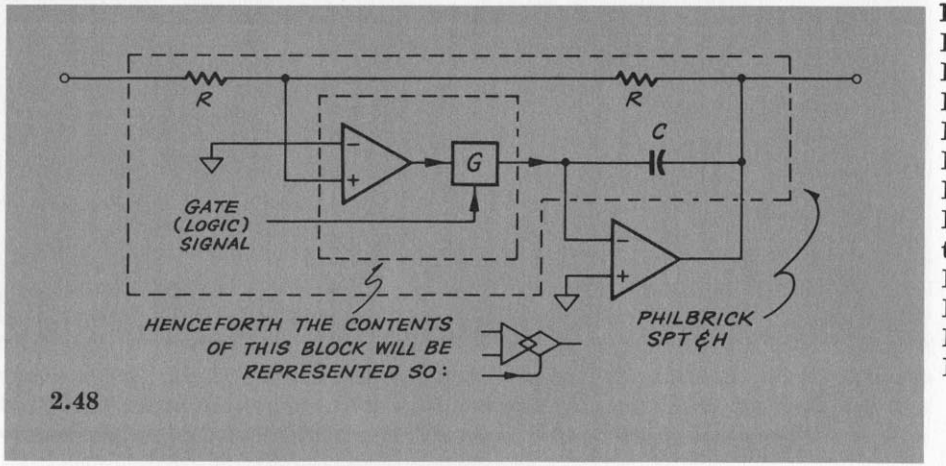


2.47

II.47
I.33
I.34
II.40
II.46
II.48
III.49
III.50
to
III.53
III.74
to
III.76

II.48 TRACK-HOLD MEMORY (Gated Amplifier). Here a gated amplifier replaces the electronic switch used in II.47, and the relay used in II.46, as the device that shifts the circuit from the Track mode to the Hold mode. Used as a current amplifier, to increase the speed of tracking by providing more charging current, it need not have voltage gain. It must be non-inverting, and, when gated off, must exhibit as little leakage as possible to the amplifier input. For stability, it must have little phase shift up to the maximum frequency for which the loop gain of the amplifier-*cum*-integrator is greater than unity, and must have at least as small input uncertainty as the computing amplifier, though its input leakage current is less important.

Anticipating your desire for a convenient and economical "black box" we have invented the Philbrick SPT&H, which will also perform peak—and valley—following operations, at the flick of a switch. (See III.53.)

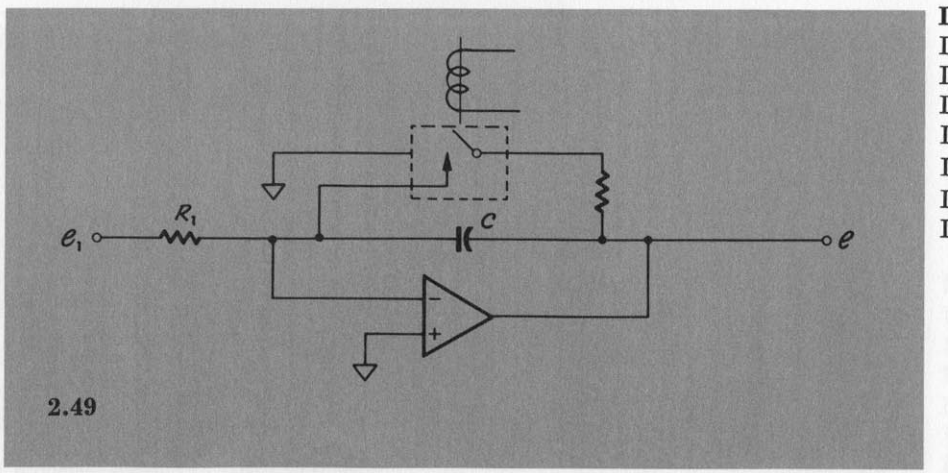


2.48

II.48
I.33
I.34
II.39
II.46
II.47
II.51
III.49
to
III.53
III.74
III.75
III.76

II.49 ZERO-VOLT RESET. Integrators must be reset to appropriate initial conditions, before each new computing cycle begins. Here we show a relay discharging the feedback capacitor to zero, thus resetting the output to zero. A small series resistor limits the capacitor discharge current to protect the relay contact and the capacitor. This resistor should be no larger than necessary, since it can allow the circuit to reach an equilibrium significantly different from zero, if its resistance is significant with respect to R_1.

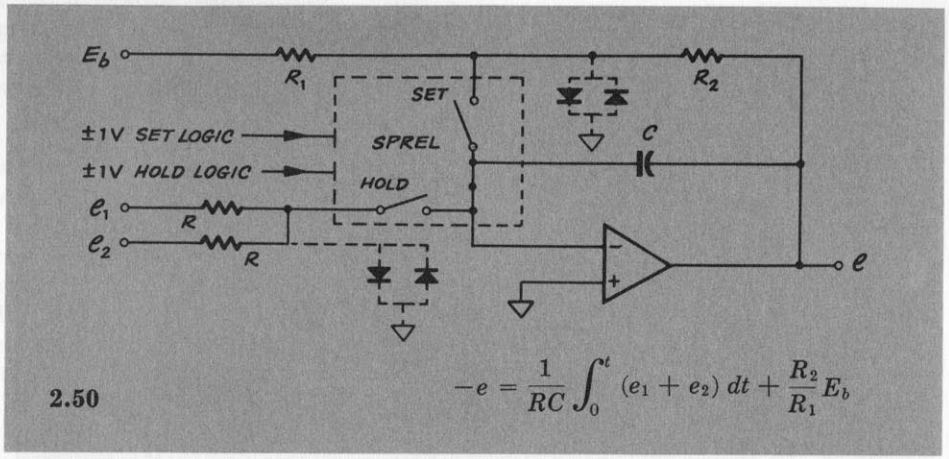
Three *caveats:* (1) Minimize leakage across the relay contacts, or the circuit will approach the function of a high-gain unit-lag, rather than a true integrator; (2) Poorly-chosen relay coils may induce an "inductive kick" into surrounding circuitry, unless damped. This occurs when the relay is deenergized (the worst possible time—just as integrating begins again); (3) Leakage and stray capacitance from the relay drive potential to the summing point can be far more serious than leakage across the contacts, because that voltage can be as high as the power supply. Hence, this switch should be appropriately shielded and grounded.



2.49

II.49
I.34
I.36
II.10
II.12
III.46
III.75
III.76

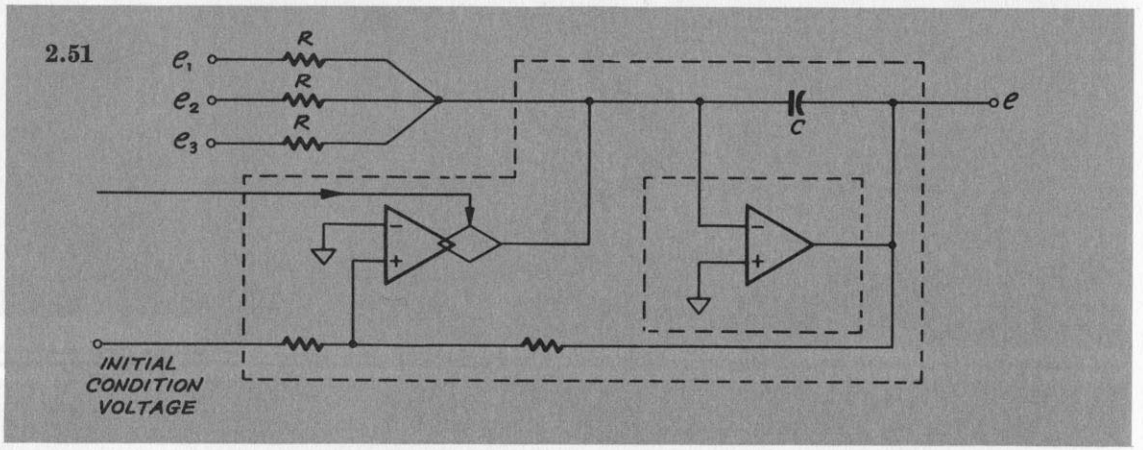
II.50 INITIAL CONDITIONS RESET. The Philbrick SPREL set-run reed relay pair is designed for this application. Resetting will be accomplished with the time constant R_2C; hence, R_2 must be low for fast reset. However, the R_1, R_2 network must not be so low in resistance as to overload either the amplifier or the initial-condition source, E_b. Independent logic input signals may be fed to the SPREL to control the Set and Hold modes. The diode clamps shown in dashed lines will help to reduce both AC and DC leakage currents across the relay.



II.50
I.33
I.34
I.36
II.10
II.49
II.51

II.51 INITIAL-CONDITIONS RESET (Gated Amplifier). Here we show a gated amplifier (non-inverting), used as a means of very quickly resetting a summing integrator to an initial condition. The circuit is identical in function to that of II.50, except that the gated amplifier is inherently faster than the relay, and the integrating network is not disconnected, because the gated amplifier has established a new summing-point for the Reset condition. See II.39.

The Philbrick SPT&H may serve in this capacity as well, provided that its built-in 0.01 μF integrating capacitor is suitable. Larger capacitors may of course be connected externally and will then be in parallel with the 0.01 μF already inside the SPT&H.



II.51
I.33
I.34
II.10
II.12
II.49
II.50