II

Applying Converters Successfully

Chapter II-6

In Chapter 5, it was pointed out that, considering the many different types of converters on the market, the complex manner in which converter specifications relate to a specific system application, and the fact that prices of converters range from less than $10 to several hundreds of dollars, selecting the most economical converter for an application is not a simple task. To make the most appropriate converter choice requires that the user consider a number of questions: What are the real objectives of the conversion process, and how do they relate to the converter's specifications? How may the system be configured to relax the converter's performance (and price) requirements, and at what overall cost? How will the other system components limit and degrade the converter's performance? What tradeoffs are available in the system error budget? Is it more economical to make a long-term choice of one "general-purpose" converter, which will meet the needs of a large number of system designs, or to go through an optimum selection process for each individual application?

In this chapter, we will discuss system aspects of selecting converters, a continuation of the discussion in the last chapter.

After selecting the appropriate converter, the user should be fully aware that the thorough preliminary analysis and economic component choice usually involved is not by itself sufficient to ensure that the system performance needs will be met. The system designer must take into account the physical surroundings, interconnections, grounding and power supplies, protection circuitry, and all the other details that constitute good engineering practice.

While these few pages cannot (and are not intended to) be a primer on engineering practice, it is useful for the converter user to become aware of those elements of practice that are of particular relevance to converter-system design.

MAKING THE PROPER SYSTEM CHOICES

A general rule of thumb used by some designers may be expressed as follows: "As the converter performance requirements approach state-of-the-art converter capabilities in *both speed and accuracy,* the price of the converter will increase exponentially." The user may expect substantial cost savings if he can relax either of these parameters.

Data-Acquisition Systems

An example will serve to illustrate the process of elimination and winnowing that can be profitably employed to determine a converter's minimum performance requirements. Figure 1 shows, in the simplest terms, a block diagram of an analog data-acquisition system, the primary application for which A/D converters are used.

The data-acquisition system, under the direction of the control unit, selects the multiplexer input points, one at a time, and directs the signal appearing on each point to the analog input of the A/D converter via the associated multiplex channel. The signal level is encoded by the converter and outputted to storage. The storage unit retains each piece of data in a predetermined format, and holds it for further processing.

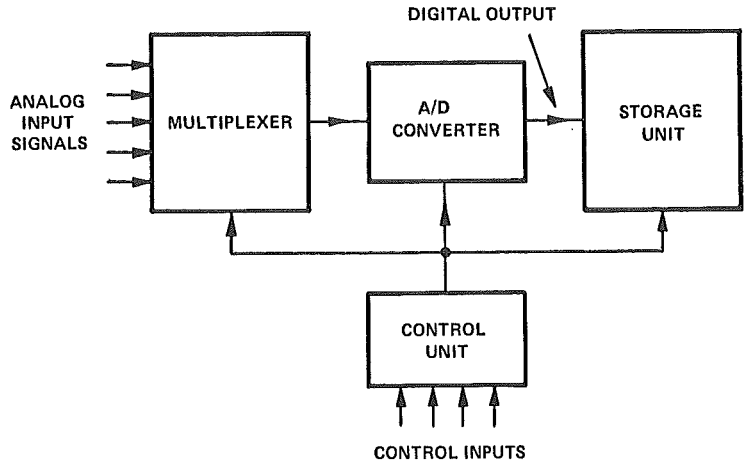

Figure 1. Data-acquisition system.

Three Classes of Converter Specifications

In attacking the problem of determining the converter performance requirements, it is useful to divide the converter specifications into three classes: Those that determine accuracy under optimum conditions, those that are dependent on time (or speed of response), and those that are substantially affected by the environment.

In the first class are included resolution, relative accuracy, differential linearity, noise, quantization uncertainty, monotonicity, and differential-linearity temperature coefficient. The reason this last term is included, though it would appear to be an environmental specification, may be somewhat unexpected: Although the ambient temperature may be in the steady state, it can be elevated (e.g., 25°C above normal room temperature) by virtue of enclosure in a cabinet. Although calibration *in situ* can correct for errors produced by variation of gain and offset with temperature, no correction can normally be effected for errors characterized by the differential-linearity T.C., due to individual bit variations with temperature. For this reason, the differential-linearity error at 25°C is augmented by the product of the steady-state temperature rise and the differential-nonlinearity temperature coefficient.

Speed-dependent specifications in the second category include conversion time, bandwidth, settling time of the input circuitry, etc. Environment-related specifications in the third category include gain (i.e., scale-factor) T.C., offset T.C., limits of the operating temperature range, etc.

Approaches to Relaxing the Specifications

Relaxation of the specifications in the first class may be effected through the use of signal conditioners. Choice of the specific form signal-conditioning may take is based on our knowledge of the input signals to be encoded and the information to be extracted from the encoded data. Known or unwanted signal components may be extracted from the input signals, and the peak-to-peak variation of the remaining signals may be scaled to equal the input voltage range of the A/D converter with an analog subtractor having adjustable gain. For example, if the signal conditioner is a differential instrumentation amplifier, such as the Model AD521 or AD522, it may be used to bias out dc offsets, and to scale the input appropriately (Figure 2).

The level-shifting-and-scaling operation can be used to obtain efficient use of the converter's input range. By scaling, voltage increments in the original signals that were less than 1 LSB of the converter's input voltage range may be measured.

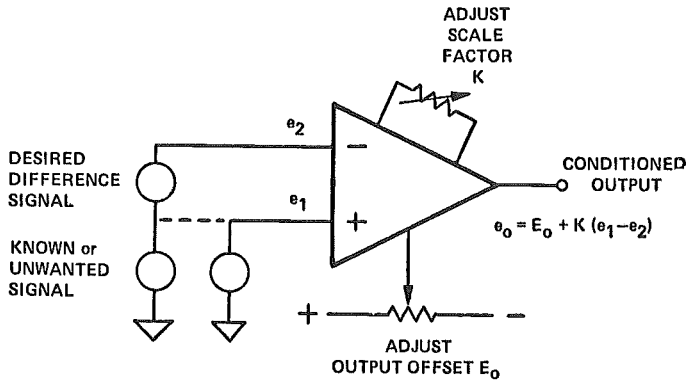

Figure 2. Differential instrumentation amplifier as a signal conditioner for data acquisition.

Logarithmic Compression

In applications calling for wide dynamic signal range but capable of tolerating constant fractional error (e.g., 1% of actual value), rather dramatic efficiency can be realized through the use of logarithmic amplifiers for data compression, as shown in Figure 3. Here, a logarithmic amplifier allows encoding of signals, that would ordinarily require a minimum of 20-bit conversion to handle the dynamic range, with a far-less-costly 12-bit converter. Modest accuracy in a fixed ratio to (e.g., % of) actual value is substituted for extreme accuracy in relation to the entire full-scale range, at considerably less cost. For many applications this is an ideal performance mode, except for those applications in which extremely small errors are required at all points in the range (e.g., measuring long-term stability of voltage sources). The logarithmic data can be dealt with easily if the data is to be processed digitally; or it can be recovered in linear analog form (if it is simply to be stored or transmitted digitally) by the use of another log amplifier, in the antilog connection, with a D/A converter.

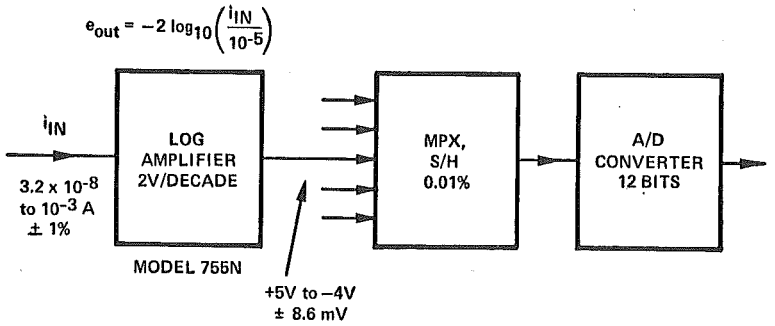

Figure 3. Using a log amplifier for range compression in a data-acquisition system.

Filtering

Another commonly-used signal-conditioning unit is the filter. Low pass filters are used to extract carrier, signal, and noise components, above the frequencies of interest, from the input signals. These components appear as noise if the converter is unable to follow them. A/D converters often incorporate follower circuits for impedance buffering. With a modicum of external wiring, they can be connected as active low-pass filters. (Figure 4)

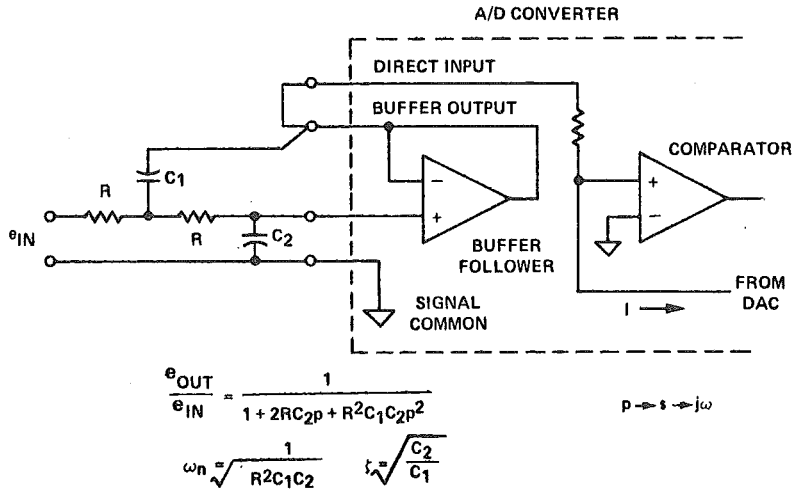

Figure 4. Input buffer of an A/D converter connected as an active low-pass filter.

Sample-Hold

A relaxation of the second class of specifications can also be effected by adding a sample-hold amplifier to the system configuration, as depicted in Figure 5.

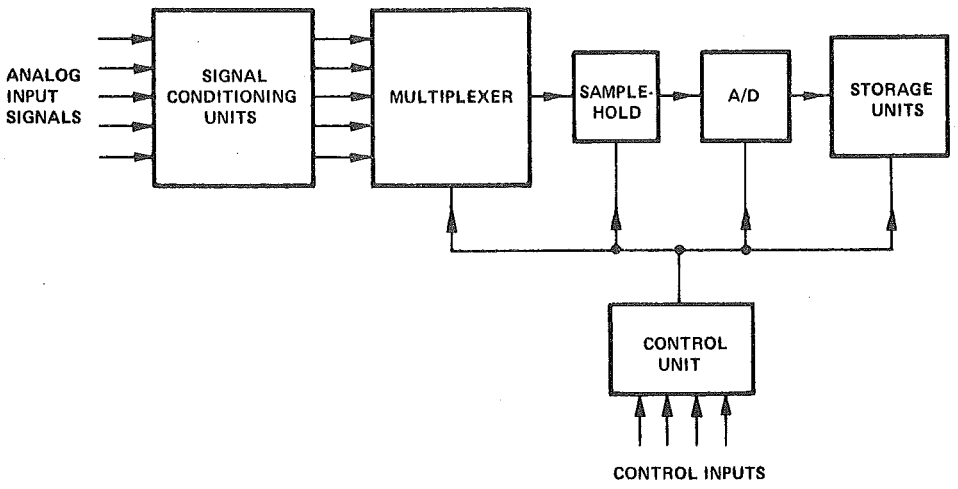

Figure 5. Data-acquisition system with sample-hold and input pre-conditioning.

The use of a sample-hold amplifier can increase the system throughput rate and increase the highest-frequency signal, of a given amplitude, that may be encoded within the resolution of the converter. The system throughput rate, without the sample-hold, is determined primarily by the multiplexer's settling time, plus the A/D converter's conversion time.

The multiplexer settling time is the time required for an analog signal to settle to within its share of the system error budget, as measured at the input to the converter, after selection by the multiplexer. For a 12-bit conversion system, with a ±10V range, multiplexers typically settle within 1μs, and typical conversion times are 20μs. The sample-hold can be used to hold the last channel's signal level for conversion, while the next channel is selected and settles. Since sample-hold amplifiers with acquisition times of less than 5μs to within 0.01% are readily available, the throughput time can be reduced to approach the conversion time. Pairs of sample-holds and A/D converters can be used for alternate conversions to increase throughput rate even further, though at considerable increase in cost.

The following example indicates the improvement possible with a sample-hold: If the input is a full-scale sine wave, $E_{FS}\sin(2\pi ft)$, the maximum rate-of-change is at zero, and (as can be

found by differentiating with respect to t) equal to $2\pi f E_{FS}$. If the change is to be less than 1 LSB in the conversion time, the highest frequency that can be applied is

$$f_{max} = \frac{\Delta E}{E_{FS}} \frac{1}{2\pi \Delta t}$$

For a 12-bit converter with a 20μs conversion time, $f_{max} \simeq 2Hz$! Using a sample-hold, one can reduce the uncertainty in the time of measurement from the ADC's conversion time to the aperture time of the sample-hold, thus effecting an improvement in f_{max} by the ratio of the conversion time to the aperture-time uncertainty.

Since 20ns or better is routinely available in sample-holds designed for operation with 12-bit converters, an improvement of 1000:1 is quite feasible, assuming that the S/H has adequate bandwidth.

If the speed of A/D conversion is significantly limited by the settling time of the input buffer-follower, the sample-hold may be connected to bypass it, providing an even greater increase in throughput rate.

Relaxation of the third class of errors, those due to environment-related specifications, may be abetted by allotting one multiplexer channel to carry a ground-level signal, and another to carry a precision reference-voltage level that is near-full scale. Data obtained from these channels may be used by a processor to correct gain and offset variations common to all channels, generated in the sample-hold, the A/D converter, and the associated wiring.

Contributions to Error

The decision to seek means of relaxing the required specifications is based on the availability and cost of devices that meet the original specifications, as compared to the cost of alternatives and any additional problems engendered by departing from a straightforward approach. To evaluate the performance tradeoffs, an error budget is a useful tool.

Three classes of errors should be considered:

Errors due to the non-ideal nature of each component

Errors due to the physical interconnections of the system components

Errors due to the interaction of system components.

The first group of errors can be determined from the spec sheets for the system components. The second group result from parasitic interactions that are a function of the way the interconnections are managed, e.g., grounding, shielding, contact resistance, etc. The third group result from specific interactions between components in the system; though they are not specifically called out in spec sheets, they can be predicted from careful reading of the specifications of the individual devices, or from the user's knowledge of how they are designed. An example of this class of error sources might be the offsets created by series impedances in the signal path (signal-source impedance, multiplexer-switch *on* impedance) and the bias and leakage currents of the stages following these impedances, to which they are connected. A second example might be disturbances caused at the signal source as the multiplexer switches it into the circuit.

By showing where the important contributions to error lie, the error budget is used as a tool for establishing tradeoffs to set the final performance requirements for the system. The error budget can be used as a tool in predicting the overall expected error, whether by worst-case summation, by root-sum-of-the-squares summation, or by combinations of the above using specific knowledge of possible compensations and common sense.

INSTALLATION AND GROUNDING

The current popularity of module and IC converters make it worthwhile to consider some elements of their design.

For one thing, many types are "customer-programmable." This means that the customer may select one of several possible signal voltage ranges by choosing the appropriate jumper-wiring configuration at the module's terminals. It goes without saying that all terminals used to determine the signal voltage range involve analog signals; to protect their low resolution levels, they should be kept away from circuit-card etch runs that carry logic signals.

Customer-programmable inputs also permit modification by the connection of external resistors, in addition to the jumpering mentioned above. Care should be exercised in doing this, for the reasons mentioned above. In addition, it should be noted that the excellent gain and offset T.C.'s of these devices are achieved by depending, not on absolute stability with temperature, but rather on the close tracking with temperature of key resistors within the module. Therefore, even if 0ppm/°C TCR resistors are used externally, the overall gain and offset performance vs. temperature may be appreciably degraded. Since there may be ways of avoiding excessive errors, the manufacturer should be consulted before external resistors are "frozen" into the design. It may also be helpful to read about resistor tracking in actual designs, as covered in Chapters II-2 and II-3.

In the design of the converter module, great care is taken to separate the analog and digital signal lines. This procedure should also be followed with the external layout of the board on which the converter is mounted. Etch runs of digital signal lines should not run parallel in close proximity with etch runs of analog signal lines. If these lines must cross, they should do so at right angles. Particular care should be taken with low-level high-gain points, e.g., the comparator input on A/D converters and the summing junction of the output amplifier on D/A converters. Etch runs to these points should be as short as possible and should not create loops. Analog-ground guard runs may also help reduce interference.

Grounding

Converter modules (actually, most data-acquisition components) have a number of ground terminals, which are not connected together within the module. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground (or Sense). These grounds must be tied together at one point, the system "mecca," usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts could be generated between the system mecca point and the ground terminal of the module. Separate ground returns are provided to minimize the current flow in the path from sensitive points to the system mecca point. In this way, supply currents do not flow in the same return path with analog signals, and logic-gate return currents are not summed into the return from a precision reference-zener diode. (Figure 6)

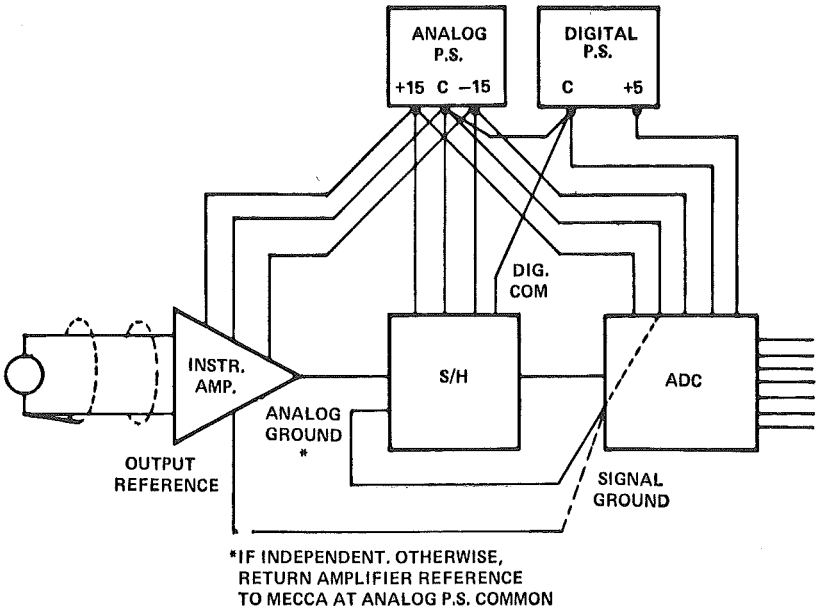

Figure 6 Basic grounding practice.

In any event, the connections between the system mecca point and the ground terminals should be as short as possible and should have the lowest feasible impedance.

Each of the module's supply terminals should be capacitively decoupled as close to the module as possible. A large-value capacitor with a high resonant frequency should be used. A 15μF solid-tantalum capacitor is usually sufficient. Analog supplies are bypassed to the module's analog power return terminal, and the logic-supply terminal is bypassed to the logic power return terminal.

When gain and offset adjustments are available and are intended to be used, the potentiometers with which they are performed should be mounted (with short leads) in such a position that they will be accessible when the mounting board is installed in the system

The same care should be taken to locate a converter properly within a system as is taken to mount a module on its circuit board. A converter should never be located near a transformer or fan blower motor. Using mu-metal shielding to protect against electromagnetic and RFI pickup is an expensive and not-always-successful proposition. D/A converters should be located at their loads. This may require long cable runs for the digital control signals; however, the reduction in noise pickup and ground-potential differences between the D/A's output and the load can easily justify the expense. Similarly, A/D converters should be located near the signal source when possible. Since this is not always possible, one suggestion is to use a differential amplifier to receive the signal at the end of a long cable run before presenting it to the A/D converter. When the system is laid out, unshielded analog signal lines should never run in channels with either digital signal lines or power lines.

Reducing Common-Mode Errors

As we have indicated, a differential amplifier may be used to eliminate ground-potential differences in various parts of the system in which the converter is used. In Figure 7, the signal source is a remotely-located transducer, and the differential amplifier is located near the A/D converter. The common-mode signal is the potential difference between the ground signal at the converter and the ground signal at the transducer, plus any undesirable common-mode signal produced by the transducer, and any voltages developed across the unbalanced impedances of the two lines.

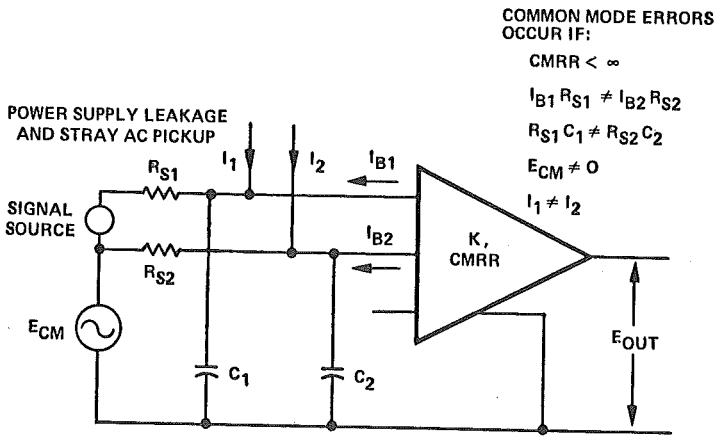

Figure 7. Common-mode and the difference signals due to line unbalance.

If the signal source is the output of the system's D/A converter, the differential amplifier would be located near the remote load. The common-mode signal is developed by the differences in ground potential at the two locations.

The amount of dc common-mode offset that is rejected depends on the CMRR of the amplifier. However, bias currents flowing through the signal source leads can cause offsets if either the bias currents or the source impedances are unbalanced. DC CMRR specifications generally include a specified amount of source unbalance (e.g., 1kΩ). Such specifications also indicate a top frequency for which the dc spec is valid, usually the line frequency (50-

60HZ), but sometimes 100Hz. At higher frequencies, unbalanced RC time constants (balanced or unbalanced series resistance and shunt capacitance to common, plus the amplifier's internal unbalances) reduce the common-mode rejection, by producing a quadrature normal-mode signal. This source of error can be greatly reduced by proper use of a guard shield, as shown in Figure 8.

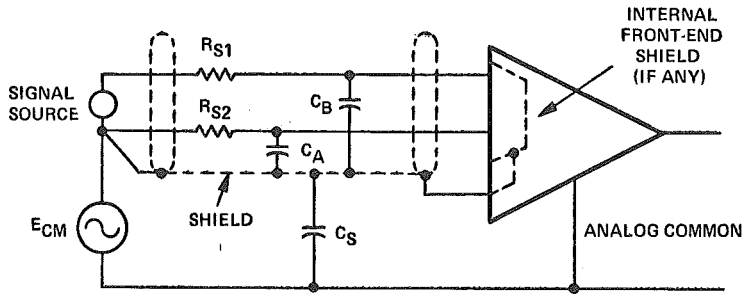

Figure 8. Use of guard shield to improve common-mode rejection at higher frequencies.

Here, no part of the common-mode signal appears across the capacitors C_A and C_B, since the shield is driven by the source of the common-mode signal. The shield also provides electrostatic shielding to minimize coupling to other signal lines in close proximity to the input leads.

When installing a guard shield, it is important that the guard shield connect only at one point to the source of the common-mode signal and that the shield be continuous, i.e., through multiplexers, connectors, patch panels, etc. Since the shield is carrying a common-mode signal, it should be properly insulated to prevent it from shorting to other shields or the earth ground. A final precaution that should be taken is to make sure that a conductive return path exists for the bias and leakage currents of the differential amplifier (unless it has transformer or optically-isolated, floating inputs).

It is helpful, in reducing noise and improving common-mode rejection, to connect the largest tolerable capacitance *between* the input leads. It will provide some filtering, and will reduce the capacitive unbalance by more than its ratio to the stray capacitance. (Figure 9)

In portions of a system where differential amplifiers are not used, sufficient precautions should be taken to insure that voltages are not induced in ground return leads to the single-point ground, and that the system is free from ground loops.

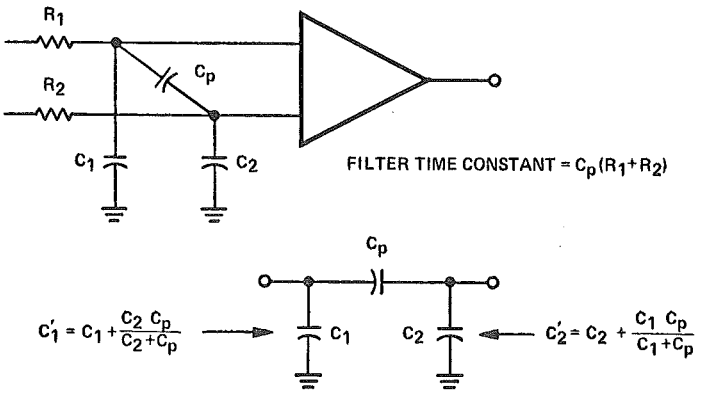

Figure 9. Capacitance between the input leads to reduce unbalance and provide filtering.

HOW TO ADJUST ZERO AND GAIN OF CONVERTERS

Many converter types are pretrimmed and require no adjustments as purchased to meet specified accuracy. For those cases where adjustments are called for, or where cost-savings can be effected by trimming inexpensive pre-trimmed devices, with modest specs, for use over narrow ranges for better-than-specified accuracy, or where long-term corrections are necessary during years of operation, here are some general principles of adjustment for converters. Naturally, the user should follow the specific instructions on product data sheets, especially where they conflict with these general guidelines.

Proper adjustment of zero and gain in DAC's and ADC's is a procedure that requires great care, and the use of extremely sensitive reference instruments. The voltmeter used to read the output of a DAC, or the voltage source used as a driving signal for the ADC, must be capable of stable and clear resolution of 1/10 LSB at both ends of the range of the converter; e.g., at zero and full scale.

Most DAC's and successive approximation ADC's manufactured by Analog Devices are provided with Zero and Gain adjustments *which are completely independent of each other,* as long as the adjustment of Zero is attempted *only* when the actual conversion circuit is producing Zero, and as long as the Zero (or Offset) adjustment is accurately completed before proceeding to adjustment of Gain (at full scale – 1LSB). Of course, it is possible to make Zero and Gain adjustments in reverse order and at other points on the transfer function – but it must be expected that the adjustments will no longer be independent, and the procedure will require a series of successive approximations.

Adjustment Process

Particularly for bipolar converters, fast and successful adjustment requires knowledge of the technique used in the circuit to convert the inherently unipolar DAC or ADC for bipolar operation.

1. Sign & Magnitude Codes are generally obtained by use of a unipolar converter with separate means of reversing polarity. The Zero adjustment is always made by calling for a zero from the converter. (Logic zero into a DAC produces zero volts output, or zero volts into an ADC produces data-zero output.)

2. Bipolar binary converters utilizing offset binary or two's complement coding usually employ analog offsetting to convert a unipolar design into bipolar. For instance, a 0 to +10V DAC may have its output amplifier offset by -5V, resulting in an output of -5 volts corresponding to 000000 input and +5 volts (minus 1 LSB) corresponding to a 111111 input. *Such a converter should have its "Zero" adjusted at* -5V (100000 in 2's complement)

An alternate explanation is as follows: converter Zero controls should always be set at the "All Bits Off" condition, and then Gain should be set at the "All Bits On" condition.

Adjustment For DAC's

ZERO: set input code so that all bits are "off", then adjust pot until output signal is within 1/10LSB of proper reading, or zero.

GAIN: set input code so that all bits are "on", then adjust pot until output signal reads within 1/10LSB of *Full Scale less 1LSB.*

Adjustment For ADC's

ZERO: set input voltage precisely at ½LSB above the "all bits off" specified input. Zero control should be adjusted so that the converter just switches in its LSB.

GAIN: set input voltage precisely at ½LSB less than "all bits on" input. Note that this is 1½LSB's less than the nominal full scale value: i.e., all-1's value of a zero to +10V 12-bit

ADC is actually +9.9976. Gain adjustment should be made with an input ½LSB less, or +9.9963 volts. With input voltage set as described, GAIN control is rotated to the point where the last bit just comes on. For instance, in a 12 bit binary converter, reading of 111111111110 would change to 111111111111.

Converter	Converter Range		
Resolution	20V	10V	5V
8 bits	39.06mV	19.53mV	9.77mV
10 bits	9.77mV	4.88mV	2.44mV
12 bits	2.44mV	1.22mV	610μV
14 bits	610μV	305μV	153μV
16 bits	153μV	76μV	38μV

Table 1. Voltage equivalent of ½LSB for various resolutions and voltage ranges.

It is important to note that this discussion is relevant for *offset-binary positive-true* coding. For 2's complement, the "all-bits-off" positive-true condition is 10000000 and " all bits on" is 01111111. For negative-true devices, the "all-bits-off" condition is 11111111 in offset binary, 01111111 in two's complement. When in doubt (or to avoid doubt), consult the data sheet.