II

Specifying Converters

Chapter II-5

The applications for digital data-handling equipment and the products of the conversion-and-data-acquisition industry have spawned a multiplicity and diversity of companies, product lines, and products. We find it sobering (though not a little gratifying) to discover that, as a major manufacturer, with a reasonably complete line of monolithic, hybrid, and modular products, we can deliver some 125 distinct converter types, of which a large number are in the "recommended-for-new-designs" category, and that the line is growing substantially each year.

Thus the very large number of converter products available in the marketplace, even from a single manufacturer, can overwhelm even the most informed engineer, when faced with the problem of selecting a device, or a group of devices, for a given application.

Interpretation of the specifications adds another dimension to the task, which is further complicated by the virtual absence, to date, of standardized definitions of specifications among manufacturers.

To remedy this situation, and attempt to make the system designer's job of finding the "right" converter a little easier,* this chapter lists some of the elements of the decision and steps a user can take to help "home in" on a near-optimum selection. In this chapter are also summarized interpretations of the specifications consistent not only with the previous three chapters and with engineering practice at Analog Devices, but also – it is to be hoped – with interpretations that may become accepted as standard within the industry.

A selection guide is provided for the convenience of the engineer who may seek orientation to the various categories of devices available off-the-shelf from Analog Devices. It is based on the 1977 Analog Devices catalog, which leads to the natural suggestion that the latest catalog available be consulted for specific choices. The reader is invited to request a copy from Analog Devices, either directly or via our nearest sales office.

Finally, a brief example of a data-acquisition design process, based on the suggestions in this chapter, is given.

TWO BASIC FACTORS

The two key factors in choosing the right device are:

Completely define the design objectives. Consider all known objectives and try to anticipate the unknowns that will pop up later. Include such factors as signal and noise levels, required accuracy, throughput rate, characteristics of the signal and control interfaces, environmental conditions and space factors, anticipated budgetary limitations that may force performance compromises or a different system approach.

Understand what the specs mean. It is essential to have a firm understanding of what the manufacturer means by his set of specifications. It should not be assumed (in 1977) that any two manufacturers mean the same thing when they publish identical numbers defining a

*It's possible that some of the points raised here, if previously unanticipated by the reader, may actually make the initial selection more involved, with the benefit that problems will be fewer at a later (and more expensive) stage.

given parameter. In most cases, the manufacturer has honestly attempted to provide accurate information about his product. This information must be interpreted, however, in terms meaningful to the user's requirements, which requires a knowledge of how the terms are defined. Two examples that give an insight into how differences arise are included and discussed at length in the Specifications section: *linearity* and *temperature coefficient.*

DEFINING THE OBJECTIVES – APPLICATION CHECKLISTS

General Considerations

A. Accurate description of input and output
   1. Analog signal range; source or load impedance
   2. Digital code needed: Binary, 2's complement, BCD, etc.
   3. Logic-level compatibility: TTL, CMOS, etc., logic polarity (Unless otherwise noted, logic levels mentioned in Analog Devices publications are standard TTL, positive true)

B. Data throughput rate

C. Control and data-interface details or constraints.

D. What does the system error budget allow for each block?

E. What are the environmental conditions: temperature range, supply voltage, re-calibration interval, etc., over which the converter should operate to the desired accuracy?

F. Are there any special environmental conditions that must be coped with? High-power RF, high humidity, shock and vibration, and cramped space are a few.

G. What are the bounds of integration for the purchased portion of the system? Turnkey system, real-time interface, data-acquisition subsystem, subassemblies, components? What are the hardware/software, analog/digital tradeoffs?

In addition to the above general considerations, there are specific items to consider when choosing each block in a system.

Considerations for D/A Converters

A. What resolution is needed? How many bits (e.g., 8, 10, 12, etc.) of the incoming data word must be converted? To what degree of accuracy, linearity, etc.?

B. What logic levels and codes can be provided to the DAC? (The most popular logic system is TTL, and the most-frequently used codes are binary, 2's complement, offset binary (2's complement with a complemented MSB), as outputs of systems, and BCD, usually derived from digital voltmeters or thumbwheel switches.) Is digital input serial or parallel?

C. What kind of output signal is needed: a current or a voltage? What is the desired full-scale range? (Most DAC's are available with either current output – at very high speed – or voltage output, with the added delay of an internal operational amplifier. Voltage-output DAC's are the more convenient to use and, with the exception of those designed specifically for high speed, will serve in all but those applications calling for μs and sub-μs settling times. Current-output DAC's are used in applications where high speed is more essential than stiff voltage output, such as circuits with comparators (e.g., A/D converters), or where fast amplification is to be provided externally (e.g., via CRT deflection amplifiers)).

D. What kind of reference is needed, fixed (internal or external) or variable (multiplying DAC)? How many quadrants are needed, and how arranged, for multiplying DAC's (1-quadrant, 4-quadrant, 2-quadrant digital, 2-quadrant analog)?

E. What is the nature of the digital interface? What are the speed requirements? What is likely to be the shortest time between data changes? After a change in the digital input data, how long can the system wait for the output signal of the DAC to settle to the desired accuracy for a full-scale change? For a 1-bit change at the major carry? Are switching transients of any consequence? Can they be filtered? Must they be suppressed (i.e., deglitched)

within the DAC? What is the analog signal feedthrough requirement for multiplying DAC's at low frequencies? At high frequency?

F. Over how wide a temperature range (at the device, including its internal temperature rise) must the converter operate? Over how much of this range must the converter perform essentially within its specifications without readjustment? What deterioration of specifications is permitted (gain vs. linearity, etc.)?

G. How stable are the terminal voltages of the power supplies that will power the DAC? Is the power-supply sensitivity specification adequate to hold errors from this source within reasonable limits? Are there constraints on converter dissipation?

Though no list can be complete, the above items will be the minimum consideration in any more-complete tabulation.

Considerations for A/D Converters

The process of selecting an A/D converter is similar to that involved in the selection of D/A converters. Some of the following considerations are analogous to those for D/A's, and others are unique to A/D's.

A. What is the analog input range, and to what resolution must the signal be measured?

B. What is the requirement for linearity error, relative accuracy, stability of calibration, etc.?

C. To what extent must the various sources of error be minimized as ambient temperature changes? Are missed codes tolerable under any conditions?

D. How much time is allowed for each complete conversion?

E. Is the reference to be fixed, adjustable, or variable (ratiometric measurement)?

F. How stable is the system power supply? How much error due to power-supply variation is tolerable in the conversion system? Are there constraints on converter dissipation?

G. What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter? What conversion circuit philosophies are acceptable for – or indicated by – the application? (e.g., successive-approximation, dual-slope integration, counter-&-comparator, etc. As a rule, integrating types are best for converting noisy input signals at relatively slow rates, while successive-approximation is best suited to converting sampled or filtered inputs at rates up to 1MHz. Counter-comparator types provide lowest cost but may be both slow and noise-susceptible; they are useful for peak followers and sample-holds that employ digital storage.)

H. What is the format of the digital interface? Parallel, byte-serial, serial? What kind of logic? Three-state, CMOS, TTL?

Considerations for Analog Multiplexers and Sample-Holds

When a sampled-data system is to be assembled, in which one A/D converter is time-shared among many input channels by the use of a multiplexer and sample-hold, their contribution to system performance errors must be taken into account. These accessory devices are discussed elsewhere, but they are also discussed briefly in this chapter because of their relevance to the converter selection process.

Multiplexers

A. How many input channels are needed? Single-ended or differential? High-level or low-level? What dynamic range?

B. What kind of hierarchy is used, if a great many channels are involved? What is the addressing scheme?

C. How much time is needed for settling to desired accuracy when switching from one channel to another? Maximum switching rate?

D. How much ac crosstalk error between channels is allowable? At what frequencies?

E. What error is produced by the leakage current flowing through the source resistance?

F. What will be the multiplexer "transfer" error, produced by the voltage divider formed by the *on* resistance of the multiplexer and the input resistance of the sample-hold. Is the multiplexer active or passive (i.e., does it have an output amplifier?)

G. Is the channel-switching rate to be fixed or flexible? Continuous or interruptible? Should it be capable of stopping on one channel for test purposes?

H. Is there danger of damage to active signal sources when the power is turned off? (MOSFET multiplexers are inherently "safe" (at least in this sense), since the switches open when power is removed. JFET multiplexer switches can conduct when power is removed, making it possible to interconnect, and therefore damage active signal sources.

Sample-Holds

A. What is the input signal range?

B. Considering the slewing rate of the signal and the multiplexer's channel-switching rate, what is the sample-holds's allowable acquisition time to within the desired error band?

C. What accuracy is needed (gain, linearity, and offset errors)?

D. What aperture delay and jitter are allowable, going into *hold*? (The delay component of aperture time is considered to be correctible, since the switching operation can be advanced to compensate. The uncertainty (jitter) cannot be compensated, and a random jitter of 5ns applied to a signal slewing at, say, 1V/μs produces an uncertainty of 5mV. In sampled-data systems, operating at a constant sampling rate, with data that is not correlated to the sampling rate, delay is of no importance, but jitter modulates the sampling rate.

E. How much droop is allowable in *hold*?

F. What are the effects of time, temperature, and power supply variation?

G. What offset error is caused by the flow of the sample-hold's input bias current through the series resistance of the multiplex switch and the signal source?

DEFINING THE SPECIFICATIONS

Figures 1 and 2 depict the specifications of typical D/A and A/D converters. Though the specs probably mean "what you think they mean," it is important that their meaning and implications be spelled out. The following list, in alphabetical order, should prove helpful.

Absolute Accuracy. Absolute accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter.

Absolute accuracy error of an A/D converter is the difference between the analog input theoretically required to produce a given digital output code and the analog input actually required to produce that same code. Since a band of analog values can produce the same code, the "input required to produce a given digital output code" is defined as the midpoint of either the theoretical or the measured band.

Absolute accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Absolute accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Acquisition Time. The acquisition time of a sample-hold circuit is the time it takes to acquire the input signal to within the stated accuracy. When conservatively specified, as in Analog Devices' specifications, it includes the *settling time* of the output amplifier. Since it is possible, in some cases, for a signal to be fully acquired (and the circuit switched into *hold*) before the output has settled, one should be sure of what a manufacturer means by this term, since the output of the sample-hold is not meaningful until it has settled.

Aperture Time. This is the time it takes in a sample and hold circuit, for the switch to open

SPECIFICATIONS (T_A = +25°C, unless otherwise specified)

MODEL	AD563K			AD563S			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DATA INPUTS							
TTL, V_{cc} = +5V, Pin 2							
Open Circuit							
Bit ON Logic "1"	+2.0			+2.0			V
Bit OFF Logic "0"			+0.8			+0.8	V
CMOS, 4.75 ≤V_{cc}≤15.8,							
Pin 2 tied to Pin 1							
Bit ON Logic "1"	70%V_{cc}			70%V_{cc}			V
Bit OFF Logic "0"			30%V_{cc}			30%V_{cc}	V
Logic Current (each bit)							
Bit ON Logic "1"		+20	+100		+20	+100	nA
Bit OFF Logic "0"		-50	-100		-50	-100	μA
OUTPUT							
Current							
Unipolar	-1.7	-2.0	-2.3	-1.7	-2.0	-2.3	mA
Bipolar	±0.85	±1.0	±1.15	±0.85	±1.0	±1.15	mA
Resistance (exclusive of							
span resistors)	5.3k	6.6k	7.9k	5.3k	6.6k	7.9k	Ω
Unipolar Zero (all bits OFF)		0.01	0.05		0.01	0.05	% of F.S.
Capacitance		33			33		pF
Compliance Voltage		-1.5 to +10			-1.5 to +10		V
RESOLUTION		12 Bits			12 Bits		
ACCURACY (Error relative to full scale)			±¼ (0.006)			±¼ (0.006)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY			±½			±½	LSB
SETTLING TIME TO ½LSB							
All Bits ON-to-OFF or							
OFF-to-ON		1.2			1.2		μs
POWER REQUIREMENTS							
V_{cc}, +4.75 to +15.8VDC		15	20		15	20	mA
V_{ee}, -15VDC ±5%		20	25		20	25	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{cc} @ +5VDC		3	10		3	10	ppm of F.S./%
V_{cc} @ +15VDC		3	10		3	10	ppm of F.S./%
V_{ee} @ -15VDC		14	25		14	25	ppm of F.S./%
TEMPERATURE RANGE							
Operating		0 to +70			-55 to +125		°C
Storage		-65 to +150			-65 to +150		°C
TEMPERATURE COEFFICIENT							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm of F.S./%
Bipolar Zero			10			10	ppm of F.S./%
Gain			20			30	ppm of F.S./%
Differential Nonlinearity		2			2		ppm of F.S./%
MONOTONICITY	Guaranteed over full operating temp. range			Guaranteed over full operating temp. range			
EXTERNAL ADJUSTMENTS*							
Gain error with fixed 10Ω resistor		±0.1			±0.1		% of F.S.
Bipolar Zero Error with Fixed							
10Ω resistor		±0.1			±0.1		% of F.S.
Gain Adjustment Range		±0.25			±0.25		% of F.S.
Binary Bipolar Zero Adjustments							
Range		±0.25			±0.25		% of F.S.
BCD Bipolar Offset Adjustment							
Range		±0.17			±0.17		% of F.S.
PROGRAMMABLE OUTPUT							
RANGES (See Figs. 1a, 1b)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
REFERENCE INPUT							
Input Impedance		5k			5k		Ω
REFERENCE OUTPUT							
Voltage	2.425	2.500	2.575	2.425	2.500	2.575	V
Current			5			5	mA
Impedance		1			1		Ω

*Device calibrated with internal reference Specifications subject to change without notice.

Figure 1. Typical microcircuit d/a converter specifications (AD563).

after the control command has been given. In a good SHA, this should not exceed 50ns delay, including 10ns uncertainty.

Common-Mode Range. Common-mode rejection usually varies with the magnitude of the range through which the input signal can swing, determined by the sum of the common-mode and the differential voltage. *Common-mode range* is that range of *total* input voltage

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0V	*	*
Unipolar	0 to +5, 0 to +10V	*	*
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5kΩ	*	*
0 to +10V, ±5V	5.0kΩ	*	*
±10V	10kΩ	*	*
Buffer Amplifier			
Impedance (min)	100MΩ	*	*
Bias Current	50nA	*	*
Settling Time			
to 0.01% of FSR for 20V step	2μs	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	0.012% FSR	*	*
Inherent Quantization Error	±½ LSB	*	*
Differential Linearity Error	±½ LSB	*	*
No Missing Codes	Guaranteed: 0 to +70°C	Guaranteed: -25 to +85°C	Guaranteed: -55 to +125°C
Power Supply Sensitivity			
±15V	±0.002% FSR/%ΔV_S	*	*
±5V	±0.001% FSR/%ΔV_S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30ppm/°C (-25 to +85°C)	±15ppm/°C (-25 to +85°C)	±15ppm/°C (-25 to +85°C) ±25ppm/°C (-55 to +125°C)
Unipolar Offset	±3ppm FSR/°C	±3ppm FSR/°C (max)	**
Bipolar Offset (max)	±15ppm FSR/°C	±7ppm FSR/°C	**
Linearity	±3ppm FSR/°C	±2ppm FSR/°C	**
CONVERSION TIME (max)	25μs	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
$\overline{\text{Status}}$	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500kHz	*	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±5mV	*	*
Max External Current	±4mA	*	*
Voltage Temperature Coefficient (max)	±20ppm/°C	±10ppm/°C	**
POWER REQUIREMENTS			
Supply Voltages/Currents	+15V, ±5% @ +25mA	*	*
	-15V, ±5% @ -20mA	*	*
	+5V, ±5% @ +50mA	*	*
Total Power Dissipation	925mW	*	*
TEMPERATURE RANGE			
Specification	-25 to +85°C	*	-55 to +125°C
Operating	-55 to +125°C	*	*
Storage	-55 to +150°C	*	*

*Same specification as AD572AD
**Same specification as AD572BD

Specifications subject to change without notice.

Note 1 Positive pulse 200ns wide (min). Leading edge ("0" to "1") resets registers. Trailing edge ("1" to "0") initiates conversion.

Note 2 With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 4 and 5.

Figure 2. Typical microcircuit a/d converter specifications (AD572).

over which specified common-mode rejection is maintained. For example, if the common-mode signal is ±5V and the differential signal is ±5V, the common-mode range is ±10V.

Common-Mode Rejection. The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. It is usually expressed either as a ratio (CMRR = 10^6) or as 20 $\log_{10}$ of the ratio (CMR = 120dB). A CMRR of 10^6 means that a 10V common-mode voltage is processed by the device as though it were an additive differential input signal of 10μV magnitude.

Common-Mode Voltage. A voltage that appears in common at both input terminals of a device, with respect to its output reference (usually "ground"). For inputs V_1 and V_2, with respect to ground, $CMV = \frac{1}{2}(V_1 + V_2)$. *Common-mode error* is any error at the output due to the common-mode input voltage.

Compliance-Voltage Range. For a current source (e.g., a current-output DAC), the maximum range of terminal voltage for which the current source will maintain its defined characteristics.

Conversion Time. The time required for a complete measurement by an analog-to-digital converter. In successive-approximation converters, it ranges typically from 1.0μs (ADC-1103-001) to 400μs (ADC-16Q). Popular 12-bit general-purpose A/D converters, such as the AD572, have conversion time of about 25μs.

Crosstalk. Leakage of signals between circuits or channels of a multi-channel system or device, such as a multiplexer. Crosstalk is usually determined by the impedance parameters of the physical circuit, and actual values are frequency-dependent.

Deglitcher (See Glitch). A device that removes or reduces the effects of time-skew pulses in D/A conversion. A deglitcher normally consists of a sample-hold circuit, which holds the DAC output constant at the previous value until the switches reach equilibrium. Since the phenomena involved can be extremely fast, the *deglitcher* is usually a portion of the circuit, rather than a specific general-purpose modular device.

Differential Nonlinearity. In a converter, differential linearity error describes the variation in the analog value of transitions between adjacent pairs of digital numbers, over the full range of the digital input or output. If each transition is equal to its neighbors (i.e., 1LSB), the *differential nonlinearity* is zero. If a transition differs from one of its neighbors by more than 1LSB (e.g., if, at the transition 01111111 to 1000000, the MSB is low by 1.1LSB), a D/A converter can be *non-monotonic,* or an A/D converter using it may miss one or more codes. A specified maximum differential nonlinearity of ±½LSB at 25°C ensures that monotonic behavior will exist over a tangible range of temperature, or each step is (1 ± ½)LSB.

Differential-Nonlinearity Temperature Coefficient. Since bit weightings vary to some degree with temperature, a converter having acceptable differential nonlinearity at 25° may have > 1LSB error at some other temperature. The temperature coefficient describes the maximum variation of differential linearity error with temperature over the specified range. Often, instead of a temperature coefficient, this specification may appear as a range of temperature for which behavior is monotonic.

Droop Rate. When a sample-hold circuit using a capacitor for storage is in *hold,* it will not hold the information forever. Droop rate is the rate at which the output voltage changes (by increasing or decreasing), and hence gives up information. As a rule, when using a SHA (sample-hold amplifier) ahead of an ADC, the SHA should not droop more than 0.1 LSB during the conversion time of the ADC.

Dual-Slope Converter. An integrating A/D converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a length of time determined by a counter. Then a reference input is switched to the integrator, which integrates "down" from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is pro-

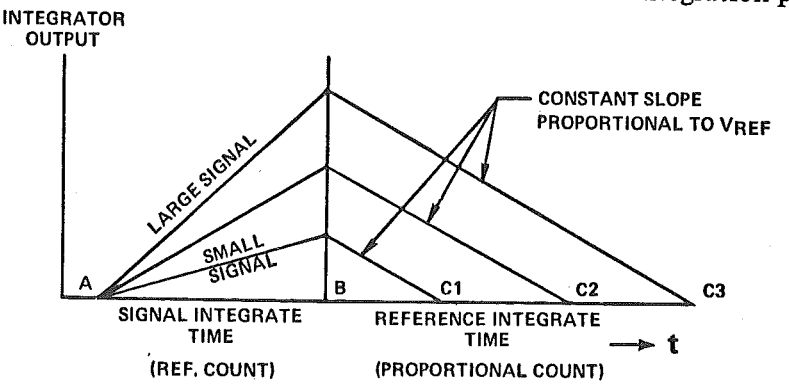


Figure 3. Voltage-time relationships in dual-slope conversion.

portional to the average of the unknown signal level over the predetermined integrating period. The same counter and clock are used for this measurement, and thus the output is immune to long-term variations of the integrator's characteristic time and the clock frequency. The counter provides the digital readout.

Feedthrough. A term referring to that characteristic of a circuit or device manifested by undesirable signal leakage around switches or other devices that are supposed to be turned off or provide isolation. Both digital and analog signals can cause analog feedthrough errors.

Four-Quadrant. In a *four-quadrant* multiplying DAC, if both the reference signal and the number represented by the input may be bipolar, the output can be either positive or negative, obeying the rules of multiplication as to algebraic sign in all four quadrants.

"Gain" Adjustment. The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is adjusted, typically, by setting the feedback resistor of a DAC, the input resistor in a current-comparing ADC, or the reference (voltage or current).

"Glitch". If one applies the output of a counter to the input of a DAC to develop a "staircase" voltage, the number of bits involved in a code change establish "major" and "minor" transitions. The most major transition is at ½-scale, when the D/A switches all bits, i.e. from 011 . . . 111 to 1000 . . . 00. If, for digital inputs having no skew, the switches are faster to switch *off* than *on,* this means that, for a short time, the DAC will seek zero output, and then return to the required 1LSB above the previous reading. This large transient spike is commonly known as a "glitch." The better-matched the input transitions and the switching times, and the faster the switches, the smaller will be the energy contained in the glitch. Because the size of the glitch is not proportional to the signal amplitude, linear filtering may be unsuccessful and may, in fact, make matters worse. (See also *Deglitcher*)

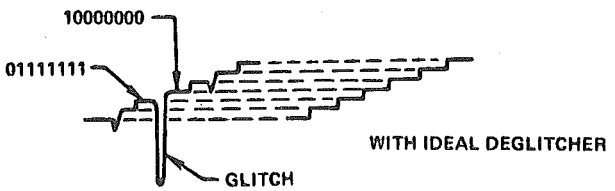


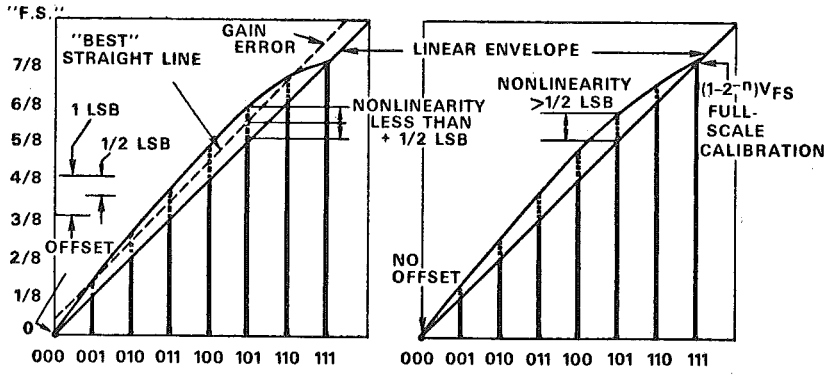
Figure 4. Glitch at a major carry.

Least-Significant Bit (LSB). In a system in which a numerical magnitude is represented by a series of binary (i.e. two-valued) digits, the *least-significant bit* is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + 2^0)$), the rightmost "1" is the LSB. The weight of 1LSB, in relation to full scale, is the *resolution* implied by the digital number.

Linearity. Linearity error of a converter is the deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (Figure 5). Sometimes referred to as "end-point" nonlinearity, the latter is the definition used by Analog Devices, both because it is a more conservative measure, and because it is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Relative Accuracy).

For Multiplying D/A converters, the analog linearity error at a given digital code is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

Once the converter has been adjusted and calibrated, deviations from linearity become absolute errors. While differential-linearity errors are cyclic, other linearity errors, such as might be caused by amplifier nonlinearity, tend to follow the usual nonlinearity patterns of other analog devices.



a. ½LSB nonlinearity achieved by arbitrary location of "best straight line".

b. Nonlinearity reference is straight line through end points. Nonlinearity ½LSB for curve of Figure 5a.

Figure 5. Comparison of linearity criteria for 3-bit D/A converter. Straight line through end points is easier to measure, gives more-conserative specification.

Monotonicity. The output of a monotonic D/A or A/D converter never decreases in response to an increasing input stimulus (or vice versa). In high-speed converters, it is not especially hard to trim a design to be monotonic over limited temperature ranges. In order to be monotonoc over very wide temperature ranges, error components of DAC switches and resistor networks must track each other very closely with temperature change. Monotonic behavior requires that the differential nonlinearity be < 1LSB. In ADC's, the counterpart of non-monotonic behavior is the "missed code," which is produced when a transition from one quantum of the analog range to the adjacent one does not result in the adjacent digital code, but in one removed by one or more counts. Monotonic behavior in high-resolution conversion over wide temperature ranges is not easy to accomplish at the present state of the art; consequently, converters like the AD572, which have no missed codes over the specified temperature range, at reasonable cost, are not commonly seen in the industry. Integrating converters, such as the AD7550 are inherently monotonic; A/D converters of this class are also inherently slow (usually more than 35ms for a full conversion).

Most Significant Bit (MSB). In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the *most-significant bit* is that digit (or "bit") that carries the greatest value or weight. For example, in the natural binary number 1101 (decimal 13, or $(1 \times 2^3) + (1 \times 2^2) + (0 \times 2^1) + (1 \times 2^0)$), the leftmost "1" is the MSB, with a weight of ½ nominal peak-to-peak full scale. In bipolar devices, the sign bit is the MSB. In A/D converters having overrange bits, the MSB is the most-significant "overrange" bit.

Multiplying DAC. A multiplying DAC differs from the conventional fixed-reference DAC in being designed to operate with reference signals that vary, often (ac) at high speeds. The output signal of such a DAC is proportional to the product of the reference voltage and the fractional equivalent of the digital input number. In addition to the usual DAC specifications, the multiplying DAC is specified as to analog signal *feedthrough* at low and high frequencies, and number of quadrants (1, 2-digital, 2-analog, or 4).

Noise. In high-resolution DAC's, such as the DAC1138, noise can be an important consideration, since the resolution is not confidently assignable when the peak noise exceeds the LSB value over a reasonable bandwidth. For an ADC, noise, either in the input signal, the input circuitry, or the conversion device itself, effectively increases the size of the quantization band, and may thus impart statistical properties to the output numbers, which may then require additional processing for successful interpretation.

Noise: RMS vs. Peak-toPeak. For all but integrating converters, peak noise must be considered carefully, especially where small numbers of readings and limited processing capacity

are available. An rms noise specification over a given bandwidth allows peak-to-peak predictions for gaussian noise (peak-to-peak values greater than 7x rms will probably occur less than 0.1% of the time). However, both peak-to-peak and rms noise specs should be looked at, since large spikes could be present on the output of a chopper-stabilized amplifier, or could be coupled into the analog portion of the system. These spikes, if narrow, will contribute little to driving the rms noise out of spec, but could nevertheless be considerably greater than 7x rms. If a DAC having spike noise on its output were used in a display system, the noise would cause distortion of the pattern, and loss of useful resolution.

Offset. For almost all bipolar converters (e.g., ±10 volts output) instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference, because the ½ scale offset completely cancels the weight of the MSB at zero, independently of the amplitude of both.

"ON" Resistance. "ON" resistance of a device such as a FET, when used as a switch performing a function (such as multiplexing), refers to the ohmic resistance while turned on. For multiplexer service, a few hundred ohms or less will usually provide adequate accuracy. For other switching service, such as in a DAC, values of 10 ohms or less are desirable.

Power-Supply Sensitivity. The sensitivity of a converter to changes in the power supplies is normally expressed in terms of percent change in analog value (D/A output, A/D input) for a 1% change in power supply, e.g., $0.05\%/\%\Delta V_S$. As a rule, for a good converter, the fractional change in scale factor should be well below the equivalent of ±½LSB for a 3% change in power-supply voltage. When power-supply voltage changes affect conversion accuracy excessively, the key culprit is often a marginal "constant-current-circuit" for the reference diode.

Quad-Slope Converter. This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme results in an extremely accurate converter. For example, the 13-bit single-chip AD7550 is a CMOS quad-slope A/D converter with tempco (gain and zero temperature coefficients) less than 1ppm/°C.

Quantizing Uncertainty (or "Error"). The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of ±½LSB, associated with the *resolution,* in addition to the actual conversion errors. This uncertainty is a property of the *system* resolution.

Relative Accuracy. Relative accuracy error is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).

The "discrete points" of a D/A transfer characteristic are measured by the actual analog outputs. The "discrete points" of an A/D transfer characteristic are the midpoints of the quantization bands at each code (see Absolute Accuracy).

Resolution. Nominal Resolution is the relative value of the LSB, or 2^{-n} for binary devices, for n-bit converters. It may be expressed as 1 part in 2^n, as a percentage, in parts-per-million, or simply by "n bits." *Useful resolution* (not usually specified explicitly) is the smallest uniquely-distinguishable bit for all conditions of required operation (time, temperature, etc.) For example, a "12-bit" converter may have a useful resolution, over its temperature range, of only 10 bits. Useful resolution of DAC's and devices using them (including ADC's) is limited by the *relative accuracy,* but resolution need not limit accuracy. For example, a

4-bit D/A converter used in a programmable power supply has 16 levels, but it could have a required accuracy within 0.01% (absolute and/or relative). Note that low-cost completely-monolithic 8-bit DAC's need not necessarily have sufficient accuracy for such an application, although their resolution is more than adequate.

Settling Time. This is the time it takes for a DAC to settle for a full-scale code change, usually to within the analog equivalent of ±½LSB. For some applications, e.g., in staircase waveform generation, another important specification is the settling time for a single LSB change (at the major carry, and elsewhere).

Slew(ing) Rate. A limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of more than a few volts/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a modern D/A converter is usually limited by the slew rate of the amplifier used at its output. Slew rate magnitude is usually a guide (but by no means infallible) to settling time.

Stability. In a well-designed intelligently-applied converter, *dynamic stability* is never a serious question. The term *stability* usually connotes the insensitivity of a converter's characteristics to time, temperature, etc. All measurements of instability are difficult and time-consuming (especially in high-resolution devices), but instabilities vs. temperature are sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see *temperature coefficient).*

Successive Approximations. A method of comparing an unknown against a group of weighted references (usually binary), capable of high speed. The process of successive approximations in an A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights, such as 1 gram, ½ gram, ¼ gram, etc.

Switching Time. In a D/A converter, the switching time is the time taken for an analog switch to change to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time.

Temperature Coefficient (See also *Differential-Nonlinearity Temperature Coefficient*). Temperature coefficients of gain and offset are defined in terms of the "average" deviation over a range of temperature variation, i.e. $(\epsilon_{T_1} - \epsilon_{T_2})/(T_1 - T_2)$. For specified temperature ranges that extend from below room temperature to above room temperature, the device is zeroed and calibrated at room temperature, and the temperature coefficient for the "high" range $(T_H - T_A)$ and for the "low" range $(T_R - T_A)$ are both compared with the specification; both must be better than specified.

a. Gain TC This is affected by the reference zener (< 5ppm/°C for a good diode) and the reference circuitry, including the reference amplifier and switches (3ppm/°C in very good converters). The total gain (or scale factor) change is specified in ppm/°C.

b. Zero TC (unipolar converters) The zero stability of a unipolar DAC is almost entirely governed by the output amplifier's zero stability. Since output amplifiers are usually employed essentially as current-to-voltage converters, they operate at low values of closed-loop gain, and the zero TC is not greatly affected by the choice of programmable gain setting (i.e., 0-5V or 0-10V). Zero TC is usually expressed in μV/°C. Zero TC in ADC's is generally dependent only on the zero stability of the input buffer amplifier (if included) and the comparator and is expressed in μV/°C, referred to the input.

c. Zero TC (bipolar converters) Converters that use offset-binary coding are "zero" set at the all-bits-off point, and their scale factor is set at either all-bits-on, or (for more precise zero) at the MSB transition. However, the zero TC is measured at the MSB transition (analog zero). It is affected by the reference TC, the tracking of the offset reference, and the tracking of the bipolar-offset and gain-setting resistors. For such precision DAC types as AD561, which use the same reference for both the scale factor and the MSB offset, and monolithic resistor networks (with their excellent tracking), the zero-TC specification differs little for both the unipolar and bipolar connections.

Zero Setting. The zero level of a unipolar DAC is set to zero volts at the code corresponding to 0V. The LSB transition of an ADC is offset by ½ LSB, so that all subsequent transitions ideally occur midway between the nominal code values. (See also *offset* and *zero TC.*)

SYSTEM-COMPONENT SELECTION PROCESS

The most natural process for selection of appropriate off-the-shelf components to meet a system requirement involves a method of "successive approximations:" Choose the least costly device that meets the most significant requirements, and perform an error analysis to check its adequacy.

If its performance seems far in excess of that needed (at possibly excessive cost), or inadequate in some respects, inspect the discrepancies for possible design tradeoffs, make a new choice (if necessary) and repeat the analysis. Remember, though, that in a maturing industry, costs can be expected to decline. *It is often less costly, in the long run, to go for better performance (rather than lowest possible cost) in the initial stages of a design.* Also, efforts aimed at reducing the cost of any element of a system should bear in mind the relationship of its cost relative to that of the entire project.

In fact, where new designs are concerned, and early results are essential, unless one is an experienced system designer with plenty of component and manufacturing experience (if quantities are involved), it is usually good judgement to ignore initial cost (within the limits of good sense) and go for performance, convenience, and the highest level of system integration that the budget will allow (see Chapter I-4).

TYPICAL CONVERTER CLASSIFICATIONS

Once the problem is defined and the key specifications have been determined, one is still faced with the question of narrowing the choices to devices (converters) likely to "fill the bill" as rapidly as possible, so as to conserve the time needed for actual evaluation.

The selection guides from the 1977 Analog Devices Short-Form catalog are useful for this purpose and are reproduced on the following 6 pages for the convenience of our readers. They are classified by family (a/d, d/a, v/f, etc.) and by technological groupings (IC's, modules), and within that grouping, by salient specifications (resolution, linearity error, settling time, gain tempco, etc.) They are up-to-date as of Spring, 1977.*

AN EXAMPLE OF THE SELECTION AND VERIFICATION PROCESS†

A computer data-acquisition system is to be assembled to process data from a number of strain gages. Signal-conditioning hardware, to be purchased with the gages, delivers ±10V full-scale signals with 10-ohm source impedance. The signal channels must be sequentially scanned in no more than 50 microseconds per channel. Maximum allowable error of the system is about 0.1% of full scale. System logic is to be TTL, and hardware may work in either binary or 2's complement code. Parallel data readout will be used.

Probable temperature range in the equipment cabinets (including equipment temperature rise) is +25°C to +55°C. Sufficient power at both ±15V and +5V is available, but the regulation of the ±15V supply is 150mV.

The objective: specify a set of conversion components having appropriate accuracy and speed.

FIRST APPROXIMATION

A useful rule of thumb that usually provides satisfactory results is this: For the critical specs of a multi-component system, choose each component to perform roughly 10 times better

*Readers of this book are invited to communicate with ADI or our representatives for more recent listings, or to receive additional product suggestions for a given application.

†For maximum tutorial benefit, to avoid clutter, and to fit the available space, some of the less-salient sources of error have been intentionally omitted. If there are any that you're concerned about for your application but don't see here, we invite you to communicate with out Applications Engineers.

CONVERTER ICs: DIGITAL-TO-ANALOG

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Description	Resolution	Accuracy	Differential Nonlinearity	Gain T.C.	Inputs	Output	Power Dissipation	Temp. Range*	Package
AD559K	8-bit DAC, replaces	8-Bits	±0.19% max	±1/2LSB max	20ppm/°C	TTL	Unipolar	280mW max	C	16 Pin DIP
AD559S	Motorola 1408/1508	8-Bits	±0.19% max	±1/2LSB max	20ppm/°C	TTL		280mW max	M	16 Pin DIP
AD7520JN/JD	10-bit monolithic	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	16 Pin DIP
AD7520SD	CMOS multiplying	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	CMOS	Bipolar	20mW	M	16 Pin DIP
AD7520KN/KD	DAC	10-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	C/I	16 Pin DIP
AD7520TD		10-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	M	16 Pin DIP
AD7520LN/LD		10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	16 Pin DIP
AD7520UD		10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	M	16 Pin DIP
AD7521JN/JD	12-bit, monolithic	12-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	18 Pin DIP
AD7521SD	CMOS multiplying	12-Bits	±0.2% max	±0.4% max	10ppm/°C max	CMOS	Bipolar	20mW	M	18 Pin DIP
AD7521KN/KD	DAC	12-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	C/I	18 Pin DIP
AD7521TD		12-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	M	18 Pin DIP
AD7521LN/LD		12-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	18 Pin DIP
AD7521UD		12-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	M	18 Pin DIP
AD7522JN/JD	10-bit, monolithic	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	28 Pin DIP
AD7522SD	CMOS multiplying	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	CMOS	Bipolar	20mW	M	28 Pin DIP
AD7522KN/KD	DAC with micro-	10-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	C/I	28 Pin DIP
AD7522TD	processor com-	10-Bits	±0.1% max	±0.2% max	10ppm/°C max			20mW	M	28 Pin DIP
AD7522LN/LD	patible input buffer	10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	28 Pin DIP
AD7522UD	& holding register	10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	M	28 Pin DIP
AD7530JN/JD	Low cost 10-bit	10-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	16 Pin DIP
AD7530KN/KD	monolithic CMOS	10-Bits	±0.1% max	±0.2% max	10ppm/°C max	CMOS	Bipolar	20mW	C/I	16 Pin DIP
AD7530LN/LD	multiplying DAC	10-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	16 Pin DIP
AD7531JN/JD	Low cost 12-bit	12-Bits	±0.2% max	±0.4% max	10ppm/°C max	TTL/	Unipolar/	20mW	C/I	18 Pin DIP
AD7531KN/KD	monolithic CMOS	12-Bits	±0.1% max	±0.2% max	10ppm/°C max	CMOS	Bipolar	20mW	C/I	18 Pin DIP
AD7531LN/LD	multiplying DAC	12-Bits	±0.05% max	±0.1% max	10ppm/°C max			20mW	C/I	18 Pin DIP
AD561J	10-bit DAC	10-Bits	±0.05% max	±0.05%	80ppm/°C max	TTL/	Unipolar/	290mW max	C	16 Pin DIP
AD561K	with reference,	10-Bits	±0.025% max	±0.05% max	30ppm/°C max	CMOS	Bipolar	290mW max	C	16 Pin DIP
AD561S	monotonic	10-Bits	±0.05% max	±0.05%	60ppm/°C max			290mW max	M	16 Pin DIP
AD561T	performance	10-Bits	±0.025% max	±0.05% max	30ppm/°C max			290mW max	M	16 Pin DIP
AD562K	12-bit DAC, mono-	12-Bits	±0.006% max	±0.012%	5ppm/°C max	TTL/	Unipolar/	475mW max	C	24 Pin DIP
AD562A	tonic performance	12-Bits	±0.006% max	±0.012%	5ppm/°C max	CMOS	Bipolar	475mW max	I	24 Pin DIP
AD562S		12-Bits	±0.006% max	±0.012%	5ppm/°C max			475mW max	M	24 Pin DIP
AD563J	12-bit DAC with	12-Bits	±0.012% max	±0.012% max	30ppm/°C max	TTL/	Unipolar/	475mW max	C	24 Pin DIP
AD563K	reference, monotonic	12-Bits	±0.006% max	±0.012% max	20ppm/°C max	CMOS	Bipolar	475mW max	C	24 Pin DIP
AD563S	performance	12-Bits	±0.006% max	±0.012% max	30ppm/°C max			475mW max	M	24 Pin DIP
AD563T		12-Bits	±0.006% max	±0.012% max	10ppm/°C max			475mW max	M	24 Pin DIP

*Note: C = 0 to +70°C I = -25°C to +85°C M = -55°C to +125°C Suffix N – Plastic Suffix D – Ceramic

CONVERTER ICs: ANALOG-TO-DIGITAL

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Description	Resolution	Accuracy	Differential Nonlinearity	Gain T.C.	Conversion Time	Power Dissipation	Temp. Range*	Package
AD7570JD	8 & 10-bit, CMOS,	8-Bits	±0.19% max	No missing	10ppm/°C max	20μs	20mW	C	28 Pin DIP
AD7570LD	successive approxi-	10-Bits	±0.05% max	codes	10ppm/°C max	20μs	20mW	C	28 Pin DIP
	mation A/D								
AD7550BD	13-bit, quad slope A/D	13-Bits	±0.006% max	No missing codes	1ppm/°C	40ms	9mW	C	40 Pin DIP
AD572A	12-bit bipolar A/D	12-Bits	±0.012% max	±½LSB max	30ppm/°C max	25μs max	900mW	I	32 Pin
AD572B	with reference,	12-Bits	±0.012% max	No missing	15ppm/°C max	25μs max	900mW	I	Metal
AD572S	comparator, buffer amplifier	12-Bits	±0.012% max	codes	25ppm/°C max**	25μs max	900mW	M	DIP

*Note: C = 0 to +70°C
I = -25°C to +85°C
M = -55°C to +125°C

**±15ppm/°C max for temperature range -25°C to +85°C

CONVERTER ICs: VOLTAGE-TO-FREQUENCY

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Description	Input	Output	Nonlinearity (10kHz)	Quiescent Current	Temp. Range*	Package
AD537J	Low cost	±10V	0.001 to 100kHz	0.15% max	1.2mA	C	14 Pin DIP
AD537K	monolithic V/F	±10V	0.001 to 100kHz	0.07% max	1.2mA	C	14 Pin DIP
AD537S	converter	±10V	0.001 to 100kHz	0.07% max	1.2mA	M	14 Pin DIP

*Note: C = 0 to +70°C I = -25°C to +85°C M = -55°C to +125°C

CONVERTER MODULES: DIGITAL-TO-ANALOG

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Description[2]	Model	Resolution	Linearity Error	Settling Time to % Accuracy for F.S. Step	Gain TC	Size (Inches)	Input Code Options[1]
General Purpose	DAC-10Z	10 bits	±0.05% max	5μs to ±0.05%	±30ppm/°C	2 x 2 x 0.4	BIN, OBN
	MDA-10Z	10 bits	±0.05% max	300ns to ±0.05%	±30ppm/°C	2 x 2 x 0.4	BIN, OBN
	DAC-12QZ	12 bits/3 digits	±0.0125%	5μs to ±0.01%	±30ppm/°C max	2 x 2 x 0.4	C-B, COB, CBD
	DAC1118	12 bits/3 digits	±0.0125% max	5μs to ±0.01%	±30ppm/°C max	2 x 4 x 0.4	BIN, BCD, OBN, 2SC
	DAC1009	12 bits/3 digits	±0.0125% max	4μs to ±0.01%	±11ppm/°C	2 x 2 x 0.4	BIN, OBN, BCD
High Performance	DAC-8QS	8 bits/2 digits	±0.2%	5μs to ±0.01%	±7ppm/°C max	2 x 2 x 0.4	C-B, COB, CBD
	DAC-10QS	10 bits	±0.05%	5μs to ±0.01%	±7ppm/°C max	2 x 2 x 0.4	C-B, COB
	DAC-12QS	12 bits/3 digits	±0.0125%	5μs to ±0.01%	±7ppm/°C max	2 x 2 x 0.4	C-B, COB, CBD
	DAC-8QM	8 bits/2 digits	±0.2%	5μs to ±0.01%	±7ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	DAC-10QM	10 bits	±0.05%	5μs to ±0.01%	±7ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC
	DAC-12QM	12 bits/3 digits	±0.0125%	5μs to ±0.01%	±7ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	DAC1132	12 bits	±0.0125%	2μs to ±0.01%	±10ppm/°C max	2 x 2 x 0.4	BIN, OBN
High Speed	DAC-10DF	10 bits	±0.05% max	200ns max to ±0.05%	±50ppm/°C max	4.5 x 6	OBN, 2SC
	MDA-8F	8 bits	±0.2%	40ns to ±0.05%	±25ppm/°C	2 x 4 x 0.4	C-B, COB
	MDA-10F	10 bits	±0.05%	40ns to ±0.05%	±25ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC1106-001	8 bits	±0.2%	25ns to ±0.2%	±10ppm/°C	2 x 2 x 0.4	BIN, OBN
	DAC1106-002	10 bits	±0.05%	50ns to ±0.05%	±10ppm/°C	2 x 2 x 0.4	BIN, OBN
	DAC1108	12 bits	±0.0125% max	150ns to ±0.01%	±30ppm/°C	2 x 2 x 0.4	BIN, OBN
High Resolution	DAC-14QG[4]	14 bits	±0.003%	250μs to ±0.0015%	±7ppm/°C	4.5 x 4.75	BIN, OBN, 2SC, SMB
	DAC-16QG[4]	16 bits/4 digits	±0.0015%	250μs to ±0.0015%	±7ppm/°C	4.5 x 4.75	BIN, OBN, 2SC, SMB, SMD, BCD
	DAC-14QM	14 bits	±0.003%	250μs to ±0.0015%	±15ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC-16QM	16 bits/4 digits	±0.0015%	250μs to ±0.0015%	±15ppm/°C	2 x 4 x 0.4	C-B, COB, CBD
	DAC1136J[5]	16 bits	±0.0015%	18μs to ±0.0015%	±5ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC1136K[5]	16 bits	±0.00076%	30μs to ±0.00076%	±5ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC1138J[5]	18 bits	±0.00038%	60μs to ±0.00038%	±1ppm/°C	2 x 4 x 0.4	C-B, COB
	DAC1138K[5]	18 bits	±0.00019%	230μs to ±0.00038%	±1ppm/°C	2 x 4 x 0.4	C-B, COB
Low Power	DAC1122J	12 bits	±0.01% max	20μs to ±0.01%	±30ppm/°C	2 x 3 x 0.4	BIN, OBIN, C-B, COB
	DAC1122K	12 bits	±0.01% max	10μs to ±0.01%	±15ppm/°C	2 x 3 x 0.4	BIN, OBIN, C-B, COB
Multiplying[3]	DAC-8M	8 bits	±0.2%	10μs to ±0.2%	±25ppm/°C max	2 x 2 x 0.4	BIN, OBN
	DAC-12M	12 bits	±0.02%	15μs to ±0.01%	±5ppm/°C max	2 x 2 x 0.4	BIN, OBN
	MDA-11MF	11 bits	±0.03%	1μs to ±0.01%	±30ppm/°C	2 x 4 x 0.4	BIN, OBN
	DAC1125	12 bits	±0.0125% max	3μs to ±0.01%	±3ppm/°C	2 x 2 x 0.4	C-B, OBN, 2SC
Herm. Sealed	MDA-12QD	12 bits	±0.0125%	3μs to ±0.01%	±15ppm/°C	1 x 1.5 x 0.4	C-B, COB
High Reliability	DAC1112	12 bits	±0.0125%	5μs to ±0.01%	±7ppm/°C max	2 x 2 x 0.4	C-B, COB
	DAC1117	12 bits	±0.0125% max	4μs to ±0.01%	±15ppm/°C max	1 x 1.5 x 0.4	C-B, COB

CONVERTER MODULES: ANALOG-TO-DIGITAL

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Description[2]	Model	Resolution	Linearity Error	Conversion Time	Gain TC	Size (Inches)	Output Code Options[1]
General Purpose	ADC-8S	8 bits/2 digits	±0.2% max	1ms max	±60ppm/°C	2 x 3 x 0.4	BIN, OBN, 2SC, BCD
	ADC-10Z	10 bits	±0.05% max	20μs max	±40ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC
	ADC-12QZ	12 bits	±0.0125% max	40μs max	±30ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC
High Performance	ADC-8QM	8 bits/2 digits	±0.2%	18μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	ADC-10QM	10 bits	±0.05%	22μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN,2SC
	ADC-12QM	12 bits/3 digits	±0.0125%	25μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	ADC-8QU	8 bits/2 digits	±0.2%	6.4μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	ADC-10QU	10 bits	±0.05%	8μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC
	ADC-12QU	12 bits/3 digits	±0.025%	15μs max	±5ppm/°C	2 x 4 x 0.4	BIN, OBN, 2SC, BCD
	ADC1133	12 bits	±0.0125% max	25μs max	±7.5ppm/°C	2 x 2 x 0.4	BIN, OBIN, 2SC
Dual Slope	ADC1100	11 bits/3½ digits	±0.05% ±1 bit	42ms max	±50ppm/°C max	2 x 4 x 0.4	SMB, SMD
	ADC-141	14 bits	±0.01% ±1 bit	40ms max	±5ppm/°C	3 x 4 x 0.4	SMB
	ADC-171	4½ digits	±0.01% ±1 bit	40ms max	±5ppm/°C	3 x 4 x 0.4	SMD
	ADC1105J	up to 1:2,000	±0.1% ±1 bit	(depends on	±20ppm/°C max	2 x 4 x 0.6	(any sign-
	ADC1105K	up to 1:20,000	±0.01% ±1 bit	the resolution)	±5ppm/°C max	2 x 4 x 0.6	magnitude code)
High Speed	ADC1102	12 bits	±0.0125% max	8μs max	±10ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC
	ADC1103-001	8 bits	±0.2% max	1μs max	±10ppm/°C max	2 x 4 x 0.8	BIN, OBN, 2SC
	ADC1103-002	10 bits	±0.05% max	1.5μs max	±10ppm/°C max	2 x 4 x 0.8	BIN, OBN, 2SC
	ADC1103-003	12 bits	±0.025% max	3.5μs max	±10ppm/°C max	2 x 4 x 0.8	BIN, OBN, 2SC
	ADC1109	10 bits	±0.05%	4μs max	±30ppm/°C	2 x 3 x 0.4	BIN, OBN, 2SC
High Resolution	ADC-16Q	16 bits	±0.0015%	400μs	±8ppm/°C max	4.5 x 6	BIN, OBN, 2SC
Low Power,	ADC-12QL/J	12 bits	±0.01%	85-130μs	±50ppm/°C max	3.65 x 4.1	BIN, OBN
	ADC-12QL/K	12 bits	±0.01%	85-130μs	±20ppm/°C max	3.65 x 4.1	BIN, OBN
	ADC1121	12 Bits	±0.0125% max	52μs max	±20ppm/°C	2 x 4 x 0.4	BIN, OBIN, 2SC
	ADC1123	10 bits	±0.05% max	65-90μs	±40ppm/°C	3.65 x 4.1	BIN, OBN
High Reliability	ADC1111	12 bits	±0.0125%	25μs max	±7ppm/°C max	2 x 4 x 0.4	BIN, OBN, 2SC

NOTES:

1. Logic Codes: BIN, binary; C-B, complementary binary; OBN, offset binary; COB, complementary offset binary; BCD, binary coded decimal; CBD, complementary BCD; 2SC, two's complement; SMB, sign-magnitude binary; SMD, sign-magnitude BCD.
2. Standard temperature range on most converters is 0 to +70°C, with storage temperature from -55°C to +125°C. Many models are available in an extended operating temperature version at extra cost. The extended operating temperature range is normally -55°C to +125°C for 8 and 10 bit devices and -25°C to +85°C for 12 bit devices.
3. Analog input range of DAC-8M, DAC-12M, and DAC1125 is ±10V; input range of MDA-11MF is 0 to -10V.
4. Also available as a card mounted assembly with input code option (see DAC16QG) and output amplifiers model 44K or model 234L.

CONVERTER MODULES: DIGITAL-TO-SYNCHRO

SPECIFICATIONS (typical @ +25°C and ±15VDC and +5VDC unless otherwise noted)

	Input Resolution Bits	Accuracy (See Note) Arc-Min	Signal & Ref. Freq. Hz	Signal Level V rms	Reference Level V rms	Minimum Output Load Z_{LL} Ohms	Output VA	Size (See Note)	Temp Range (See Note)	Settling Time Micro-Sec
DSC1605511	14	±4	400	11.8	26	107	1.3	A	C	100
DSC1605512	14	±4	400	90	115	6200	1.3	A	C	100
DSC1605507 plus STM1634522	14	±4	60	90	115	6200	1.3	A plus E	C	100
DSC1605711	14	±4	400	11.8	26	107	1.3	A	M	100
DSC1605712	14	±4	400	90	115	6200	1.3	A	M	100
DSC1605707 plus STM1634722	14	±4	60	90	115	6200	1.3	A plus E	M	100
DSC1606511	10	±30	400	11.8	26	107	1.3	A	C	80
DSC1606512	10	±30	400	90	115	6200	1.3	A	C	80
DSC1606507 plus STM1633522	10	±30	60	90	115	6200	1.3	A plus E	C	80
DSC1606711	10	±30	400	11.8	26	107	1.3	A	M	80
DSC1606712	10	±30	400	90	115	6200	1.3	A	M	80
DSC1606707 plus STM1633722	10	±30	60	90	115	6200	1.3	A plus E	M	80
DSC1607517	16	±1	50–1000	7.5	2	2000	N/A	A	C	150
DSC1607717	16	±1	50–1000	7.5	2	2000	N/A	A	I	150

Sizes: A is 3.125" x 2.625" x 0.8"
E is 4.5" x 2.0" x 1.5"

Temp Ranges: C is 0°C to +70°C
I is -55°C to +85°C
M is -55°C to +105°C
full power to +85°C
½ power at +105°C

Accuracy applies: over operating temp range and ±10% reference frequency and amplitude changes and 10% harmonic distortion and ±5% power supply variation and any balanced load from no load to full load.

DSC1605 and DSC1606 models shown are synchro outputs. Consult factory for resolver versions.
DSC1607 is resolver form, without power amplifiers.

CONVERTER MODULES: SYNCHRO-TO-DIGITAL

SPECIFICATIONS (typical @ +25°C and ±15VDC and +5VDC unless otherwise noted)

	Output Resolution Bits	Accuracy (See Note) Arc-Min	Signal Ref. Freq. Hz	Signal Level V rms	Reference Level V rms	Tracking Rate Deg/Sec	Acceleration for 1LSB Error Deg/Sec^2	Size (See Note)	Temp Range (See Note)	Frequency Range Hz
SDC160251Z	14	±4	400	11.8 or 90	26 or 115	2800	240	A	C	350–1500
SDC160261Z	14	±4	400	11.8 or 90	26 or 115	2800	240	A	M	350–1500
SDC1602507 plus STM1631522	14	±4	60	90	115	430	6	A plus D	C	50–450
SDC1602607 plus STM1631622	14	±4	60	90	115	430	6	A plus D	M	50–450
SDC160351Z	10	±30	400	11.8 or 90	26 or 115	2880	480	A	C	350–1500
SDC160361Z	10	±30	400	11.8 or 90	26 or 115	2880	480	A	M	350–1500
SDC1603507 plus STM1630522	10	±30	60	90	115	2880	48	A plus D	C	50–450
SDC1603607 plus STM1630622	10	±30	60	90	115	2880	48	A plus D	M	50–450
SDC1604507 plus STM163251Z	16	±1.3	400	11.8 or 90	26 or 115	360	60	A plus D	C	350–450
SDC1604707 plus STM163271Z	16	±2	400	11.8 or 90	26 or 115	360	60	A plus D	I	350–450
SDC178651Z	10	±30	400	11.8 or 90	26 or 115	8640	34,000	A	C	350–1500
SDC178661Z	10	±30	400	11.8 or 90	26 or 115	8640	34,000	A	M	350–1500
SDC1786507 plus STM1630522	10	±30	60	90	115	1260	850	A plus D	C	50–450
SDC1786607 plus STM1630622	10	±30	60	90	115	1260	850	A plus D	M	50–450
SDC170051Z	12	±8.5	400	11.8 or 90	26 or 115	12,960	10,800	B	C	350–1600
SDC170052Z	12	±8.5	60	11.8 or 90	26 or 115	1800	200	B	C	50–1200
SDC170054Z	12	±8.5	2600	11.8 or 90	26 or 115	27,000	54,000	B	C	2300–2700
SDC170061Z	12	±8.5	400	11.8 or 90	26 or 115	12,960	10,800	B	M	350–1600
SDC170062Z	12	±8.5	60	11.8 or 90	26 or 115	1800	200	B	M	50–1200
SDC170064Z	12	±8.5	2600	11.8 or 90	26 or 115	27,000	54,000	B	M	2300–2700
SDC170451Z	14	±5 ±1LSB	400	11.8 or 90	26 or 115	3240	720	B	C	350–1000
SDC170452Z	14	±5 ±1LSB	60	11.8 or 90	26 or 115	500	16	B	C	50–500
SDC170461Z	14	±5 ±1LSB	400	11.8 or 90	26 or 115	3240	720	B	M	350–1000
SDC170462Z	14	±5 ±1LSB	60	11.8 or 90	26 or 115	500	16	B	M	50–500

Sizes: A is 3.125" x 2.625" x 0.8"
B is 3.125" x 2.625" x 0.4"
D is 3.125" x 1.5" x 1.0"

Temp Ranges: C is commercial 0°C to +70°C
I is industrial -55°C to +85°C
M is military -55°C to +105°C

Accuracy: Applies over operating temp range and ±10% frequency variation and ±10% signal and ref amplitude variation and 10% signal and ref harmonic distortion and ±5% power supply variation.

Z is replaced by a number, when ordering, to specify input type:
Z = 1 signifies synchro, signal 11.8V, reference 26V
Z = 2 signifies synchro, signal 90V, reference 115V
Z = 8 signifies resolver, signal 11.8V, reference 26V

Consult factory for other options.

CONVERTER MODULES: FREQUENCY-TO-VOLTAGE

SPECIFICATIONS (Typical @ +25°C and V_S = ±15VDC unless otherwise noted)

Model	10kHz Full Scale 451J (K) (L)	100kHz Full Scale 453J (K) (L)
Frequency Input		
Frequency Range	DC to 10kHz min	DC to 100kHz min
Overrange	10% min	10% min
Waveforms	← Sine, Square, Triangle, Pulse Train →	
Threshold	+1.4V	+1.4V
With External Adjustment	0V to ±12V	0V to ±12V
Hysteresis	±50mV	±100mV
Levels (TTL Compatible) High	+1.45V to +12V	+1.5V to +12V
Low	-12V to +1.35V	-12V to +1.3V
Accuracy		
Nonlinearity		
F_{IN} = 1Hz to 11kHz	±0.03%(0.015%)(0.008%) max	— —
F_{IN} = 1Hz to 110kHz	— —	±0.03%(0.015%)(0.008%) max
Gain vs. Temperature. (0 to +70°C)	±100 (50) (50) ppm/°C max	±100 (50) (50) ppm/°C max
Response		
Step Response to ±0.5% of Final Value		
F_{IN} = DC to Full Scale	4ms	0.8ms
F_{IN} = Full Scale to DC	30ms	4ms
Output		
Voltage (F_{IN} = Full Scale).	+9.85V min; +9.95V max	+9.85V min; +9.95V max
Current (E_O = +10V, -10V)	(+20, -2)mA min	(+20, -2)mA min
Offset Voltage @ +25°C	±7.5mV max	±7.5mV max
vs. Temperature (0 to +70°C)	±30μV/°C max	±30μV/°C max
Power Supply		
Voltage, Rated Performance	±15VDC	±15VDC
Current, Quiescent	(+10, -8)mA	(+10, -8)mA
Temperature Range		
Rated Performance	0 to +70°C	0 to +70°C
Case Size	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"

CONVERTER MODULES: VOLTAGE-TO-FREQUENCY

SPECIFICATIONS (typical @ +25°C and V_S = ±15VDC unless otherwise noted)

Model	Economy 10kHz 456J (K)	High Performance 10kHz 450J (K)	Versatile 20kHz 454J (K)	Economy 100kHz 452J (K) (L)	Low Drift 100kHz 458J (K) (L)	Low Drift 1MHz 460J(K) (L)
Analog Input						
Voltage Signal Range	0 to +10V, min	0 to +10V, min	0 to +20V, min	0 to +10V, min	0 to ±10V, min	0 to ±10V, min
Current Signal Range	— —	— —	0 to +0.67mA, min	0 to +0.5mA, min	0 to +0.5mA, min	0 to +1.0mA min
Overrange	50%, min	50%, min	10%, min	10%, min	10%, min	10%, min
Accuracy						
Nonlinearity, max						
Voltage Input	±0.03%(±0.2%)	±0.01%(±0.005%)	±0.01%(±0.005%)	±0.015%	±0.01%	±0.015%
Current Input	— —	— —	±0.01%(±0.005%)	±0.015%	±0.01%	±0.015%
Gain vs. temperature, ppm/°C, max	±120(±80)	±50(±25)	±50(±25)	±150(±100)(±50)	±20(±10)(±5)	±50(±25)(±15)
Input Offset Voltage	±10mV	±5mV, max	±5mV, max	±7.5mV, max	±10mV, max	±10mV, max
vs. Temperature (0 to +70°C)	±100μV/°C	±50(±25)μV/°C, max	±50(±25)μV/°C, max	±30μV/°C, max	±30μV/°C, max	±30μV/°C, max
Response						
Settling Time	120μs	120μs	120μs	22μs	22μs	15μs
Overload Recovery	15ms	15ms	22ms	1.5ms	10ms	1ms
Output						
Waveform	← TRAIN OF TTL/DTL COMPATIBLE PULSES →					
Pulse Width	50μs	50μs	25μs	6μs	5μs	0.5μs
Pulse Polarity	← POSITIVE →					
Logic "1" (HIGH) Level	← +2.4V, min →					
Logic "0" (LOW) Level	← +0.4V, min →					
Power Supply						
Voltage, Rated Performance	← ±15VDC →					
Current, Quiescent	(+15, -9)mA	(+15, -9)mA	(+15, -9)mA	(+25, -10)mA	(+25, -8)mA	(+35, -8)mA
Temperature Range						
Rated Performance	← 0 to +70°C →					
Case Size	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"	1.5" x 1.5" x 0.4"	2" x 2" x 0.4"	2" x 2" x 0.4"

IC SAMPLE-HOLD AMPLIFIERS

SPECIFICATIONS (typical @ +25°C)

	AD582K	AD582S	AD583K
Open Loop Gain $R_L = 2k\Omega$	25k min	25k min	25k min
Output Swing	±10V min	±10V min	±10V min
Gain Bandwidth	1.5MHz	1.5MHz	2MHz
Acquisition Time (0.1%) $A_V = 1$, $R_L = 2k$, $C_L = 50pF$	5μsec	5μsec	4μsec
Aperture Time	150nsec	150nsec	50nsec
Drift Current	50pA max	50pA max	50pA max
Charge Transfer	5pC max	5pC max	20pC max
Operating Temp.*	C	M	C

*C = 0 to +70°C; M = 55°C to +125°C

MODULAR SAMPLE-HOLD AMPLIFIERS

SPECIFICATIONS (typical @ +25°C)

Model	Product Classification	Acquisition Time To % Accuracy	Droop Rate	Aperture Delay	Aperture Jitter	Input Resistance	Size (inches)
SHA-1A	General Purpose	5μs max to ±0.01%	±50μV/ms max	40ns max	5ns max	$10^{12}\Omega$	2 x 2 x 0.4
SHA1134		3.4μs to ±0.01%	±50μV/ms	50ns max	5ns max	$10^{7}\Omega$ min	1.125 x 2 x 0.4
SHA-2A	High Speed	500ns max to ±0.01%	±10μV/μs	10ns	0.25ns	$10^{11}\Omega$	2 x 3 x 0.4
SHA-3	Low Droop	75μs to ±0.01%	±10μV/ms	50ns	5ns	$10^{8}\Omega$	1.125 x 2 x 0.4
SHA-4		75μs to ±0.01%	±10μV/ms	50ns	5ns	$10^{8}\Omega$	1.125 x 2 x 0.4
SHA-5	Low Cost	15μs max to ±0.01%	±20μV/ms	40ns	4ns	$4 \times 10^{9}\Omega$	1.125 x 2 x 0.4
SHA-6	High Resolution	5ms max to ±0.00075%	±10μV/ms max	-1.7μs	10ns	$10^{9}\Omega$ min	2 x 4 x 0.4
SHA1114	High Reliability	500ns max to ±0.01%	±100μV/μs max	10ns	0.25ns	$10^{11}\Omega$	2 x 3 x 0.5

NOTES

[1] Gain of all SHA's is +1 except that the SHA-6 and SHA-2A can be connected for gains greater than unity: the SHA-2A can also be operated in the inverting mode.

[2] SHA-3 and SHA-4 differ only in that the SHA-4 settles much faster when switched from HOLD to SAMPLE. Settling time to ±1mV is 100μs for SHA-3 and 20μs for SHA-4.

CMOS MULTIPLEXERS

SPECIFICATIONS (T_A = +25°C, V_{SUPPLY} = ±15V unless otherwise noted)

Type[1]	Function	R_{ON}	Out Leakage	Temp[2] Range	Package
AD7501JN/JD	8-Channel MUX	300Ω, max	10nA, max	C/I	16-pin DIP
AD7501KN/KD			10nA, max	C/I	
AD7501SD			5nA, max	M	
AD7502JN/JD	Dual 4-Channel MUX	300Ω, max	5nA, max	C/I	16-pin DIP
AD7502KN/KD			5nA, max	C/I	
AD7502SD			3nA, max	M	
AD7503JN/JD	8-Channel MUX	300Ω, max	10nA, max	C/I	16-pin DIP
AD7503KN/KD			10nA, max	C/I	
AD7503SD			5nA, max	M	
AD7506JN/JD	16-Channel MUX	450Ω, max	20nA, max	C/I	28-pin DIP
AD7506KN/KD		450Ω, max	20nA, max	C/I	
AD7506SD/TD		400Ω, max	10nA, max	M	
AD7507JN/JD	Dual 8-Channel MUX	450Ω, max	10nA, max	C/I	28-pin DIP
AD7507KN/KD		450Ω, max	10nA, max	C/I	
AD7507SD/TD		400Ω, max	5nA, max	M	

[1] Suffix "N": plastic; Suffix "D": ceramic

[2] C: Commercial (0° to +70°C)
I: Industrial (-25°C to +85°C)
M: Military (-55°C to +125°C)

MODULAR MULTIPLEXER

SPECIFICATION SUMMARY (typical @ +25°C)

Model	MPX-8A
Channels	
Single-Ended	8[1]
Differential	4
Voltage Range	
Rated Operation	±10V
Overload Protection	±15V
Transfer Error	0.01%
Settling to 0.01%	<2μs
Cross Channel Coupling	<-80dB
Common Mode Rejection	
DC	120dB
60Hz	106dB
Package Dimensions	2" x 2" x 0.4"

[1]MPX-8A includes logic for expansion to 64 channels.

CMOS SWITCHES

SPECIFICATIONS (T_A = +25°C, V_{SUPPLY} = ±15V unless otherwise noted)

Type[1]	Function	R_{ON}	Off Leakage	Temp[3] Range	Package
AD7510DIJN/JD	Quad SPST Note 2	100Ω, max	5nA, max	C/I	16-pin DIP
AD7510DIKN/KD			5nA, max.	C/I	
AD7510DISD			3nA, max	M	
AD7511DIJN/JD	Quad SPST Note 2	100Ω, max	5nA, max	C/I	16-pin DIP
AD7511DIKN/KD			5nA, max	C/I	
AD7511DISD/TD			3nA, max	M	
AD7512DIJN/JD	Dual SPDT Note 2	100Ω, max	15nA, max	C/I	14-pin DIP
AD7512DIKN/KD			15nA, max	C/I	
AD7512DISD/TD			9nA, max	M	
AD7513JN/KN	Dual SPST	80Ω, max	5nA, max	C	14-pin DIP
AD7513JH/KH		80Ω, max	5nA, max	I	TO-100
AD7513SH/TH		70Ω, max	2nA, max	M	TO-100
AD7516JN/KN	Quad SPST Note 4	400/280Ω, max	100pA	C	14-pin DIP
AD7516 SD/TD		400/280Ω, max		M	
AD7519JN	Quad SPST Current Switch Note 5	100Ω, max	50nA	C	14-pin DIP

[1]Suffix N: plastic/Suffix D: ceramic/Suffix H: TO-100
[2]Dielectrically isolated-features latch free, overvoltage proof operation
[3]C: Commercial (0°C to +70°C
I: Industrial (-25°C to +85°C)
M: Military (-55°C to +125°C)
[4]VDD - VSS (supply voltages) = +15V
[5]VDD (supply voltage) = 8V

IC REFERENCES

SPECIFICATIONS

Model	Output Voltage	*Error, mV max T_{min}, T_{max}	Temp Range††
AD580J	2.500 ±3%	±90	C
AD580K	2.500 ±2%	±57	C
AD580L	2.500 ±2%	±54.3	C
AD580M	2.500 ±1%	±26.75	C
AD580S	2.500 ±3%	±100	M
AD580T	2.500 ±2%	±61	M
AD580U	2.500 ±1%	±29.5	M
AD2700L/U	10.000 ±0.025%	±5	I/M
AD2701L/U	-10.000 ±0.025%	±5	I/M
AD2702L/U	±10.000 ±0.025%	±5	I/M

*Including initial offset.

††C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C

than the overall desired performance. Thus, for a system that needs 0.1%-grade performance, use a 0.01% converter (12 bits) with compatible multiplexer and sample-hold

Reviewing the available A/D converters, we find ADC-12QM to be a possible choice. The ADC-12QM completes a conversion in 25μs. For sample-hold, the compatible SHA-1A is chosen, adding 5μs of settling time. Thus, the combination appears to be amply capable of meeting the 50μs/channel scanning requirement. Since the multiplexer will scan sequentially, its settling time is inconsequential. The multiplexer can be switched to the next address as soon as the SHA goes into *hold* on data from the current address. Thus it has at least 25μs to settle before a measurement is called for. For convenience, one may use the MPX-8A; the small 2" x 2" x 0.4" module fits into the packaging concept, and the built-in complete binary-address decoding makes it easy to work with.

ERROR ANALYSIS

It's clear that the MPX-8A, the SHA-1A, and the ADC-12QM generally meet the problem's requirements for speed and resolution. Now we must look further into the details of errors, to determine if the worst-case situation is within the allowable 0.1% system error.

Multiplexer

The switches of the MPX-8A, being MOSFET's, with variable-resistance channels, are not subject to voltage offset errors. Errors here will be due to two factors:

1. Leakage current into the *on* channel from the *off* channels develops an offset voltage across the source impedance.

   Leakage current @ 25°C 10nA
   Source impedance 10Ω
   Error voltage = $10 \times 10 \times 10^{-9} = 10^{-7}$ V (negligible

2. Transfer error due to voltage division across the MOSFET *on* resistance and input impedance of the SHA-1A:

   ON resistance 1000Ω maximum
   SHA-1A R_{in} $10^{12}\Omega$
   Divider ratio attenuation error: 10^{-9} (negligible)

Sample-Hold

1. Nonlinearity is 2mV over the 20V range, or 0.01%
2. Gain error of 0.05% maximum (and other similarly small initial gain errors in the system) may be compensated for overall when calibrating the system by setting the scale constant of the ADC. It is not considered as part of the error budget.
3. Input bias current of 10nA (max) causes an offset error voltage in the source resistance.

   Source resistance = 10Ω (source) + 1kΩ(MPX switch)
   Offset error = $10^3 \times 10^{-8} = 10\mu$V (negligible)

4. Offset vs. temperature = 25μV/°C

Since the temperature inside the housing may change by as much as 30°C, the total change over the range will be

$$25 \times 30 = 750\mu\text{V, or 75 ppm of } \pm 10\text{V}$$

An offset adjustment is provided for initial trimming.

5. Offset vs power supply = $100\mu\text{V}/\%\Delta V_s$

Since the supply may vary by 150mV or 1% of 15V, the error contribution is 100μV, or 0.001% of full scale.

By an analysis comparable to the above, we would normally also prepare a system timing diagram, and assign operate-and settling-time allowances. However, the components selected for this example have more than adequate settling time, even for 0.01% operation; consequently, we can overlook the need for a formal timing analysis to determine whether settling times are adequate.

Converter

1. Specified linearity error (relative accuracy) ½LSB, or 0.0125%

2. Quantizing uncertainty: ½LSB, or 0.0125%. This is a resolution limitation, not normally considered in the error budget.

3. Temperature errors
   a. Gain temperature coefficient: 5ppm/°C for 30°C
      5 x 30 = 150 ppm, or 0.015%
   b. Zero temperature coefficient: 5ppm/°C for 30°C
      5 x 30 = 150 ppm, or 0.015%

4. Power supply sensitivity error: 0.002%/%ΔV_s
For a 1% shift, the error is 20ppm

5. Differential nonlinearity temperature coefficient, 3ppm/°C.
For 30°C temperature change, error is 90ppm, less than ½LSB. Therefore, 12-bit monotonicity can be maintained, with no missing codes.

In this example, the worst-case arithmetic sum of these errors is 0.07%, and the rms sum is 0.03%. Since these values are reasonably conservative for a system with specified error of 0.1%, the designer may either rest with these choices and go on to the more-difficult hardware, software, interface, and wiring problems, or – if absolute-minimum cost or size of conversion hardware is an important objective – seek to reduce cost by considering a perhaps more marginal design.

Two approaches might be considered. The first would use integrated-circuit components, such as the AD572 12-bit A/D converter, the AD582 or AD583 sample-hold, and the AD7501 or AD7503 multiplexer. The compromises that this approach makes necessary would have to be determined and negotiated in terms of the advantages gained. On the other hand, one might consider a product embodying a higher level of integration, such as the DAS1128 data-acquisition subsystem (Chapter I-4). The advantages gained by this approach would include the consolidation of a number of specifications, the elimination of a number of system-design details, and possible savings in both space and initial cost.

CONCLUSION

In this chapter, we have sought to help the designer in his process of choosing a converter by providing checklists of relevant questions in making a choice, definitions of specifications and related features, a selection guide, and an example of selection and evaluation. We now go on to some considerations for what must be done to make the system work as expected.