Data Distribution

Chapter I-3

After analog data have been converted to digital form and have been duly stored, transmitted, or processed, the results of this handling, as well as some newly-created digital numbers, may be required once again in the "real world" of phenomena. In analog or digital form, they may be used to drive meters or motors, display information, stimulate devices under test, generate heat or light, modulate waveforms, sound the alarm, or – in short – they are converted from abstract numbers to the manipulation of energy.

The multiplexed digital output words are made available in serial order at an output register, for distribution to their destinations. Though an increasing number of real-world functions, such as numerical displays, stepping motors, printers, and the like, are effected by digital numbers (perhaps with "decoding," but without the interposition of electronic analog variables), there is still a widespread – and growing – use of electronic D/A converters in distribution systems. This chapter treats of those systems that use D/A converters.

FACTORS AFFECTING DISTRIBUTION-SYSTEM DESIGN

The configuration, choice of components and their specifications, the system timing, and location of multiplexing, depend, as with data acquisition, on

1. Number of channels
2. Settling time per channel
3. Update rate
4. Output resolution
5. Output linearity and accuracy
6. The nature of the loads
7. The cost function

There are a number of areas for decision by the system designer:

Digital signal readout: Serial paths or parallel paths? Serial words or parallel words?

Signal storage between updates: in digital or analog form? Registers or sample-holds? Single-rank or dual-rank? Sample-holds or inertia?

Multiplexing: Digital or analog? If digital, parallel or serial? If analog, with sample/holds or multiplex switching?

Update: Simultaneous, sequential, or random?

Conversion: At computer or at load? Single converter with analog multiplexing, or many converters with digital multiplexing?

Analog output: Voltage or current? Discrete values or smoothed? Permissible level of switching transients? Isolated or galvanically-connected circuitry?

Techniques to reduce costs: Combining sample-hold and multiplexing. Inertial filtering. Using low-precision DAC's in "slave" circuit for standardized calibration.

DIGITAL vs. ANALOG DISTRIBUTION

The systems designer has a choice between feeding data to analog actuating and indicating devices via either a D/A converter (with storage register) for each channel (Figure 1), or a single D/A converter, with a sample-hold circuit for each channel (Figure 2).

Once updated, a D/A converter-with-input-register will store an analog value indefinitely, or at least, for so long as the power is connected. By contrast, a sample-hold circuit, since it holds the analog data on a capacitor, is susceptible to a definite "droop" (positive or negative) in the analog output as the charge on the capacitor changes due to leakage across the switch, from the amplifier's summing point, or from the supplies (or perhaps even due to the capacitor's own leakage resistance or dielectric absorption). Thus, even though the data may not change at all, as is ideally the case for an aircraft simulator's altimeter in "straight & level" flight, it is necessary to update sample-hold circuits periodically to correct for output droop. On the other hand, so long as the data remains unchanged, a distribution system based on D/A converters (with registers) need not be periodically refreshed.

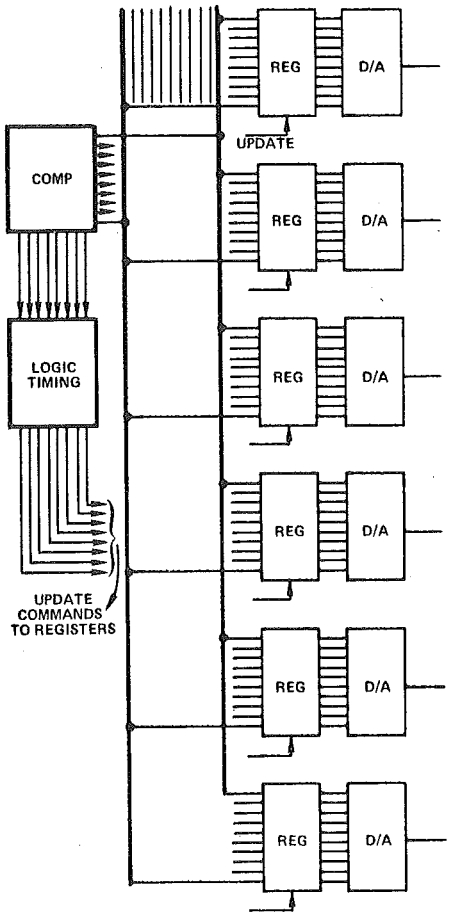

Figure 1. D/A Converter for each channel; parallel-word distribution.

The D/A converter's ability to store without error lays the foundation for an "updating by exception" rule, whereby the data channels are only updated if the *information* changes. Otherwise, the computer leaves the D/A unrefreshed.

A further consideration in the use of D/A converters vs. sample-hold circuits lies in the matter of allowing for acquisition and settling time. The data sheet for a typical data-distribution sample-hold circuit at reasonable cost may call for acquisition periods ranging from 2μs to 20μs or more. Thus, it is often necessary for the computer to remain connected to each channel for the duration of this acquisition period (unless buffered), which may use up appreciable main-frame time. By contrast, the storage register of a D/A con-

verter can be updated in a fraction of a microsecond, so it is quite conceivable that an entire 10-channel data-distribution system, using one D/A per channel, can be updated in the time required to refresh a single sample-hold circuit.

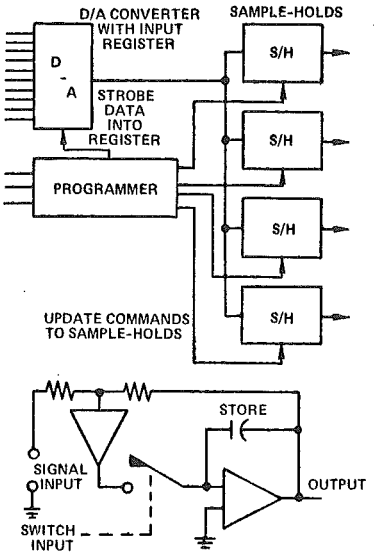

Figure 2. Sample-hold for each channel, with single fast, accurate D/A Converter. Multiplexing occurs by sampling each channel individually as its associated data appears on the input bus.

Offsetting some of the flexibility of the D/A-per-channel data-method is the cost of interconnecting the D/A's to the data source. Parallel data at the 10-bit level requires at least 12 conductors (10 data lines, ground, and command line) from the computer to the D/A converter, which, for fast transmission rates, requires costly multiple twisted pairs. If the D/A's are widely-distributed, as, for example, in a steel rolling mill, installation cost for the cable may easily be the largest single economic factor, far outweighing the cost of the D/A converters. Cable and installation costs can be reduced somewhat by introducing serial, instead of parallel data transmission. However, the penalty now lies in more-involved logic and added updating time (which may not be a problem at all), since each 10-bit channel requires at least 10 times as long to update. (See also SERDEX, in Chapter I-4).

CONVERTER-PER-CHANNEL DISTRIBUTION

Figure 1 illustrates the main ingredients of the distribution approach based on one D/A converter for every channel. Computer data is fed on a parallel bus to all D/A-converter input registers, while an update command is addressed individually to each register. Whenever the computer strobes a new data word into the data bus, it emits a command signal that causes one of the storage registers to accept this new word. A succession of parallel digital words and update commands then completes the data-refreshing cycle. The converters may be randomly addressed (and with varying numbers of data points per channel) or a computer may program sequential addresses, if the data is programmed to arrive in the same order.

Simultaneous Updating

In some instances – for example, in semiconductor test equipment – it is advantageous to update all analog channels simultaneously, thereby minimizing settling time in both the converter's output amplifiers and the IC device undergoing test. A data-distribution arrangement that eliminates delays caused by sequential refreshing of each D/A converter is shown in Figure 3.

This arrangement (used in the AD7522) interposes an extra digital buffer between the computer's data bus and the D/A converter's input register. The system updates the

buffer registers serially while a previously-programmed semiconductor test takes place; then, as soon as a new set of analog voltage and current values are required, a command signal feeds the new set of digital words from the buffer registers to the input registers. While the device is being tested at these new voltage and current excitation levels, the buffer registers are again loaded sequentially for the following test.

Serial data transmission, to remote DAC's (with or without galvanic isolation) is conducted in much the same way, using two wires for the data, plus an extra conductor for command signals. However, the buffer register in this case is a shift register, accepting the data serially, but passing it on to the converter in parallel. In the AD7522, the buffer registers can be operated in parallel, byte serial, or bit serial.

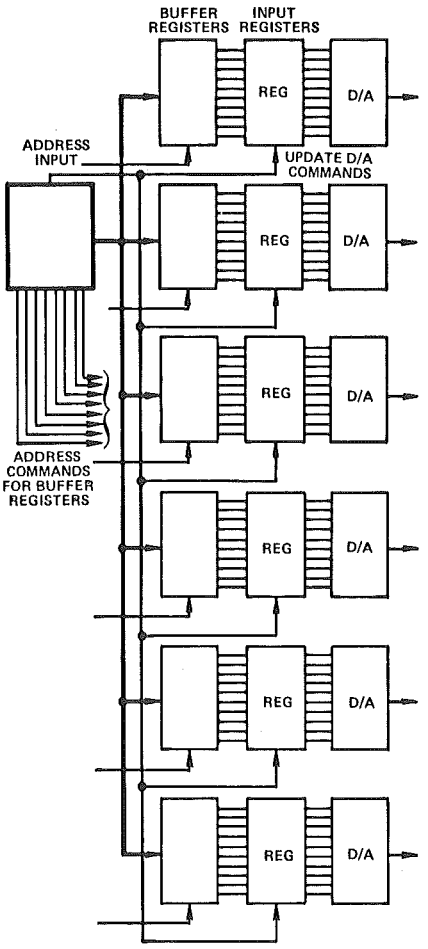

Figure 3. Simultaneous D/A updating.

ANALOG DISTRIBUTION

Two approaches to sample-hold-circuit updating are shown in Figures 2 and 4. In Figure 2, analog data is "shipped" over a common cable to all the sample-hold circuits. However, each sample-hold device, normally in *hold*, remains oblivious to the input data until a command signal connects it momentarily to the data bus (*sample*). On receipt of its update pulse, the sample-hold circuit acquires whatever analog information appears on the data line and holds this value until subsequently commanded to acquire a new signal level.

An alternative arrangement, using a modular (de)multiplexer for distribution of analog data among individual channels, is shown in Figure 4. Here, the sample-hold circuits respond to whatever signals are presented at their input terminals, and then hold this signal level when the analog input is disconnected. The multiplexer switches serve double duty, both in multiplexing and for charging the *hold* capacitor. Though more subject to leakage and crosstalk than the circuit of Figure 2, this is a simple and low-cost arrangement.

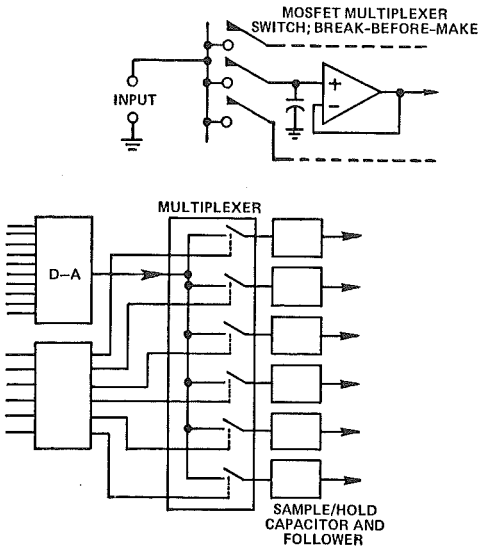

Figure 4. Multiplexing and sample-hold using multiplex switches.

A data-distribution arrangement that eliminates sample-hold circuitry is presented in Figure 5. Here, the purpose is to utilize the inherent storage capacity of the device being activated. For example, it is possible to distribute data among several d'Arsonval indicators in a utility substation simply by exploiting the natural inertia of the meter movement. So long as the data can be refreshed with sufficient rapidity, the meter's average response is simply dependent on the "duty cycle" (dwell time at each switch point to refresh period). Thermal ovens can be controlled by pulsing in this way, as can instrument servos and other devices with built-in inertia of one kind or another. For such applications, the converter should have sufficient peak output current-handling capacity and the switches low-enough resistance (perhaps even electromechanical relays) to avoid introducing errors.

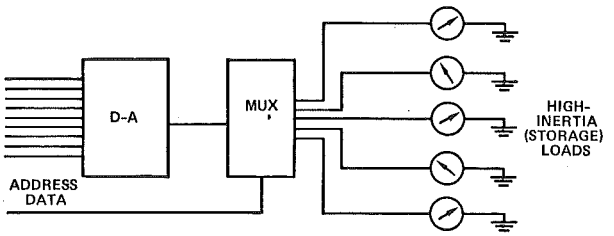

Figure 5. Using output-transducer inertia for averaging and data storage, eliminating per-channel storage (registers or capacitors/op amps).

ACQUISITION vs. DISTRIBUTION

As a rule, data *acquisition* poses more challenging problems than data *distribution,* but some of the problems assume different shapes. Since data distribution can take place at macroscopic power levels (volts and milliamperes), noise is not a great problem (except for *induced* noise in hostile environments). To the contrary, DAC outputs are sometimes boosted, as in programmable power supplies; in such cases, it is useful for the DAC's output amplifier system to have remote sensing to avoid errors due to voltage drops in the wiring. This may also be the case for high-resolution DAC's (such as DAC-1138) at more-modest power levels.

Sample-holds used in data acquisition must have short aperture time (or at least small aperture uncertainty) because they must either deal with the "instantaneous" value of a signal, or sample it rapidly at equal time intervals. Their *hold* time need be no longer than is necessary for the ADC to digitize the signal. In short, the emphasis in sample-

hold circuits for data acquisition lies on rapid acquisition, followed by rapid conversion. By contrast, sample-hold configurations used for data distribution usually permit relaxed update timing, but the analog values may have to be preserved for long periods without "droop." Thus, sample-holds for data distribution must have long *hold* times, and short acquisition-and-settling times. Where high resolution (12 bits or better) and large ratios of *hold* to *settling time* are necessary, multiple D/A distribution, with storage in registers becomes preferable; the decreasing cost of IC DAC's makes the choice easy.

FILTERING/SMOOTHING

In data acquisition, the purpose of filtering is to remove (or at least reduce) analog transmitted, inherent, or induced input noise. In distribution, filtering is used to reduce "noise" caused by quantization (finite increments of digital resolution causing discontinuous analog outputs – the obverse side of quantization uncertainty in A/D conversion), and to deal with coupled-in switching transients and "glitches" (which are large spikes caused by intermediate codes introduced by asymmetrical switching times at such transitions as 0111 1111 to 1000 0000.

Discontinuities are often tolerable, especially in DC-value testing, where they occur at the application of test conditions, and readings are not taken until the system has settled. On the other hand, if the converter is producing an analog ramp in discrete steps, the discontinuities may have to be smoothed, and certainly any feedthrough transients and/or "glitches" must be minimized. Linear filtering of glitches is impractical, because they have far from uniform magnitudes and they do not occur at uniform intervals; hence, filtering leads to badly-distorted waveforms. Glitches are minimized at the DAC by very fast switching with the best-possible matching of rise and fall times (to minimize the energy in the pulse), and then plucked out by "deglitcher" circuitry, which *holds* the output fixed during switching, then releases it for normal settling. The DAC-10DF is an example of a DAC specifically designed for this purpose.

For reconstructing very coarse sampled data, sophisticated interpolation techniques are used to overcome the limitations of simple filtering. An example is integration of the difference between two adjacent values so that the "points" are connected by straight lines, and the discontinuities become more-easily-filtered changes in slope rather than steps.

THE COST FACTOR

As of this writing, costs of low-resolution monolithic DAC's are very low and still decreasing. For modest-resolution systems (8-10 bits), multiple DAC usage (for example, employ- the AD7522, which is double-buffered and even permits serial input, as well as direct interfacing with microprocessors) is competitive with sample-holds, and generally gives better performance, as we have noted. From 10 to 12 bits, sample-holds appear to hold the cost edge. Above 12 bits, it is difficult to obtain sample-holds with adequate resolution and speed because of the problem of obtaining capacitors with decent dielectric absorption characteristics. So, for high resolution, converters-with-registers, though more expensive, must win by default.

MINIMIZING CALIBRATION ERRORS BY SERVOING

Where many low-cost DAC's are used, it is possible to produce outputs that have absolute accuracy limited only by their resolution. This is done by slaving their outputs to that of a high-resolution, accurately-calibrated, temperature-stabilized master DAC (Figure 6).

Figure 6a shows the basic principle, with "master" and "slave" DAC's. In this illustration, computer data fed to D/A(1) is converted and applied to a comparator in which it is compared with the output of the slaved DAC, D/A(2). The comparator's output drives an up/down counter in the appropriate sense to drive the output of the slaved DAC up if it lower than the master and down if it is higher. Thus, at balance, the slaved DAC will hunt between the two values adjacent to the "correct" value. Filtering provides a degree of interpolation.

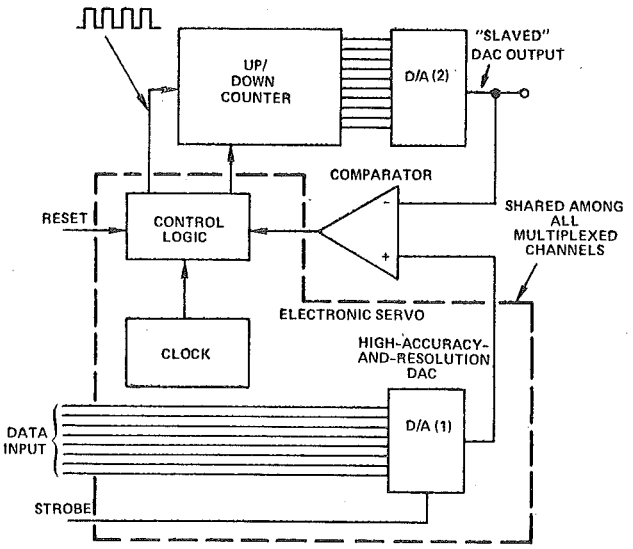

Figure 6a. Controlled-output DAC.

In Figure 6b, this process is extended to multi-channel multiplexing, to update a number of lower-resolution DAC's. Use of feedback as part of the updating process permits an array of low-cost, low-resolution (monotonic) converters to establish precisely-controlled analog output voltages, regardless of calibration drift, but limited by the resolution.

The principal disadvantage of this scheme is its slowness, since the precision DAC must first settle, then the analog output of the DAC being updated must settle to each new trial value before the next clock pulse can be applied to the counter. If the high-precision DAC is a 16-bit unit, (e.g., DAC-1136) with settling-time just under 100μs, and the DAC's being updated are 12-bit units, with LSB-settling time of 2μs, each channel can require at least 8ms for updating, but a possible minimum of less than 100μs. The comparator reversal can be used to signal completed conversion and initiate updating of the next channel, to minimize throughput time per cycle of update.

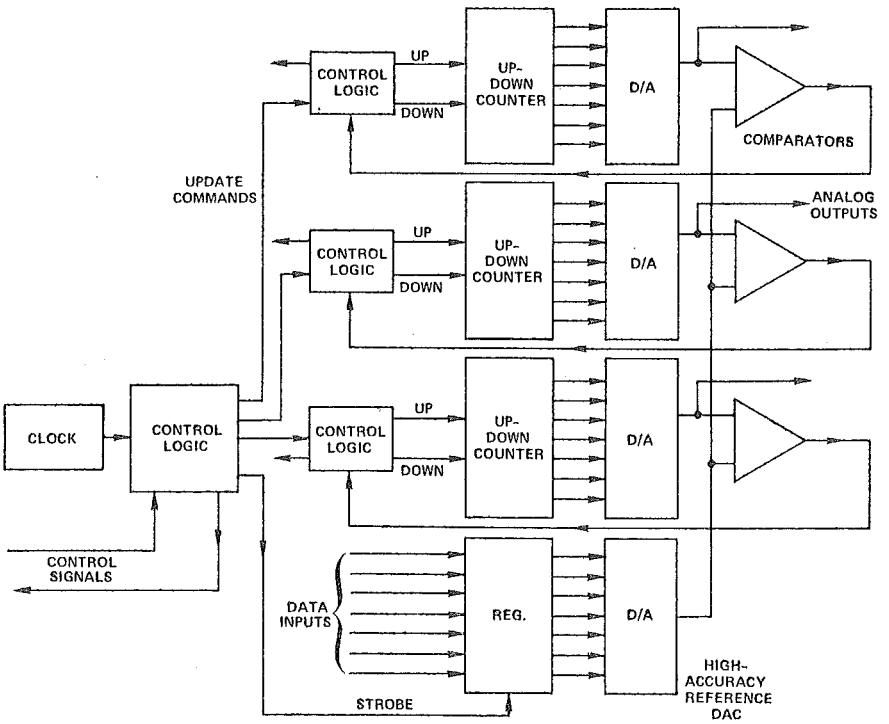

Figure 6b. Low-cost high-accuracy distribution.

ISOLATION

If a data-distribution system is spread over a large geographical area, it frequently becomes necessary to isolate the various analog loads from the digital data source. Otherwise, substantial differences in ground potential at the various locations could cause large ground currents or excessive induced noise. Isolation could be accomplished by transformer or optical coupling, applied either to the digital signals (two-wire line with serial-to-parallel-to-analog conversion at the load), or to the analog signals after conversion, using (for example) isolation amplifiers in the 284 family, which also provide auxiliary floating power for additional remote circuitry, such as low-level preamplifiers.