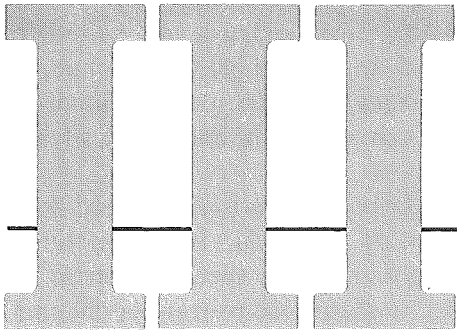


Multiplexers

Chapter 3

MULTIPLEXING AND MULTIPLEXERS

When more than one quantity has to undergo analog-to-digital conversion, it is necessary either to time-division multiplex the analog inputs to a single A/D converter, or to provide an A/D converter for each input and combine the converter outputs by digital multiplexing.

Until recently, analog multiplexing was the universally-favored technique for achieving lowest system cost, but the rapidly-decreasing cost of A/D converters and the availability, at low cost, of digital integrated circuits specifically designed for multiplexing provide a viable alternative with many advantages.

A decision on the correct technique to use for a given system will have to make tradeoffs between the following factors:

1. Resolution of measurement. The cost of A/D converters rises very steeply as the resolution increases, due mainly to the cost of precision elements used in the converter. At the 6-8 bit level, the per-channel cost of an analog multiplexer ("MUX") is likely to be a considerable proportion of the cost of a converter, and at lower resolutions it may actually exceed the converter cost. At higher resolutions, above 12 bits, the reverse is at present (but decreasingly) true and analog multiplexing has tended to be most economical.

2. Number of channels. This controls the size of the multiplexer required and the amount of wiring and interconnections that will be needed. Digital multiplexing onto a common data bus

cuts wiring to a minimum. Analog multiplexing is best-suited to handling 8-256 channels; beyond this number, the technique becomes unwieldy and analog errors are difficult to minimize. Analog and digital multiplexing can often be combined advantageously in very-large systems.

3. Speed of measurement, or *throughput rate.* High-speed A/D converters carry a considerable cost premium. If analog time-division multiplexing will demand a very high speed converter to achieve the desired sample rate, a slower converter-per-channel with digital multiplexing may be a better choice.

4. Signal level and conditioning. Wide dynamic ranges between channels are difficult to handle with analog multiplexing. Small signals less than 1V will generally require differential low-level analog multiplexing (which is expensive), and programmable-gain amplifiers may well be required after the MUX. The alternative is fixed-gain converters on each channel, with signal-conditioning specifically designed for the channel requirement, again combined with digital multiplexing.

5. Physical location of measurement points. Analog multiplexing is best suited to making measurements at distances no farther than a few hundred feet (100m) from the converter. Analog lines are inherently prone to losses, transmission-line reflections, and interference. Satisfactory lines range from simple twisted wire-pairs to multiconductor shielded cable, depending on the signal level, distance, and noise environment. Digital multiplexing is a viable technique from zero distance to thousands (perhaps millions) of miles, with suitable transmission equipment. Digital transmission systems generally possess useful noise-rejection characteristics, which are essential for long-distance transmission.

MULTIPLEXER FUNCTIONAL REQUIREMENTS

The most important single requirement for a multiplexer is that it operate without introducing unacceptable error at a speed consistent with the sample-rate requirements. For a digital MUX, it is relatively straightforward to determine speed from propagation-delay parameters and the time required to achieve an adequately-settled output on the data bus. Considerable informa-

tion exists on calculating the performance of logic families, and it is not proposed to consider the problem here.

Analog multiplexers are much more difficult to characterize, as their speed is a function, not only of their internal parameters, but also of such external parameters as channel source impedance, stray capacitance (i.e., due to layout and following amplifier characteristics), and also the number of channels and the circuit organization. The user must be aware of the limiting parameters in his system to gauge their effect on performance. These are detailed in succeeding sections.

Because of their non-ideal transmission and open-circuit characteristics, analog multiplexers introduce static and dynamic errors into the selected signal path. These include leakage through switches, coupling of control signals into the analog path, and interaction with both sources and following amplifiers. Poor circuit layout and cabling can compound these effects and further degrade performance.

As analog multiplexers are usually connected directly to sources (which may be delicate, have little overload capacity or poor settling after an overload), practical requirements dictate that the switches have an inherent break-before-make action to preclude any possibility of shorting channels together. Some commercially-available multiplexers can be deficient in this respect. Frequently it is necessary to avoid shorted channels when power is removed from the multiplexer and an "all channels off with power down" characteristic is desirable in a general-purpose MUX. Again, many commercial devices do not embrace this feature.

Besides the channel-addressing lines, which are usually binary-coded, it is useful to have one or more *inhibit* or *enable* lines to turn all switches off regardless of the channel being addressed. This greatly economizes on external logic required to cascade multiplexers and is also useful in certain types of channel addressing.

A final requirement for both analog and digital multiplexers is adequate tolerance of likely line transients and overload conditions, and the ability to absorb transient energy without damage.

MULTIPLEXER SWITCHING ELEMENTS

Analog Elements

Many alternative types of analog switches are available in electromechanical and solid-state (discrete and integrated) forms.

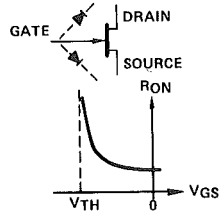
Electromechanical types include relays, stepper switches, cross bar and reed (mercury-wetted and dry) relay switches. The best switching speed can be realized with reed relays, $<$ 1 ms. All mechanical switches provide high dc isolation resistance, low contact resistance, and the capacity to handle high voltages directly (typically up to 1kV), and they are usually inexpensive. Multiplexers employing mechanical switches are suited to low-speed applications and also those having high resolution requirements, and they interface well with the slower types of A/D converters, e.g., integrating dual-slope. All mechanical switches have a finite life, usually expressed in number of operations. A good reed relay may well have a life of 10^9 operations, which, for instance, would amount to a life of 3 years at 10 operations/second continuously.

Solid-state switches are capable of high-speed operation ($<$ 30ns), and have a life likely to exceed most equipment requirements. Field-effect transistors (FET's) are universally used in multiplexers and have superseded bipolar transistors (which can introduce large voltage offsets when used as analog switches).

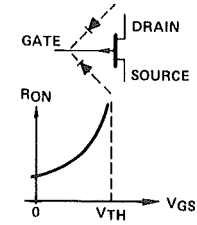
The FET is a majority-carrier device, and, depending on whether the majority carriers are holes or electrons, the FET is termed P or N-channel, respectively. Due to the greater mobility of electrons, a given FET geometry has a lower *on* resistance if it is an N-channel structure, rather than P; and for a given *on* resistance, N-channel structures have lower capacitance and superior parameters to those of P-channel devices. Consequently, for use in MUX, N-channel junction FET's are preferred to P-channel devices of comparable cost. Metal-oxide silicon (insulated gate, or MOS) transistors have only recently become available at competitive cost in N-channel structures; the P-channel device has been available for several years and is in common usage in multiplexers.

N-channel junction and MOS devices suitable for use in multiplexers typically provide *on* resistances in the 10-100-ohm region (extended limits from 2 to 1000 ohms), and P-channel devices fall in a higher band, typically 100 to 1000 ohms.

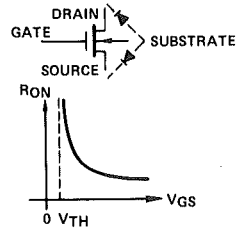
Junction FET's operate in the depletion mode and are turned on fully with zero gate-source voltage ($V_{GS} = 0$). MOS FET's are available in both depletion and enhancement mode (enhancement-mode devices are off with $V_{GS} = 0$, and once the gate voltage exceeds a threshold level V_{th}, the *on* resistance falls as the gate voltage increases). The characteristics of these devices are shown in Figure 1.



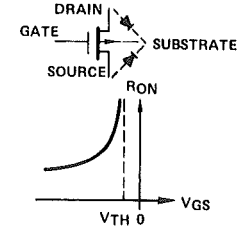
a. N-Channel Junction FET



b. P-Channel Junction FET



c. N-Channel Enhancement-Mode MOSFET



d. P-Channel Enhancement-Mode MOSFET

Figure 1. Junction FET's and Enhancement-Mode MOS FET's

Circuit arrangements in multiplexers usually ensure that the gate voltage of a conducting junction-FET tracks the drain-source voltage to maintain $V_{GS} = 0$. Thus, the *on* resistance of a switch is constant and is not a function of the signal level being multiplexed. This is not true of MOS FET multiplexers, where the insulated gate is driven to a fixed potential in the *on* condition, so

that V_{GS} and the *on* resistance vary with the level of the applied signal. This variation can be considerable: a typical P-channel device operating on ±15V supplies may have R_{ON} = 200Ω with the channel at +10V, and R_{ON} = 1000Ω with the channel at −10V, the gate being switched to −15V.

All FET devices suffer from leakage from drain to source in the *off* state and leakage from gate or substrate to drain and source in both the *on* and the *off* states. Gate leakage in MOS devices is negligible compared to other sources of leakage, unless the device has a Zener-diode-protected gate, in which case an additional leakage path exists between gate and source. Generally, the leakage characteristics of junction FET's are superior to those of MOS FET's. Junction FET's with drain-source leakages of 100pA at 25°C are commonplace, but MOSFET's are typically in the range 1-5nA. As leakages double every 8-10°C, junction FET's are superior at the higher temperatures, where leakage becomes a severe problem.

Enhancement-mode MOSFET's have the theoretical advantage that the switch turns off when power is removed from the MUX, as V_{GS} = 0. In fact, the advantage may be lost unless the drive circuit around the FET is correctly designed. The circuit shown in Figure 2 allows positive input voltages to be short-circuited to ground when the power is removed (the +15V line falls to ground potential, and conduction takes place through the drain-substrate isolation diode). Additional components are required to ensure that the switch remains off under all conditions of input with the power shut down. Figure 3 shows the necessary modification: negative input voltages are blocked by the drain-substrate diode of the MOSFET Q1, and positive voltages are blocked by D1 and the collector-base diode of Q2, while R ensures that the gate-substrate voltage of Q1 remains zero, keeping it turned off. Even with this modification, leakage is likely to be several nA greater with power down than with power on. As an inherent matter of their processing, most integrated-circuit MOS multiplexers do not incorporate this feature, and it is up to the user to provide protection, both for the multiplexer and the signal sources. (As a final note, junction-FET multiplexers *always* turn on with the

power down, so it is necessary to maintain supply voltage to maintain channel isolation.)

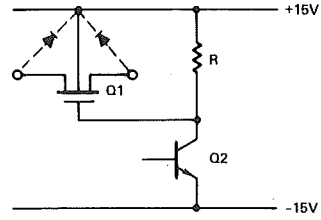


Figure 2. MOSFET Power-Off Short-Circuit Mode

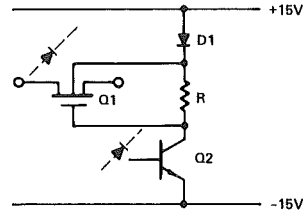


Figure 3. Circuit to Maintain Power-Off Open Circuit

A more recent development is the CMOS (COSMOS) complementary MOS switch, which has the great advantage of being able to multiplex voltage up to and including the MUX supply voltages, i.e., a ±10V signal can be handled with a ±10V supply to the MUX. A P-channel device can only switch signals between $+V_s$ and a voltage slightly greater than $-(V_s - V_{th})$, and an N-channel device can only switch signals between a voltage slightly less than $(V_s - V_{th})$ and $-V_s$. In both cases, there is considerable variation of *on* resistance with signal level. By combining an N- and a P-channel device in parallel, each makes up for the deficiencies of the other, and it is possible to switch signals between $\pm V_s$ (Figure 4). Since the *on* resistances of the switches are in parallel, device geometries and thresholds can be adjusted so that the parallel sum of the *on* resistances varies little over the signal range (Figure 5). Note that $2V_s > (V_{thP} + V_{thN})$, or a conduction deadband will exist in the switch. With most types of CMOS processing, this is a problem only when $2V_s < 5V$. The switches require complementary gate drive, which is usually derived from an inverter, resulting in an integrated structure similar to that shown in Figure 4.

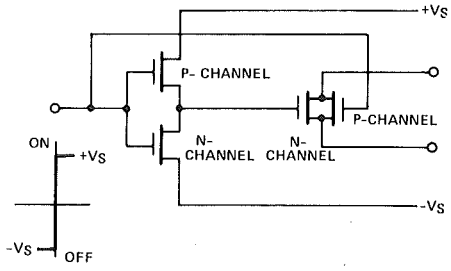


Figure 4. Complementary MOS Switch

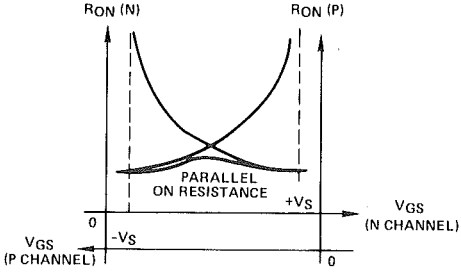


Figure 5. On-Resistance of CMOS Switch vs. Input Voltage

Digital Elements

For small numbers of channels, medium-scale integrated digital multiplexers are available in TTL and MOS logic families. The SN74151 is a typical example, as shown in Figure 6. Eight such integrated circuits could be used to multiplex 8 A/D converters of 8-bit resolution onto a common output bus.

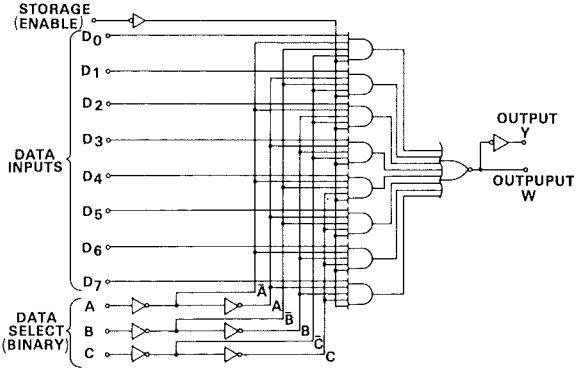


Figure 6. Typical Digital Multiplexer SN74151

This type of digital multiplexing offers little advantage in wiring economy, but it is low in cost, and, through its very high switching speed, operation is possible at sampling rates far in excess of those obtainable with analog multiplexers. Also, the multiple A/D converters used are required only to keep up with the channel sample rate, and not with the commutating rate of the MUX.

Where larger numbers of A/D converters are to be multiplexed, the data-bus technique shown in Figure 7 provides great economies in system interconnection and organization. This alone may in many cases justify multiple A/D converters. Data can be bussed onto the lines in bit-parallel or bit-serial format (many converters have both serial and parallel outputs to allow this choice to be made readily). A wide variety of devices exist to drive the bus, from open-collector and tri-state TTL gates, special line drivers and opto-electronic isolators, giving a wide range of common-mode and noise-margin performance to suit the most rigorous requirements. Channel-selection decoders can be built up from 1-of-16 decoders to any required size. This system also contains some redundancy, in that a failure of one A/D, or overload of one source, will not affect the other channels.

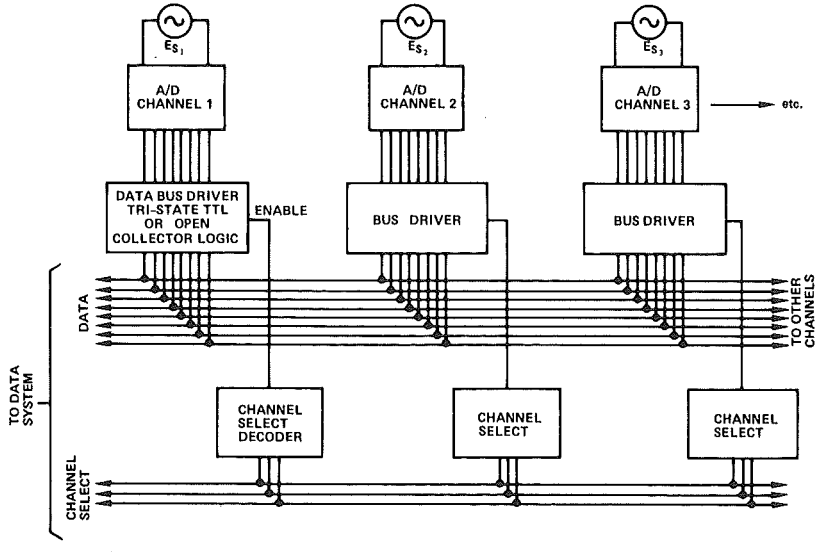


Figure 7. Digital Multiplexing on to a Common Data Bus

BASIC ANALOG MULTIPLEXER CONFIGURATIONS

High-Level Multiplexers

High-level multiplexers are designed to handle input signal voltages greater than 1V without introducing significant error. The most-common type consists of a bank of switches connected to a common output bus, as shown in Figure 8. The bus output may be buffered by a non-inverting operational amplifier, as shown. This configuration is simple, and, when used with an output amplifier, offers high input impedance.

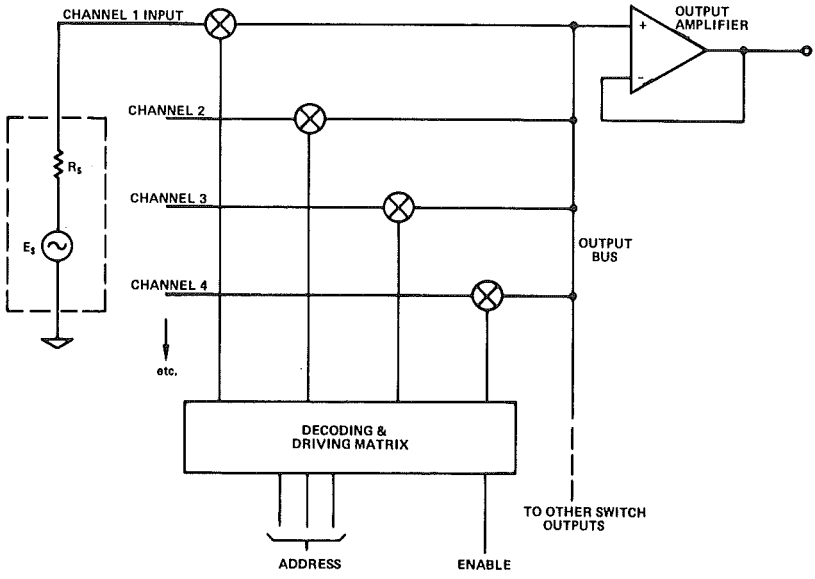


Figure 8. High-Level Voltage Multiplexer

Depending on the choice of switching device, this type of multiplexer can operate over a wide range of input voltage. With solid-state devices, input-voltage excursion is usually limited to ±20V, and most multiplexers are designed to handle the standard analog range of ±10V; but some devices that use high-threshold switches are suitable for only ±5V operation.

When it is desired to switch high voltages (up to several hundred volts) with the speed of solid-state switching, the inverting current-switching MUX should be used (Figure 9). Since all switching takes place at the summing junction, with protective diodes to ground, the switches are never exposed to high voltage. This type of MUX is characterized by high immunity to transient voltages, constant but low input resistance (equal to the channel input resistor) while conducting and is inherently safe when power is removed from the MUX. Each channel can be adjusted to an appropriate gain to suit the input. If R_c is large, so that switch R_{on} temperature variations are small in comparison, the transfer ratio for the circuit

$$-\frac{R_f}{R_c + R_s}$$

can be set to a high degree of accuracy, provided R_s is constant. No common-mode voltage is applied to the amplifier, so no common-mode error can be generated.

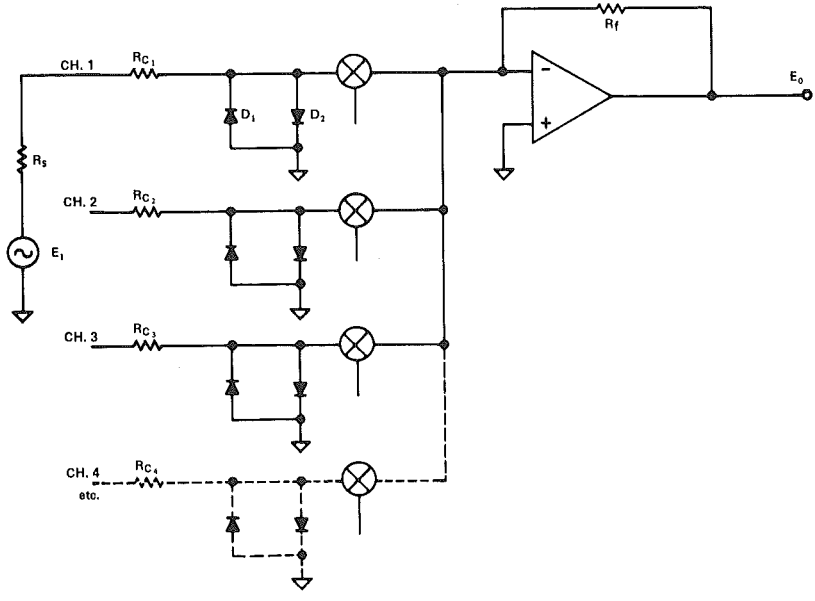


Figure 9. Inverting (Current) Multiplexer

This type of multiplexer is very robust and is particularly suited to industrial system control and interfacing with the older type of ±100V analog computers.

Two modifications are popular: The diodes D1, D2, etc., can be replaced by FET's driven in complementary fashion to the transmission switch to ensure that the input resistor R_c is always terminated in a real or virtual ground, so that the input resistance is nearly-constant, whether the channel is selected or not (Figure 10). This avoids settling problems at the transducer during switching, due to change of loading (the diode resistance is a function of the current through them). In a second modification, R_c can be removed (i.e., set equal to zero) to render the circuit suitable for multiplexing current-output transducers (Figure 11). If current output switching is used, then transfer accuracy is unaffected by variations in line- and interconnection resistances.

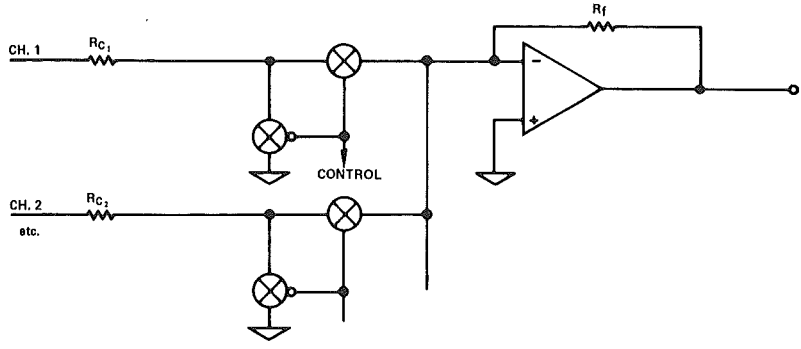


Figure 10. Constant-Impedance Multiplexer

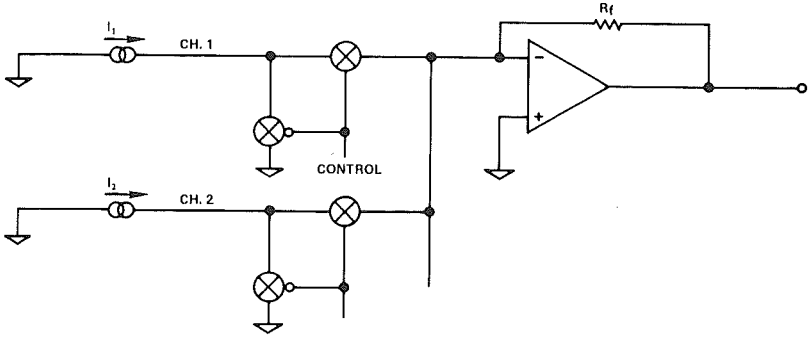


Figure 11. Current Multiplexing

Low-Level Multiplexing

For multiplexing small voltages in the millivolt range, up to 1V, more-sophisticated multiplexers are required. Problems most frequently arise at low levels due to interference and thermal effects, so lines are run in pairs, and differential techniques are used to remove any interference that is induced as a common-mode signal. Where very-high common-mode voltages are present, guarding techniques also improve performance, and 3-wire multiplexers are required with shielded input pairs.

A simple 2-wire differential MUX is constructed using pairs of switches, as shown in Figure 12. The output amplifier usually consists of a data or instrument amplifier designed to have very high common-mode rejection (generally $>$ 100dB). Such high rejection can only be achieved if the input lines are identical. This requires twisted pairs for cabling and great attention to matching the dc and the ac parameters of the channels and switches in the MUX. Integrated structures and dual-FET switches are superior in achieving the matching required. Also, switch leakage and thermal EMF's can introduce serious errors in low-level inputs, and drift can also be a problem. The amplifier configuration shown indicates how operational amplifiers are classically used to form a differential high-gain amplifier. Modular and integrated-circuit instrumentation amplifiers, specifically-designed for the purpose,

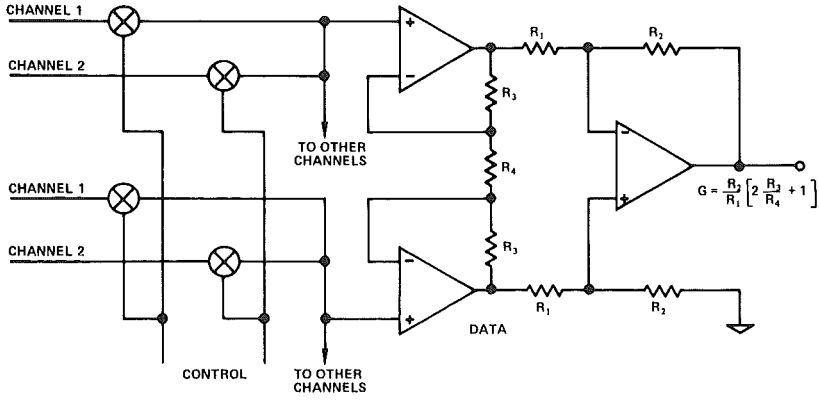


Figure 12. Differential Multiplexer and Amplifier

are, of course, available; they require much less effort to use, and – in IC form (e.g., the AD520) – they are not at all costly.

To reduce the effects of unbalance in the input cabling, cables can be made up as shielded pairs, and the shield driven by common-mode voltage, either by the source or a mid-position tap on R4 in the data amplifier (or a mid-position tap between the input terminals, unloaded by a unity-gain follower). This shielding, or "guarding" is commonly used in high-resolution data-acquisition systems, where common-mode interference levels are frequently very high.

Another type of low-level multiplexer that provides considerable immunity against common-mode interference is the flying-capacitor multiplexer. Essentially, this is a two-wire sample-hold (Figure 13). Switches A and A′ are turned on (with B & B′ off) to acquire the input signal. When capacitor C is fully charged, all switches are momentarily turned off; then B & B′ are turned on to transfer the signal to the output amplifier. Since no common-mode voltage is transferred across the switches, the output amplifier can be a simple single-ended-input non-inverting amplifier. This is an effective method of eliminating common-mode voltage; but it is a poor choice if normal-mode interference is present as well, since much-better rejection of both normal mode and common mode could be obtained with a "straight-through" multiplexer and a floating-input integrating converter. (An integrating converter used with a flying-capacitor multiplexer will integrate the *sample* of the input rather than the input, and the sample will include variations due to normal-mode interference.)

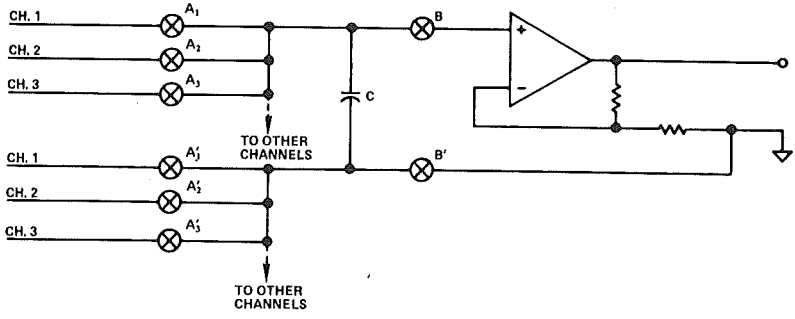


Figure 13. Flying-Capacitor Multiplexer

ERRORS IN HIGH-LEVEL MULTIPLEXERS

Multiplexing introduces static (i.e., dc) and dynamic errors into the signal. If these errors are large in relation to the resolution of measurement, they will produce undesirable variations in system performance. It is therefore necessary to determine the errors and compare them against the system requirements.

Broadly, errors arise from two sources. Static errors originate from switch leakage, offset in output buffer amplifiers, and gain errors due to switch *on* resistance, source resistance, amplifier input resistance, and amplifier-gain non-linearity. Dynamic errors arise from charge injection of the switch control voltages, settling times of the common bus and input sources due to circuit time constants, crosstalk between channels, and output-amplifier settling characteristics. Dynamic errors are greatly affected by multiplexer organization and system layout, and can prove difficult to calculate to any degree of accuracy. A rough estimate of their magnitude is, however, usually adequate for design purposes. Other errors may arise through characteristics peculiar to the multiplexer components, e.g., reed relays may generate thermal EMF's up to 40μV/°C. These require additional consideration.

Static Errors

Gain or Transfer Ratio

The circuit resistances controlling transfer accuracy are shown in Figure 14. R_s is the internal resistance of the source; it will generally vary from channel to channel, and it is likely to be temperature-dependent. $R_{leakage}$ is distributed along the input cabling and output bus and is controlled by circuit insulation. It should always be several orders of magnitude greater than R_s; use Teflon-insulated wiring, if necessary, to achieve this. $R_{leakage}$ can then be safely neglected. Good wiring practice and board layout are also helpful in minimizing $R_{leakage}$ and are essential in high-humidity environments.

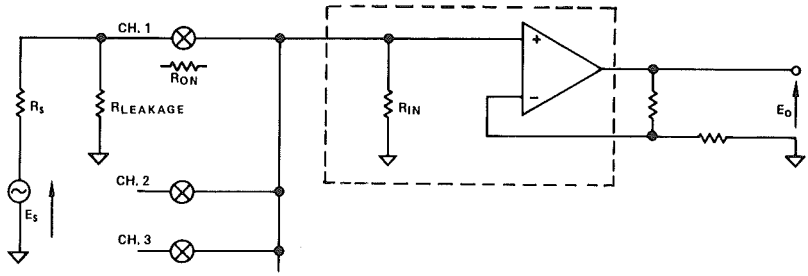


Figure 14. Resistances Affecting Gain Error of MUX

R_{on}, the switch *on* resistance, is a function of the switch design. Mechanical switches have the lowest initial contact resistance but can develop enormous variations of resistance under dry-circuit conditions and towards the end of switch life. Solid-state switches have reproducible *on* resistance, with R_{on} of FET switches ranging from a few ohms to a few thousand ohms. The very-low *on*-resistance large-geometry FET's give excellent static performance at the expense of dynamic performance, as they are handicapped by very large gate capacity and drain-source capacitance. The *on* resistance of FET's is a function of temperature, increasing with temperature at roughly ½ to 1%/°C.

The input resistance, R_{in}, of the amplifier is a function of its differential and common-mode input resistances and loop gain

$$R_{in} = \frac{1}{\frac{A_c}{A_o R_d} + \frac{1}{R_{cm}}}$$

where

A_c Closed-loop gain of the amplifier circuit
A_o Open-loop gain of the amplifier
R_d Differential input resistance of the amplifier
R_{cm} Common-mode input resistance of the amplifier

Since open-loop gain and input resistance are functions of temperature, input voltage, and supply voltage, a worst-case figure for R_{in} should be calculated (or estimated). It is easy to achieve an input resistance of 100MΩ for a unity-gain follower with low-cost monolithic IC amplifiers; higher input resistance may require the

better amplifier parameters obtainable with FET-input IC and modular amplifiers.

If $R_{leakage}$ is neglected, the dc transfer ratio is clearly

$$\frac{E_o}{E_s} = \frac{A_c R_{in}}{R_s + R_{in} + R_{on}}$$

The effect of A_c, R_s, R_{in}, R_{on}, and their variations may be calculated. Constant errors in the transfer ratio, due, for example, to a constant-but-high source resistance, may not be serious, as they will introduce systematic errors that can be allowed for. The variations in transfer ratio due to temperature and voltage generally require careful consideration, as they cannot easily be compensated.

Gain nonlinearity of the amplifier is likely if the loop gain is inadequate. In general, it is easy to achieve 80dB of loop gain with low-cost amplifiers used as followers.

$$A_c = \frac{(\text{ideal gain})}{1 + \frac{1}{(\text{loop gain})}}$$

Loop gain = $A_o\beta$, where β is the fraction of output fed back. Nonlinear CMR at extreme values of CMV is a more-important source of error in followers.

Leakage Errors

FET switches have finite *off* resistance and consequently are afflicted by drain-to-source leakage currents. In addition, junction FET's and Zener-diode-protected MOSFET's have leakage paths between gate and channel. Unprotected insulated-gate MOSFET's generally have negligible gate leakage (while they last).

The leakage currents of all the switches in a multiplexer return to ground via the input source resistance and the input resistance of the amplifier. Leakage on the input side of non-conducting channels is usually of little interest, as it does not affect the signal path; but leakage of all the output sides of the channels and the conducting channel into the signal path causes a voltage error (Figure 15).

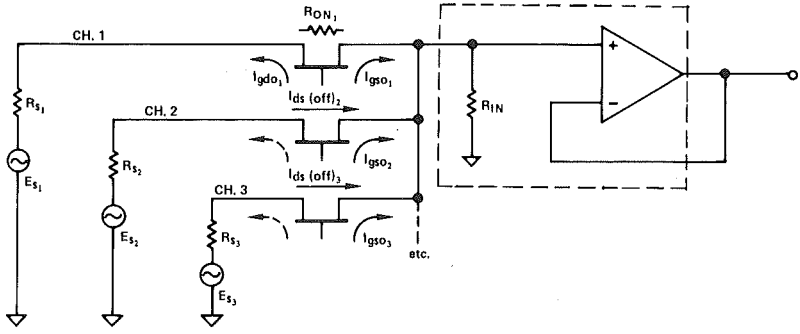


Figure 15. Sources of Current Error in Multiplexer

If the gate-to-drain leakage of the conducting channel is neglected in comparison to the sum of the leakages of all the other channels, an error voltage is developed:

$$V_{e(CH1)} = \frac{(R_{on1} + R_{s1})(R_{in})}{(R_{on1} + R_{s1} + R_{in})} \left\{ I_{gso1} + \sum_{j=2}^{N} (I_{gsoj} + I_{ds(off)j}) \right\}$$

Typically, $I_{ds(off)}$ and I_{gso} are about 0.1nA at 25°C for junction FET's and double for every 11°C rise. Insulated-gate MOSFET's have higher $I_{ds(off)}$, typically 1 to 5nA at 25°C, and gate leakage in the femtoampere (10^{-15}A) region, which can be neglected. For either type, 10:1 variations of leakage parameters can be expected from device to device.

Generally, leakage is a problem only when working from high source impedances, since $R_{in} >> R_{sl} >> R_{on}$ under these conditions. The term $(I_{gso} + I_{ds(off)})$ is usually lumped together on the multiplexer data sheet and termed "channel leakage". The above error equation can then be simplified to the form

$$V_{e(CH1)} = R_{sl} \cdot (\text{number of channels} - 1) \cdot (\text{channel leakage})$$

For an 8-channel multiplexer with channel leakage of 2nA at 25°C with source resistance of 50kΩ, leakage error would be 0.7mV. At 50°C, this error would increase to 2.8mV.

It is manifest that if 8-channel multiplexers were paralleled to form, say, a 256-channel multiplexer, the leakage error would

increase to a massive 25.5mV. Although it leads to additional complexity (and the purchase of additional multiplexers), it is usually considered good practice to cascade multiplexers in a serial pyramid fashion (or sub-multiplex), as shown in Figure 16. This greatly reduces the leakage problem and also improves the dynamic performance. Leakage error in the submultiplex connection becomes:

$$V_e = R_s \cdot (\text{Number of channels/stage} - 1) \cdot (\text{Number of stages}) \cdot (\text{Channel leakage})$$

Multiplexing 256 channels by submultiplexing with the 8-channel multiplexers of the previous example would lead to a leakage error of 2.1mV at 25°C, better than an order-of-magnitude improvement over simple parallel connection.

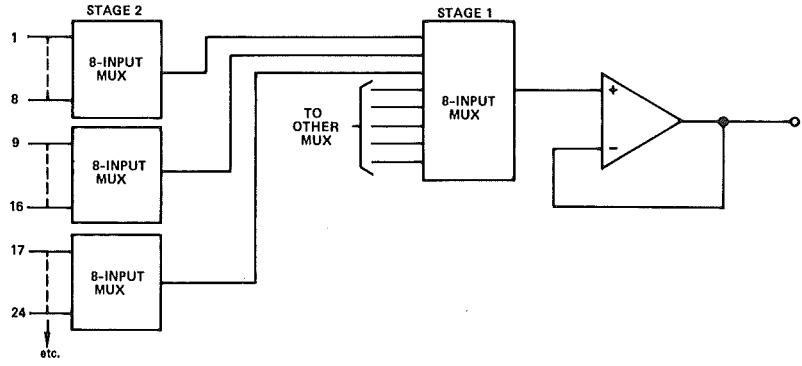


Figure 16. Use of Submultiplexers to Reduce Errors

Offset Errors and Errors Due to the Buffer Amplifier

The appreciable *on* resistance of most types of multiplexer switches calls for a high-input-impedance buffer amplifier to buffer the voltage on the output bus of the MUX. This amplifier may be provided as an integral part of the multiplexer module (but its inclusion tends to limit the versatility of the module, e.g., it is not required in every multiplexer in a subMUX connection), or it may be included as part of a sample-hold or A/D converter following the multiplexer, or it may have to be provided

separately by the user. In some cases where large dynamic range is required, a programmable-gain amplifier will be needed.

In all of these situations, the offset drift and bias-current drift, and common-mode performance of the amplifier will introduce errors in addition to those already considered. Clearly, the errors introduced by the buffer amplifier should be much less (and certainly not greater) than errors associated with the multiplexer.

The need to use an amplifier with adequate open-loop gain to avoid gain-nonlinearity has already been mentioned. Calculation of voltage and current drift in non-inverting connections is covered in the chapter on operational amplifiers. Voltage drift is seldom much of a problem in high-level multiplexers operating with low-gain buffers, but current drift and offset can be very serious, since the bias current flows through the multiplexer and the source resistance. With varying values of source resistance from channel to channel, it is difficult to compensate the inverting input of the buffer so that *offset* current controls the drift; instead, the full bias-current variation with temperature controls the drift. (All of this assumes the use of the cheapest-available "general-purpose" monolithic IC's. An easy out is to use low-cost IC FET-input op amps, such as the AD540.) This sets up a static offset:

$$V_{offset} = I_{bias} \ (R_{on} + R_{source})$$

and a temperature variation:

$$\frac{\delta V_{offset}}{\delta T} = \frac{\delta I_{bias}}{\delta T} (R_{on} + R_{source})$$

Operating an AD741C amplifier following a multiplexer driven by a 10kΩ source would produce a static offset of up to 5mV and a temperature variation of ±1mV over the range 0 – 70°C due to current drift alone (neglecting R_{on}).

A common technique in large systems where a computer is available is to ground the input of one channel. This then becomes a drift-reference channel, and readings from this channel can be subtracted from those obtained from each of the other channels to

give correct readings. This compensates, not only for the drift in the amplifier, but also A/D converter zero-drift and multiplexer leakage errors. It is a particularly-useful technique when measuring low-level signals (and substituting a $5 amplifier for a 50¢ amplifier hasn't solved the problem).

Dynamic Errors

Output-Bus Settling

The output bus of a multiplexer has considerable capacitance to ground. When switched to a new channel, the output voltage cannot change instantaneously to the signal-source voltage. In the simple case where $R_s = 0$, the settling is controlled by the time constant $R_{on}C_{bus}$, where C_{bus} is the sum of C_{gs} and C_{ds} (FET capacitances), C_{in} (amplifier input capacitance, may be a function of frequency), and C_{stray} (stray bus-to-ground capacitance), as depicted in Figure 17.

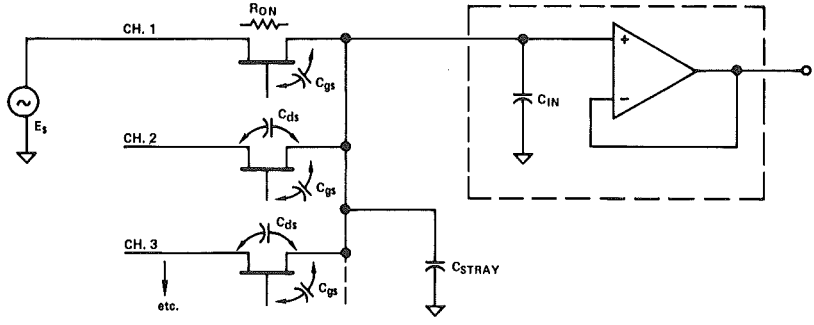


Figure 17. Factors Affecting MUX Settling Time With Negligible Source Resistance

Typically, C_{gs} and C_{ds} are 2-5pF for small-geometry FET's with *on* resistances in the 200-500Ω range; but there are wide variations depending on construction, and large-geometry low-*on*-resistance FET's have considerably higher capacitances. Stray capacitance, to a large extent a function of layout, may typically be 15pF or more. Input capacitance of the buffer amplifier will probably be about 5 to 10pF (simple buffer-amplifier designs may have considerable Miller input capacitance).

For an 8-channel multiplexer, the bus capacitance may therefore be typically in the range 36 to 65pF, which gives a time constant of 18 to 34ns with $R_{on} = 500\Omega$. The settling time to 0.01% (9.2τ) would therefore be 0.165 to 0.31μs. This figure will increase in rough proportion to the number of channels working into a common bus. For large numbers of channels, this is one more good reason for submultiplexing; dynamically it will decrease the output bus capacitance and so keep the bus settling time within reasonable bounds.

In the case where R_s is appreciable, the settling time is controlled by two time constants. In general, the settling time will be longer than with $R_s = 0$, but the exact behavior depends on the relative magnitudes of the two time constants (Figure 18).

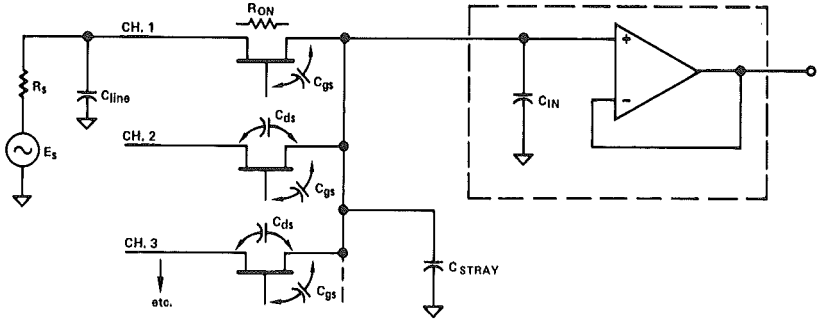


Figure 18. Factors Affecting MUX Settling Time With Appreciable Source Resistance

The settling mechanism consists of a charge transfer between C_{line} and C_{bus} through R_{on} ($\tau_1 = R_{on} \cdot C_{line} \cdot C_{bus}/(C_{line} + C_{bus})$) and charging of C_{line} and C_{bus} through R_s by E_s (time constant $\tau_2 = R_s(C_{line} + C_{bus})$). The charge-transfer time constant τ_1 is usually the shorter, controlling the initial settling, while τ_2 controls the final settling.

In cases where $C_{line} >> C_{bus}$, settling is controlled mainly by charge transfer and may not require much more time than with $R_s = 0$, provided that the line capacitance has adequate time to be recharged between samples. This is usually the case when an input

filter is used and C_{line} becomes part of the rather large filter capacitance. Without a filter, C_{line} depends largely on the choice of input cable and is typically greater than 8pF/ft. When C_{line} is of the same order as C_{bus}, it is necessary to solve the differential equations to obtain a reasonably exact value of settling time to a given resolution. These are easily derived using the equivalent circuit of Figure 18.

Output Amplifier Settling

When the settling time of the output bus has been calculated, an output buffer amplifier should be selected; its speed of response should be such that it does not further degrade the settling time seriously. Operational-amplifier manufacturers can usually provide settling-time data for most of their products, particularly wide-band amplifiers with fast settling time that have been specifically designed for such applications as high-speed multiplexing. If settling performance is not a critical parameter and you wish to reassure yourself only as to the order of magnitude of the settling time, you can obtain a rough estimate from the slew rate and bandwidth of the operational amplifier. This technique is not recommended for situations in which accurate estimates are required, since the true settling time of an amplifier in a given circuit configuration is a function of more parameters than slew rate and bandwidth, but, as mentioned, it can prove useful for rough checks where settling data is not available.

As fast multiplexers and amplifiers carry a considerable cost premium, you should aim to design closely to your system requirements. Do not degrade a fast multiplexer with a slow amplifier, or waste a fast amplifier on a slow multiplexer; aim for a good balance of cost and performance in both components.

"Pumpback" and Charge Injection

Each time a channel is switched in any type of multiplexer, some of the switch-control signal is coupled inductively and capacitively into the analog signal path. In FET multiplexers, coupling occurs mainly via the gate-drain and gate-source capacitance of the FET switches. Each time a switch is operated, a quantity of charge,

$V_c(C_{gd} + C_{gs})$, is injected into the bus and line (V_c = gate-driving voltage). This charge has to leak away through the switch *on* resistance and the source resistance R_s. In cases where $R_s \rightarrow 0$, charge injection produces a short spike on the output bus each time a switch operates. The spike consists of an initial voltage step of approximate magnitude $V_c(C_{gs} + C_{gd})/C_{bus}$, and an exponential decay with time constant $R_{on}C_{bus}$.

If the output amplifier response to the transient remains in the linear range (i.e., the amplifier is not overloaded or driven into slewing), charge injection will only produce a slight increase in settling time: the time required for most of the injected charge to leak away and for the amplifier to recover from the (small) transient.

If R_s is large, the initial voltage step will be reduced to $V_c(C_{gs} + C_{gd})/(C_{bus} + C_{line})$, but the decay time constant will be increased to $R_s(C_{bus} + C_{line})$ while the switch remains on. The effective values of C_{gs} and C_{gd} may differ between the switch *on* and switch *off* conditions, due to nonlinear switching effects, and for this reason the line capacitance may remain charged, decaying through its own time constant R_sC_{line}. Operating the switch again will add to the charge on the line capacitance, and at high sample rates, charge can be pumped into the line capacitance more rapidly than it can leak away to zero, producing a standing offset voltage in series with the signal source. This phenomenon, known as "pumpback," can limit the sampling rate in very high-speed systems. For high sampling rates, it is therefore essential to use low-capacitance, medium *on*-resistance switches to minimize pumpback error.

Crosstalk

This is a measure of the coupling between the *off* channels and the conducting channel of a multiplexer. It is very largely a function of the cable and circuit-board layout used for the multiplexer, but it is also a function of switch *on/off* impedance. Manufacturers specify crosstalk figures for multiplexers, but these figures are liable to be enormously modified in a practical system.

Crosstalk is measured by applying a voltage of known magnitude and frequency at one or more of the *off* channels of a multiplexer and measuring the output voltage on the bus or at a source with a defined R_s (usually 1kΩ). The results will differ slightly, depending on where the output voltage is measured (bus or source), so the test configuration should be specified. Also, crosstalk varies according to which channels are used for measurement; it is customary (or at least, desirable) to give a figure for the worst-case pair. Measurement details are shown in Figure 19. Crosstalk can be measured at both dc and ac (usually 1kHz) and is strongly affected by the source resistance.

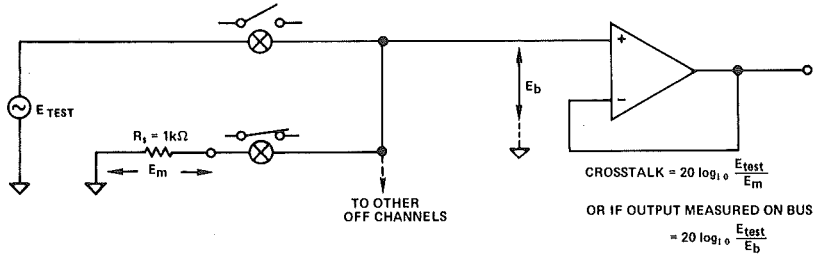


Figure 19. Measuring MUX Crosstalk

Switching Time

Besides the delays required for analog settling, there are propagation and risetime delays associated with the digital logic that drives the switching elements, and corresponding delays inherent in the operation of switches, e.g., mechanical switching time of reed relays. Turn-on and turn-off times of switches are measured on each channel with full-scale input voltage. *Turn-on* time is the delay from application of channel address to 90% output voltage appearing on the bus, and *turn-off* time is the delay from removal of channel address to 10% output voltage on the bus. In practice, to make a meaningful measurement, it is necessary to load the bus with a resistive load to make the bus time-constant short with respect to the switching time.

Switching time must be added to the total settling time to obtain the minimum delay required between channel address and conversion command of a multiplexed A/D converter.

ERRORS IN LOW-LEVEL MULTIPLEXERS

All the errors encountered in high-level multiplexers also occur in low-level multiplexers but the effects are more serious because of the small signal amplitude involved. Low-level multiplexers are always made differential or two-wire, and a data amplifier is used, so that the converter sees only the difference in the errors of two identical channels. Leakage, gain, pumpback, crosstalk, etc., can all be greatly reduced, provided that adequate matching is maintained for the channels. The *magnitudes* of settling errors are also decreased, although their *time constants* (and hence duration) remain unchanged.

The calculation of the magnitudes of these effects in each side of a differential channel is performed as for high-level multiplexers and the results subtracted to obtain the differential error. Clearly, the result would always be zero if channels were perfectly balanced, but this is never attainable in a practical system. Calculation then has to be based on some known or estimated unbalance on each side of the channel.

As channels are differential, they also have the ability to reject common-mode interference. To do so effectively requires maintenance of a high degree of balance in the channel to avoid common- to differential-mode conversion. The equivalent circuit of a channel of a differential multiplexer is shown in Figure 20.

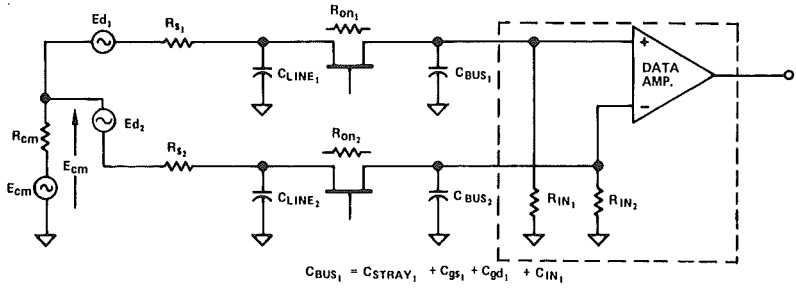


Figure 20. Equivalent Circuit of a Differential-MUX Channel.

From this equivalent circuit, in the case where $R_s >> R_{on}$, the effective common-mode driving voltage E_{cm}' at the source is

$$E_{cm}' = \frac{E_{cm}}{1 + \dfrac{2R_{cm}}{R_s + \dfrac{\dfrac{1}{j\omega(C_{line} + C_{bus})} \cdot R_{in}}{\dfrac{1}{j\omega(C_{line} + C_{bus})} + R_{in}}}}$$

The differential error V_e produced by this common-mode voltage is then:

$$V_e = E_{cm}' \left[\frac{1}{1 + j\omega(C_{line_1} + C_{bus_1})R_{s_1}} - \frac{1}{1 + j\omega(C_{line_2} + C_{bus_2})R_{s_2}} \right]$$

neglecting R_{in}. Clearly, for "infinite" CMR,

$$(C_{line_1} + C_{bus_1}) \cdot R_{s_1} = (C_{line_2} + C_{bus_2}) \cdot R_{s_2}$$

The C_{line} terms are commonly matched by twisting the input lines together. A typical twisted shielded pair may have a line-to-shield capacitance of 55pF/ft and a mismatch of about 3 – 5pF/ft. The C_{bus} terms must be matched by careful layout and the use of matched components, and R_s must be matched as closely as practical arrangements allow. If $R_s \rightarrow 0$, the CMR is controlled mainly by the match of the switch R_{on}'s.

In all these cases, the common-mode to differential conversion of the channel can be approximately calculated. A good design goal is to aim to achieve a channel CMR about an order-of-magnitude greater than the CMR of the following data amplifier. There is little point in buying a 120dB-CMR data amplifier if the channel rejection due to imbalance is only 90dB; an 80-90dB device would provide essentially identical performance at lower cost.

THE MULTIPLEXER SYSTEM IN HIGH-NOISE-LEVEL ENVIRONMENTS

When multiplexers are operated in conditions of high common-mode interference, two-wire differential and guarded or flying-capacitor multiplexers are mandatory. If, as is likely, considerable normal-mode interference also exists, further precautions will be required to make reproducible measurements. Common techniques include filtering, digital averaging, and the use of integrating converters. These are briefly outlined as follows.

Filtering

The addition of low-pass filters to the channel inputs of a multiplexer is an economical method of reducing normal-mode interference. The filter characteristics can be tailored to the requirements of the channel it serves. Filters may increase the settling time of a channel and aggravate pumpback effects, but these are usually small tradeoffs. It is also possible to place the filter after the multiplexer, but this is not recommended, since each channel will have to charge the filter, increasing the settling time enormously.

In differential systems, filters should have balanced impedance in both inputs (or be connected differentially) to preserve common-mode performance.

Integrating A/D Converter

Where passive filtering of each channel is not practicable, an integrating A/D converter can provide very high normal-mode rejection, particularly at frequencies which have periods that are integral submultiples of the integration interval. Such rejection is obtained with a conversion time that is usually much shorter than the settling time of a filter required to provide the same rejection. Rejection of normal-mode interference to the extent of 40-70dB is easily obtained with an integrating converter. Many integrating converters are also designed for floating guarded-input operation

and provide the best overall common- and normal-mode performance attainable with any type of converter.

Digital Averaging

In systems where a computer or small central-processing unit and store are available, and where the converter can track the variations in input signal produced by interference (a sample-hold can assist), a software approach can be used to reduce the effects of interference. Multiple samples can be taken on each channel and the results digitally summed and averaged. The signal/noise ratio improves as the square-root of the number of samples, provided that sampling and interfering frequencies are uncorrelated.