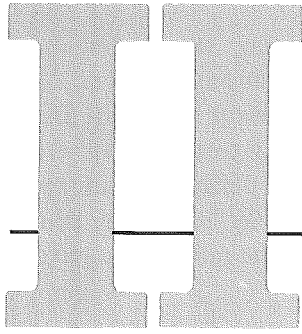


Testing Converters

Chapter 3

INTRODUCTION

The methods and test fixture configurations used to test DAC's and ADC's are influenced by a number of factors relating to converter applications, nature and speed of tests to be performed, and skill of test personnel involved. The relative importance of various converter performance specifications is dependent on each particular application, and the converter user is naturally interested in testing those parameters which significantly influence his system performance to a greater extent than those which have little effect on this performance. Two typical applications illustrate how usage influences the relative importance of various performance parameters:

Differential linearity, fast settling time, and small switching transient (glitch) amplitude are generally of great concern when DAC's are used as cathode-ray tube vector generators, since display quality is critically dependent on these parameters. Small absolute calibration errors or zero drift are generally of little consequence, since they cause only small display size and position shifts, which can be corrected easily by operator display adjustments.

By contrast, a DAC used as a programmable stimulus generator in an automatic checkout system might require good absolute calibration and zero-stability, while not requiring fast dynamic response, transient-free switching, or exceptional differential linearity. Converter test circuit configuration and degree of automation is influenced by: the purpose of the test, e.g.,

engineering performance evaluation, incoming inspection, functional checks only, etc., its versatility, measurement speed, data reduction and display capability, and skill level required for its operation. Simple test fixtures designed to test relatively few converter parameters can be implemented easily and inexpensively. These generally must be operated by relatively skilled persons, and test data obtained usually must be reduced to extract meaningful performance information.

Versatile automatic testers are of necessity complex and are generally costly. A general-purpose automatic tester generally performs tests faster, and can be operated by less-skilled personnel, however. High-resolution converters have a potentially large number of data points which must be examined to extract meaningful converter performance information. A 12-bit DAC or ADC, for example, has 2^{12}, or 4096 possible input/output combinations. Fortunately, by knowing the type of converter errors, or deviations from ideal performance that are commonly encountered, one can devise tests which permit useful performance data to be gained by investigating significantly fewer than the 2^n possible input/output combinations associated with an n-bit converter.

Converter performance parameters that are generally of importance are: calibration accuracy (both absolute and relative to full-scale), linearity (both cumulative and differential), offset, noise, conversion time, and, in the case of DAC's, output switching transient amplitude-time product. Also of concern are stability of these parameters with variations in time and temperature. The purpose of this chapter is to illustrate common converter errors and deviations from ideal performance, and to outline test schemes, for evaluating converter performance, that can be adapted to both manual and automatic testing.

LINEARITY

D/A CONVERTERS

The analog output of the n-bit binary DAC shown in Fig. 1a is

related to its input binary number in the following manner:

$$E_0 = E_{NFS} (B_1\ 2^{-1} + B_2\ 2^{-2} + B_3\ 2^{-3} + \ldots B_n\ 2^{-n}) \qquad (1)$$

where the digits $B_1 \ldots B_n$ of the binary number N each have the value 0 or 1, and E_{NFS} is the nominal full-scale output. Since

$$\sum_{i=1}^{n} 2^{-i} = 1 - 2^{-n}, \qquad (2)$$

the relation between the output with all bits "1", and nominal full-scale output E_{NFS} is

$$E_0\Big|_{B_1, \ldots B_n = 1} = E_{NFS} (1 - 2^{-n}) \qquad (3)$$

and, since 2^{-n} = 1LSB, E_{FS}, the output with all bits "1" is the nominal full-scale output minus 1LSB. That is

$$E_{FS} = E_{NFS} [1 - LSB] \qquad (4)$$

The analog values associated with each of the bits acting individually can be found by setting the desired bit B_i to logic "1" and all other bits to "0". Then

$$E_0\Big|_{B_i} = E_{NFS}\ 2^{-i} \qquad (5)$$

Relation (1) indicates a linear relationship between analog output and digital input. It follows that the sum of the analog output values obtained for any combination of bits acting individually should equal the analog output obtained when all bits of this combination are applied simultaneously. This forms the basis for a simple and effective linearity test: Various combinations of bits are turned on and the associated analog output noted. Each bit of this combination is then applied independently and its output recorded. The algebraic sum of these outputs is then compared to that obtained for all bits of the chosen combination turned on together. The difference is the linearity, or summation, error.

With most converters, the maximum linearity error occurs at full-scale. In this case, "all bits on" is the worst-case bit combination.

Converter linearity errors are independent of scale-factor calibration or gain errors. Accurate linearity measurements can be

made, even on an uncalibrated DAC. The nonlinearity of the measurement device must be significantly less than that being measured. A 12-bit DAC having a nonlinearity of the order of ±½ LSB (= 1 part in 8192) requires a 5-digit DVM for meaningful linearity measurements in the circuit of Figure 1a. In addition, one should note that a zero error (non-zero output for zero input) must be corrected, so as not to introduce an error in the linearity measurement, since it is added once for each output reading taken. Consider the inequality,

$$E_0 (B_1 + B_2 + \ldots + B_n) + \epsilon_{LIN} + \epsilon_Z \neq E_0 B_1 + E_0 B_2 + \ldots E_0 B_n + n\epsilon_Z \quad (6)$$

where ϵ_{LIN} is the full-scale linearity error and ϵ_Z is the zero error. The left side of inequality (6) has the zero error added once (all bits on), while the right side has the zero error added n times (n individual readings). Converters using a half-scale offset to accomplish bipolar operation (e.g., offset-binary coding) must be tested for linearity (by this method) in the unipolar operating mode (half-scale offset disconnected) to prevent large errors similar in nature to those indicated by relation (6), but greater in magnitude. When making linearity (or gain) measurements, there is less possibility for computational error if the zero error is recorded and subtracted from each subsequent bit reading before any linearity or gain calculations are made. The simplest way to correct for zero (computationally, at least) is to electrically zero the converter before data are taken.

A/D CONVERTERS

The process of ascertaining linearity of an ADC is similar to that described above for a DAC. Consider the ADC of Fig. 1b, having its output binary number N related to its input analog signal E_{IN} in the following manner:

$$E_{NFS} (B_1 2^{-1} + B_2 2^{-2} + B_3 2^{-3} + \ldots + B_n 2^{-n}) = E_{IN} \pm ½ \text{ LSB (quantizing uncertainty)} \quad (7)$$

where the definitions associated with relation (1) apply. The analog input E_{IN} required to turn each bit on can be found by

setting each bit except the desired one to zero in the relation (7). That is,

$$E_{IN}\big|_{N = B_i 2^{-i}} = E_{NFS}\, 2^{-i} \tag{8}$$

ADC linearity can be evaluated by applying each of the analog input values required to turn on only one bit of a particular bit combination to be examined for linearity. The sum of these analog inputs, when applied to the ADC input, should turn on all bits of the selected combination, and no others.

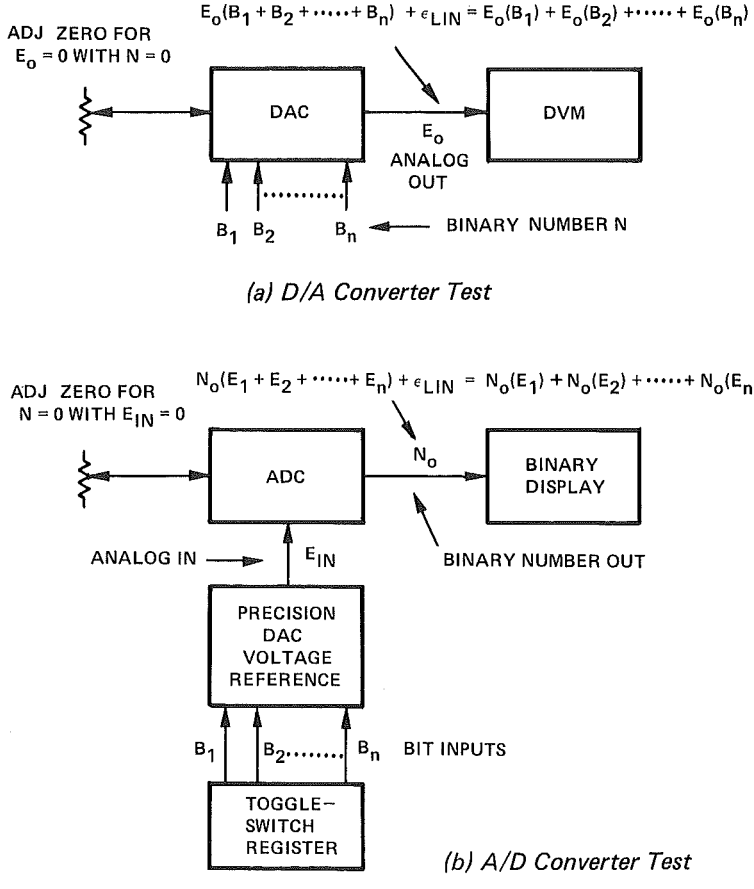


Figure 1. Linearity (Summation) Test

The most convenient method of generating binarily-scaled analog reference values, with which to test ADC's for gain calibration or linearity, is by means of a precision reference DAC and associated toggle switch register, as shown in Fig. 1b. To simplify linearity measurement, the ADC is first calibrated in the following manner: all bits of the reference DAC are turned off; this applies zero analog input to the ADC. The ADC zero control is adjusted for digital zero on the binary display. (The reference DAC and ADC are assumed to have identical scale factors so that ideally, the ADC, when properly adjusted, will have a full-scale output for full-scale input to the toggle-switch register. For convenience, the ADC is calibrated at half-scale. Bit 1 (MSB) of the toggle switch register is turned on, and the ADC gain control is adjusted for bit 1 on only, as viewed on the binary display.

Individual bit gains can then be checked by turning each of the toggle switch bit inputs on and off in succession and looking for correspondence on the binary display. Since linearity error is generally greatest at full-scale, nonlinearity can be checked quite easily, assuming that the individual bit gains are correct, as determined by correspondence between ADC output and reference DAC input for each individual bit. Starting at the most-significant reference-DAC bit-input, each bit, in descending order, is turned on and left on. Any difference between the displayed ADC output and toggle-switch-register input codes, as full-scale is approached, is then caused by an ADC nonlinearity (assuming the nonlinearity of the reference DAC to be negligible).

The methods described above for ADC calibration and linearity testing tacitly assume that the ADC can be calibrated so that each analog calibration value is centered in the respective quantization band corresponding to the desired output code. Methods for accomplishing this are described in the section on ADC testing.

GAIN CALIBRATION

Converter accuracy can be specified in two ways: (a) absolute and (b) relative to full-scale. In testing for (a), one is concerned with ascertaining the calibration of any bit or combination thereof with

respect to some absolute external standard. In testing for (b), one is concerned only with ascertaining calibration accuracy relative to the converter's full-scale value. Since, in most instances, the converter's internal calibration reference consists of a temperature-compensated zener reference diode, which might age at the rate of 0.01%/1000hrs. operation, one usually accepts the fact that high-accuracy converters require periodic recalibration to maintain rated absolute calibration accuracy.

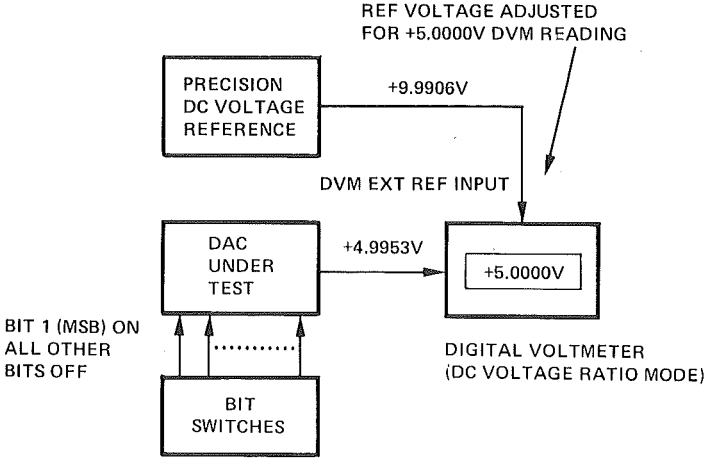
Testing for converter accuracy relative to full-scale is generally of greater interest, since this tests the stability and ratio accuracy of the converter's precision weighting network and active switching elements; weighting network ratio adjustments are normally not provided on contemporary modular converters (whereas full-scale adjustment is, because of the realities mentioned above.) The evaluation of converter gain accuracy can be expedited by normalizing gain to some convenient reference value. In the case of converters having *zero* and *gain* adjustments, this is simply accomplished by calibrating zero and full-scale before recording the various bit (or combination of bits) readings. The evaluation of gain accuracy relative to full-scale for units having no external calibration adjustments can be expedited by normalizing gain prior to recording the data.

Two methods for accomplishing gain normalization external to the DAC under test are shown in Figs. 2a and 2b. In both figures, it is assumed that the relative accuracy of the individual bit gains and the linearity of the converter are to be tested.

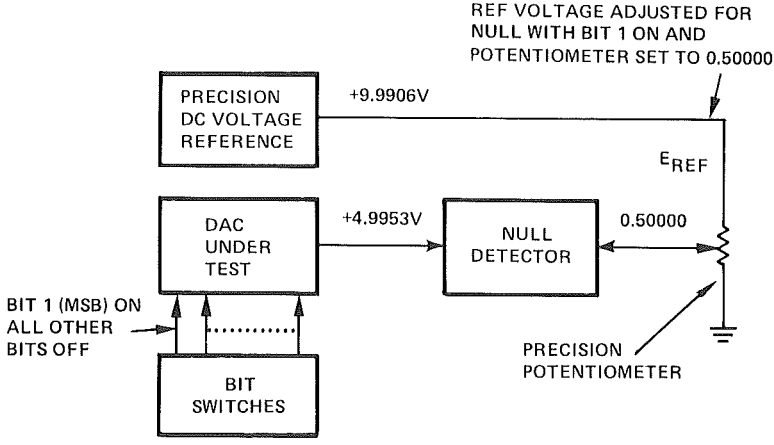
In Figure 2a, a DVM, operated in the ratio mode, is used to read the DAC output. The DAC zero output is first adjusted (all bits off). Bit 1 is then turned on. The value of a stable dc precision reference standard applied to the DVM ratio reference input is adjusted to make the DVM read +5.0000V (nominal full-scale assumed to be +10V).

In Figure 2b, a precision potentiometer is used to measure the DAC output as a fraction of some reference voltage applied to the high side of the potentiometer. At any bit setting, the position of the potentiometer arm is varied until the pot output voltage equals that of the DAC, as indicated by a zero reading

at the null detector. The measurement is first normalized at any desired DAC setting –half-scale in the example of Figure 2b– by adjusting the reference voltage for null at the corresponding potentiometer setting.



(a) DVM in Ratio Mode



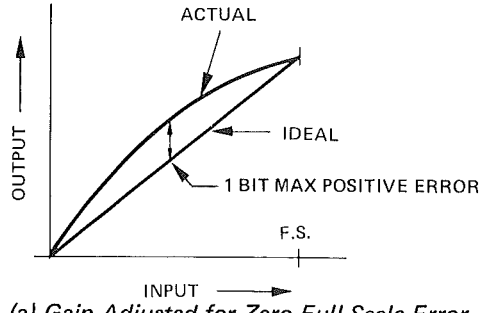
(b) Precision Potentiometer & Null Meter

Figure 2. DAC Gain Normalization Methods

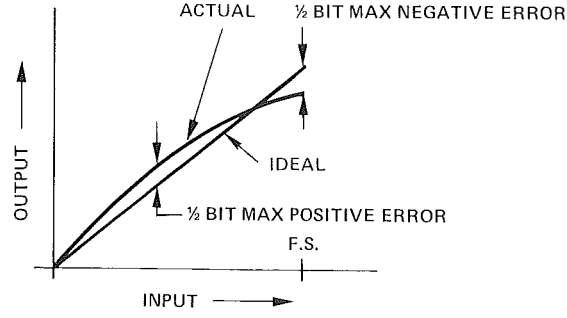
If the converter is nonlinear, the peak linearity error is dependent upon the point chosen for gain calibration or normalization, as illustrated in Figure 3. In Figure 3a, a peak error of 1 bit is assumed to exist at some point on the device transfer function

when the unit is calibrated at full-scale. In Figure 3b the device gain has been adjusted to minimize the peak error – in this case, to ±½ bit. In practice, it is generally found that peak linearity error (deviation from a "best straight line") will be minimized if the converter gain is calibrated at roughly 3/4 scale. If the device nonlinearity is less than ¼ bit, the exact point chosen for gain calibration has little effect on device accuracy.

If this nonlinearity is greater than ¼ bit, the output point chosen for gain calibration can determine whether or not the converter meets its accuracy specification (generally ±½ bit), since some differential nonlinearity (to be described shortly) must be presumed to exist in any converter. Because calibration at full-scale is straightforward and requires the most conservative linearity and relative-accuracy specification, Analog Devices does this as a standard practice in specifying converters, rather than choosing a "best straight line" approach.



(a) Gain Adjusted for Zero Full-Scale Error



(b) Gain Adjusted to Minimize Peak Error

Figure 3. Effect of Gain Adjustment on Linearity Error for Non-Linear DAC or ADC

ZERO AND GAIN CALIBRATION

Calibration of the transfer function of a linear device requires determination of two points within the linear operating region of the device. The choice of calibration points and exact procedure depends somewhat on the nature of the particular device under test; generally, device zero is adjusted and then gain is calibrated.

UNIPOLAR DAC

The typical calibration procedure for a unipolar DAC is illustrated in Figure 4a: all bits are turned off (binary zero), and the zero control is adjusted for zero analog output. All bits are then turned on and the gain control is adjusted for correct full-scale output. (Gain could equally-well be calibrated at either 1/2 or 3/4 scale, as discussed above. Device accuracy can then be checked by turning on and off each bit in succession and comparing each bit output with its corresponding theoretical reference value. Worst-case gain error can then be found by turning on all bits having low individual outputs in relation to their respective reference values and noting the DAC output. The process is repeated for all bits having high individual bit outputs with respect to their respective reference values. The DAC output for each of these two bit combinations, which corresponds to worst-case negative and positive gain error, respectively, is then compared to the theoretical value for each of these sums. The worst-case + or − bit sum error should be less than the device error specification − generally ±½ bit at room temperature.

It should be noted that testing for worst-case calibration error in the manner described above assumes negligible nonlinearity errors. The bit combination corresponding to worst-case positive or negative gain error will not necessarily correspond to that which causes greatest nonlinearity. Nonlinearity can be checked independently of calibration as described earlier.

BIPOLAR DAC USING OFFSET BINARY OR 2'S COMPLEMENT (OB WITH COMPLEMENTED MSB)

DAC's or ADC's having offset binary coding (as distinguished from

sign-magnitude coding) are generally made bipolar by summing with the unipolar output of the DAC weighting network a fixed analog output equal in magnitude, but opposite in polarity, to the first bit (MSB) analog equivalent. This shifts the DAC unipolar transfer characteristic of Fig. 4a down by half-scale, as shown in Figure 4b. With most DAC's (or ADC's), the gain control affects only the unipolar scale factor, and not that of the bipolar offset. DAC's (or ADC's) of this type are generally calibrated in the following manner: All bits are turned off (binary zero) and the bipolar offset is adjusted for correct negative full-scale reading. Bit 1 is then turned on and the gain is adjusted for zero output. All bits can then be turned on, providing a calibration check at + full scale. (Alternatively, the gain can be calibrated at + full scale, with zero analog output providing the calibration check point.) The general calibration procedure, while described for DAC's, is quite similar for ADC's (ADC calibration is discussed under ADC testing).

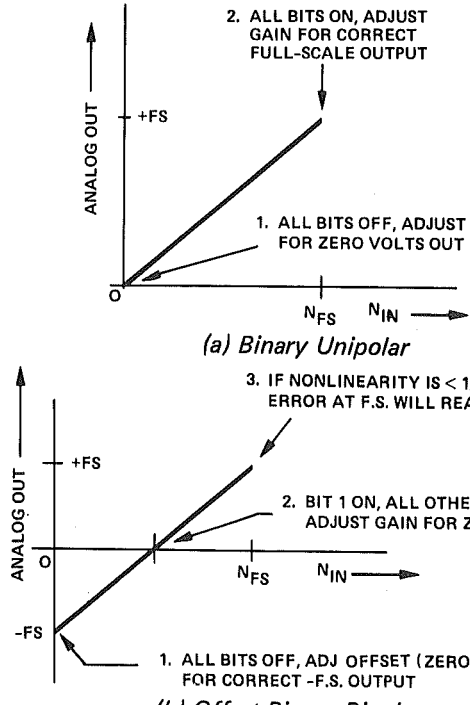


Figure 4. Typical DAC Calibration Procedure

TEMPERATURE EFFECTS

The manner in which the DAC unipolar and offset binary bipolar DAC output can shift with temperature is illustrated in Figures 5a, 5b, and 5c. In the unipolar DAC transfer curve of Figure 5a, a zero shift moves the transfer curve up or down. Since a zero shift affects all output readings by the same amount, zero temperature coefficient is expressed either directly in $\mu V/^{\circ}C$, or as a fraction (% or ppm) of *full-scale* per °C. A gain shift, on the other hand, causes the slope of the transfer curve to change. This affects all output readings by the same percentage. Gain temperature coefficient is therefore generally specified as % or ppm of *reading*/°C.

In the case of a bipolar DAC, if the temperature coefficient of the half-scale offset were exactly matched to that of the unipolar transfer curve, and there were no zero shift, the bipolar transfer curve would rotate about the zero output point with temperature, as shown in Figure 5b. In actual practice, this does not occur. The difference between the bipolar offset and unipolar gain temperature coefficients, plus the zero temperature-coefficient of the unipolar transfer characteristic will cause the bipolar transfer curve to shift up or down with temperature. The unipolar gain-temperature coefficient causes the bipolar transfer curve to rotate about the intersection of this curve with the output axis as shown in Figure 5c. Figure 5c illustrates that in the case of bipolar converters having offset binary coding, the shift in output zero with temperature is a function of both gain *and* offset shifts.

DIFFERENTIAL NONLINEARITY

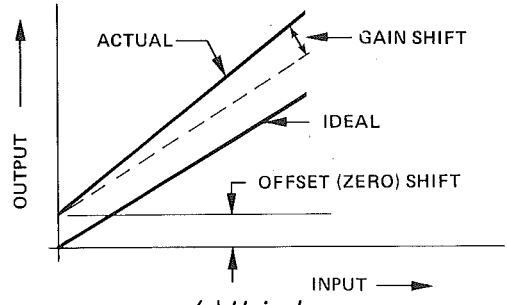
Differential nonlinearity is a measure of the variation in analog value change associated with a one-bit change in the associated digital number, for either a DAC or an ADC. Ideally, a one-bit digital value change should have associated with it a constant (i.e., 1LSB) incremental change in analog signal anywhere on the input/output transfer characteristic. Differential nonlinearity can be quantified in the following manner: Assume an analog signal span E_s, and an n-bit binary converter. A normalized 1-bit increment ΔE_N can be defined, such that

$$\Delta E_N = E_S \, 2^{-n}$$

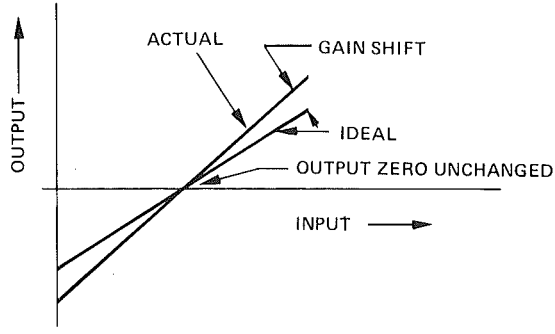
Differential linearity error, ϵ_{DL}, can then be defined by the relation:

$$\epsilon_{DL} = (\Delta E - \Delta E_N)/\Delta E_N$$

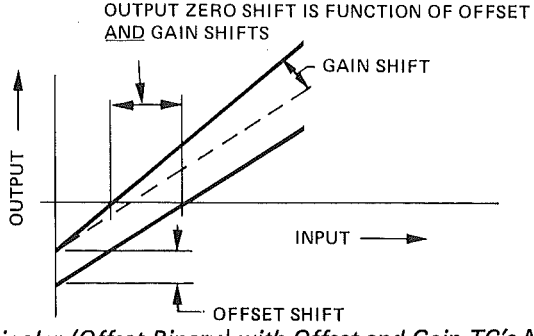
where ΔE is the actual change in analog value associated with any 1-digit change in the binary number.



(a) Unipolar



(b) Bipolar (Offset Binary) with Offset and Gain TC Matched



(c) Bipolar (Offset Binary) with Offset and Gain TC's Not Matched

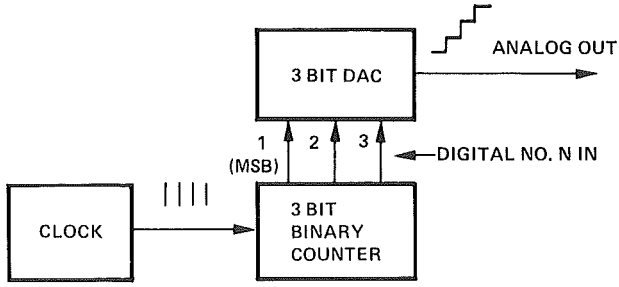
Figure 5. Effects of Gain and Offset Shifts on DAC Output

The greatest differential nonlinearity occurs at major carry transitions of the digital number, where significant weighting network gain-factor switching occurs. To illustrate, consider a 3-bit DAC, driven by a 3-bit binary counter to sequentially generate all possible 3-bit codes corresponding to the fractions 0 to 7/8 of full-scale, as shown in Figure 6a. Ideally, this should produce a staircase output waveform having equal step heights. If the weight of the MSB (Bit 1) is ½-bit low, the output transition from code 011 (3/8) to 100 (4/8) will be ½-bit too small. All succeeding code transitions will have correct amplitude, but the output values associated with each of the codes 5/8 . . . 7/8 will be ½-bit low in terms of absolute calibration. In this case, a ½-bit differential linearity error occurs at the major carry code transition, as shown in Figure 6b.

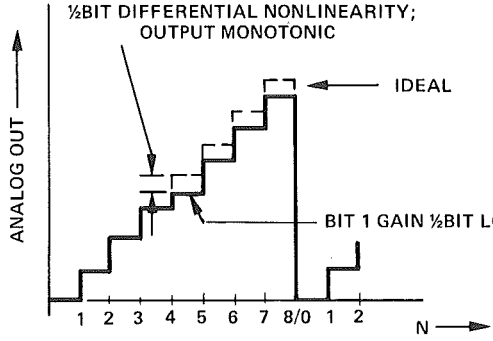
MONOTONICITY

A monotonic output is one that either increases or remains constant, for increasing input, so that the output will always be a single-valued function of input. (Mathematically, this requires that the 1st derivative of a continuous output-input transfer function be $\geqslant 0$; for a variable having discrete steps, the first *difference* must be $\geqslant 0$.) Assume in the example of Figure 6a that the DAC has a bit 1 weight more than one bit low in relation to the weights of bit 2 and bit 3. In this case, the code transition from step 3 to step 4 will actually be *negative,* as shown in Figure 6c, a non-monotonic response. It should be noted that a converter specification of ±½-bit differential nonlinearity is more stringent than one of guaranteed monotonicity, since non-monotonicity implies a differential nonlinearity greater than 1 bit.

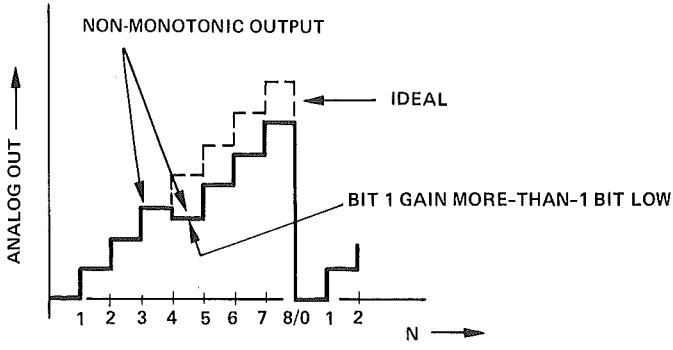
Normal device nonlinearity, as shown in Figure 3, has negligible effect on differential nonlinearity. To illustrate, consider a 10-bit converter having a ±½-bit nonlinearity. If this nonlinearity is assumed uniformly distributed over the full range of $2^{10} = 1024$ bits, the differential nonlinearity contributed at any code transition by this ±½-bit linearity error is no greater than 1/2048 bit.



(a) DAC Driven by Counter



(b) Differential Non-Linearity Error

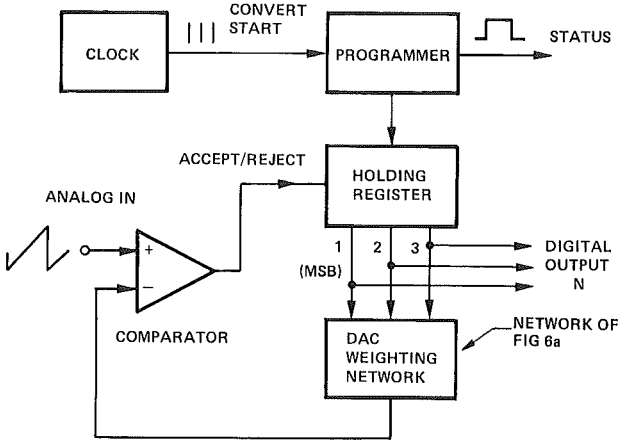


(c) Non-Monotonicity

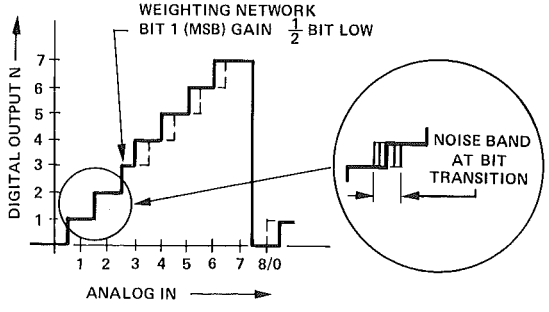
Figure 6. DAC Differential Linearity and Monotonicity Errors

The effect of switch and weighting-network differential non-linearity on the digital output of a successive-approximation ADC is illustrated in Figure 7. Figure 7 shows a 3-bit successive-approximation ADC configuration using the DAC of Figure 6a as its weighting network. The analog ramp input to this converter is

assumed to be slowly-varying with respect to the conversion rate, so that each point on the analog waveform is successively digitized within the ±½-bit quantization-error limits inherent in the A/D conversion process. The converter's ideal output is a sequence of codes corresponding to the binary numbers 000 through 111 (0-7), with each code corresponding to the ideal analog value. If bit 1 (MSB) of the weighting network has a weight ½ bit low with respect to those of bits 2 and 3, as in the example of Figure 6, the digital output will jump to the code 100 (4) ½-bit sooner than it should. The effect on the output is to cause a narrowing of the step width corresponding to the code 011 (3) immediately



(a) Successive Approximation ADC



(b) Digital Output

Figure 7. Effects of Noise and Weighting Network Differential Non-Linearity on ADC Output

preceding the code 100 when bit 1 turns on and bits 2&3 turn off, as shown in Figure 7b. Conversely, if the weighting network has its bit-1 gain ½-bit high with respect to bit-2 and bit-3 gains, the width corresponding to the code 011 (3) will be ½-bit too large. In both cases, the widths corresponding to output levels 4-7 will have a correct 1-bit amplitude.

The waveform inset of Figure 7b illustrates that noise in the analog input to the converter circuit introduces an uncertainty in the analog code transition value. (The noise band associated with each code transition value can be found using an ac dither signal, as will be described in the section on ADC testing.)

If the bit 1 gain of the weighting network is more than 1 bit low, as in the DAC output waveform of Figure 6b, the code 011 will not occur and the digital output will skip from 010 (2) to 100 (4), i.e., a non-monotonic weighting network causes missing ADC output codes. A comparison of the waveforms of Figures 6b and 7b shows that a differential nonlinearity causes a variation in the output step *height* for the case of a DAC transfer function, and causes a variation in output step *width* for the case of an ADC transfer function.

DAC TESTING

A simple and effective DAC test configuration is shown in Figure 8. The digital inputs to both the device under test (DUT) and a highly-accurate reference DAC are driven in parallel from either a toggle-switch register or a dynamic programmer. Both the reference DAC and the DUT have the same output range. The output of the reference DAC is compared to that of the DUT. The difference between the two outputs is amplified in an error amplifier, which has its gain calibrated to provide a defined error output with some convenient volts-per-bit scale factor. The toggle-switch register permits selection of logic 0, logic 1, or "dynamic program" for each input bit. This permits entry of any desired code for static-accuracy tests, or dynamic programming for high-speed dynamic testing. Gain and zero adjustment can be provided in the reference DAC to effect gain normalization and zero calibration in the event the DUT has no provision for internal gain or zero calibration.

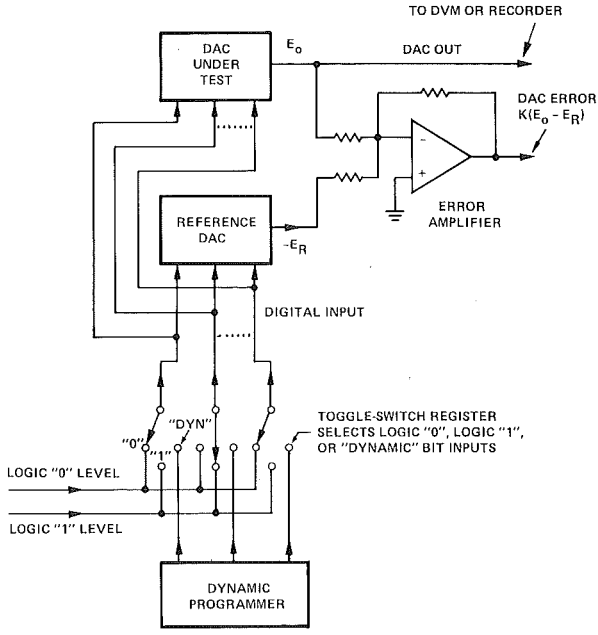


Figure 8. Basic DAC Tester

DYNAMIC PROGRAMMING

There are two dynamic programming modes that are of particular value in permitting the linearity and accuracy characteristics of the DUT to be assessed quickly; they are the *bit-scan* and *count* modes.

Bit-Scan Mode

In the "bit-scan" mode, the individual bit inputs to both the DUT and the reference DAC are time-division multiplexed, so that each bit input is turned on and off in succession. Two additional multiplexed time slots are allocated to full-scale (all bits on) and zero (all bits off) to facilitate device calibration. A bit-scan dynamic programming configuration is illustrated in Figure 9. The resulting bar graph of output error can be displayed on an oscilloscope or a high-speed strip-chart recorder (if a permanent record is desired). Figure 10a shows a typical commutator time-slot allocation for testing a 12-bit DAC in the bit-scan mode.

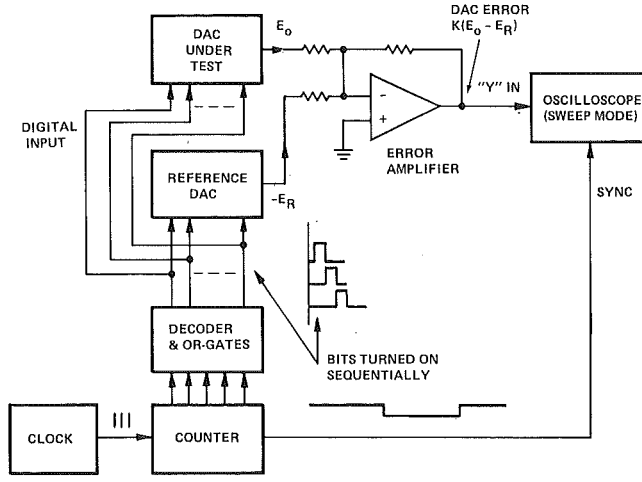
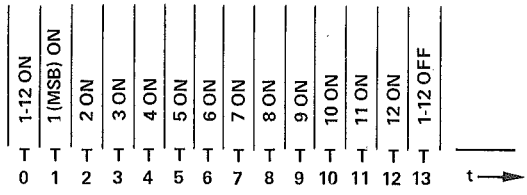


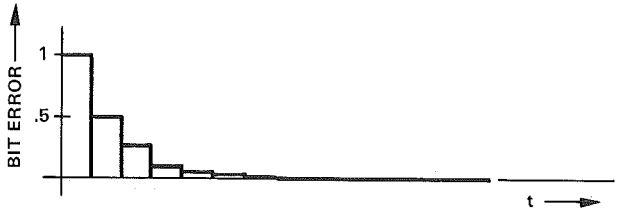
Figure 9. DAC Dynamic Test – BIT-SCAN Mode

Typical error displays resulting from this test are shown in Figures 10b, c, and d. Figure 10b illustrates an error display for a DAC having the correct binary scaling weights for all bits, but full-scale gain calibration 1-bit high. Since a 1 LSB full-scale gain error (with correct relative scaling) causes the bit 1 error to be ½-bit high, bit 2 to be ¼-bit high, bit 3 1/8-bit high, etc., the error display is exponential in shape, in this case. Figure 10c illustrates the error display for the case of a +¼-bit offset error, combined with a −1-bit full-scale gain error, assuming perfect relative weighting (i.e., differential linearity). This causes a reversal in full-scale error polarity from that shown in Figure 10b. In addition, the +¼-bit offset (zero) error shifts the complete display +¼ bit from the zero error baseline. The DUT is calibrated in the following manner, using the bit scan display: Zero is adjusted to bring the bar representing the zero error (time slot T13 in Figure 10a) to the display baseline. The gain is then adjusted to bring the bar corresponding to full-scale (time slot TO) to the baseline. Zero and full-scale of the DUT are now calibrated. (If the DUT does not have zero full-scale or full-scale adjustments, zero and full-scale of the reference DAC can be adjusted instead, to normalize the display.)

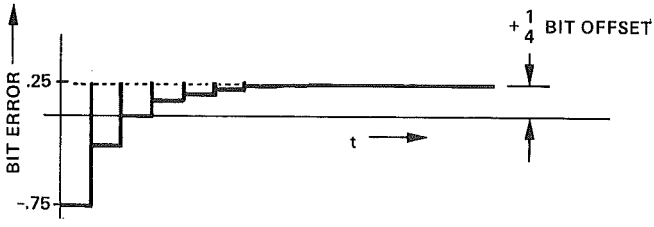
A typical "bit scan error" display after zero and full-scale of the DUT (or reference DAC) have been calibrated, is shown in Figure 10d. If the DUT is perfectly linear, the sum of all positive bit errors should equal the sum of all negative bit errors after zero and full-scale calibration; any residual error is caused by device nonlinearity.



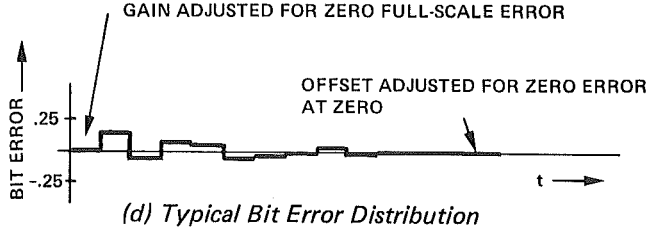
(a) Commutator Time-Slot Allocation



(b) DAC Full-Scale Gain 1-Bit High and Zero Offset



(c) DAC Full-Scale Gain 1-Bit Low and ¼-Bit Offset



(d) Typical Bit Error Distribution

Figure 10. 12-Bit DAC Dynamic Test Waveforms Bit-Scan Mode

Count Mode (Figure 11)

In the dynamic programming "count" mode, the digital inputs to both the reference DAC and DUT are driven from a counter so that all possible DAC input code combinations are sequentially generated. This produces a staircase output waveform from the DUT and the reference DAC. Zero and full-scale are most conveniently calibrated in the bit scan mode, as described above. After this calibration has been completed, the error display in the "count" mode is ideally a straight line. Using this testing technique, combined with a high-speed recording oscillograph, and a count rate of 1ms/step, all codes can be generated and a permanent error record obtained in approximately 4 seconds for a 12-bit DAC, and 64 seconds for a 16-bit DAC.

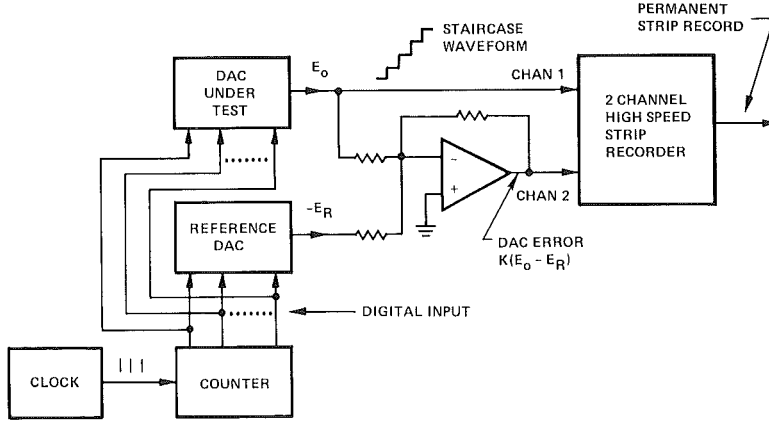
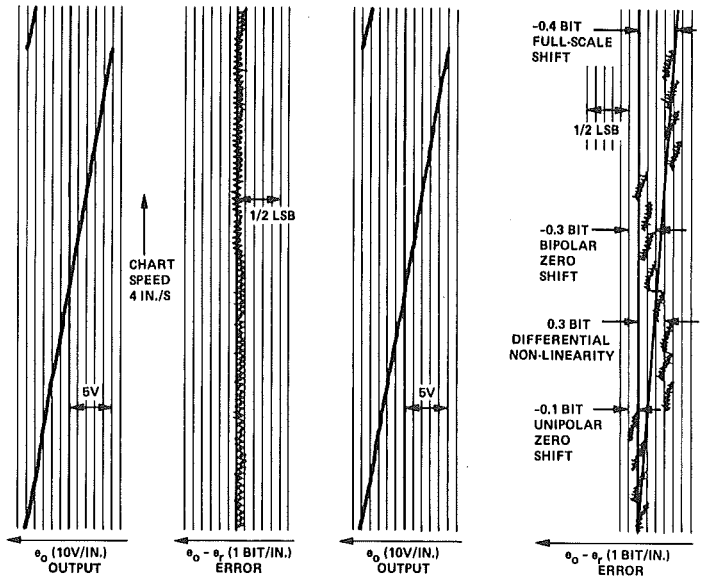


Figure11. DAC Dynamic Test – COUNT Mode

COUNT-MODE ERROR RECORD EXAMPLE

The usefulness of the error record obtained in the *count* mode as a means of quickly assessing DAC performance at various temperatures is shown by the error records in Figures 12a and 12b, obtained from an ADI Model DAC-10Z-2 10-bit ±5V bipolar D/A converter, tested at 25°C and 70°C, respectively. In these figures, the output e_o of the DUT is recorded directly on another oscillograph channel, to provide a scale reference. A line is drawn through the error-sweep waveform between zero and full-scale.



(a) DAC-10Z-3 @ +25°C *(b) DAC-10Z-3 @ +70°C*

Figure 12. DAC Tester Output Waveform-COUNT Mode Typical Chart Recording

The slope of this line represents the gain error of the DUT. Deviations from this straight line are caused by linearity and differential-linearity errors. Differential nonlinearity is measured by the peak-to-peak amplitude of the abrupt transition in the error curve occurring at the major-carry transitions of the digital-input code to the DUT. This is a measure of the difference in analog increment corresponding to a change of 1 LSB in the input digital code.

As can be seen from the error record of Figure 12a, the DUT has gain, offset, differential linearity, and linearity errors less than 0.1 bit at +25°C. The error waveform of Figure 12b shows that, at +70°C ambient temperature, full-scale and bipolar zero outputs

have shifted −0.4 bit and −0.3 bit from their respective values at 25°C. At 70°C, the differential nonlinearity is 0.3 bits; the nonlinearity (deviation from the straight line joining the digital zero and full-scale analog values) is approximately half the differential nonlinearity, or 0.15 bit. Since 1 LSB, for a 10-bit DAC, is 1/1024 of FS (or 977ppm), the average gain and zero TC's in the range 25°C to 70°C are 0.4 X 977ppm/45°C = 8.7ppm/°C and 0.3 X 977ppm/45°C = 6.5ppm/°C. The unipolar zero (all bits off) has shifted −0.1 bit, while the bipolar zero (digital half scale) has shifted −0.3 bit at 70°C, corresponding to average unipolar and bipolar zero TC's of 2.2 and 6.5ppm/°C, respectively, in the temperature range 25°C to 70°C.

The error records of Figure 12 illustrate the important point that device differential nonlinearity is almost independent of the gain calibration points. That is, choosing a "best straight line" through the DAC output/input transfer curve to minimize gain or linearity error will have negligible effect on the differential linearity of the device, since the differential nonlinearity is the *peak-to-peak* error occurring at the 1-bit code changes associated with major carries in the input digital number.

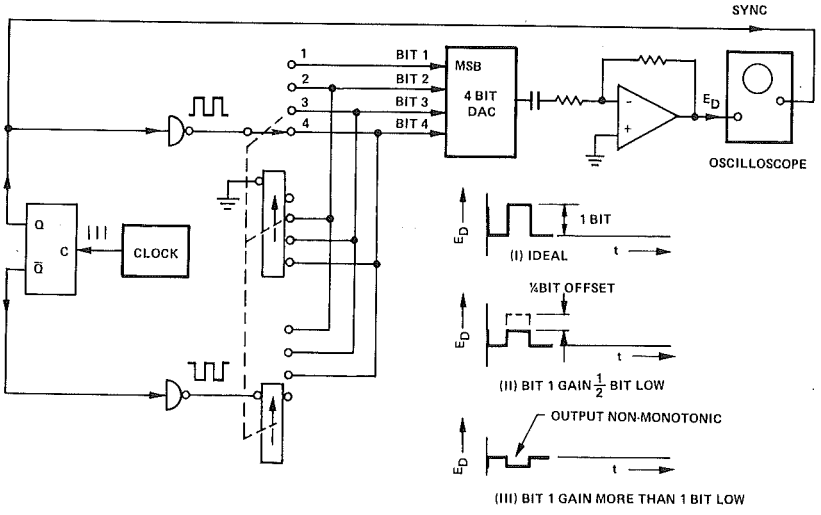
DIFFERENTIAL LINEARITY TESTER

A simple scheme for testing DAC differential linearity is shown in Fig. 13a, for the case of a 4-bit DAC (for simplicity). A three-section ganged switch is wired to the DAC bit inputs so that the bit codes at either side of each carry-transition are examined by means of two out-of-phase square-waves applied to the two switch input lines. The carry transitions examined in each switch position are tabulated in Table 1 below.

Switch position	1	2	3	4
Code transition	1000 0111	0100 0011	0010 0001	0001 0000

Table 1. 4-bit DAC Code Transitions for Differential Linearity Test

Ideally, the ac component of DAC output for each switch position is a square-wave having 1 LSB amplitude. Waveforms for several differential linearity possibilities are shown in Figure 13b. It should be noted that this test configuration tests differential linearity at major carry transitions only up to half-scale. This is generally sufficient to accurately characterize the differential linearity behavior of the device, since, unless the device is markedly nonlinear, the differential nonlinearity pattern associated with bit-2-bit-4 code transitions will repeat itself in the range from half-scale to full-scale output.



(a) Circuit Diagram *(b) Waveforms at Half-Scale*

Figure 13. Simple DAC Differential Linearity Tester

Offset Method of Differential Nonlinearity Measurement

An alternate technique to that shown in Figure 13 for measurement of differential nonlinearity is shown in Fig. 14. The reference number, N_R, corresponding to the code of interest is applied to the DUT through the toggle-switch register. A digital subtractor subtracts 1 digit from this reference number so that $N_R - 1$ is applied to the input of a highly-accurate reference DAC.

The difference between the output of the DUT and the reference DAC is amplified and displayed on an error indicator. Ideally, this indicator should display a constant 1-bit difference for any number, N_R, applied to the input of the DUT. Differential nonlinearity at each bit code transition is tested merely by turning each individual bit switch in the toggle-switch register on and off in succession. For example, at the major carry, N_R = 1 0 0 0 0. . 0, and $N_R - 1$ = 0 1 1 1 1 1 1. . 1. Differential nonlinearity is measured as the deviation from the ideal 1-bit step.

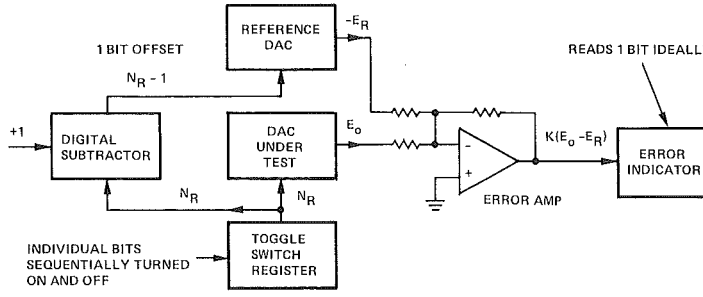


Figure 14. Offsetting Digital Input to DAC Under Test to Check Differential Linearity at Major Carry Transitions

DIGITAL DITHER GENERATOR

Frequently, the evaluation of DAC dynamic response characteristics relating to differential linearity, settling time, and switching transient (glitch) amplitude can be expedited if the DAC output can be periodically cycled through a few counts either side of each specific input code transition of interest so that the DAC output can be observed with an oscilloscope as that particular code transition is repetitively traversed from each direction. Two methods for accomplishing this are now described.

Open-Loop Digital Dither Generation

An open-loop scheme for generating a digital dither signal is shown in Figure 15. An up/down counter is preset to the reference number N_R corresponding to the code of interest. A divide-by-four binary counter and count direction control flip-flop are

driven from the clock so that groups of 4 clock pulses are counted in the up and down directions alternately, so that there is no net change in the counter state at the completion of an 8-count up-down cycle. The up/down counter is preset to N_R in the middle of each burst of up and down pulses. This redundant input forces the up/down counter into the correct reference state twice per cycle, thus preventing this counter from becoming inadvertently offset from the desired reference state N_R by spurious noise pulses.

Alternatively, by incorporating independent digital high and low limit comparators, the count direction of the up/down counter can be reversed each time the high or the low limit is reached, rather than after a defined number of pulses has been counted in each direction, as in the scheme of Figure 15. This variation of the scheme permits independent control of digital dither amplitude as well as the reference code through the application of programmed high and low limits.

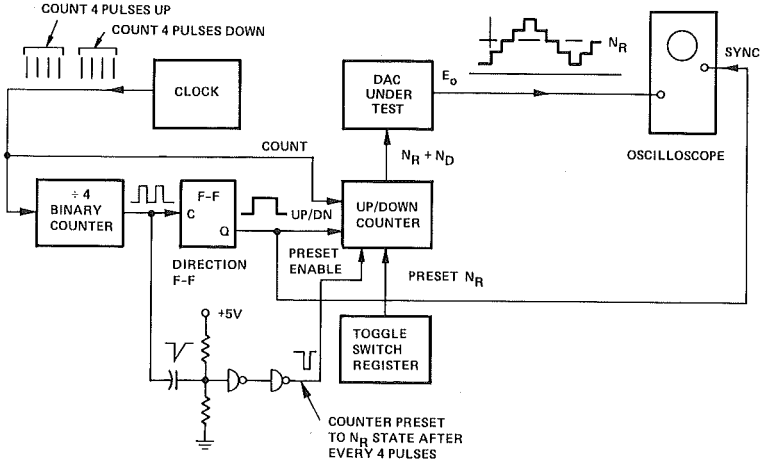


Figure 15. Digital Dither Generation for DAC Differential-Linearity Dynamic Testing

Closed-loop Dither Generation

A closed-loop digital dither generation scheme is shown in Figure 16. In this scheme, the reference number, N_R corresponding to

the code of interest is applied to the digital input of a reference DAC. A digital accumulator configured as a 1-bit adder/subtractor generates the digital dither, causing the code applied to the DUT to oscillate about the reference number N_R. This is accomplished in the following manner: At each "add" time the digital number stored in the accumulator is incremented 1 bit, either up or down, depending on the state of the add/subtract *enable* line. The output of the DUT is compared to that of the reference DAC, which has N_R as its input. The difference in these two outputs is amplified and applied to the input of a Schmitt trigger. The output of this Schmitt trigger drives the add/subtract *enable* line of the digital accumulator. A cycle of operation is as follows: The analog error increases at each "add" time until the output of the error amplifier exceeds the Schmitt trigger hysteresis threshold reference level. This causes the Schmitt trigger to change state, causing the accumulator to increment in the opposite direction until the analog error exceeds the new threshold level of the Schmitt trigger, at which point the add/subtract *enable* line again changes state, causing the accumulator to increment in the original direction. Dither amplitude can be controlled by varying the gain of the error amplifier to control the number of increments required to overcome the Schmitt trigger hysteresis level. Sufficient filtering must be provided to avoid triggering the Schmitt trigger by transient spikes (glitches).

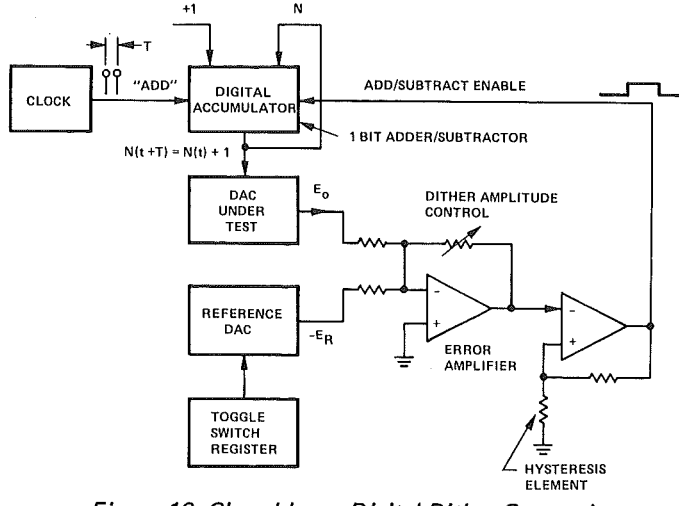


Figure 16. Closed-Loop Digital Dither Generation

DAC SETTLING-TIME MEASUREMENT

DAC settling time is a parameter of importance in high-speed applications. Settling time is defined as the time required for the output to approach a final value within the limits of a defined error band, for a step change in input. This fixed error band is generally expressed as a fraction of full scale, typically ±½-bit. If the device step response is oscillatory, so that the output swings through the defined error band before entering it for the final time, the above definition tacitly implies that settling time is measured as the time required for the output to enter the defined error band for the *final* time. The above settling time definition implies that the greater the output step change, the longer the settling time (a 1-bit output step change, for example, will be within ±½ bit of final value when this change has reached only 50% of its final value).

In addition to the usual constraints imposed on settling time by normal closed-loop linear bandwidth considerations, large output changes are generally slew-rate limited. There are two settling times of interest, depending on the application. These are *full-scale* and *bit-to-bit tracking,* depending on whether successive digital inputs are sequential or completely random in nature.

The accurate measurement of settling time for a high-resolution, high-speed DAC is fraught with practical difficulties. Measurement instrument bandwidth and thermal unbalance effects, coupled with the unavoidable presence of noise, can introduce significant measurement uncertainties when high-speed settling times to within error bands of the order of the order of 0.01% of final value are being measured.

Zero and Full-Scale

The general test configuration for measuring full-scale settling time is shown in Figure 17a. All digital input lines except that driving the LSB are connected together and driven with a square-wave having fast rise and fall times with respect to the response times being measured. The LSB DAC input line is connected to a

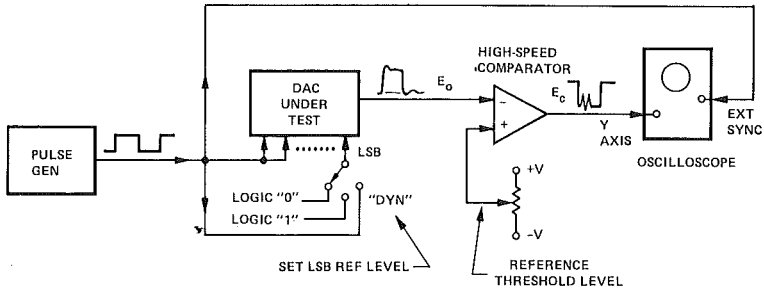
three-position switch so that logic "0", logic "1", or "dynamic" input (consisting of the square-wave drive applied to the other bits) can be selected. When this switch is in the "dynamic" position, the DAC output is driven alternately between zero and full-scale. The DAC output is compared to a threshold reference level at the input to a high-speed comparator so that the comparator output will change state when the DAC output E_0 exceeds the threshold reference level E_R. The comparator output is displayed on an oscilloscope having its sweep start synchronized to the square-wave applied to the DAC's digital input. Choice of logic "0", logic "1", or "dynamic" for the LSB DAC digital input facilitates setting the comparator threshold reference level to within ½-LSB of the DAC full-scale output.

Full-scale settling time measurement is made in the following manner: The comparator threshold reference level is adjusted to bias the comparator output corresponding to DAC full-scale digital input into its linear operating region with the LSB set to "dynamic." This line is then switched to logic "0", reducing the full-scale DAC output level by 1 bit. This, in turn, causes the comparator output corresponding to full-scale DAC output to shift by the equivalent of 1 LSB. In the case of high-resolution DAC's having small LSB analog equivalent values, the comparator output will still remain in its linear region. This procedure establishes a calibrated 1-LSB band on the oscilloscope tube face, independent of comparator gain. Settling time is then measured from the time the digital input code changes until the time the comparator output enters a 1-bit band centered about full-scale for the final time. Typical waveforms associated with settling-time measurements made in this manner are shown in Figure 17b.

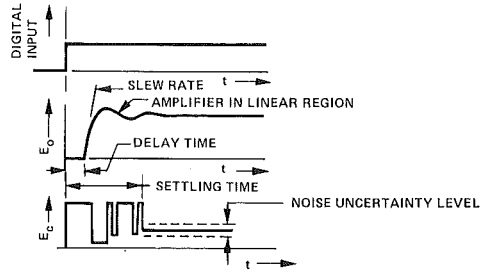
In the case of current-output DAC's, settling time can be measured by terminating the output in the inverting node of a high-speed operational amplifier, such as the ADI Model 46, connected in the inverting configuration, and making the measurement in the manner described above. Alternatively, the current output can be terminated in a resistor to convert to voltage directly. Since most current-output DAC's are output-voltage limited to approximately ±2V, the 1 LSB analog voltage equivalent is less than 1mV for

DAC's having resolution beyond 11 bits, using this technique. This reduced voltage range heightens the problem of making accurate settling-time measurements, since any noise voltage present becomes a more significant fraction of full-scale.

In general, to make accurate settling-time measurements for a current-output DAC terminated directly in a resistor, it is necessary to keep all lead lengths to an absolute minimum to reduce spurious noise pickup and ringing due to excessive lead inductance. The general tendency of high-gain comparators to oscillate can sometimes be reduced by connecting the output of the DUT to the negative, rather than the positive, comparator input, to reduce inter-wiring capacitive coupling from the comparator output to its positive input, as shown in the configuration of Figure 17.



(a. Measuring Circuits)



(b. Waveforms)

Figure 17. DAC Zero and Full-Scale Settling Time Measurement

Comparator Thermal Effects

High-speed comparators of the type used in the test setup of Figure 17a generally have input stages biased at a relatively large current level to maximize comparator gain-bandwidth. As a result, these comparators generally exhibit a thermal time constant of the order of several milliseconds, due to differential self-heating of the input transistor pair as the comparator output changes state. This can add a "tail" of several parts in 10,000 to the final settling time of the comparator output, attributable to the comparator, rather than the DUT. The most effective way of establishing with certainty that observed thermal settling times are due to the measurement system, rather than the DUT, is to make the settling time measurement using the technique described above twice: first with a high-speed comparator, using a square-wave frequency consistent with the anticipated settling time, then with an ultra-low-drift comparator which has been designed to minimize thermal effects (at the expense of gain-bandwidth), and a square-wave frequency below 100Hz.

Alternate Method for Zero and Full-Scale Measurement

A simpler scheme for settling-time measurement than that shown in Fig. 17a, which does not require a differential comparator is shown in Figure 18. A square-wave, synchronized to the dynamic digital input square-wave drive, but out of phase with the output of the DUT, is summed with this output. The amplitude of this reference square-wave, E_R, is adjusted to exactly equal that of the DAC output E_0 when switching transients have subsided. This produces a zero-volt steady-state error signal or "virtual ground," by analogy to the error voltage existing at the inverting node of an operational amplifier configured in the inverting mode.

Clamp diodes at the "virtual ground" point limit the voltage excursion during the switching transient period, and the subsequent oscilloscope overdrive; this reduces the oscilloscope overload recovery time. A calibrated 1-bit threshold level at either zero or full-scale DAC output can be established by switching the LSB

digital input from "dynamic" to logic "1", or logic "0", respectively, as in the scheme of Figure 17a. A 1-bit band centered about the steady-state display level corresponding to full-scale, or zero, DAC output, can then be readily established on the oscilloscope tube face, and settling time to ±½ bit of final value is measured as the time for the error voltage existing at the "virtual" ground point to enter this band for the final time.

If only settling time from full-scale to zero volts is to be measured, the offset square-wave reference, E_R, and its summing resistor R can be eliminated, simplifying the measurement process, using the scheme of Figure 18.

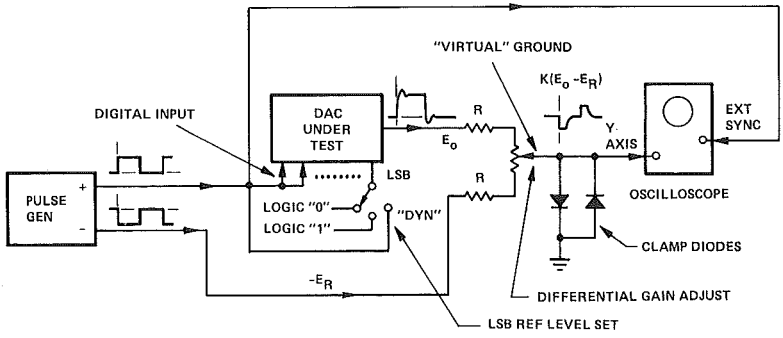


Figure 18. DAC Zero and Full-Scale Settling Time Measurement — Virtual Ground Method

Major Carry

When a DAC is operated in a tracking mode, as shown in Figure 6a, for example, the bit-to-bit, rather than full-scale settling time is of importance. The one-bit digital code transition causing the greatest switching transient, and consequently, the longest settling time at the DAC output, generally occurs at the major (½-scale) carry transition of the digital code. At this particular code transition, the digital number changes from 0111. .1 to 1000. .0 (or vice-versa when counting in the opposite direction), causing all bits to change state, and generally introducing the worst-case 1-LSB switching transient into the DAC output.

Figure 19 illustrates a test configuration for measuring settling time at the major-carry code transition. All bits, except the MSB, are driven in parallel by a square-wave alternating between logic "0" and logic "1" levels. This square-wave is inverted and applied to bit 1, causing this bit to be driven out-of-phase with all the other bits. The steady-state output for this input drive is a square-wave having a 1-LSB peak-to-peak amplitude at half-scale DAC output, corresponding to the major-carry input code transition being traversed from either direction. The DAC output is ac-coupled into an oscilloscope having its sweep *start* synchronized to the input square-wave. Settling time to ±½ bit of final value, in this case, is merely the time required for the 1-bit output step-change to reach 50% of its final value. (If the amplitude of the square-wave output is used to establish a 1-bit calibration reference band to expedite the measurement of tracking settling time, the differential nonlinearity occurring at the major carry should first be checked, since this generally represents the code transition causing greatest differential nonlinearity, as well as the greatest switching transient at the DAC output (as discussed under *Differential Linearity*).

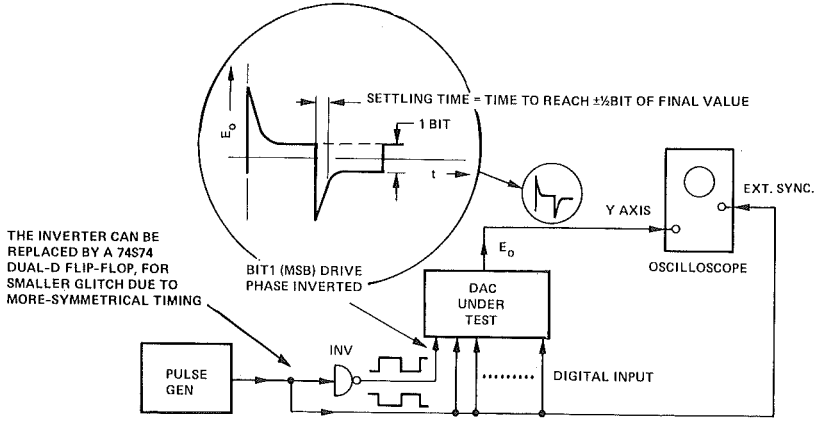


Figure 19. DAC Major-Carry Settling Time Measurement

Accurate measurement of DAC major carry transient "glitch" duration or amplitude using the scheme of Figure 19 is significantly easier than that of full-scale settling-time measurement, since the DAC analog output steady-state signal excursion in this

instance is only 1 bit. As a result, amplifier or comparator overload recovery and thermal response time problems associated with large signal swings at the input to the measurement system are virtually eliminated.

ADC TESTING

Because of the fundamental ½-bit quantization uncertainty associated with analog-to-digital conversion, ADC testing is more difficult than DAC testing, owing to the need for determining both the output code and the transition point, referred to the input, rather than simply measuring an output response to a predetermined code. The effects of noise (occurring in either the signal or the converter, or picked up in the wiring) are to introduce an uncertainty in the precise determination of the analog input values at which the output code transitions take place, and to, in effect, increase the quantization band. The nature of these quantization and noise uncertainty errors is shown in Figure 20. (It should be noted, in passing, that the fundamental ±½-bit worst-case quantization uncertainty sets the requirement that the device accuracy can be no better than its resolution in the case of ADC's. This is in contrast to DAC's, which can have accuracy specifications exceeding their resolution capability. This distinction (or duality) comes about because of the inverse nature of the devices: the DAC output can, with arbitrary precision,

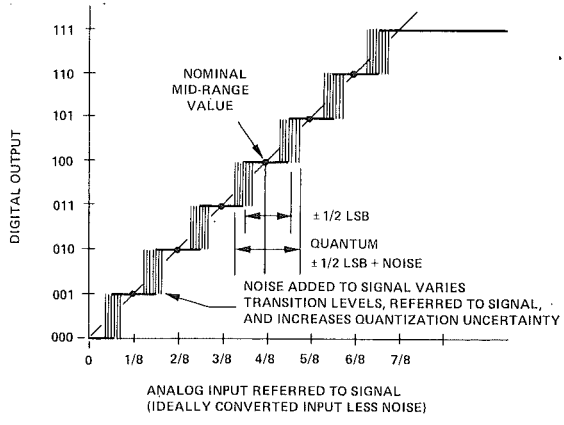


Figure 20. Quantization and Noise Uncertainty Error

locate a level which is a measure of one precise number representing either itself or the quantum determined by the digital number, while the ADC's output level is determined by any input value within the quantized range of input.)

A simplified diagram of an ADC test setup was seen in Figure 1a. The ADC calibration is established by observing correspondence between the state of the input digital toggle-switch register driving the reference DAC and the output digital display representing the state of the ADC. This simplified setup suffers from the disadvantage that the precise location of each analog calibration level within the 1-bit quantization band encompassing each of these respective values cannot be determined. As a result, calibration accuracy, linearity, and differential linearity cannot be determined to a precision greater than 1 LSB using this basic scheme.

One is generally concerned with establishing the calibration of the ADC so that the nominal analog calibration voltage is centered in the quantization band determined by the adjacent transition values. In addition, one normally is interested in checking linearity and differential linearity to a degree better than the ±½-bit quantization uncertainty imposed on accuracy.

DYNAMIC CROSSPLOT

By summing a small ac signal with the analog reference voltage applied to the input of the ADC under test, the ADC output can be dithered about each of its digital output codes of interest with a large number of analog inputs in a short time. This permits the analog values corresponding to the transitions and the center of each code quantization level to be readily determined, using a dynamic crossplot test. This in turn permits determination of device nonlinearity and differential nonlinearity to a precision greater than ±½-LSB.

The dynamic crossplot test configuration is shown in Figure 21. The digital code of interest, N_{REF}, is entered into the reference DAC via the toggle-switch register, thereby applying E_{REF}, the analog equivalent of N_{REF}, to the analog input of the DUT. Low-frequency ac dither E_{ac} and adjustable dc offset E_{os} voltages

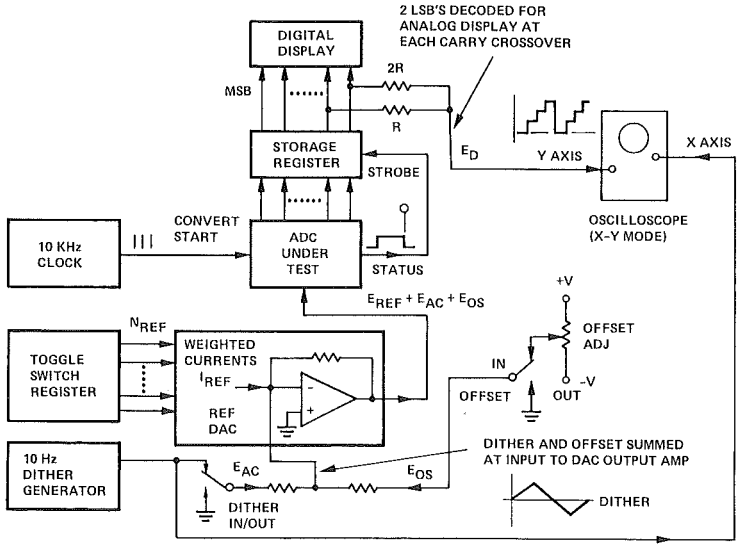


Figure 21. ADC Dynamic Cross-Plot Test

are summed with the reference DAC's output. The dither signal has a frequency that is low with respect to the conversion rate, so that the digitized output of the DUT will exactly track its analog input, within the ±½-LSB quantization limits. A digital register stores the results of each conversion. A 2-bit DAC is formed using resistors having weights of 2R and R to sum the LSB and the adjacent bit, respectively, of the stored ADC output. The decoded 4-step analog output, corresponding to the two stored-ADC least-significant-bit states, is applied to the Y axis of the oscilloscope. The ac dither signal is applied to the X axis of the oscilloscope, which is operated in the X-Y crossplot mode. A number of dynamic-crossplot waveforms, obtained using the test configuration of Figure 21, are shown in Figures 22b-22e.

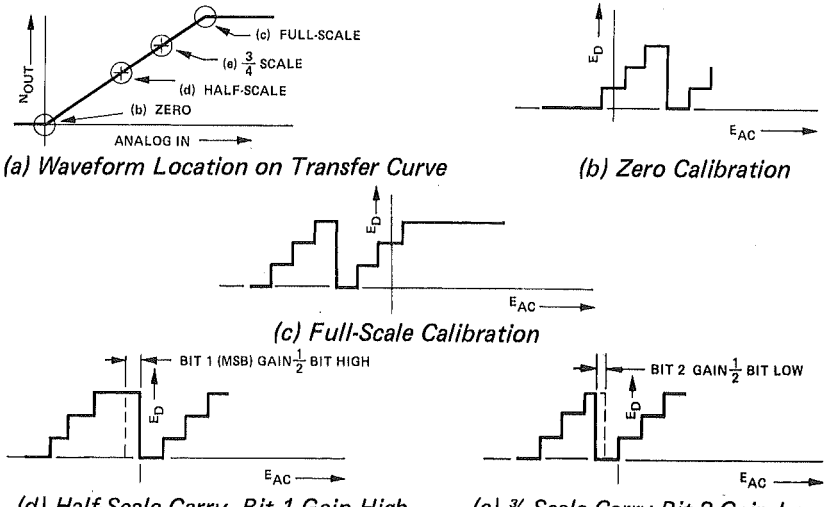
The DUT is calibrated using the dynamic-crossplot display in the following way: The CRT beam is positioned in the center of the tube face, with the X-axis drive signal initially removed, to establish the Y-axis position. All bits, except the LSB of the reference DAC, are turned off; the LSB is turned on. The DUT's zero is adjusted to center the first step of the decoded output staircase waveform, corresponding to the digital code 000. . .01 on the Y-axis of the display, as shown in Figure 22b. Next, all bits,

except the LSB of the reference DAC are turned on, corresponding to the digital code 111...10, and the gain of the ADC is adjusted to center the next-highest step of the decoded staircase waveform on the Y axis, as shown in Figure 22c. These steps calibrate zero and full-scale.

Using the dynamic crossplot display, differential nonlinearity and noise at each bit code transition can be investigated. Figure 22d illustrates the waveform that appears at the major (half-scale)-carry code transition (0 1 1 1 . . . 1 to 1 0 0 0 . . . 0) of the digital output code of the DUT when its bit-1 gain is ½ LSB too large with respect to the gains of the other bits. This causes the staircase step width corresponding to the code 0 1 1 1 . . . 1 to be ½-LSB too wide.

Figure 22e shows the waveform at the 3/4-scale-carry code transition, 1 0 1 1 . . . 1 to 1 1 0 0 . . . 0, when the bit-2 gain of the DUT is ½-LSB too small with respect to the other bit gains. This causes the staircase step width corresponding to the code 1 0 1 1 1 . . . 1 to be ½-bit too narrow. ADC differential nonlinearity is measured as the deviation in staircase step width from the average step width. The waveforms in both Figures 22d and 22e, show ½-LSB differential nonlinearity.

Differential nonlinearity, non-monotonicity (missing codes), and



(a) Waveform Location on Transfer Curve

(b) Zero Calibration

(c) Full-Scale Calibration

(d) Half-Scale Carry, Bit-1 Gain High

(e) ¾ Scale Carry-Bit 2 Gain Low

Figure 22. ADC Dynamic Cross-Plot Waveforms

noise can be investigated at each bit code-carry transition by turning on and off each bit of the reference DAC in succession and observing the dynamic crossplot waveform in each case. Summation errors are investigated by turning on all bits, one at a time, in descending order of significance, and leaving them on. The dynamic crossplot waveform is observed as each new bit is turned on. This tests the performance of the DUT in the range from half scale to full scale.

The effects of noise and nonlinearity can also be assessed using the dynamic crossplot test. Noise is seen as a jitter in the location of each staircase-waveform step transition. Device nonlinearity will gradually displace the staircase waveform either to the left or right, as successive bits are turned on and full-scale is approached.

Several points should be noted with respect to the dynamic crossplot test configuration of Figure 21:

1) Since, for simplicity, only the two least-significant bits of the DUT's digital output are decoded, the dynamic crossplot waveform repeats every four steps. Initial DUT calibration must therefore be made statically to an error less than 2 bits before the dynamic crossplot is used, so that one can be assured that the desired code transition is being examined, and not one that is 4 LSB's away, which does not have associated with it the desired carry transitions.

2) A triangular dither waveform is shown in Figure 21. This waveform could just as well be a sine-wave, since a linear time relationship is not required in the X-Y display mode for a linear X vs Y presentation.

3) The external storage register shown in Figure 21 can be eliminated (at the expense of minor crossplot display degradation) if the conversion rate is reduced so that the time between conversions is large, compared to the conversion period, since conversion switching transients will be observed in the crossplot display in this case. Typical dither and conversion clock frequency ranges that have been found useful for dynamic crossplot analysis of high-speed successive-approximation ADC performance using the configuration of Figure 21 are 4-40Hz, and 10kHz to 100kHz, respectively.

ANOMALOUS ERRORS

The dynamic crossplot test just described is very useful in quickly detecting certain ADC performance anomalies, such as might be caused by oscillating comparators and hysteresis, for example. An oscillating comparator causes an excessive randomness in the code transition points on the displayed crossplot – more than could be attributable to random noise.

Some converters exhibit a hysteresis effect, which causes the location of the code transition points to be dependent on the direction from which the point is approached. This causes two horizontally-separated dynamic-crossplot waveforms to appear, much like a series of hysteresis loops. In addition, some converter families have been found to exhibit excessive noise at certain code transitions. The dynamic crossplot test is especially effective in facilitating discovery of such anomalies, because they are displayed quite prominently.

Single-Shot Conversion Errors

Some converters, which appear correctly calibrated when triggered at a high repetition rate, exhibit conversion errors when triggered intermittently at a low rate. Errors of this type can generally be traced to a thermally-induced offset voltage at the comparator input when this device has remained in one state for more than a few hundredths of a second. These effects are more common in older designs, which incorporate discrete-transistor comparators. Use of monolithic comparators in most contemporary converter designs has largely eliminated this problem. One-shot conversion errors are not readily detected using the dynamic-crossplot test configuration of Figure 21, since repeated conversions at a high rate are necessary to obtain a useful display, owing to the restriction on low dither rates imposed by the oscilloscope's short display persistence. Single-shot errors can be detected by removing the dither and observing the binary display as the conversion rate is reduced, while holding the analog input constant. Errors of this type will generally show up (if present) when the conversion rate is lowered to 1Hz or less.

SEMI-AUTOMATIC TESTING

A more elaborate ADC test configuration than that of Figure 21, which lends itself to semi-automatic ADC testing, is shown in Figure 23. A 3-position toggle switch permits selection of logic "0", logic "1", or "dynamic" for each reference-DAC bit input. The output E_R of the reference DAC is applied to the input of the DUT. The digital output word N_O of the DUT is transferred to a storage register at the completion of each conversion. The digital word N_R at the input of the reference DAC is subtracted from N_O, and the digital error $N_O - N_R$ is applied to a low-resolution DAC, permitting analog presentation of the error. Alternatively, this error $N_O - N_R$ can be applied to a limit comparator having preset high and low error limits, permitting go-no testing.

Dynamic testing using the configuration of Figure 22 can be done in two principal modes: *bit-scan,* and *count,* by analogy to the DAC test configuration, shown in Figures 9 and 11. The resolution of the reference DAC used in the configuration of Figure 23 should be at least two bits better than that of the ADC being tested, so that quantization of the analog input to the DUT will not limit the error readout resolution to less than that imposed by the ±½-bit quantization band attributable to the DUT.

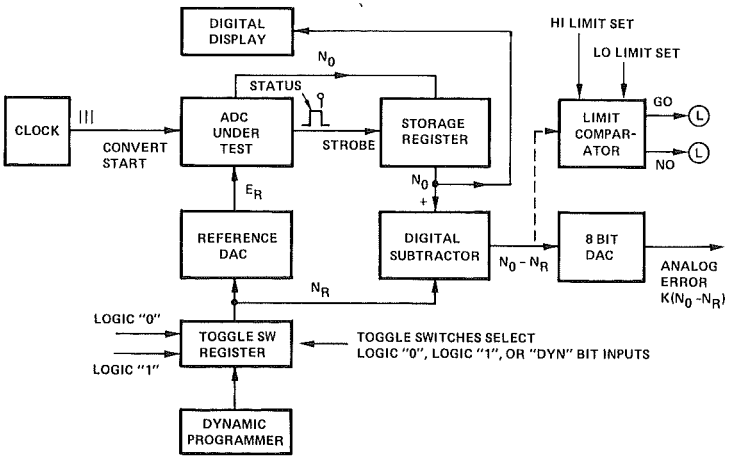


Figure 23. ADC Test Configuration