

SECTION V

APPLICATIONS FOR AMPLIFIERS IN AUDIO

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SECTION V

APPLICATIONS FOR AMPLIFIERS IN AUDIO

WALT JUNG

INTRODUCTION

Today, IC amplifiers are available which perform many of the tasks required within audio systems. Many of these functions can be performed by standard op amps, although not always with optimum performance.

Audio circuit performance requirements can often be demanding in terms of very low noise, very high current and/or voltage outputs, and low signal distortion. While standard amplifiers exist which excel in all of these areas, some functions may need higher levels of system integration to make them performance and cost effective to the audio designer. Some cases in point are described in the sections following, under audio line drivers and receivers.

Another factor strongly influencing audio circuit design is the concept of the *universal* single/dual audio op amp readily available at low cost. Quite often however the only critical specification qualifying such devices is simply and solely their low cost. Frequently other IC devices might be available which can meet or exceed

performance in one or more key areas, but don't get due consideration because of entrenched standards.

Audio, like many other electronic design areas, needs full and thoughtful regard of many issues for the most effective device selection. Distortion under load must be low, common mode rejection must be high, power consumption must be reasonable, and a minimum of related components should be required.

Fortunately, a wide variety of very high performance IC amplifiers are available to meet these audio demands. Some of them are designed specifically for audio application requirements, such as balanced input/output interfacing, very low voltage noise, high output currents, etc. Others achieve one or more of these objectives through the use of standard IC devices, in topologies most useful to audio requirements. The circuits following illustrate examples of both of these design approaches in high performance audio applications, with characterization data accompanying them to aid assessment.

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A LOW NOISE MICROPHONE PREAMPLIFIER WITH DC SERVO OUTPUT

The SSM-2017 audio preamplifier chip is a versatile differential input IC with an input voltage noise of less than $1\text{nV}/\sqrt{\text{Hz}}$, and low distortion. The gain of the device is set via one external resistor, R_g , and it is adjustable over a range of 1-1000 times. Differential inputs of the SSM-2017 allow balanced input signal operation, and the single-ended output signal of the device appears between the output and reference terminals. It operates from dual power

supplies of $\pm 22\text{V}$ or less, and drives loads of $2\text{k}\Omega$ or more.

Figure 5.2 is an application which employs the best advantages of the SSM-2017, combined with the OP-275 dual bipolar/JFET op amp. Although this circuit is labeled a microphone preamp (an application for which it is well suited) the gain range over which it operates and relative ease of output interfacing make it general purpose as well.

AUDIO SPECIFICATIONS AND CONSIDERATIONS

- Total Harmonic Distortion (THD)
- Noise
- Output Level and Drive Capability
- Power Dissipation
- Cost
- Single IC or Multiple Components

Figure 5.1

LOW-NOISE MICROPHONE PREAMP WITH DC SERVO LOOP

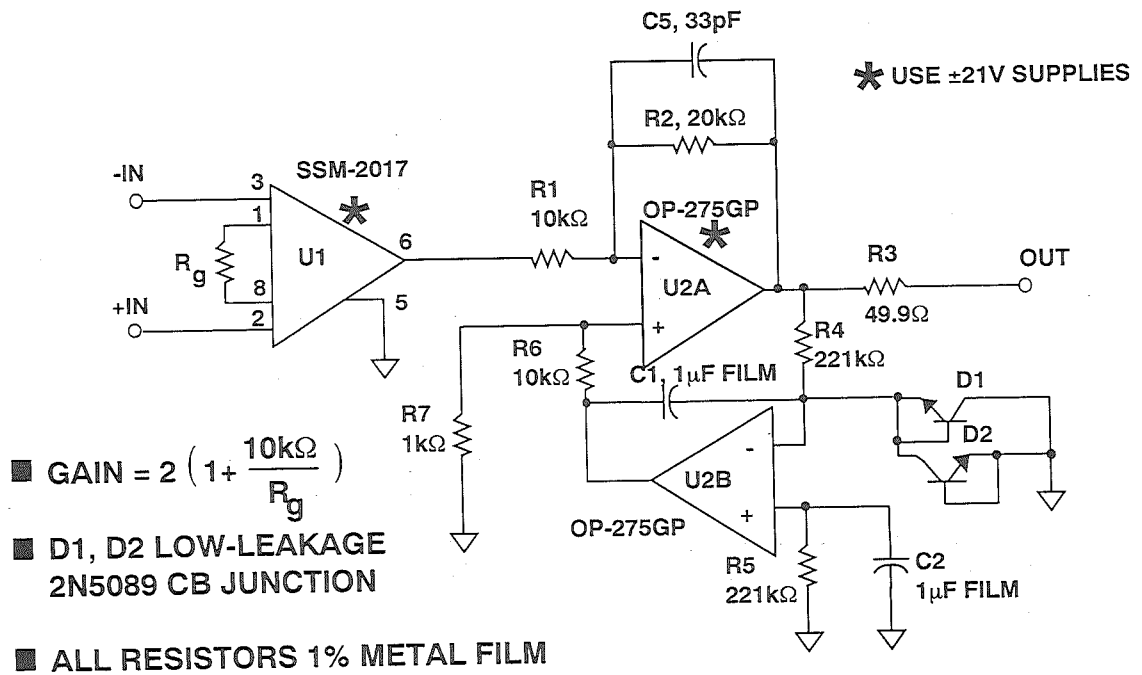


Figure 5.2

As noted, the SSM-2017's strengths lie in low noise and distortion, and gain flexibility/simplicity. It is, however, rated only for 2kΩ or higher loads, making drive for 600Ω loads relatively limited with the basic device. However, the circuit here uses a combination technique, where virtues of two different IC amplifiers merge into a single overall structure which is useful to these points.

Here, the SSM-2017 is used to high advantage in the programmable gain input stage, and it is combined with a

fixed gain, high current output buffer with DC servo stage, using the OP-275. This allows the best performance features of both ICs to be realized, each optimized for their respective input/output functions. The OP-275 output buffer provides the low distortion high level drive into 600Ω loads, with the second half of the IC used as a servo to control output offset. The OP-275 gain stage U2A also is operated at a modest gain of 2 times, keeping the required output swing of the SSM-2017 to a minimum and distortion low.

DESIGN CONSIDERATIONS

The circuit uses stage U1 as a gain programmable SSM-2017 preamp block, where the gain of this stage is set by R_g . This gain, G_1 , is essentially as described on the SSM-2017 data sheet, or:

$$G_1 = \frac{10k\Omega}{R_g} + 1$$

The second stage of the circuit is a inverting buffer using the OP-275 op amp U2A, where the stage gain (G_2) will be:

$$G_2 = -R_2/R_1$$

In this design the values for R_1 - R_2 are fixed at 10kΩ/20kΩ, so the gain G_2 is -2. The overall gain G is the product of G_1 and G_2 , or:

$$G = 2 \left(\frac{10k\Omega}{R_g} + 1 \right)$$

In practice, R_g is selected as a gain control for the entire circuit, using a minimum gain of 2, as:

$$R_g = \frac{20k\Omega}{G - 2}$$

Note that these gain figures will be altered somewhat by loading due to R_3 .

Also, because of the signal inversion in stage U2, the respective input signs of U1 are reversed regarding overall operation. Various input interface schemes to U1 can be used for connections to both microphones or other sources.

The DC servo stage U2B senses the output DC from U2A and compares this level against the common reference point. U2B is an inverting integrator with an overall low frequency rolloff of about 0.12 Hz. With this servo loop operating, the net output DC offset will be essentially the sum of the voltage offset of U2B, and the offset current errors, and will be independent of the output DC offset of U1. With 1% values used for R_4 and R_5 , the circuit's overall DC offset should typically be about 2mV. For lowest integration errors, film capacitors should be used for C_1 and C_2 , such as polycarbonate or polyester types. Diodes D_1 and D_2 provide protective clamping for U2B.

MICROPHONE PREAMP PERFORMANCE

This amplifier's performance is quite good over programmed gain ranges of 2-2000. For a typical audio load of 600Ω, THD+N at various gains and an output level of 10Vrms is shown in Figure 5.3. For all but the very highest gain the THD+N is consistent and well below 0.01%, while the gain of 2000 becomes more limited by noise.

In terms of other operating hints, maximum output will be a function of the power supplies, and can be as high as 10Vrms, with higher voltage supplies. Note that output resistor R₃ will limit the swing available when driving 600Ω, but should be retained for short circuit protec-

tion. Thus supplies on the order of ±20V are appropriate for the highest output into 600Ω. Aside from this maximum swing consideration, the circuit can be operated on lower supply voltages, with proportionally less output.

To get the most from this circuit 1% metal film resistors are recommended, and a neat, compact layout should be used. Regulated power supplies should be used, and they should also be well bypassed with large electrolytics returned to the output common point.

LOW NOISE MICROPHONE PREAMP THD + N PERFORMANCE, V_{out} = 10V rms, R_{load} = 600Ω

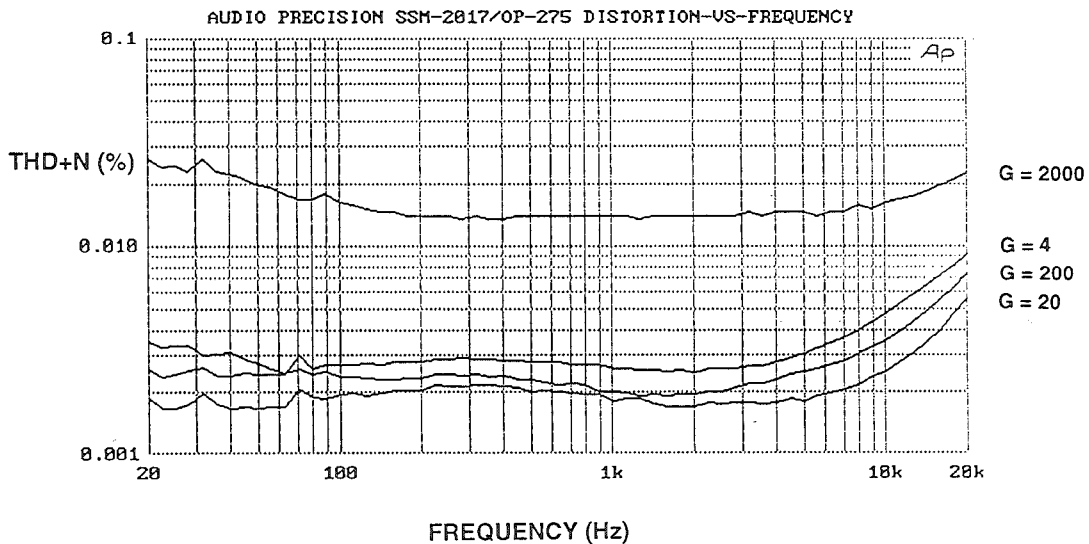


Figure 5.3

LINE DRIVERS AND RECEIVERS FOR HIGH PERFORMANCE AUDIO

The functions of sending and receiving audio signals between the various components of audio systems has traditionally involved tradeoffs between expense and performance. Everyone can easily understand that fully differential or balanced transmission systems are best at rejecting noise, both low frequency and RF. Given

that, what is more difficult is the management of large system designs using differential drivers/receivers. Keeping the final design within reasonable boundaries of cost, size and weight while reaping the technical benefits has not always been a straightforward task.

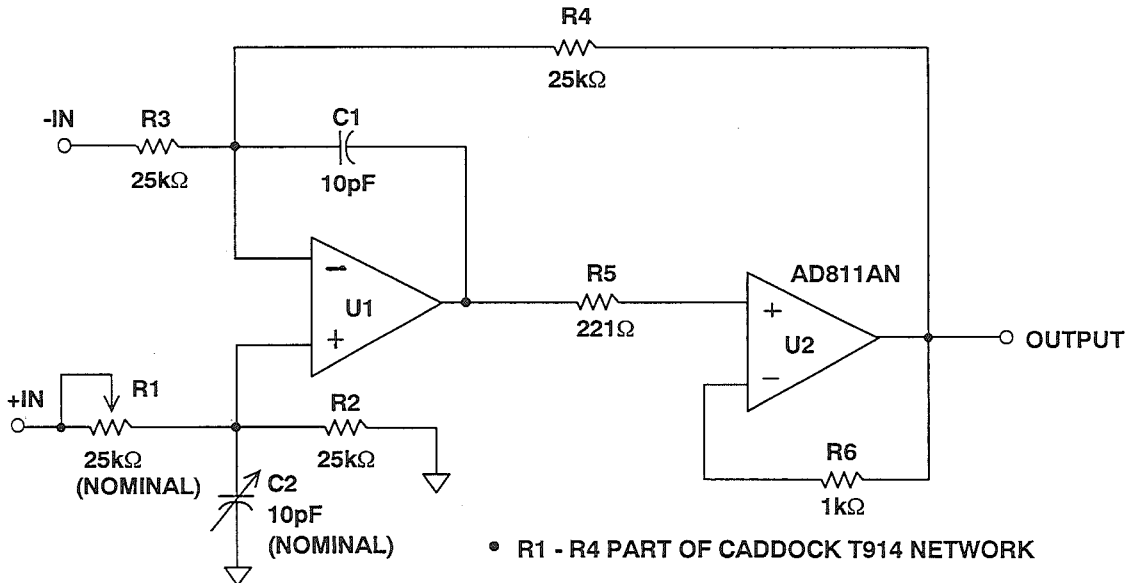
LINE RECEIVERS

A brief operational review of a standard differential line receiver function will help understand why designs for these devices have evolved into what they are today. Figure 5.4 is a diagram of a classic differential amplifier, using a four resistor bridge and a single (buffered) op amp for the gain stage. (In system terms, this general circuit is also known as an *instrumentation amplifier*, IA for short, and is discussed elsewhere in these notes.

Within this audio discussion, we will call it simply a line receiver for brevity — to be understood as short for *differential* line receiver). This line receiver is *critically* dependent upon the resistors for good performance, a point which should be clear shortly. The amplifier can also be critical; if not chosen carefully for such parameters as CMRR it also can limit performance, as it can for other reasons.

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BASIC AUDIO LINE RECEIVER



- R1 - R4 PART OF CADDOCK T914 NETWORK
- SUGGESTIONS FOR U1, U2:
 - (a) U1 = OP-275, U2 OPTIONAL
 - (b) U1 = OP-275, U2 = AD811
 - (c) U1 = AD744, U2 = AD811

Figure 5.4

As a matter of fact, this circuit appears (on the surface at least) to be somewhat trivial... all one needs to implement it are four good resistors and a decent op amp. Dependent upon your definition of "good", this can indeed get you going, at least in a functional sense. But how well the circuit will work in terms of common mode rejection (CMR) is another story altogether.

The main purpose of this circuit is to reject noise common to both inputs, as might be picked up on a twisted pair cable for example. However, even with a high quality op amp for U1, the noise rejection properties of the circuit can only be as good as the matching of the four resistors. To be more precise, the resistors *ratios* R_2/R_1 and R_4/R_3 must match extremely

well to reject noise (their absolute values are secondary in importance to their ratio matching).

It is tempting to just pick four 1% resistors from a batch, a step which can yield ratio matching of say 0.1% (at least for a while). However, even with care this will just achieve a CMR of better than 60dB, and if you used the four 1% resistors where only *one* was off by 1%, you'd get about a 46dB CMR.

Clearly then, this circuit is one which needs four resistors made and trimmed simultaneously on a single substrate, to be most effective. Only in this way can the very tight ratio requirements be achieved initially and held stable over time and temperature.

SIMULATION RESULTS

A couple of simulations show just how critical the circuit is with regard to the resistors, and is reflected in Figure 5.5.

In this figure, a display of CMR in dB of this circuit is shown, with three of the four resistors fixed at 25kΩ, and one, R1,

BASIC LINE RECEIVER COMMON MODE REJECTION VERSUS FREQUENCY FOR VARIOUS DC TRIMS (SIMULATION)

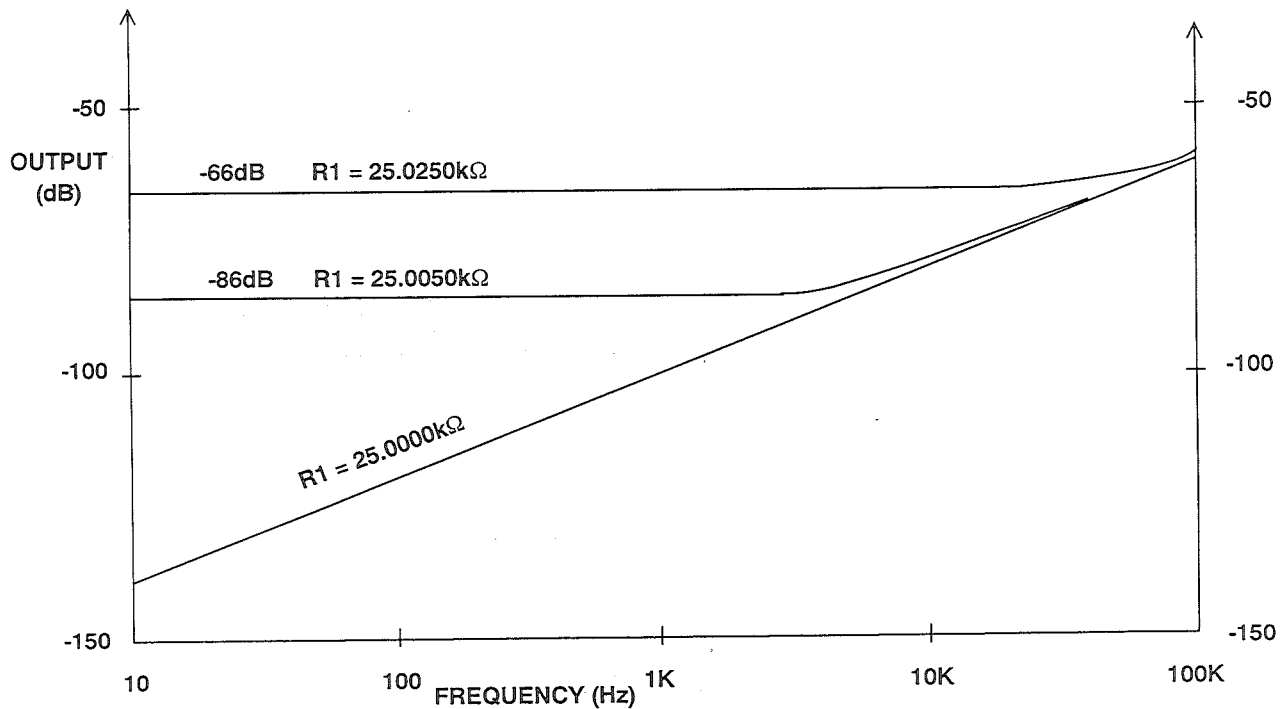


Figure 5.5

is stepped. In the simulation, R_1 ranges from 25.025k Ω (plus 25 Ω or 0.1%) down to exactly 25k Ω (a perfect match), with steps of 0.0025k Ω (2.5 Ω or 0.01%). For clarity, only the range extremes are shown in the figure. The 0.1% mismatch curve is at the top of the display, where the CMR is 66dB. The CMR increases to 86dB for the step where R_1 is 25.0025k Ω (plus 0.01%). For the last step, where the four resistors are balanced perfectly, the CMR is frequency dependent, limited by the mismatch of capacitors C_1 - C_2 (10 and 10.1pF).

Some important points come from this experiment. To realize a CMR of greater than 80dB, the resistors need to be matched to 0.01%. In more general terms, one can extrapolate up/down this scale as well, that is more than 100dB CMR requires matching to 0.001%. Obviously, high CMR performance with this type of circuit demands extreme perfor-

mance of the resistor network, more so when potentially degrading effects of time and temperature are factored in. Stable networks of this type using thin film technology are commercially available from companies such as Caddock and Vishay, but they are not inexpensive in the tight ratio matches required.

The above discussions deal with DC matching, but in fact the ratio needs to be maintained for AC as well as DC, to achieve flat noise rejection over frequency. For this to be effective, the nodal capacitances from the R_2/R_1 and R_4/R_3 junctions need to be balanced. In an actual circuit this can be achieved with very low and balanced parasitic capacitances at these points. In an AC simulation, the capacitors C_1 and C_2 were used to illustrate this point, with C_2 varied in 1pF steps from 5pF to 10pF. The results are shown in Figure 5.6.

BASIC LINE RECEIVER COMMON MODE REJECTION VERSUS FREQUENCY FOR VARIOUS AC TRIMS (SIMULATION)

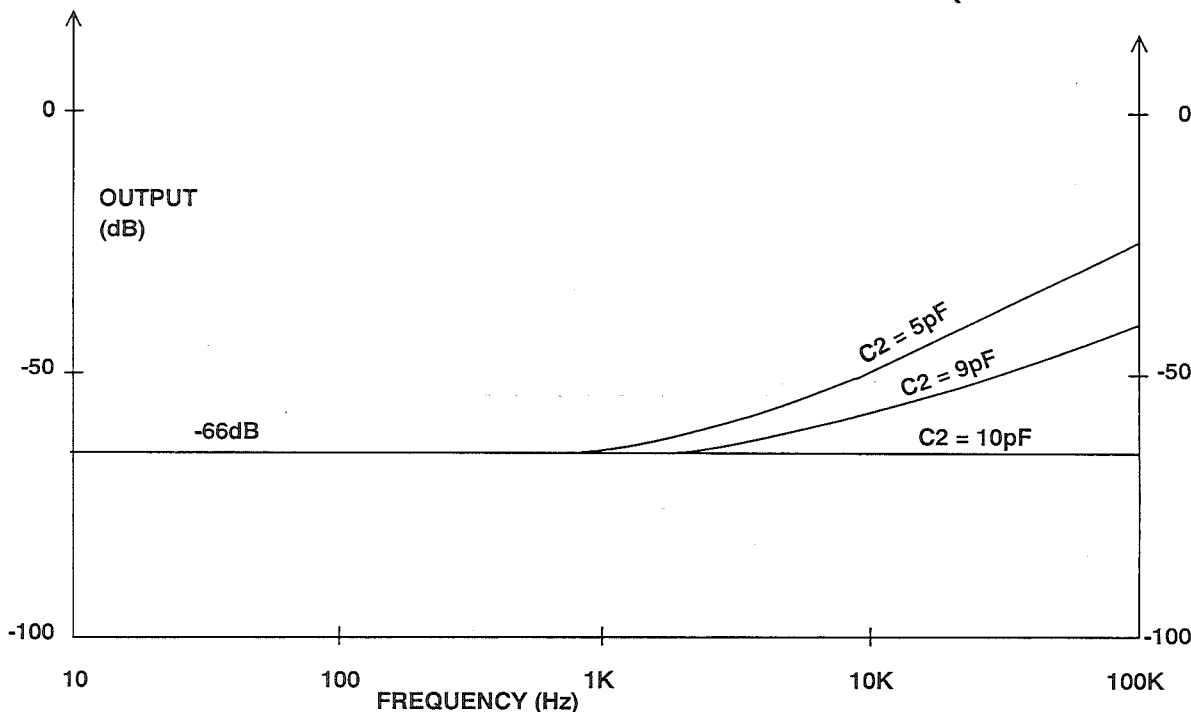


Figure 5.6

In this test R_1 is fixed at the 0.1% mismatch point, making the DC CMR 66dB (as before). C_2 is 5pF at the top curve, and steps up in value to 10pF for the bottom curve (best AC balance). As

MEASURED PERFORMANCE

The circuit of Figure 5.4 is not just hypothetical, it was built with the components as noted, and lab results show good agreement with the simulations. With the circuit as shown, the user has an option of operating U1 either buffered or unbuffered, by the optional use of the U2 follower. If an AD811 is used here as noted, the circuit has an output capability of more than 100mA, making it useful with lower output drive ICs for U1 such as the AD744. Or, if a huskier output device such as the OP-275 is used for U1, the need for a buffer is more moot, since the OP-275 by itself is rated to drive 600Ω loads. For loads appreciably lower than 600Ω, use of the U2 buffer will preserve

can be seen, this capacitive unbalance starts to degrade the CMR at progressively lower frequencies for larger capacity imbalances.

the low distortion typical of this circuit. (Note that if an AD811AN is used for U2 above ±12V, a heat sink such as Aavid 5801 is suggested).

CMR performance of the circuit is shown in Figure 5.7, for conditions of trimmed and untrimmed for AC, and a 5Vrms CM input, with ±15V supplies.

The upper curve represents CMR performance of either the OP-275 or the AD744 (both buffered) with a 0.1% ratio match type T914 25kΩ network, and no capacitive trimming. The stray capacity mismatches of the breadboard limit the high frequency CMR to much less than the DC level, with CMR deteriorating above 1kHz. With trimmed 10pF

EFFECTS OF AC TRIM ON CMRR PERFORMANCE OF BASIC LINE RECEIVER (MEASURED)

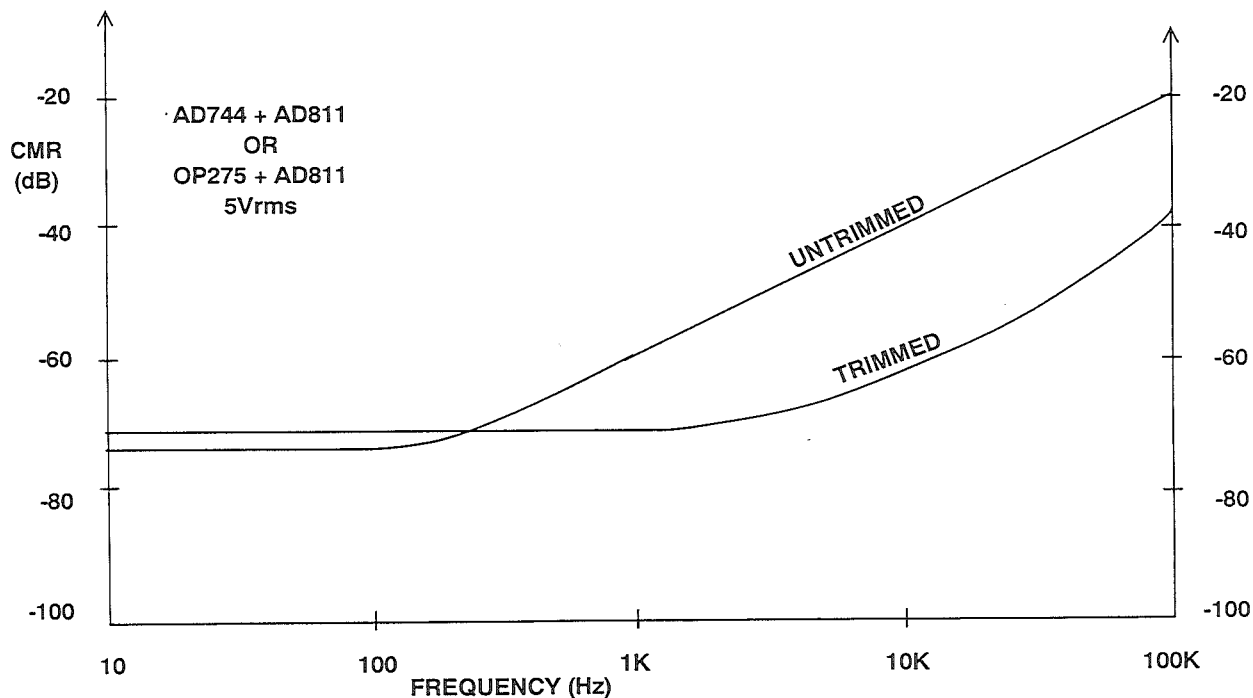


Figure 5.7

BASIC LINE RECEIVER THD+N PERFORMANCE USING VARIOUS OP AMPS

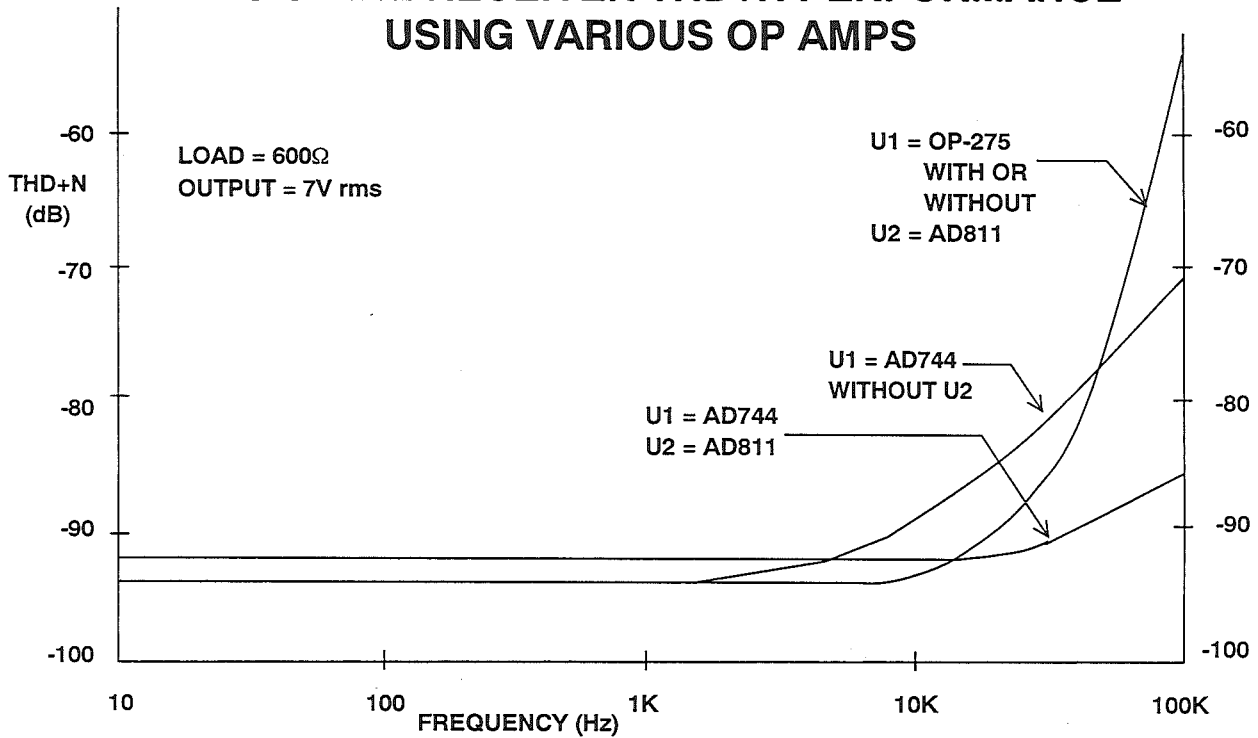


Figure 5.8

capacitors added, CMR is preserved to above 10kHz. These CMR data show that both DC and AC balance are necessary for best performance.

In terms of distortion, THD+N data at a 7Vrms level with a load of 600Ω is shown in Figure 5.8, with the two op amps operated both buffered and unbuffered.

INTEGRATED LINE RECEIVERS

An optimum way to build the line receiver circuit under discussion is via *monolithic* technology. With this method, using a high performance op amp plus a trimmed thin film resistor network with low parasitics, all pertinent aspects which impact line receiver performance are under direct control during manufacture. As has been observed, getting the highest performance from an op amp plus resistor network approach such as Figure 5.4 demands either precise control of a single

The OP-275 shows little consequence operating without a buffer, while the AD744 THD+N at high frequencies shows a rise from -86dB to -73dB at 100kHz. The distortion performance of both devices in this circuit is excellent.

network, or circuit-by-circuit trim of one of the four resistors for the optimum ratio. In addition to this low frequency CM trim, there must also be an AC trim. These factors make the duplication of a high performance version of this circuit expensive, time consuming, and demanding of both instrumentation and operator skills.

In contrast, the precise trim of thin film networks is one of the strengths of the AD manufacturing processes. Low parasitic capacitance can be designed into

this architecture, and, importantly, it is highly reproducible. To these two major design assets can be added a high quality op amp to complete the design.

The SSM-2141 and SSM-2143 are monolithic IC line receivers which work very much like the circuit of Figure 5.4, differing only in their individual gains. They are shown in functional diagram form in Figure 5.9, along with a table describing their gains.

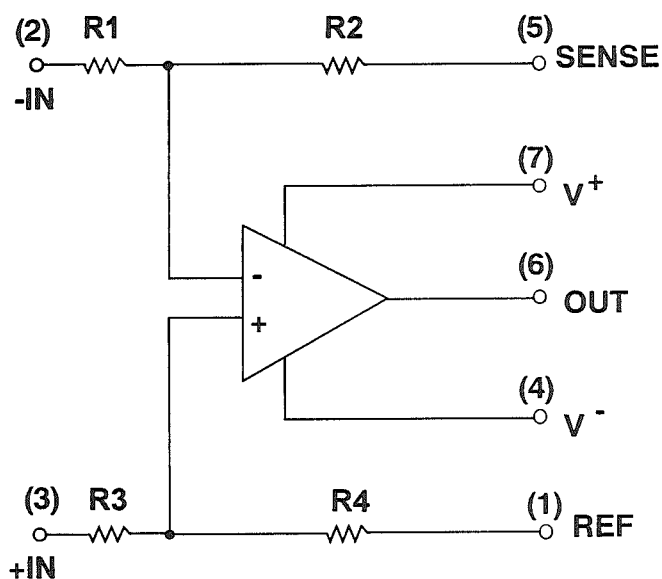
The 8 pin Mini-DIP footprint of both devices is the same as shown, the major difference between the two is in the gain determination resistors R_1 - R_2 and R_3 - R_4 . The SSM-2141 operates as a unity gain device, while the SSM-2143 operates either at a nominal gain of 0.5 (-6dB), or it can optionally be strapped with the input/output of the resistor pairs reversed, to operate at a gain of 2 (6dB).

Both devices operate from supplies up to $\pm 18V$, can drive 600Ω loads, and they have low distortion and excellent CMR

characteristics. For reference, the op amp used in these receivers is similar to one half of an OP-271. The output appears at pin 6 and is uncommitted, with conventional use it gets tied to R_2 (pin 5) for feedback. However, if desired, an external in-loop buffer can optionally be added. This step will allow either line receiver device to drive even lower Z loads if desired (analogous to U2 of Figure 5.4).

In applying these devices to outside circuits, the designer should bear in mind that all external resistances in series with any of the four resistances can (and will) compromise CMR, unless they are held to a minimum and/or are equal in value. To place this in a useful perspective, a 0.25Ω mismatch can easily occur due just to wiring, and if it is not equalized at the opposite resistor, the mismatch will degrade the effective CMR of an otherwise perfect $25k\Omega$ array to 106dB, just as if the internal resistors had drifted. In practice then, these circuits are best fed from low

SSM-2141/SSM-2143 LINE RECEIVER



DEVICE	R1, R3	R2, R4	GAIN
SSM-2141	25k Ω	25k Ω	0dB
SSM-2143	12k Ω	6k Ω	-6dB

Figure 5.9

SSM-2141 AUDIO LINE RECEIVER CMR AND THD + N PERFORMANCE

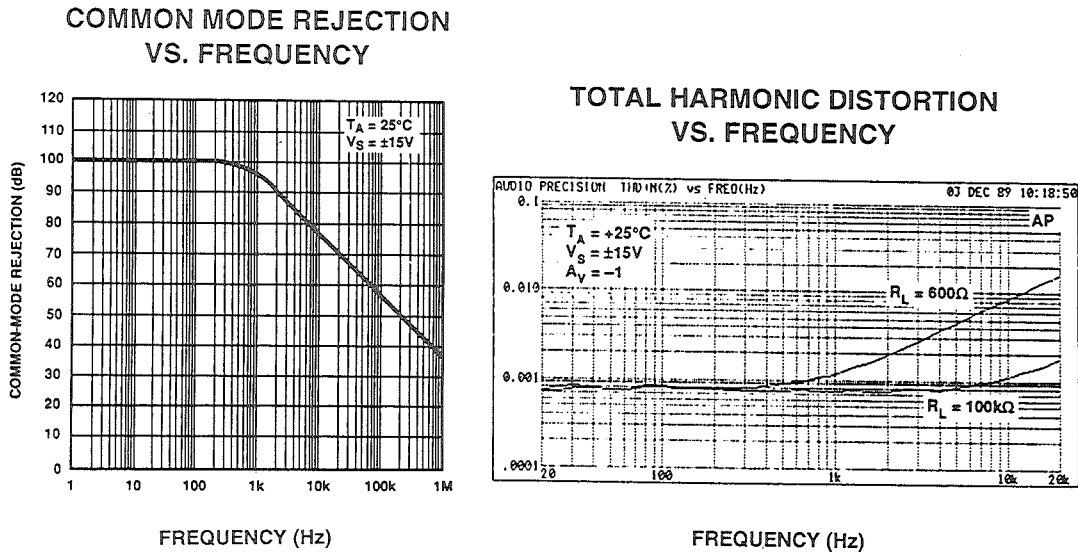


Figure 5.10

impedance and truly balanced sources, and all interfacing to them should be done mindful of this goal.

Perhaps the most outstanding attribute of these devices is their CMR performance, shown in Figure 5.10 (these data are for the SSM-2141, but the SSM-2143 is similar). For the SSM-2141 the DC-to-1kHz CMR is typically 100dB, and even at 10kHz it is still about 80dB. The SSM-2143 (not shown), using lower resistor values, has a somewhat lower typical CMR of 90dB, but maintains this to about 10kHz. The SSM-2141 THD+N performance also shown in Figure 5.10 is also very good for both 600Ω and 100kΩ loads.

With a companion differential line

driver (next section), these two line receivers allow convenient as well as flexible interfacing between points in audio systems, as well as other instrumentation up to 100kHz. However, they both are also more generally useful as flexible gain blocks within a system, not necessarily requiring the full CM performance aspects. For example, they are useful as either precise inverting or non-inverting gains blocks, due to the very accurate internal resistor ratios. With the SSM-2141 typical gain accuracy of 0.001%, very precise, single chip unity gain inverters and summers can be built at low overall cost.

LINE DRIVERS

Unlike the case for the differential line receiver, a standard circuit topology for differential line drivers is not quite as

clear-cut. Two circuit types are discussed in this sections, with their contrasts in performance and complexity.

“INVERTER-FOLLOWER” LINE DRIVERS

One straightforward approach to developing a unity gain differential audio drive signal for a balanced line is to process in complementary fashion a single-ended input V_{in} . This can be achieved with a like-gain inverter and follower op amp pair. With these complementary drivers operating at gains of $\pm 1/2$, this develops dual output signals of $V_{o1} = -V_{in}/2$ and $V_{o2} = V_{in}/2$ with respect to common, or V_o differentially equal to V_{in} . Note that in the same process the output V_o can also be scaled up if desired, since there is an inherent 6dB gain in headroom with differential operation.

This “inverter/follower” driver can be easily accomplished with a dual op amp such as the OP-275, and a set of discrete resistors (or a 20k Ω /10k Ω thin film network), as shown in Figure 5.11.

Here U1A provides the gain of $-1/2$ channel, while U1B operates at a gain of $+1/2$. The differential output signal across the balanced line is V_{in} for high impedance loads, and the differential output impedance is 600 Ω . Output current drive can be increased by lowering the matched resistances R_a and R_b . Note that the similar values for the gain resistors around U1A/U1B make their purchase easy in either discrete or network form. Like gain values for the A and B circuit halves also provide matched bandwidth and good balance versus frequency. Overall, this circuit is high in performance for its cost and reasonable simplicity.

Figure 5.12 shows a similar but more concise arrangement using a pair of SSM-2143 line receivers as integral precision amplifiers to develop the $\pm V_{in}$ signals.

The theory of operation here is the same as Figure 5.11 but fewer parts are used, just the 2 SSM-2143 ICs connected in differential fashion, plus R_a and R_b .

Choice between these two approaches can be in terms of complexity, or performance, with the twin SSM-2143 version optimum in terms of complexity. On the other hand, for output drive, the OP-275 version may be a better choice.

In system terms, this type of differential line driver can potentially run into application problems, and should be used with some caveats in mind. In reality, these two driver circuits are mirror-imaged single-ended drivers, and they produce voltage output signals with respect to the source (V_{in}) common point.

At the load end of a cable being driven, if the stage receiving the signal is a differential input with high impedance (i.e., like the SSM-2141 or SSM-2143), there is no real problem in application for either of these two line driver circuits. Note however that R_a must be *closely* matched to R_b for best CMR, if a 25k Ω receiver is to be used. This suggests low values for R_a and R_b , such as 100 Ω or less.

However, one side of the differential output from Figure 5.11 or Figure 5.12 *cannot be grounded without side effect*. This is because the source drive V_o is *not* truly floating, as would be in the case of a transformer winding. In this application sense, these two circuits are *pseudo differential*, and as such they shouldn't be used indiscriminately. Nevertheless, within small and defined systems they do have an obvious advantage of simplicity,

INVERTER/FOLLOWER DIFFERENTIAL LINE DRIVER USING OP-275 DUAL OP AMP

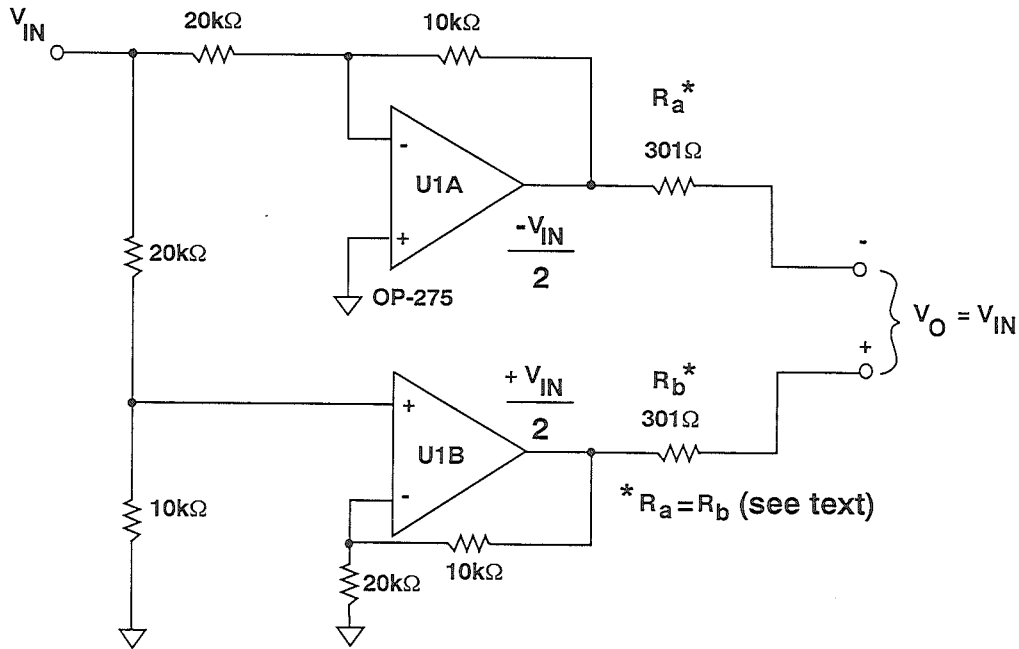


Figure 5.11

INVERTER/FOLLOWER DIFFERENTIAL LINE DRIVER USING SSM-2143 GAIN BLOCKS

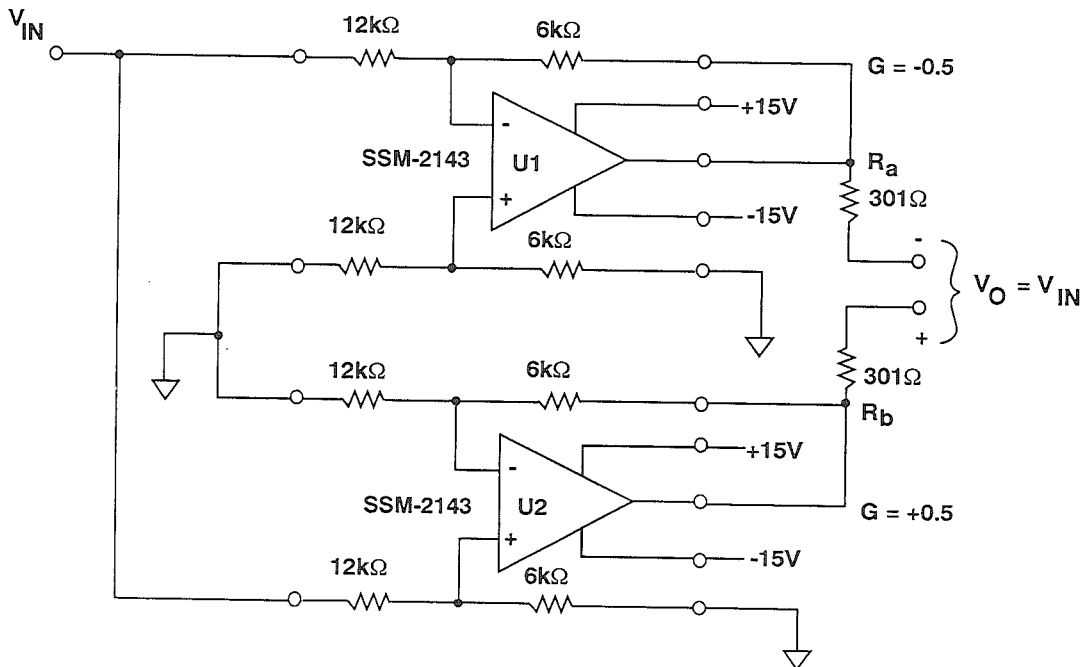


Figure 5.12

and can achieve high performance in signal fidelity. Note that with the matched source resistances R_a and R_b relatively high in value as shown, nothing

will be damaged even if the output is shorted... other than a loss of half the signal!

CROSS-COUPLED DIFFERENTIAL LINE DRIVERS

A more sophisticated form of differential line driver uses a pair of cross-coupled op amps with positive and negative feedback paths. This configuration provides maximum flexibility¹. It allows the differential output V_o to be maintained constant independent of the load common connections (either one can be shorted to common, as a transformer).

Figure 5.13 is a basic line driver circuit of this type, set up for the purposes of tests. Disregarding buffer stage U4 for the moment, amplifiers U1B-U2 and U1A-U3 are a pair of (buffered) op amps which are cross-coupled in terms of feedback. Each amplifier has a precision four resistor bridge network for feedback, and feeds a differentially connected load R_L through the 49.9 Ω build out resistors. The two

1.21k Ω resistors provide an output DC CM return.

As shown the circuit has maximum flexibility, and can be used with or without the input buffer, U4. This stage is advantageous for adding gain without disturbing the critical 5k Ω /10k Ω bridge resistors. If it is not used, then the input signal should be from an op amp or other low impedance source. Output buffer stages U2/U3 are AD811s, used for reasons similar to the line receiver of Figure 5.4. In the case here however, the output can develop appreciably higher currents for loads below 600 Ω (due to 2x greater voltage swing). Again, heat sinking of the AD811AN is suggested above $\pm 12V$ supplies.

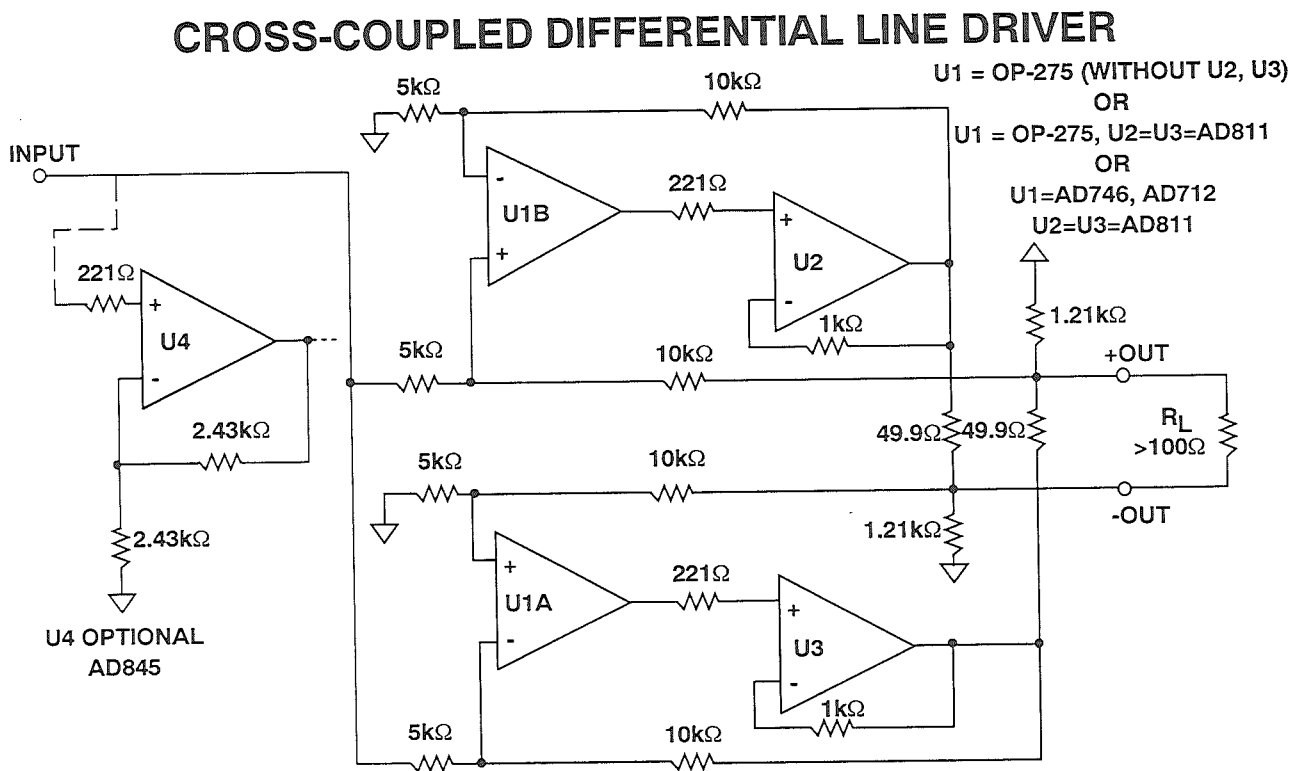


Figure 5.13

CROSS COUPLED DIFFERENTIAL LINE DRIVER THD+N PERFORMANCE USING VARIOUS OP AMPS

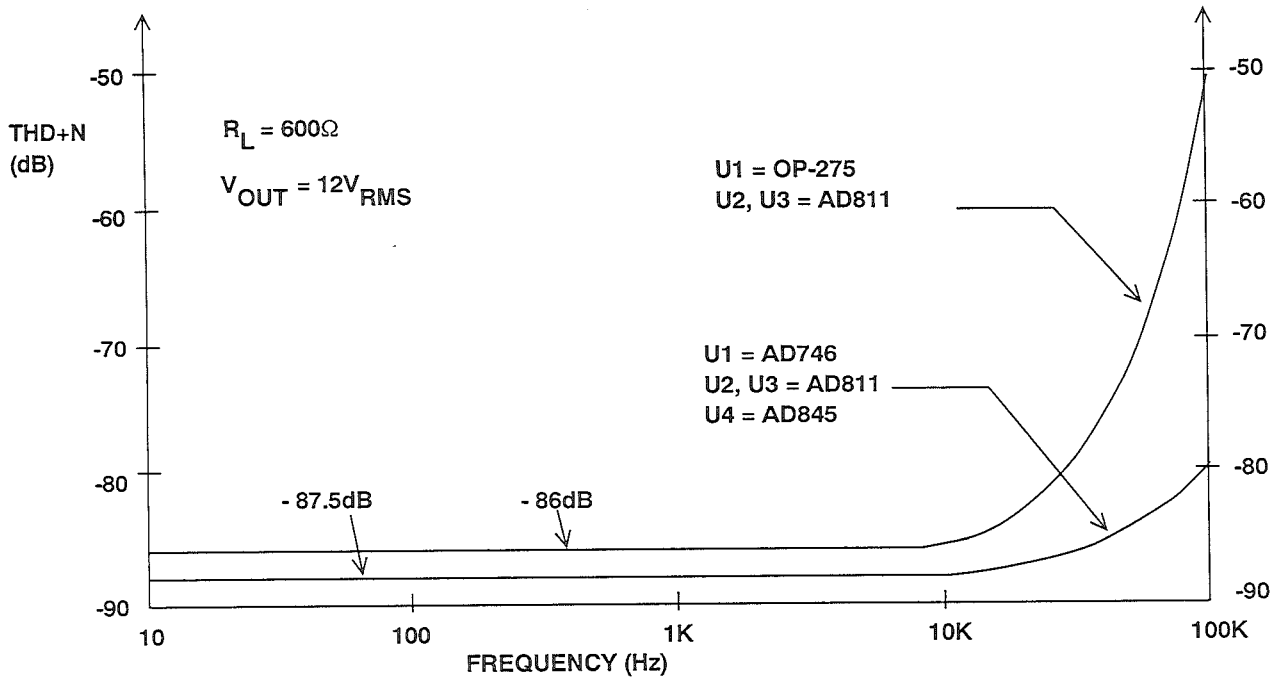


Figure 5.14

PERFORMANCE MEASUREMENTS

The circuit was tested with a variety of op amps used for U1 and U4, and with AD811 output buffers. The loading used was 600Ω , with an output swing of $12V_{rms}$; Figure 5.14 shows the results of these tests.

For frequencies approaching $100kHz$, the higher SR devices show the lowest distortion, as indicated by the AD845/AD746 curve. With OP-275 devices used for U1 and U4, the distortion is higher at the high frequency extreme due to the device's $20V/\mu s$ SR, but is still very low

below $20kHz$. Other amplifiers useful in this configuration are the AD711 and AD712 (not shown). Or, OP-275 devices can be used *without* the output U2-U3 buffer, allowing a minimum component circuit.

Like the line receiver circuit, this line driver is quite critical as to resistor ratios, in fact it is even more demanding since it uses more of them. This factor tends to make it impractical just as it is shown, for any amplifier combination or performance level.

SSM-2142 LINE DRIVER CONFIGURATION

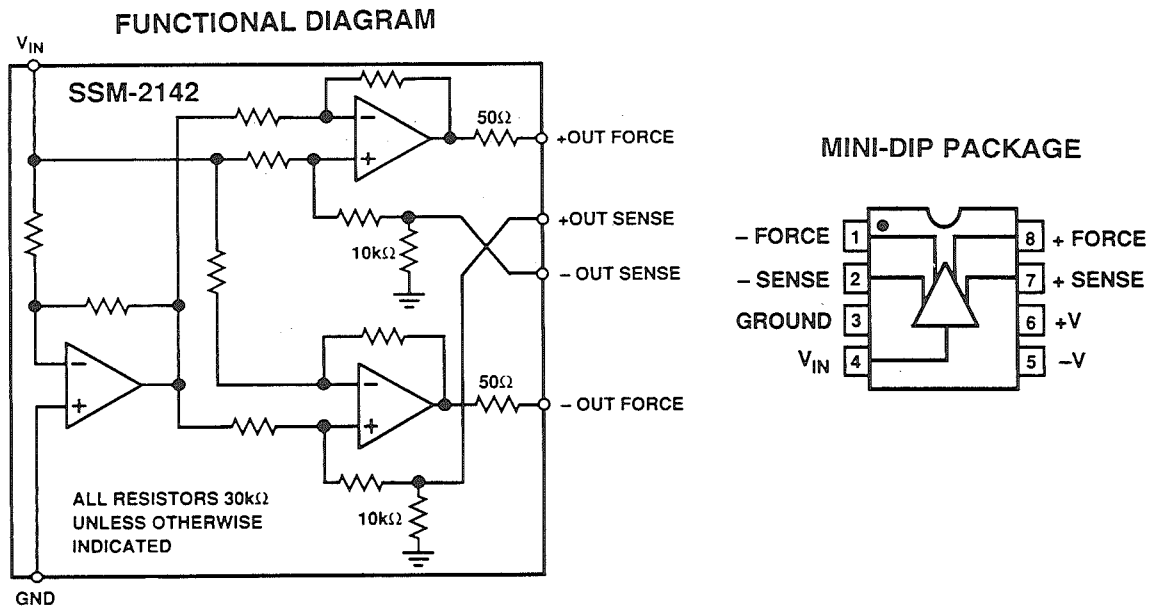


Figure 5.15

SYSTEM APPLICATION OF SSM-2142 LINE DRIVER WITH SSM-2141 OR SSM-2143 LINE RECEIVER

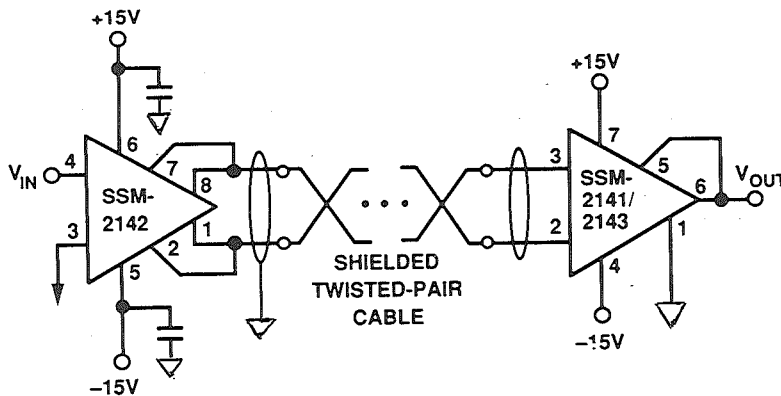


Figure 5.16

INTEGRATED LINE DRIVERS

On the other hand, the inherent features of laser trimmed monolithic technology can make a complex circuit such as the balanced line driver thoroughly practical. Like the SSM-2141 and SSM-2143 line receivers, applying these concepts to a driver circuit results in an efficient and useful IC. This product, the SSM-2142 balanced line driver, is shown in functional form in Figure 5.15. The multiple resistor array and trio of op amps shown in Figure 5.15a is packaged in the 8 pin miniDIP IC footprint of Figure 5.15b.

The SSM-2142 is designed for a single-ended to differential gain of 2 times, and in use can be simply strapped with the respective FORCE/SENSE pins tied together. In a system application, the SSM-2142 is used with either an SSM-

2143 or an SSM-2141 line receiver, as shown in Figure 5.16, with the differential mode signal being transmitted via shielded twisted pair cable. This hookup comprises a complete single-ended to differential and back to single-ended transmission system, with noise isolation in the process.

With the use of the SSM-2143 gain of 0.5, the SSM-2142 gain of 2 is complemented, and the overall system gain is unity. If the SSM-2141 is used as the receiver, the gain is 2 overall. The THD+N performance of the unity gain SSM-2142/SSM-2143 system is shown in Figure 5.17, for the conditions of a 5Vrms input/output signal, both with/without a 500' cable.

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SSM-2142/SSM-2143 SYSTEM THD + N PERFORMANCE,
 $V_{in} = V_{out} = 5V_{rms}$

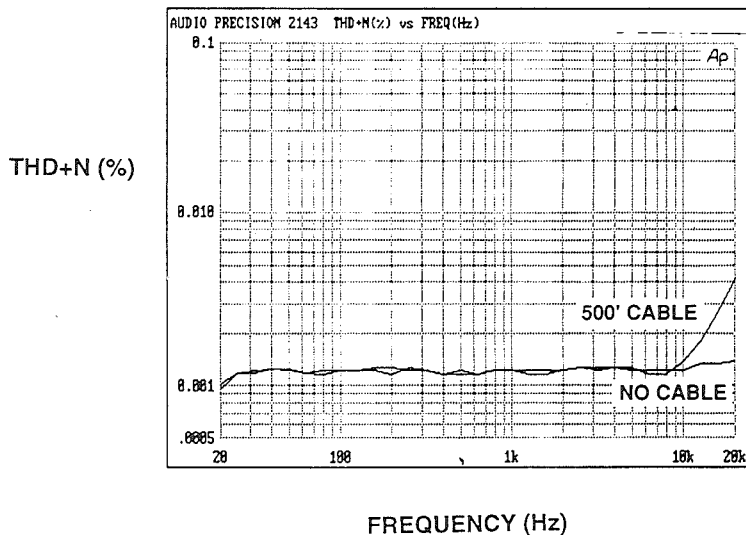


Figure 5.17

A HIGH PERFORMANCE AUDIO COMPOSITE LINE DRIVER STAGE

IC op amps of various types are often used as simple non-inverting gain stages to drive output lines. Typically, such line driver stages operate with voltage gains of 5-10 times (14-20 dB), work from medium-to-high impedance sources, and may drive difficult loads (600Ω or less, paralleled with several nF of capacitance). Ideally these goals are achieved with minimum non-linearity, providing low distortion operation over the full audio range.

However, this line stage has some requirements which basically conflict; it must drive low Z loads, but it cannot distort in doing so. It must operate with stability from medium to high Z sources, with minimal changes in DC offset, noise, and distortion as the source impedance changes (for example, operating from a level control). Unfortunately, high output currents can evoke thermal feedback in an op amp IC. When present, this result can also be a problem for both DC and low frequency AC signals.

A family of op amps with general specifications meeting these goals is the

FET input category. Better quality FET op amps have good DC specs, namely low offset voltage. In addition, they have input bias currents of just a few pA (low enough that DC current related errors are generally negligible for source resistances below a megohm). The combination of these attributes makes net DC errors low enough that an entire line driver stage can be DC coupled. Sadly though, while many good to excellent FET input op amps exist, very few have outstanding audio performance driving 600Ω (or lower) loads.

For ±10V peak signals (7Vrms), a 600Ω load requires ±17mA. However, this Ohm's law criterion is too simplistic. Actually, these levels must be delivered with low levels of total harmonic distortion (THD), preferably 0.001% (10ppm) or less over the audio range. When lower full scale distortion is desired, and/or lower impedances must be driven, the optimum IC choice becomes more challenging.

COMPOSITE AMPLIFIERS TO THE RESCUE

Fortunately, the technique of combining the best aspects of two different amplifiers into a single composite amp structure produces real dividends for a line driver. A high performance FET input IC can be used as the input stage, combined with a high current, wide band output stage. This allows the positive features of two dissimilar ICs to be exploited, with each optimized for their respective input and output tasks.

Figure 5.18 shows this low distortion composite amplifier, using a cascade of two amplifier ICs. Two gain stages are used, U1 and U2, with individual performance selected as follows.

In the topology shown, stage U1 provides the bulk of the overall amplifier open loop gain and determines the basic input characteristics. With U1 loaded as shown, by only the high impedance input (+) of U2, it has virtually zero drive requirements. This helps to maximize linearity. Stage U2 provides primarily a high current output, but it also provides additional voltage gain via local feedback.

With this topology, individual U1/U2 ICs can be selected for unique input or output performance advantages. These are characteristics not available in one device, or, even when available, not cost effective.

LOW DISTORTION COMPOSITE AMPLIFIER

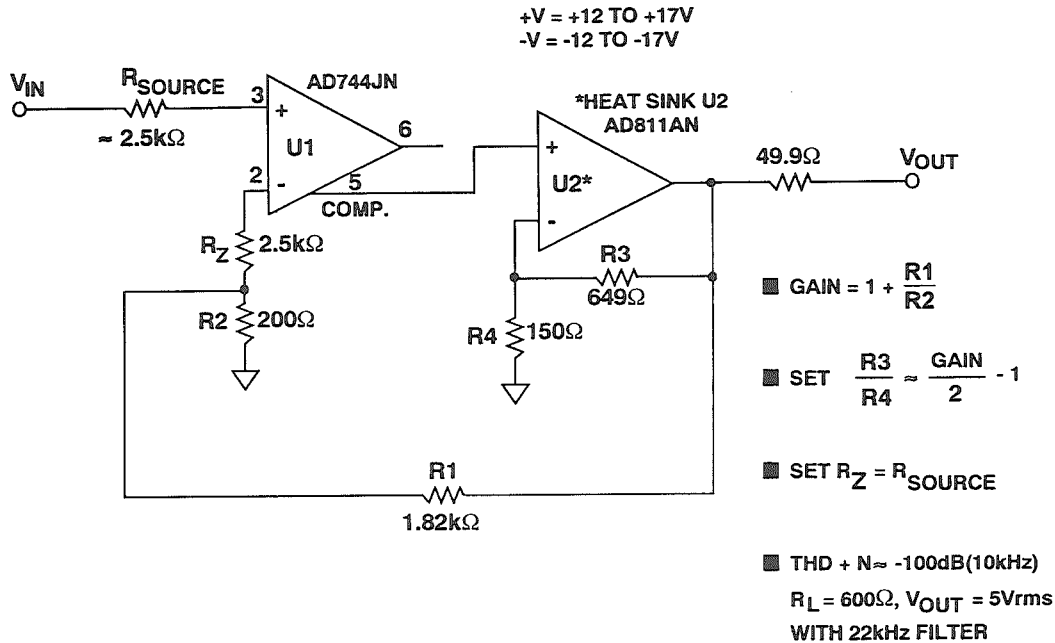


Figure 5.18

CIRCUIT DESCRIPTION

In this application U1 is an AD744, a high SR, fast settling FET input op amp with a basic THD of 0.001% below 10kHz (See Figures 16 and 20 of AD744 data sheet.) Note however, that since this characterization data is for a standard gain-of-10 follower, the net performance of the AD744 in this composite amplifier is appreciably better. This is due to several topology dependent factors.

One factor is that the U1 stage operates unloaded, which removes any output current related distortion within this stage. Another key point is that the overall gain bandwidth and SR of U1 are boosted, by a factor equal to the voltage gain of U2 (G2). For example, a 75V/μs SR in stage U1 becomes 75V/μs times G2, assuming the SR of U2 is appreciably higher (discussed further below).

A third ingredient which can lower frequency dependent distortion products is the use of input impedance compensation, which ideally balances both the R and C components seen at the input amp's two inputs (See the AD743 data sheet for a more detailed discussion of input impedance compensation in FET input op amps.) If used, this compensation serves to minimize the non-linear effects of FET input amplifier common mode capacitance. To implement this in Figure 5.18, an optional feedback resistance R_Z is added, between R₁-R₂ and U1's (-) input. R_Z is simply made equal to the nominal source impedance, R_{source} (R_{source} is shown here as the equivalent source resistance typical of a 50kΩ level control, operating at a low nominal level). For the performance tests below, R_Z was not used.

U2 in this application is an AD811AN, a high performance transimpedance amplifier. While designed primarily for video use, the AD811's key specs are a SR 2500V/ μ s, a bandwidth of 120 MHz, and 100mA of output current. These factors greatly enhance this circuit, by providing both high and linear load current capability. Simultaneously, since U2 operates with local feedback and is also a transimpedance amplifier, its own band-

DESIGN FACTORS

The design as shown in Figure 5.18 operates at an overall voltage gain "G" of 10, set by R₁ and R₂ as in a conventional non inverting amplifier, or:

$$G = 1 + (R_1/R_2)$$

The individual stability requirements of U1 and U2 must also be met by the design. In this case U1 is stable at a gain G₁, which is 2 (or more), therefore U2's gain G₂ should be made equal to

$$G_2 \leq G/(G_1)$$

In the design process, by first considering G and G₁, stage two gain G₂ is made to satisfy the overall stability require-

MEASURED PERFORMANCE

With these design and device selection factors, the composite amplifier performance is remarkable for its modest complexity. For a typical audio load of 600 Ω , THD+N at an output level of 5V_{rms} is on the order of 10 ppm (-100dB) for frequencies below 20kHz, as shown in Figure 5.19. Note that lower operating levels may appear to have higher distortion, but will actually be more limited by the noise of the AD744.

In terms of operating hints, maximum output will be a function of the power supplies, and can approach 10V_{rms} with supplies of about \pm 17V supplies (both

width remains essentially high and constant as the U2 local gain changes. With the AD811 used for U2, this has the effect of making the stage transparent to overall operation in terms of bandwidth and SR limitations. There still remains the potential for loading effects in U2. But, as U2 in this instance is designed for low video distortion driving low impedance loads, this likelihood is minimal.

Here, with a G₁ of 2, G₂ becomes 10/2 or 5, and R₃/R₄ are then selected for a ratio of (G/G₁)-1 to provide this.

It is important to note that because U2 is a transimpedance amplifier, local feedback resistor R₃ has a preferred value for stability purposes; here the value is 649 Ω . The designer should fix R₃ at 649 Ω , then set U2 stage gain via R₄, as:

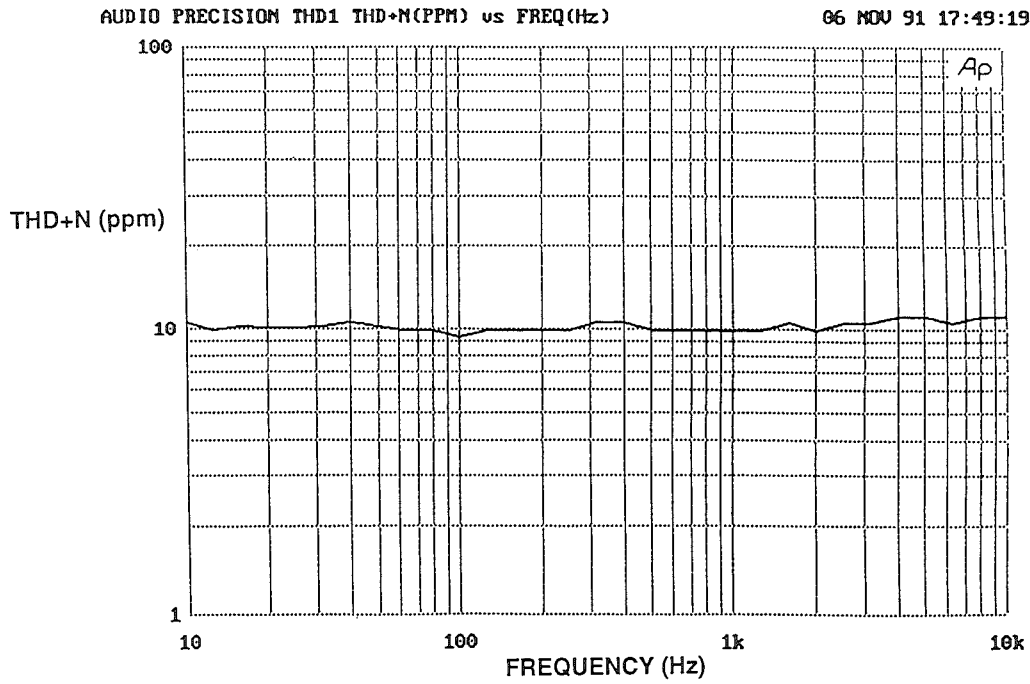
$$R_4 = \frac{649\Omega}{(G/G_1)-1}$$

(Note: R₄/R₃ are not as critical to gain as R₁/R₂, and they can be more loosely specified).

devices are rated for a maximum of \pm 18V). For supply voltages of \pm 12 or more however, a clip-on heat sink is recommended for U2, such as the Aavid 580100. For low impedance loads, the supplies should be well bypassed with large electrolytics, returned to the load common point.

Note that the general principles of this composite amp can be used for other devices in the U1/U2 positions, with different factors of optimization. For example, for lowest voltage noise from high Z sources, an AD745 (or AD743) device will be useful at U1.

COMPOSITE LINE AMPLIFIER THD + N PERFORMANCE,
 $V_{out} = 5V$ rms, $R_{load} = 600\Omega$, 22kHz Filter



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Figure 5.19

REFERENCES

¹ Circuits of this general form are known as cross-coupled Howland types, after the classic resistor bridge based current pump (see Dan H. Sheingold, "Impedance and Admittance Transformations Using Operational Amplifiers", *The Lightning Empiricist*, Vol. 12, #1, Jan. 1964, Philbrick Researches, Inc. Dedham, MA.).

For audio use, a cross coupled form was described by George D. Pontis, in "Floating a Source Output", *HP Journal*, August 1980.

²Walter G. Jung, **Audio IC Op Amp Applications, 3rd Edition**, 1987, Howard W. Sams.

³Heatsinks may be obtained from: Aavid Engineering Co., P.O. Box 400, Laconia, NH, 03247.