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RF TECHNOLOGY FOR THE 5G MILLIMETER WAVE RADIO

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Introduction

It's generally agreed that hybrid beamforming, such as that shown in Figure 1, will be the architecture of choice for 5G systems operating at microwave and millimeter wave frequencies. In this architecture, a combination of digital (MIMO) and analog beamforming is employed, to overcome the high path loss and improve the spectral efficiency. As shown in Figure 1, a combination of m data streams are split into n RF paths, to form beams in free space, making the total number of antenna elements a product of m × n. The digital streams may be combined in a number of fashions, whether to direct all energy at a single user with high layer MIMO, or to support several users with multiuser MIMO.

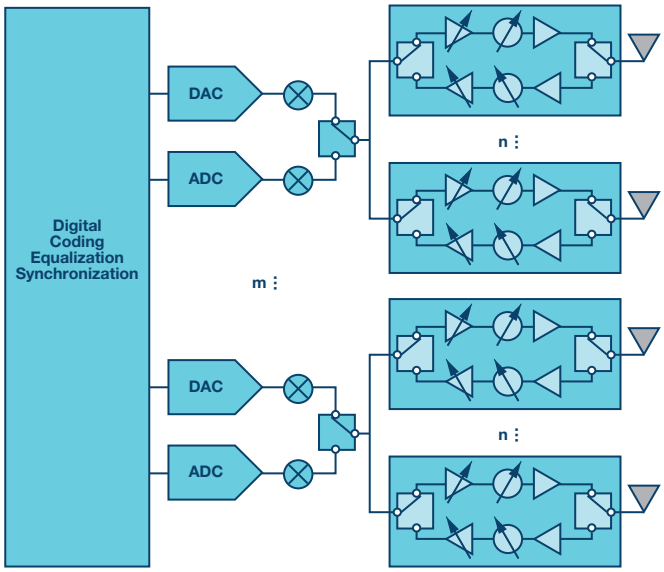

Figure 1. Hybrid beamforming block diagram.

In this article, we will work through a simple example of a large scale antenna array, to examine the optimum technology choice for the millimeter wave radio. Now, drilling into the block diagram of the radio section of the millimeter wave system, we see a classic heterodyne structure connected to a multiplicity of RF paths. In these paths, we employ phase shifters and attenuators to shape the beam.

Historically, millimeter wave systems have been built up using discrete components, resulting in large form factors and high cost. Legacy systems are comprised of a combination of CMOS, SiGe B*i*CMOS, and GaAs, with each technology selected to provide the optimum performance. For example, data converters are now developed in fine line CMOS processes, resulting in sampling rates in the GHz range. The up and down conversion and beamforming functions can be implemented efficiently in SiGe B*i*CMOS. Depending on the radio requirements, GaAs may be required for the power amplifier and low noise amplifier, but SiGe B*i*CMOS enables a higher level of integration if it can meet the requirements.

For the 5G millimeter wave systems, there is a desire to mount the RFICs on the backside of the antenna substrate, introducing a form requirement that drives aggressive integration. For example, the half wavelength element spacing for an antenna centered at 28 GHz is approximately 5 mm. For higher frequencies this becomes smaller, making the die or package size a significant consideration. Ideally, the entire block diagram for a single beam should be integrated in a single IC, but at the minimum, the up and down converter should be integrated with the RF front end on a single RFIC. The level of integration and technology of choice is somewhat dictated by the application, as we will see in the example analysis.

Example Analysis: Antenna Centered at 28 GHz with EIRP of 60 dBm

For this analysis, we consider a typical base station antenna system with an EIRP requirement of 60 dBm. The following assumptions were made:

- Element gain = 6 dBi at boresight
- Waveform PAPR = 10 dB (OFDM with QAM)
- Power amplifier PAE at P1dB = 30%
- Transmit/receive switch loss = 2 dB
- Transmit/receive duty cycle = 70%/30%
- Number of data streams = 8
- The power consumption of individual circuit blocks is based on currently available technology.

The model is built up on a base of eight data streams, connected to a varying number of RF chains. The number of antennae in the model scales in multiples of eight, up to 512 elements.

In Figure 2, we illustrate how the linearity of the power amplifier scales with increasing the gain of the antenna. Note that due to the switch loss, the output power of the amplifier is 2 dB higher than that presented to the antenna. As we add elements to the antenna, the directivity gain increases linearly against the logarithmic x-axis and subsequently, the power contribution required from each individual amplifier decreases.

For illustrative purposes, we have overlaid a technology map on top of the curves, to indicate which technology is optimal across the range of antenna elements. Note that there is overlap between the individual technologies, as each technology can be used over a range of values. Also, there is a range of performance that can be achieved in a given technology, dependent on process and circuit design practices. For very few elements, high power PAs (GaN and GaAs) are required in each chain, but as the number of elements exceeds 200, the P1dB crosses below 20 dBm, bringing the value into a range that can be satisfied by silicon processes. As the number of elements exceed 500, the PA performance is in the range that can be achieved with current CMOS technology.

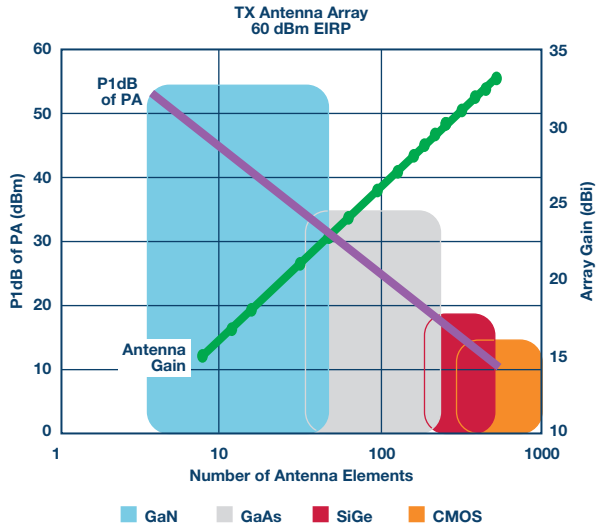

Figure 2. Antenna gain vs. output level requirement of power amplifier.

Now, consider the power consumption of the antenna Tx system as elements are added, as shown in Figure 3. As expected, the power consumption scales inversely with the gain of the antenna, but to a limit. Beyond a few hundred elements, the power consumed by the PA no longer dominates and results in diminishing returns.

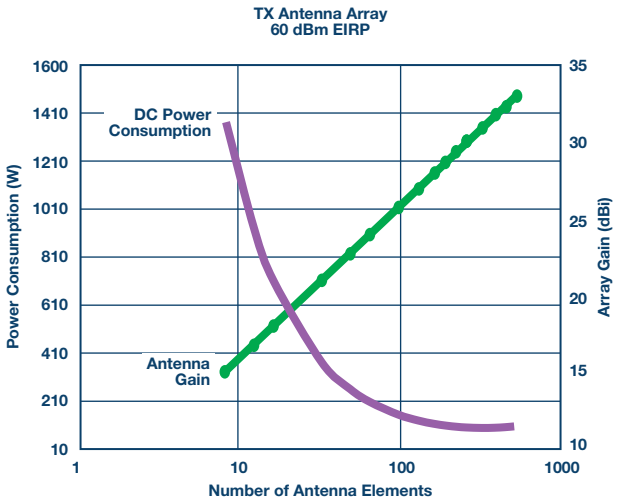

Figure 3. Antenna gain vs. the power dc power consumption of the Tx section of the antenna.

The power consumption of the entire system is shown in Figure 4 (transmitter and receiver). As expected, the power of the receiver increases linearly as RF chains are added. If we superimpose the declining Tx power curve on the increasing Rx power curve, we observe an area of minimum power consumption.

In this example, the minimum occurs at approximately 128 elements. Recalling the technology map introduced in Figure 2, in order to achieve an EIRP of 60 dBm with 128 elements, the optimum PA technology is GaAs.

While the use of a GaAs PA will result in the minimum power consumption for the antenna with 60 dBm EIRP, this may not meet all of the requirements for the system design. Recall earlier, it was mentioned that there is a requirement in many cases to fit the RFIC within the λ/2 spacing of the antenna elements. Using a GaAs-based transmit/receive module will provide the necessary performance, but it will not fit within the size constraints. An alternative packaging and routing scheme would need to be adopted, in order to utilize a GaAs transmit/receive module.

A preferred option may be to increase the number of antenna elements to accommodate a SiGe B*i*CMOS power amplifier, integrated within an RFIC. Our graph in Figure 4 shows that a SiGe amplifier will meet the output power requirement by doubling the number of elements, to approximately 256. While the power consumption increases marginally, the use of a SiGe B*i*CMOS RFIC can be made to fit within the λ/2 spacing of the antenna elements, at 28 GHz.

Extending this trend now to CMOS, we see that CMOS is also capable of achieving the overall 60 dBm EIRP, but from our technology map, this would require an additional doubling of antenna elements. Given that this solution will result in additional size and power consumption, we do not see the CMOS approach as a viable option, given current technology limitations.

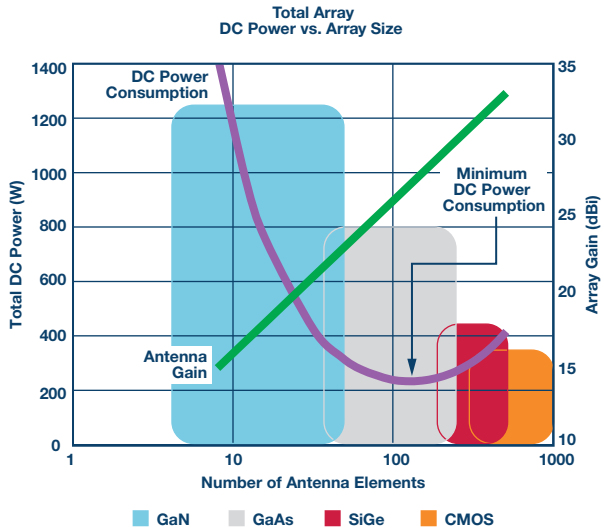

Figure 4. DC power consumption of entire antenna array vs. antenna gain.

Our analysis suggests that the optimum implementation of the 60 dBm EIRP antenna, considering both power consumption and integration form factor, is currently best achieved using a SiGe B*i*CMOS technology for the RFIC integration. However, if we consider a lower power antenna for a CPE, then of course CMOS is viable option.

While this analysis is based on currently available technology, there is great progress being made in millimeter wave silicon processes and design techniques. We expect improved power efficiency and higher output power capability from silicon processes in the future, which will enable smaller form factors and improved optimization of the antenna form factor.

As the arrival of 5G gets ever closer, it will continue to generate challenges for designers. When determining the best technology solution for millimeter wave radio applications, it is beneficial to consider all aspects of the signal chain, as well as the various advantages of different IC processes. As the 5G ecosystem develops, Analog Devices is focused on and committed to providing our customers with a broad technology portfolio, including a wide range of circuitry design processes, and a systems level approach, based on our unique bits to millimeter wave capability.

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