

Evaluates: RHP51002

General Description

The [EVAL-RHP51002-CSLZ](#) features the RHP51002, an ultralow noise, ultrahigh power supply rejection ratio (PSRR) negative low dropout (LDO) regulator. EVAL-RHP51002-CSLZ operates over an input range of -3.8V to -20V and can deliver up to 500mA output current. It features ultralow noise ($0.8\mu\text{V}_{\text{RMS}}$ from 10Hz to 100kHz) and very high PSRR (75dB at 1MHz).

The RHP51002 enable function (EN/UVLO pin) is bidirectional and can be controlled with either a positive or a negative voltage. The RHP51002 also offers programmable current limit functionality by connecting a resistor from I_{LIM} to GND. Current monitoring is also achieved by sensing the I_{LIM} pin voltage. The V_{IOC} tracking function controls an upstream switching converter to maintain a constant voltage across the regulator and, hence, minimize power dissipation. The power good feedback (PGFB) pin sets a programmable power good threshold and activates the fast start-up circuitry. To use the power good function, connect an external voltage source at V_{EXT} . If power good and fast start-up functionality are not needed, tie PGFB to IN.

Built-in protection includes reverse battery protection, reverse current protection, internal current limit with foldback, and thermal limit with hysteresis.

For a complete description of the RHP51002, including operating details and application information, refer to the [RHP51002 data sheet](#). The data sheet must be read in

conjunction with this valuation board user guide for EVAL-RHP51002-CSLZ. The RHP51002 is assembled in a 12-lead micro small outline Package (MSOP) and $3\text{mm} \times 3\text{mm}$ dual flat no-lead (DFN) packages with an exposed pad on the bottom side of the device. Proper board layout is essential for maximum thermal performance.

Quick Start Procedure

EVAL-RHP51002-CSLZ is easy to set up to evaluate RHP51002 performance. See [Figure 1](#) for proper measurement equipment setup and use the following procedure:

1. Connect a load between the V_{OUT} and GND terminals.
2. With power off, connect the input power supply to the V_{IN} and GND terminals.
3. Apply -3.8V across V_{IN} to GND. The output voltage should be $-3.32\text{V} \pm 3\%$ (-3.39V to -3.25V).
4. Vary V_{IN} from -3.8V to -20V and vary the load current from 0mA to 500mA . **Note:** Ensure that the power dissipation is below the thermal limit.
5. Apply a power source at V_{EXT} . The PG pin voltage should be approximately equal to V_{EXT} .
6. Refer to Application Notes [AN70](#) and [AN159](#) for measuring output noise and PSRR.

PERFORMANCE SUMMARY

Specifications are at $T_A = 25^\circ\text{C}$.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range (V_{IN})	$I_{\text{OUT}} = 150\text{mA}$, $V_{\text{OUT}} = -3.3\text{V}$	-20		-3.8	V
Input Voltage Range (V_{IN})	$I_{\text{OUT}} = 500\text{mA}$, $V_{\text{OUT}} = -3.3\text{V}$	-7		-3.8	V
Output Voltage (V_{OUT})	$V_{\text{IN}} = -5\text{V}$, $I_{\text{OUT}} = 500\text{mA}$	-3.39	-3.32	-3.25	V
Shutdown Input Current (I_{IN})	$V_{\text{EN}} = 0\text{V}$, $V_{\text{IN}} = -5\text{V}$		5		μA

*The maximum input voltage for a 500mA load current is set by the 60°C temperature rise of RHP51002 on the evaluation board. Higher input voltages can be applied if a larger copper area and/or forced-air cooling are applied. The difference between the input and output voltages also limits output current. Refer to the [RHP51002 data sheet](#) for details.

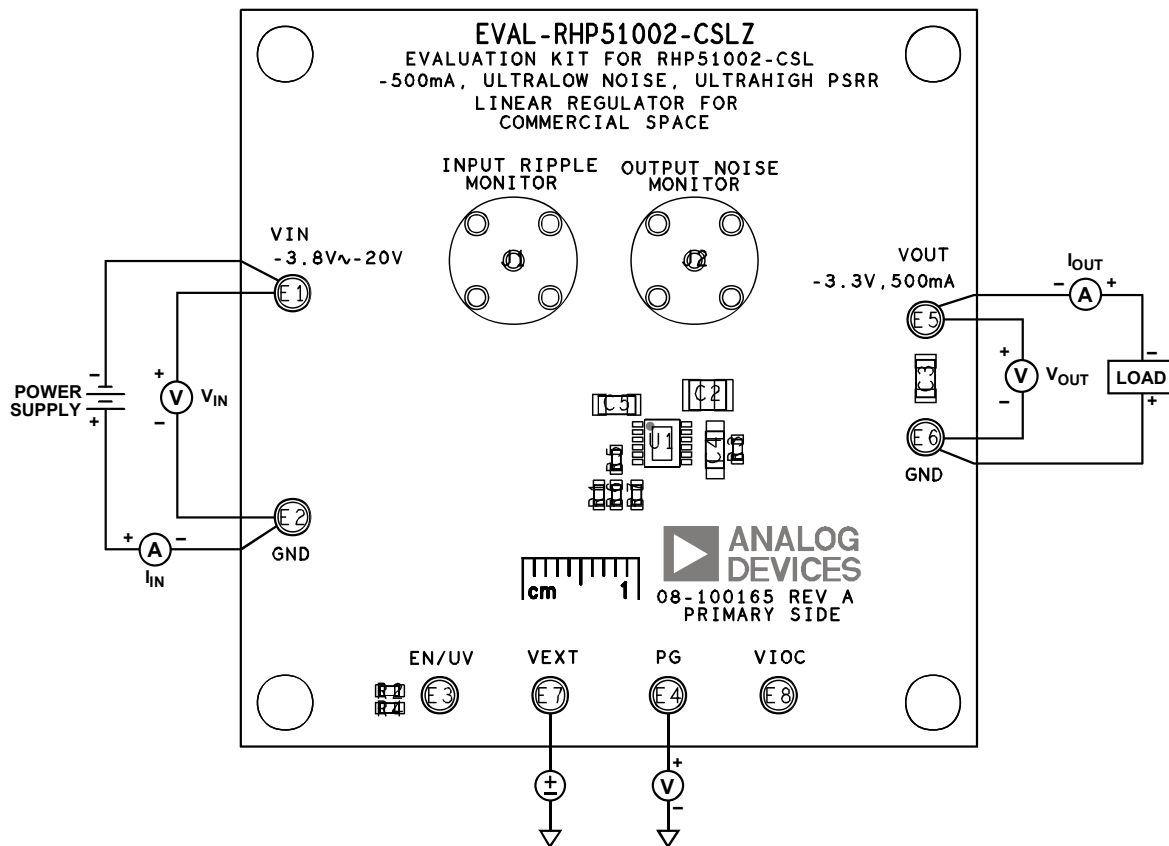


Figure 1. Test Procedure Setup Drawing for EVAL-RHP51002-CSLZ

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Printed Circuit Board (PCB) Layout Guidelines

Best PSRR Performance: PCB Layout for Input Trace

For applications using the RHP51002 for post-regulating switching converters, placing a capacitor directly at the RHP51002 input causes AC (at the switching frequency) to flow near the RHP51002. Without careful attention to PCB layout, this relatively high-frequency switching current generates an electromagnetic field (EMF) that couples to the RHP51002 output, degrading its effective PSRR. Highly dependent on the PCB, the switching preregulator, and the input capacitor size, among other factors, the PSRR degradation can easily be 30dB at 1MHz. This degradation is present even if the RHP51002 is desoldered from the board, because it effectively degrades the PSRR of the PC board itself. While negligible for conventional low-PSRR LDOs, RHP51002's ultrahigh PSRR requires careful attention to higher-order parasitics to realize the regulator's full performance.

The EVAL-RHP51002-CSLZ reduces this PSRR degradation by using a specialized layout technique. As shown in [Figure 2](#), the input trace (V_{IN}) and input capacitor C1 are highlighted in red. [Figure 3](#) highlights the return path (GND). Typically, when an AC voltage is applied to the board input, AC flows through this path and generates an electromagnetic field (EMF).

This EMF couples to output capacitor C2 and related traces, making the PSRR appear worse than it actually is. With the input trace directly above the return path, the EMFs are in opposite directions and consequently cancel each other out. Ensuring these traces overlap as closely as possible maximizes the cancellation effect and provides the regulator's maximum PSRR.

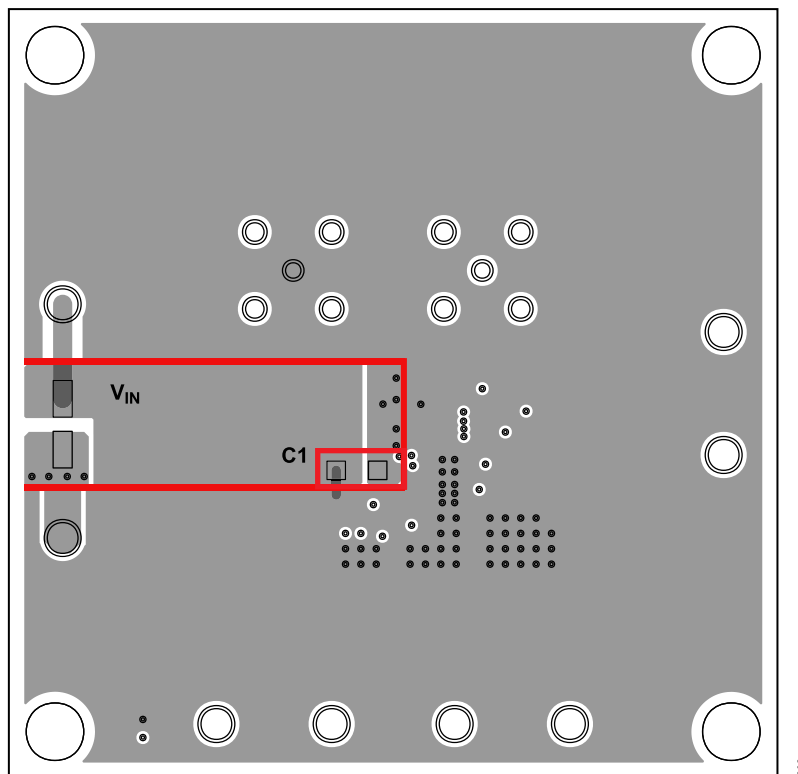


Figure 2. Bottom Layer of EVAL-RHP51002-CSLZ

Best AC Performance: PCB Layout for Output Capacitors C2

For ultrahigh PSRR performance, the RHP51002 bandwidth is quite high ($\sim 1\text{MHz}$), making it very close to the output capacitor's self-resonance frequency ($\sim 1.6\text{MHz}$). Therefore, avoid adding extra impedance (equivalent series resistance(ESR)) and equivalent series inductance(ESL)) outside the feedback loop. To that end, minimize the effects of PCB trace and solder inductance by Kelvin connecting OUTS and SET pin capacitor GND directly to the output capacitor (C2) terminals using split-capacitor techniques as shown in [Figure 4](#) and [Figure 5](#). Because only a small AC flows through these connections, solder joint/PCB trace inductance does not affect stability. While the RHP51002 is robust enough not to oscillate if the recommended layout is not followed, phase/gain margin and stability will degrade.

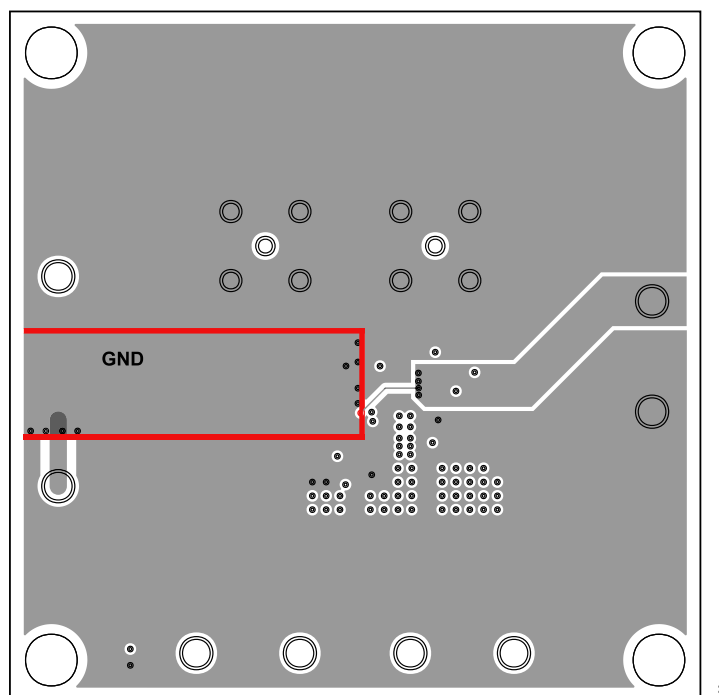


Figure 3. Layer 3 of EVAL-RHP51002-CSLZ

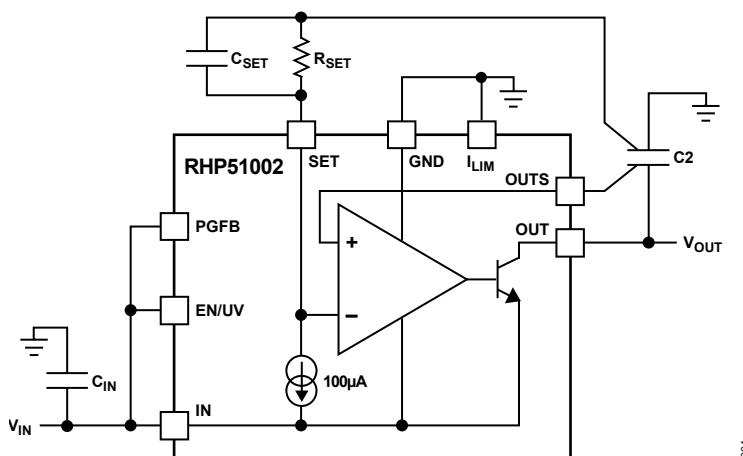


Figure 4. C2 and C_{SET} Connections for Best Performance

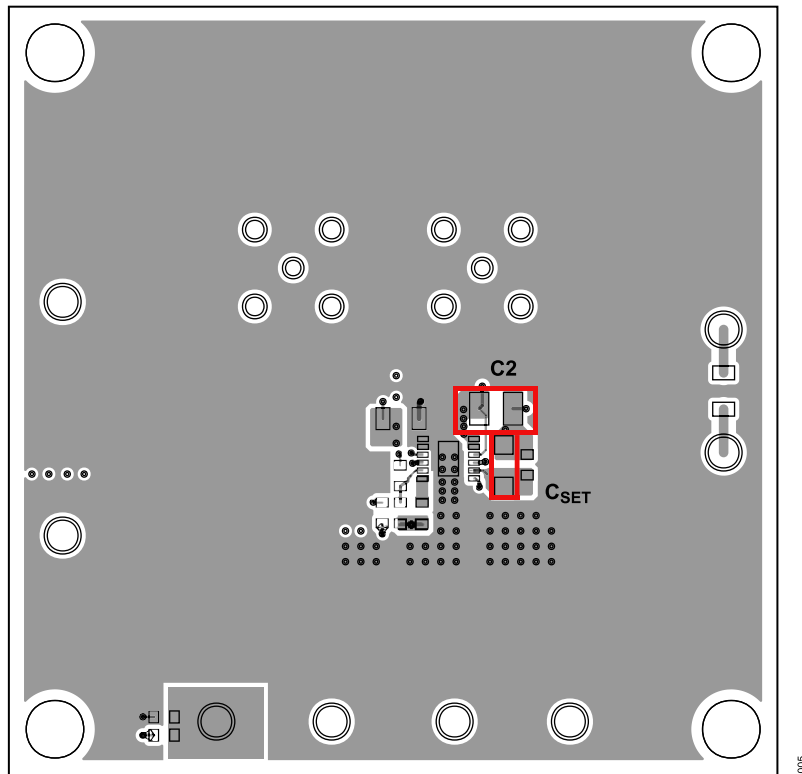


Figure 5. Split Pads for Output Capacitors on Top Layer of EVAL-RHP51002-CSLZ

Ordering Information

MODEL	DESCRIPTION
EVAL-RHP51002-CSLZ	RHP51002 Evaluation Board

EVAL-RHP51002-CSLZ Bill of Materials

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN	Capacitor, Aluminium, 22 μ F, 35V, 5mm $\times$ 5.4mm	Sun Electronic Industries Corp, 35CE22BSS
2	2	C1, C4	Capacitor, X7R, 4.7 μ F, 50V, 10% 1206	Murata, GRM31CR71H475KA12
3	1	C2	Capacitor, X7S, 10 μ F, 50V, 10% 1210	Murata, GCJ32EC71H106KA01
4	1	R1	Resistor, Chip, 200k Ω , 1/10W, 1% 0603	Vishay Dale, CRCW0603200KFK
5	1	R2	Resistor, Chip, 100k Ω , 1/10W, 1% 0603	Vishay, CRCW0603100KFKEA
6	1	R3	Resistor, Chip, 33.2k Ω , 1/10W, 1% 0603	Vishay Dale, CRCW060333K2FK
7	1	R5	Resistor, Chip, 453k Ω , 1/10W, 1% 0603	Vishay, CRCW0603453KFKEA
8	1	R6	Resistor, Chip, 49.9k Ω , 1/3W, 1% 0603	Vishay, CRCW060349K9FKEAHP
9	1	R7	Resistor, Chip, 4.99k Ω , 1/10W, 1% 0603	Vishay Dale, CRCW06034K99FK
10	1	U1	IC, RHP51002, MSOP-12	Analog Devices Inc., RHP51002IMSE-CSL#TRPBF
Additional Evaluation Board Circuit Components				
1	0	C3, C5 (OPT)	Capacitor, Optional, 1206	
2	0	R4 (OPT)	Resistor, Optional, 0603	
Hardware: For Evaluation Board Only				
1	8	E1 TO E8	Test Point, Turret, 0.094" PBF	MILL-MAX, 2501-2-00-80-00-00-07-0
2	2	J1, J2	Connector, BNC, 5 PINS	Connex, 112404
3	4	MH1 TO MH4	Stand-off, Nylon 15mm	Keystone, 9032

EVAL-RHP51002-CSLZ Schematic Diagram

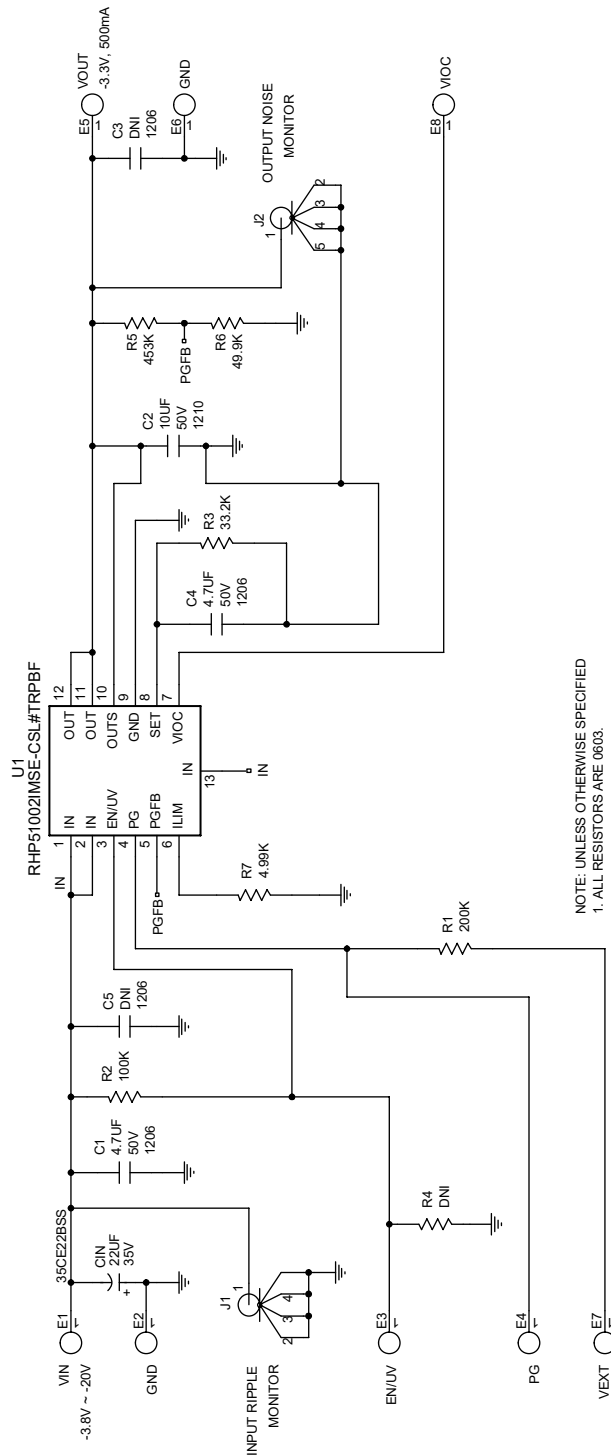


Figure 6. EVAL-RHP51002-CSLZ Schematic Diagram

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/26	Initial release	—

Notes

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