Evaluation Board User Guide

RHP51000 Evaluation Board

Evaluates: RHP51000

General Description

The EVAL-RHP51000-CSLZ features the RHP51000-CSL, a 20V, 500mA, ultra-low noise, and ultra-high power-supply rejection ratio (PSRR) low dropout (LDO) regulator with programmable current limit. Additionally, the RHP51000-CSL incorporates voltage input-to-output control (VIOC) tracking function that controls an upstream switching converter to maintain a constant voltage across the RHP51000-CSL and, therefore, minimize power dissipation.

The EVAL-RHP51000-CSLZ operates over an input range of 3.8V to 20V. The RHP51000-CSL delivers a maximum output current of 500mA and features ultra-low noise and ultra-high PSRR. The power good feedback (PGFB) pin is used to set a programmable power-good threshold. This IC also offers programmable current-limit functionality, and current monitoring is achieved by sensing the ILIM pin voltage.

Built-in protection includes reverse-battery protection, reverse-current protection, internal current limit with foldback and thermal limit with hysteresis. The RHP51000-CSL data sheet provides a complete description of the device, operation, and applications information. The data sheet must be read in conjunction with this user guide for the EVAL-RHP51000-CSLZ. The RHP51000-CSL is assembled in a 12-lead (3mm x 3mm) plastic DFN package with an exposed pad on the bottom side of the IC. Proper board layout is essential for maximum thermal performance.

Quick Start Procedure

The EVAL-RHP51000-CSLZ is simple to set up to evaluate the performance of the RHP51000-CSL. See *Figure 1* for the proper measurement equipment setup, and take the following steps.

1. Connect a load between VOUT and GND terminals.
2. With power off, connect the input power supply to the VIN and GND terminals.
3. Ensure that the shunt of JP1 is in the ON option.
4. Turn the input power supply on, and ensure that the voltage is between 3.8V and 20V.
5. Refer to *Application Note AN70* and Application Note *AN159* for measuring the output noise and PSRR.
6. With JP1 at USER SELECT option, R4 and R2 can be used to set an accurate undervoltage lockout (UVLO) threshold.

Ordering Information appears at end of data sheet.

Performance Summary

Specifications are at T_A = 25°C, unless otherwise noted.

Table 1. Performance Summary

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	I_{OUT} = 150mA, V_{OUT} = 3.3V	3.8		20	V
		I_{OUT} = 500mA, V_{OUT} = 3.3V	3.8		9.3[1]	V
Output Voltage	V_{OUT}	V_{IN} = 5V, I_{OUT} = 500mA	3.2	3.3	3.4	V
Shutdown Input Current	I_{IN}	JP1 = OFF, V_{IN} = 5V		0.1		µA

[1] *The maximum input voltage for a 500mA load current is set by the 65°C temperature rise of the RHP51000-CSL on the evaluation board. Higher input voltages can be reached if larger copper area or forced-air cooling is applied. The RHP51000-CSL limits output current at higher input-to-output voltage differentials. Refer to the RHP51000-CSL data sheet for more details.*

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

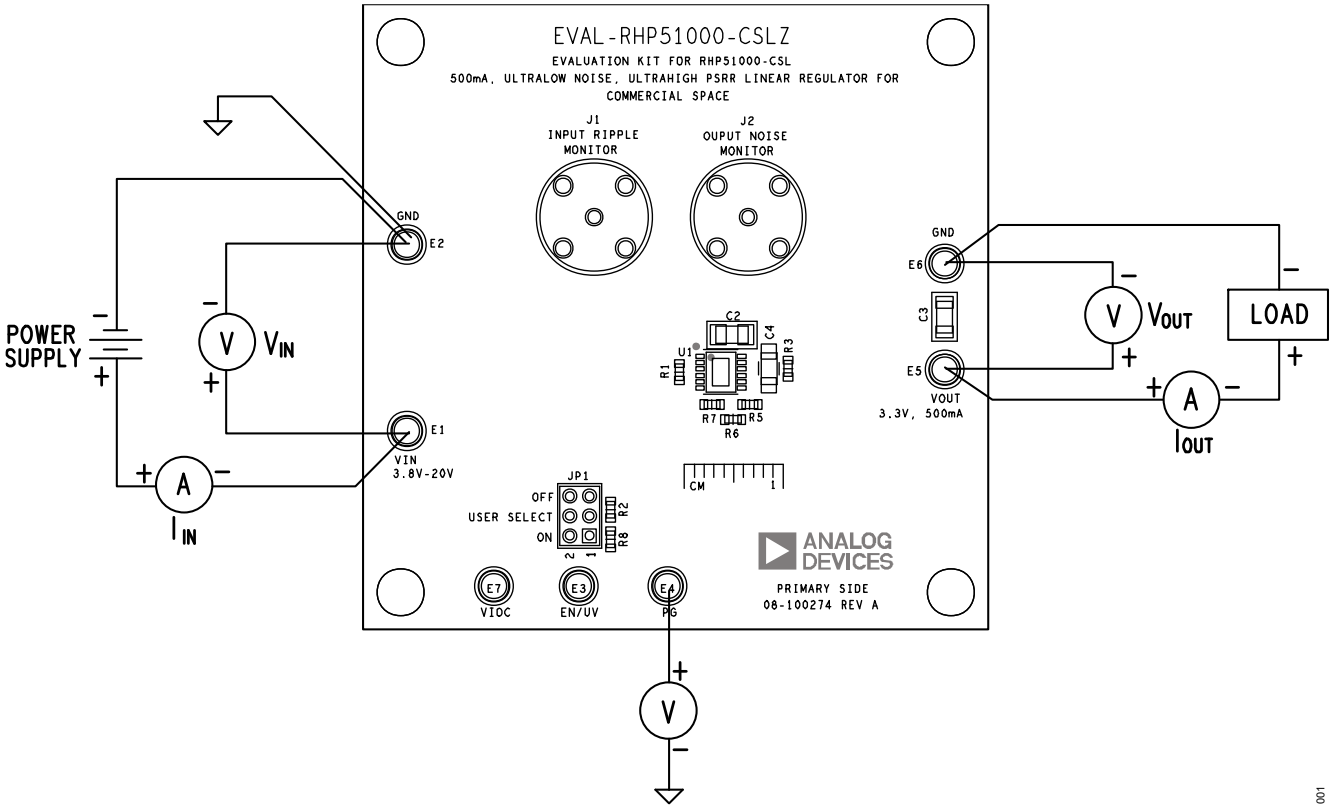


Figure 1. Test Procedure Setup Drawing for EVAL-RHP51000-CSLZ

Printed Circuit Board (PCB) Layout

Best PSRR Performance: PCB Layout for Input Traces

For applications using the RHP51000-CSL for post-regulating switching converters, placing a capacitor directly at the RHP51000-CSL input results in AC current (at the switching frequency) flowing near the RHP51000-CSL. Without careful attention to PCB layout, this relatively high-frequency switching current generates an electromagnetic field (EMF) that couples to the RHP51000-CSL output, degrading its effective PSRR. Highly dependent on the PCB, the switching preregulator, and the input capacitor size, among other factors, the PSRR degradation can easily be 30dB at 1MHz. This degradation is present even if the RHP51000-CSL is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional low PSRR LDO regulators, the ultra-high PSRR of the RHP51000-CSL requires careful attention to higher-order parasitics to realize the full performance offered by the regulator.

The RHP51000-CSL evaluation board alleviates this degradation in PSRR by using a specialized layout technique. On layer 3, the input trace (V_{IN}) is highlighted in red, while the return path (GND) is highlighted on the bottom layer, along with the input capacitor C1. Normally, when an AC voltage is applied to the input of the board, AC current flows on the path, thus generating EMF. This EMF couples to the output capacitor C2 and related traces, making the PSRR appear worse than it actually is. With the input trace directly above the return path, the EMFs are in opposite directions, and consequently, cancel each other out. Making sure that these traces exactly overlap each other maximizes the cancellation effect and thus provides the maximum PSRR offered by the regulator.

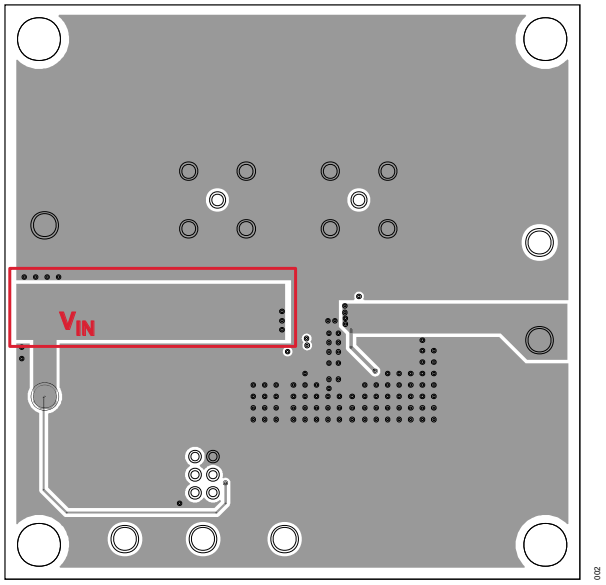


Figure 2. Layer 3 of EVAL-RHP51000-CSLZ

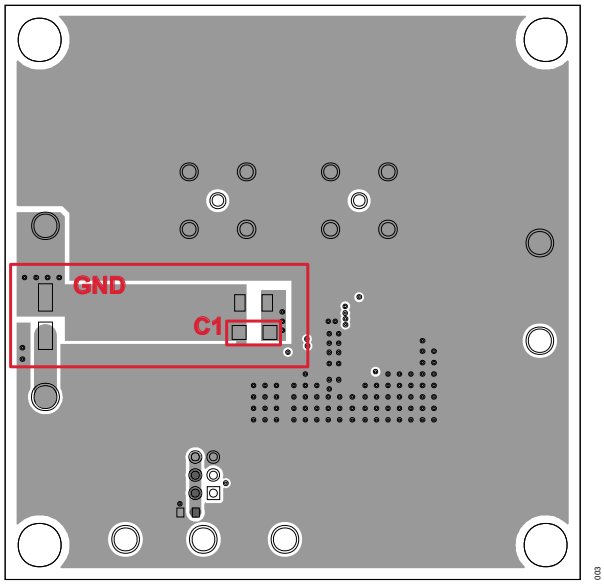


Figure 3. Bottom Layer of EVAL-RHP51000-CSLZ

Best AC Performance: PCB Layout for Output Capacitor C2

For ultra-high PSRR performance, the RHP51000-CSL bandwidth is quite high (~1MHz), making it close to the self-resonance frequency (~1.6MHz) of the output capacitor. Therefore, it is important to avoid adding extra impedance (effective-series inductance (ESL) and effective-series resistance (ESR)) outside the feedback loop. To that end, minimize the effects of the PCB trace and solder inductance by Kelvin connecting the output sense pin (OUTS) and SET pin capacitor (C_{SET}) GND directly to the terminals of the output capacitor (C2) using a split capacitor technique. Pad 4 connects to the OUTS pin and Pad 1 connects to the GND side of the SET pin capacitor. With only small AC current flowing through these connections, the impact of the solder joint and/or PCB trace inductance on stability is eliminated. While the RHP51000-CSL is robust enough not to oscillate if the recommended layout is not followed, phase and gain margin and PSRR degrade.

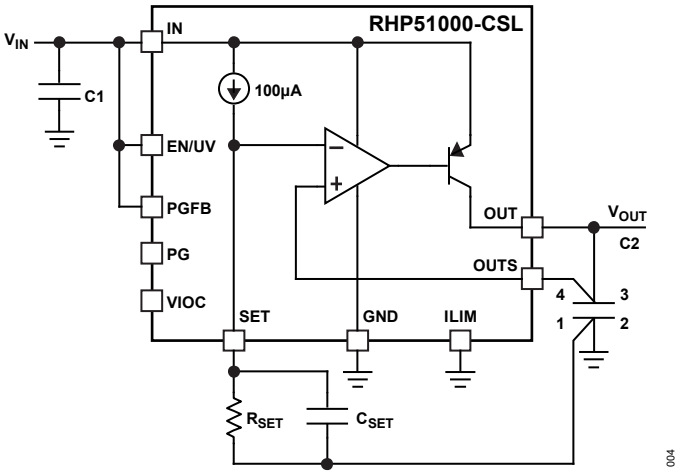


Figure 4. C2 and C_{SET} Connections for Best Performance

RHP51000 PCB Layout

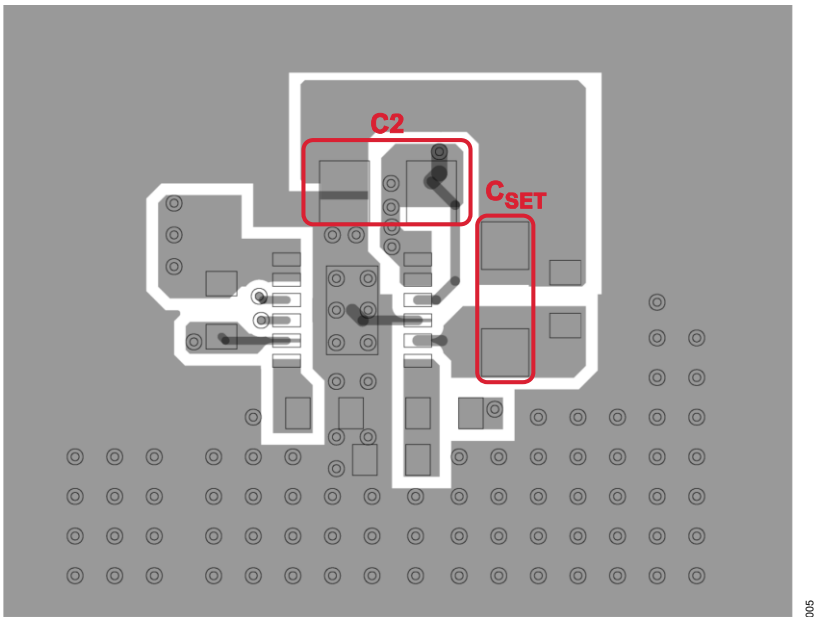


Figure 5. Split Pads for C2 on the Top Layer of EVAL-RHP51000-CSLZ

Ordering Information

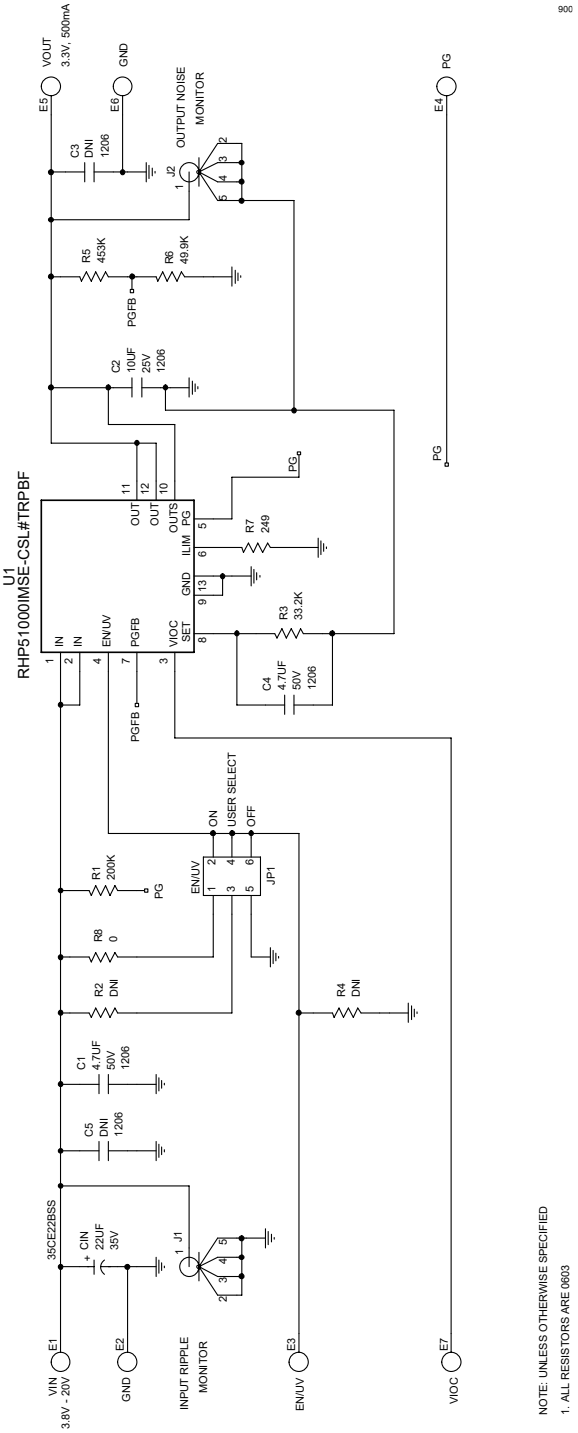
MODEL	DESCRIPTION
EVAL-RHP51000-CSLZ	RHP51000 Evaluation Board

Z = RoHS-Compliance Part.

RHP51000 Bill of Materials

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CIN	Capacitor, Aluminum, 22µF, 35V, 5mm × 5.4mm	Sun Electronic Industries Corp, 35CE22BSS
2	2	C1, C4	Capacitors, X7R, 4.7µF, 50V, 10%, 1206	Murata, GRM31CR71H475KA88L
3	1	C2	Capacitor, X7R, 10µF, 25V, 10%, 1206	TDK, C3216X7R1E106K160AB
4	1	R1	Resistor, Chip, 200kΩ, 1/10W, 1%, 0603	Vishay, CRCW0603200KFK
5	1	R3	Resistor, Chip, 33.2kΩ, 1/10W, 1%, 0603	Vishay, CRCW060333K2FK
6	1	R5	Resistor, Chip, 453kΩ, 1/10W, 1%, 0603	Vishay, CRCW0603453KFKEA
7	1	R6	Resistor, Chip, 49.9kΩ, 1/10W, 1%, 0603	Vishay, CRCW060349K9FKEAHP
8	1	R7	Resistor, Chip, 249Ω, 1/10W, 1%, 0603	Vishay, CRCW0603249RFK
9	1	U1	IC, RHP51000-CSL, 12 Pin DFN, 3mm × 3mm	Analog Devices, Inc., RHP51000IMSE-CSL#TRPBF
Additional Evaluation Board Circuit Components				
1	0	R2, R4 (OPT)	Resistor, 0603	
2	0	C3, C5 (OPT)	Capacitors, 1206	
3	1	R8	Resistor, Chip, 0, 1/10W, 5%, 0603	Vishay, CRCW06030000Z0EA
Hardware: For Evaluation Board Only				
1	7	E1 to E7	Testpoint, Turret, 0.094" PBF	Mill-Max, 2501-2-00-80-00-00-07-0
2	1	JP1	Header, 3 Pin, 0.079, Double Row	Wurth Elektronik, 62000621121
3	2	J1, J2	Connector, BNC, 5 Pins	Connex, 112404
4	4	MH1 to MH4	Standoff, Nylon, 15mm	Keystone, 9032

Evaluation Board Schematic



Notes