

Power Conditioner for APL Field Devices

General Description

The EVAL-LT8440-AZ evaluation circuit features the LT8440 used in a load power port of an intrinsically safe field device. It can regulate and limit the power drawn by the port according to the Ethernet Advanced Physical Layer (Ethernet-APL) standard. The EVAL-LT8440-AZ is designed with three LT8440s in series to meet the triple redundancy requirement of intrinsic safety Ex ia for class A field devices, but it can be configured to work with a lower LT8440 count. See the [Redundancy of LT8440](#) section for more details.

The evaluation circuit is also equipped with filters and protection components to meet the Ethernet-APL and intrinsic safety standards, including IEC60079-11 and IEC60079-47 standards. Communication signal integrity is

well preserved on this evaluation circuit, allowing seamless link up between 10BASE-T1L devices.

The EVAL-LT8440-AZ board is designed to operate from 9V to 17.5V input voltage. Across the input voltage range, the LT8440 draws current in parallel with the load up to the 500mW minimum guaranteed for Class A load power ports in compliance with Advanced Physical Layer (APL) standards. In case of load circuit failures, the evaluation board also limits input power below 650mW. The LT8440 shunts current even at no load to ensure at least 20mA input current during normal operation, which is required by APL specification for signal integrity.

Design files for this circuit board are available at [Product Evaluation Boards and Kits](#) | [Design Center](#) | [Analog Devices](#).

Performance Summary ($T_A = 25^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{INPUT}		9		17.5	V
Output Voltage	V_{OUTPUT}	Open output			16.2	V
Input Current	I_{INPUT}	Open output, steady state			43.3	mA
		Shorted output, steady state	28.5		55	mA
Load Current ¹	I_{LOAD}	$V_{\text{INPUT}} = 9\text{V}$	0		49.5	mA
		$V_{\text{INPUT}} = 15\text{V}$			36.7	mA
		$V_{\text{INPUT}} = 17.5\text{V}$	0		31.3	mA
Input Power ²	P_{INPUT}		340		650	mW
Load Power ³	P_{LOAD}	$V_{\text{INPUT}} = 9\text{V}$			371	mW
		$V_{\text{INPUT}} = 15\text{V}$			501	mW
		$V_{\text{INPUT}} = 17.5\text{V}$			507	mW

¹ Allowed load current before the LT8440 enters the current limit mode.

² Input port power consumed by the evaluation circuit and load.

³ Available power at the output port for the load.

Quick Start Procedure

The EVAL-LT8440-AZ evaluation circuit is used to evaluate the performance of the LT8440 and as a reference for customer applications. See [Figure 1](#) for proper measurement equipment setup and use the following procedure:

1. Ground the EVAL-LT8440-AZ board to Earth using the Earth GND turrets.
2. With power off, connect the input power source (APL field switch) using a 10BASE-T1L cable (a twisted pair of conductors) to the input terminal block J1.
3. Connect a 10BASE-T1L transceiver (ADIN1110 or ADIN1100) to the header J2 to receive communication signals.
4. Connect the load (APL field device) to the output terminal J3. Make sure the load current stays within APL standards.
5. Turn on the input power supply (APL field switch) at 12V, 0.5A limit.
6. Check for the proper output voltage, which should be around 10.5V.
7. If the circuit is not stable, adjust the compensation according to the [Compensation Values](#) section.
8. Once the proper output voltage is established, adjust the input voltage and load within the operating range and observe the input current, load current, and Ethernet signals.

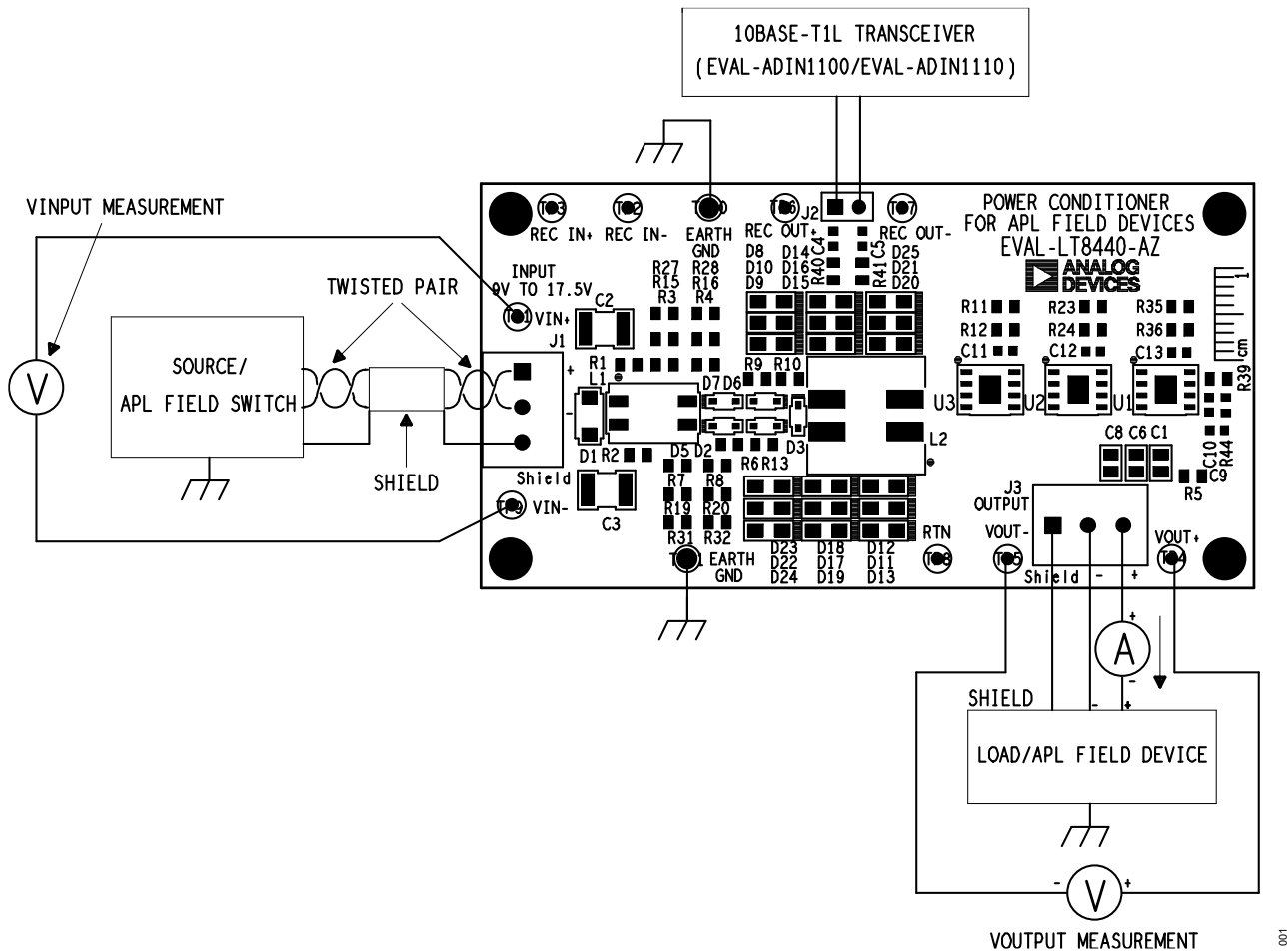


Figure 1. EVAL-LT8440-AZ Connection

Input Voltage

The EVAL-LT8440-AZ is designed to operate with an input voltage ranging from 9V to 17.5V. The upper input voltage limit is specified in the intrinsic safety standard IEC 60079-47. Due to the full bridge rectifier at the input port, the EVAL-LT8440-AZ is polarity insensitive, meaning it can also operate normally with negative input voltage from -17.5V to -9V. In addition, it can be reconfigured to work with a higher input voltage of up to 36V, which is the rated input voltage of the LT8440. The TVS diode D1 needs to be replaced by another TVS diode that can provide overvoltage protection for the new input voltage range.

Load

On the evaluation board, the LT8440's LINEA and LINE pins are used to sense voltage after the common-mode choke, which is nearly equal to the input voltage. Depending on the sensed voltage and the load, the LT8440 regulates or limits the consumed power at the input terminal to comply with the APL standard for a Class A power port load.

At light loads, the rightmost LT8440 (U1) shunts current at the output by controlling the integrated shunt FET in parallel with the load. The shunt and load currents return to the input through the integrated pass FET in three LT8440s series. These pass FETs are normally on. This current shunt scheme of the LT8440 helps the evaluation circuit achieve significant requirements in the APL standard. It guarantees that a minimum of 20mA input current is drawn to keep the forward diodes in the signal path always on, maintaining the signal integrity. It also ensures that the total power consumption at the input port is semi-constant, around 440mW, as shown in [Figure 5](#). When the load current exceeds the bottom curve in [Figure 4](#), the LT8440 completely turns off the shunt FET to stop drawing extra current. As a result, the power consumption at the input port is nearly identical to the load.

In events of circuit failure or heavy load, the LT8440 partially turns off the integrated pass transistor, limiting the input power consumption to the top curve shown in [Figure 5](#), which is less than 650mW. Consequently, the output voltage drops to reduce the available power at the output port. Therefore, the load current should be designed accordingly to keep the load power below the limit curve in [Figure 5](#) at the steady state.

The load circuitries are recommended to start up slowly to avoid current spikes that can trigger the LT8440 into the current limit mode. In addition, the output capacitor should be sized large enough to accommodate the load without dropping too much voltage. As the load capacitance directly affects the current shunt control loop of the rightmost LT8440 (U1), the compensation network of U1 needs to be tuned for stability purposes for different load capacitance values. See the [Compensation Values](#) section for more details.

The maximum load current should be derated as the junction temperature approaches its maximum temperature rating. Power dissipation within the IC can be estimated by calculating the total power loss. The junction temperature can be calculated by multiplying the total IC power dissipation by the junction-to-ambient thermal resistance and adding the ambient temperature. The overtemperature protection shuts down the IC when the junction temperature exceeds 175°C (typ).

Redundancy of LT8440

The highest level of intrinsic safety (Ex ia) allows the system to withstand two countable faults. Countable faults refer to arbitrary faults imposed by the examiner to analyze the efficacy of protection against thermal and spark ignition faults. Therefore, three independent power-limiting devices are required in series, and the LT8440 has been designed so that three instances of the part can operate in series. The RTN and RTP pins are positioned on opposite sides of the package so that the current exiting from the RTN pins of one instance can enter the RTP pins of the following instance by a short and direct path.

The LT8440 can operate in single, double, or triple redundant circuits to provide Ex ic, ib, or ia level of circuit protection. To reduce the level of redundancy, the unused LT8440 can be removed from the board. Its unpopulated RTN and RTP pads must be connected to allow a continuous current flow in the return path. U1 should always be used in the evaluation circuit as it is configured to control the shunt current.

Additional Protection Features

As required in the standard, the shield of the twisted pair of conductors must be connected to the chassis of the field device, which is also Earth-grounded. Hence, the EARTH GND turrets are used to connect the evaluation board's chassis to Earth Ground to meet this requirement.

The TVS diode D1 protects surge or ESD events in the input cable. D1 is sized to withstand a peak current of 25A for a pulse shape of 8/20 μ s, which is specified in the IEC 61643-21 standard. The breakdown voltage of D1 is greater than 17.5V and lower than the absolute maximum voltage ratings of the LT8440 to ensure normal operation below 17.5V and overvoltage protection above 17.5V.

A common-mode choke L1 suppresses the common-mode noise in the twisted pair. Following L1 is a diode bridge used to ensure normal operation in both polarity configurations at the input terminal. An additional diode D3 blocks the spark energy when faults happen in the diode bridge. Low forward-voltage diodes are chosen for the diode bridge to reduce the voltage drop on the diodes and increase the available power to the load and input voltage of the LT8440. Schottky diodes are not selected because they have high leakage currents at high temperatures, which can't be sensed by the LT8440.

According to IEC60079, components in the power path should be able to withstand 1.5 times the worst-case stress, which is 17.5V and 380mA. Hence, all protection components on the power path are rated at least 26.25V and 570mA.

LINEA/LINEB Connection

At the default configuration, the LINEA/LINEB pins of the LT8440 are connected to the front of the diode bridge. This connection position allows the LT8440 to sense the input voltage more accurately compared to the back of back of the diode bridge. However, in this configuration, a two-point failure scenario where LINEA/LINEB shorts to SHUNT and RTP, respectively, can form a leakage path from the input port to load the capacitor through LINEA/LINEB resistors. If the total capacitance on the load side is large, LINEA/LINEB pins should be connected to the back of the diode bridge by populating R10 and R13 and removing R6 and R9.

Differential Choke

A 220 μ H coupled inductor is used as the differential-mode choke L2 to isolate the signal from the DC power path. This inductance value is selected to preserve the signal integrity from the transceiver passing through the evaluation circuit. It meets the APL requirement of droop and return loss on the Ethernet signal. See the [Signal Droop](#) and [Return Loss](#) sections for more details.

Diodes are used to clamp the voltage surge across L2 caused by a large di/dt during a fault event. Because the ethernet signal voltage is 1.0V_{PP}, the total diode voltage drop must be higher than 1.0V to not interfere with normal communication. Therefore, the evaluation board is designed with three diodes in series to have sufficient voltage drop across the full temperature range. Also, there are two diode strings in parallel across each winding of the inductor for safety redundancy.

Signal Droop

To measure the EVAL-LT8440-AZ circuit's attenuation on the communication signal, the EVAL-ADIN1110/EVAL-ADIN1100 board is used to transmit a test signal into signal chain port J2. Ideally, the resulting signal from the EVAL-LT8440-AZ board is a square waveform. However, different factors, including the circuitry around the signal port, surge protection, and power coupling inductors, affect the high and low states of the waveform. As a result, there is a decay in the voltage level during the high and low times of the waveform. The measurement of this decay is called transmitter output droop and is specified in subclause 146.5.4.2 of the IEEE 802.3cg-2019 standard. The proper test setup for measuring the signal droop on the EVAL-LT8440-AZ board is illustrated in [Figure 2](#). The voltage droop measurement is defined as in equation (1):

$$Droop \% = 100\% \times \frac{V_{133.3} - V_{800}}{V_{133.3}} \quad (1)$$

Where $V_{133.3}$ and V_{800} are the voltages measured at 133.3ns and 800ns, respectively, after the zero crossing of the test waveform. Droop is defined both for the positive and negative portions of each cycle of the waveform, and both must be below 10%.

A 12V power source is applied to the input port to turn on the LT8440 ICs. Two 2mH inductors are added between the power source and the input port to inject power and mimic the inductance of the Ethernet cable and the switch-side power supply. The final test signal is measured across a 100 Ω in parallel with the input port as this voltage droop measurement requires a 100 Ω termination. A low capacitance differential probe such as the Tektronix IsoVu probe is recommended for measuring the droop. [Figure 16](#) shows the resulting waveform of the test signal, where the $V_{133.3}$ and V_{800} points corresponding to the positive droop measurement are indicated. The measured droop of the test signal is 8.87%, which meets the requirement.

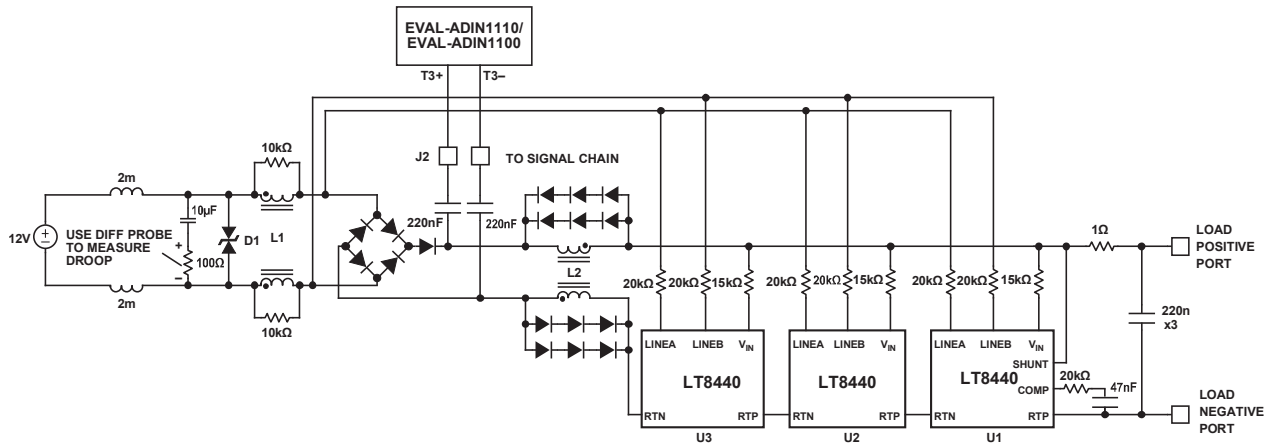


Figure 2. Signal Droop Test Setup

Return Loss

The medium-dependent interface (MDI) return loss is the ratio of the power of the differential signal reflected due to impedance mismatch to the power of the differential incident signal. The IEEE 802.3cg-2019 standard requires the MDI return loss to meet or exceed the limits shown in [Table 1](#) for all frequencies from 100kHz to 20MHz (with 100Ω ± 0.1% reference impedance) at all times while transmitting data or idle symbols.

Table 1. MDI Return Loss Specifications Based on IEEE 802.3cg-2019 Standards

Frequency Range	Limit in dB
$0.1\text{MHz} \leq f \leq 0.2\text{MHz}$	$20 - 18 \times \log_{10}\left(\frac{0.2}{f}\right)$
$0.2\text{MHz} \leq f \leq 1\text{MHz}$	20
$1\text{MHz} \leq f \leq 10\text{MHz}$	$20 - 16.7 \times \log_{10}(f)$
$10\text{MHz} \leq f \leq 20\text{MHz}$	$3.3 - 7.6 \times \log_{10}\left(\frac{f}{10}\right)$

The 10BASE-T1L transceiver ADIN1110/ADIN1100 is set to the transmit disable mode, where it transmits only 0 symbols to the signal chain port J2 on the EVAL-LT8440-AZ board. This mode keeps both transmit and receive paths in the normal operation of the transceiver, complying with subclause 45.2.1.186a.2 of the IEEE 802.3cg-2019 standard. The signal is measured by the vector network analyzer Bode 100 at the input terminal to analyze the return loss on the evaluation board. The test setup for measuring the return loss is demonstrated in [Figure 3](#). The measured return loss from the evaluation circuit exceeding the limits is shown in [Figure 17](#).

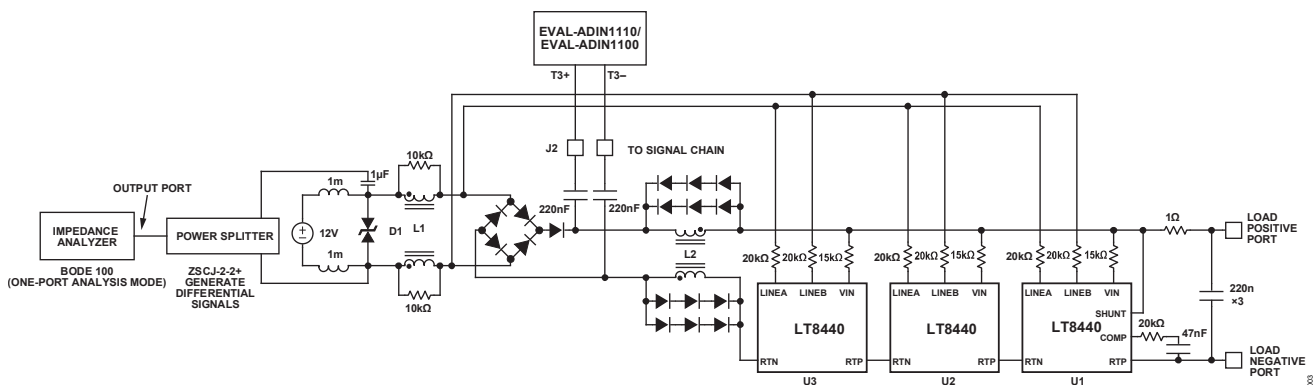


Figure 3. MDI Return Loss Test Setup

Compensation Values

The current shunt loop compensation network consists of R44, C9, and C10. These component values must be carefully optimized at different load conditions to stabilize the current shunt loop and compensate for the fast-changing load current. [Table 2](#) shows the choice of compensation for certain output capacitor Cload values. A practical approach is to start from a similar condition in the table and tune the compensation until the performance is optimized. The LTspice® model can be used to simulate various compensation values for quick estimation. Stability should then be checked across all operating conditions, including load current, input voltage, and temperature.

Table 2. Recommended Compensation Values

C _{LOAD}	R5	L _{SOURCE}	L2	R44	C9	C10
660nF	1Ω	0mH~4mH	220μH	20kΩ	47nF	Open
6.6μF	1Ω			62kΩ	22nF	Open
	10Ω			470kΩ	2.2nF	Open
100μF	1Ω			470kΩ	4.7nF	Open

PCB Layout Recommendation

Care must be taken in designing the Printed Circuit Board (PCB) layout to ensure good thermal dissipation of the LT8440 and compliance with the intrinsic safety standard IEC60079-11. Be aware that the EVAL-LT8440-AZ board is not certified for intrinsic safety, but the layout is designed to meet most of the protection level “ia” requirements. Customers can use this design as a reference and adjust it as needed with extra attention to guarantee that the designed circuit board is intrinsically safe.

According to IEC60079-11 Ed. 7.0 Table 7, with peak voltage of 10V ~ 30V, level ia/ib protection requires $\geq 2\text{mm}$ conductor separation without coating, or $\geq 0.7\text{mm}$ clearance with coating. Due to the limit of SOIC pin spacing, the LT8440 needs to be at least coated (or potted) on the application circuit board, to be able to treat the pin shorts as countable faults. The evaluation board EVAL-LT8440-AZ has at least 0.7mm clearance between traces and components, but it is not coated to ensure the circuit's ease of evaluation and modification. For other requirements on the PCB layout, refer to the IEC60079-11 standard for more details.

Typical Performance Characteristics

($T_A = 25^\circ\text{C}$, unless otherwise noted)

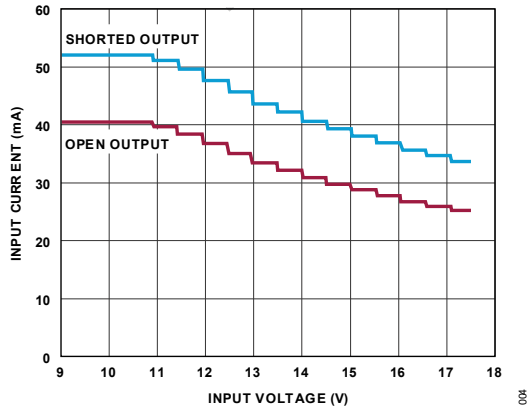


Figure 4. Input Voltage vs. Input Current

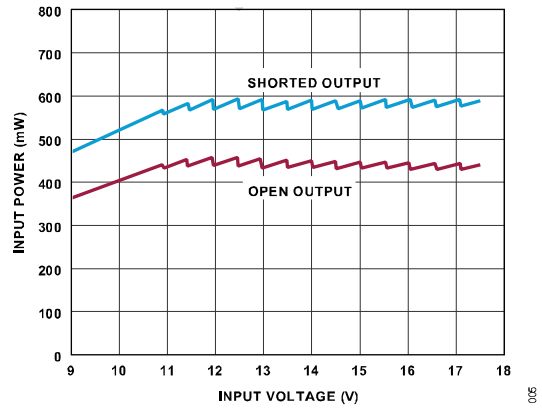


Figure 5. Input Voltage vs. Input Power

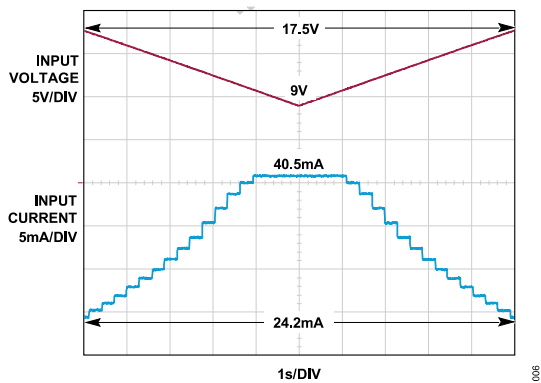


Figure 6. Input Voltage Sweep with Open Output

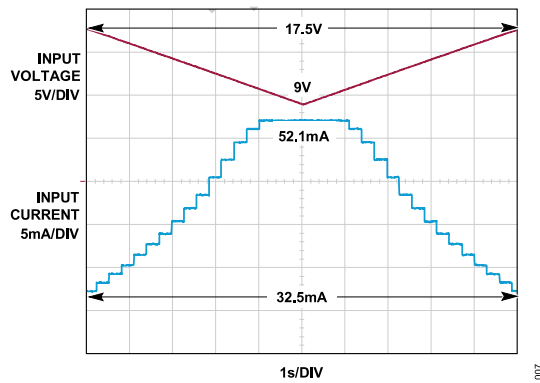


Figure 7. Input Voltage Sweep with Shorted Output

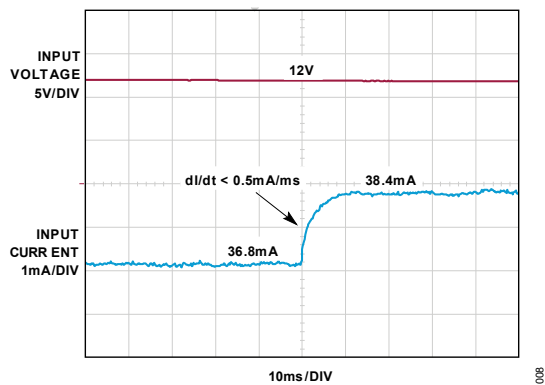


Figure 8. Zoom-In of Current Step Up with Open Output

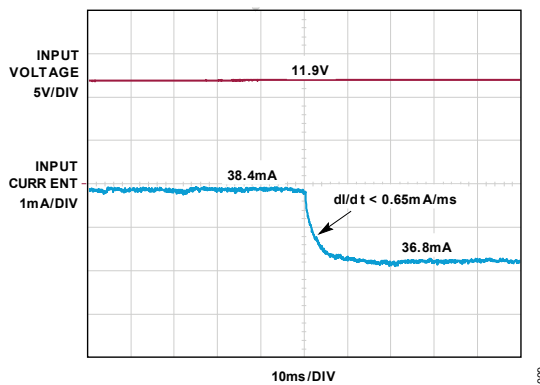


Figure 9. Zoom-In of Current Step Down with Open Output

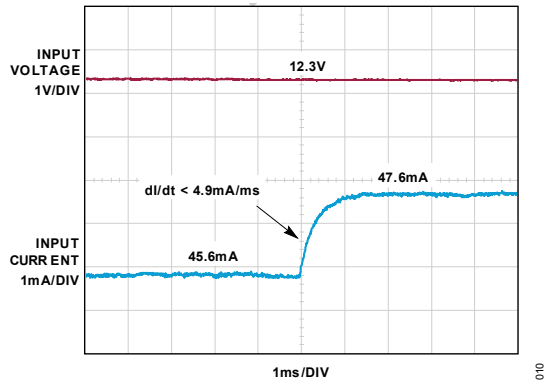


Figure 10. Zoom-In of Current Step Up with Shorted Output

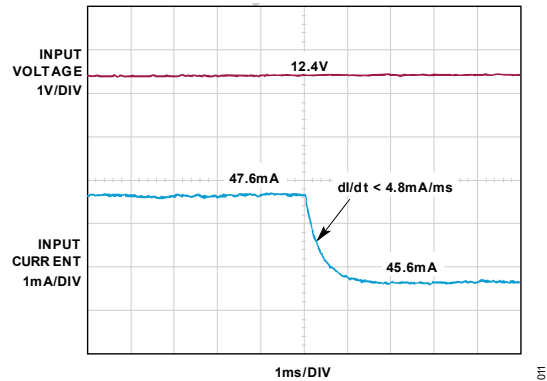


Figure 11. Zoom-In of Current Step Down with Shorted Output

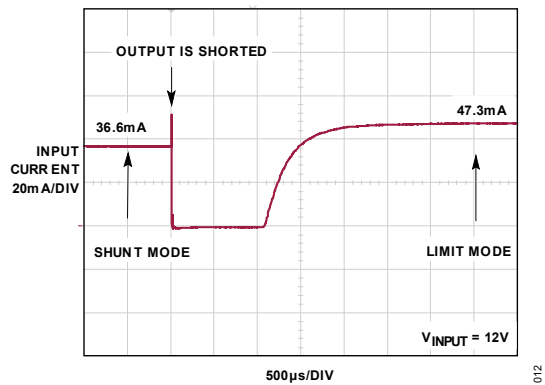


Figure 12. Short-Circuit Protection

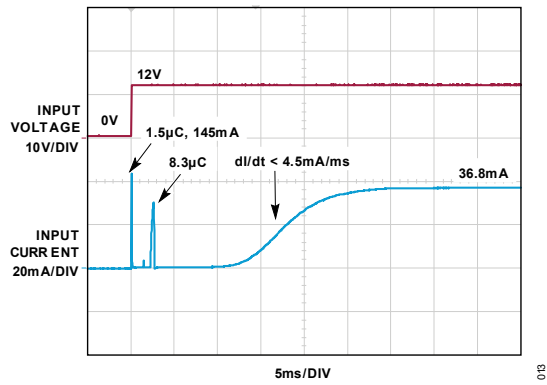


Figure 13. Hot Input Connection

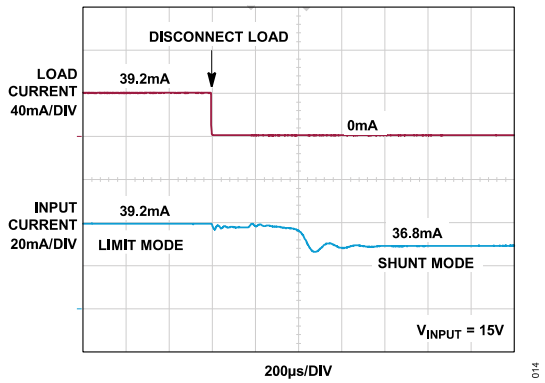


Figure 14. Transition From Current Limit Mode to Current Shunt Mode

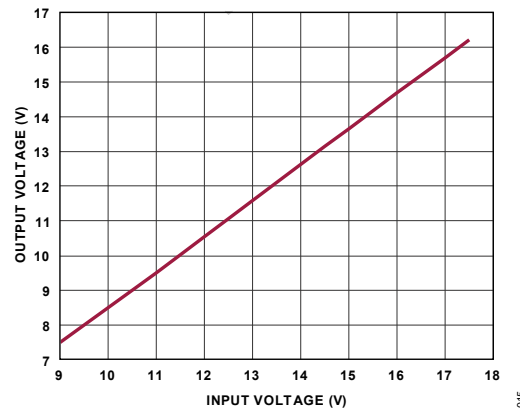


Figure 15. Input Voltage vs. Output Voltage with Open Output

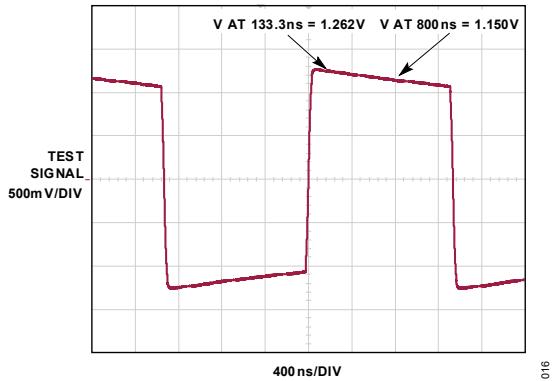


Figure 16. Measured Signal Droop

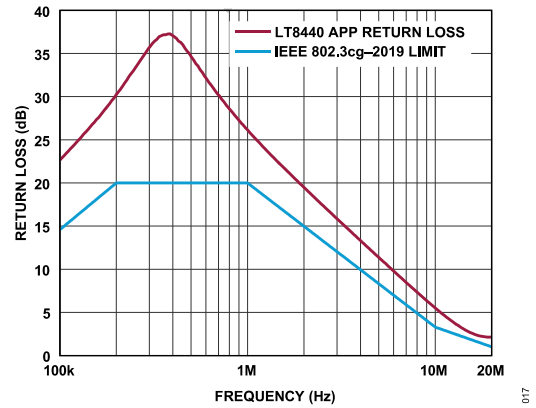


Figure 17. MDI Return Loss

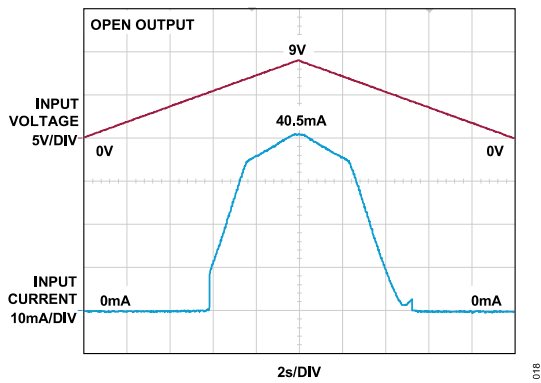


Figure 18. Undervoltage Input Sweep with Open Output

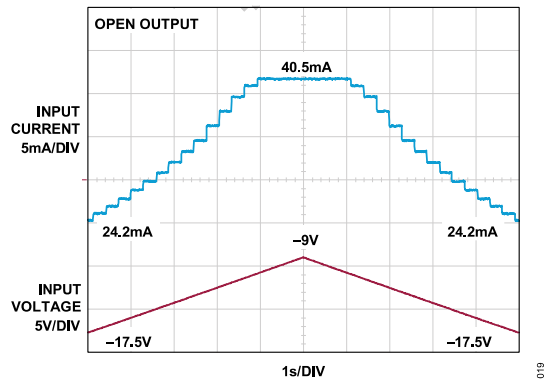


Figure 19. Reversed Input Voltage Sweep with Open Output

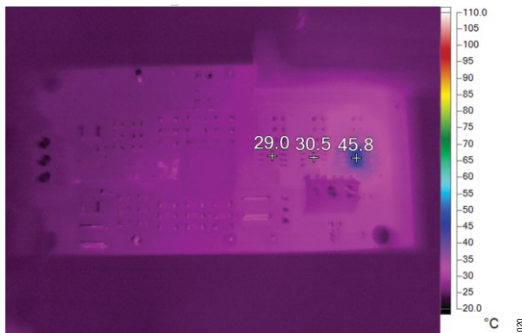


Figure 20. Thermal Image of Top Layer at $V_{INPUT} = 12V$, Open Output

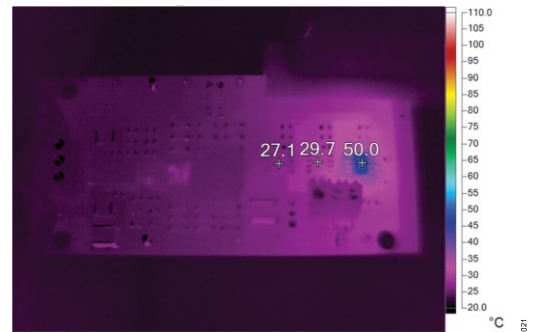


Figure 21. Thermal Image of Top Layer at $V_{INPUT} = 12V$, Shorted Output

Bill of Materials

ITEM	QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	3	C1, C6, C8	CAP., CER., 0.22 μ F, 50V, 10%, X7R, 0805, LOW ESR	TDK, C2012X7R1H224K125AA
2	2	C2, C3	CAP., CER., 47pF, 3000V, 5%, C0G, 1812, HIGH VOLTAGE, LOW ESL	KEMET, C1812C470JHGAC7800
3	2	C4, C5	CAP., CER., 0.22 μ F, 100V, 10%, X7S, 0603, AEC-Q200	TAIYO YUDEN, HMK107C7224KAHTE
4	1	C9	CAP., CER., 0.047 μ F, 50V, 10%, X7R, 0603, AEC-Q200	KEMET, C0603X473K5RACTU
5	1	D1	TVS DIODE, BIDIRECTIONAL, 26V, 400W, AEC-Q101	ST MICROELECTRONICS, SM4T30CAY
6	12	D8, D9, D12-D15, D18-D20, D23-D25	DIO., GEN. PURPOSE RECTIFIER, 50V, 1A	ONSEMI, S1AFL
7	5	D2, D3, D5-D7	DIO., SCHOTTKY, 40V, 0.75A, SOD-323, AEC-Q101	INFINEON TECHNOLOGIES, BAT165E6327HTSA1
8	1	L1	IND., COMMON MODE CHOKE, 500 μ H, 3.3k Ω , 100kHz, 1A, 0.15 Ω , AEC-Q200	WURTH ELEKTRONIK, 744223
9	1	L2	IND., SHIELDED, COUPLED, 1.02A, 0.691 Ω DCR	COILCRAFT INC., MSD1260-224KLD
10	14	R1-R4, R7, R8, R15, R16, R19, R20, R27, R28, R31, R32	RES., SMD, 10k Ω , 1%, 1/2W, 0805, AEC-Q200	VISHAY, CRCW080510K0FKEAHP
11	6	R11, R12, R23, R24, R35, R36	RES., SMD, 7.5k Ω , 1%, 1/10W, 0805	TE CONNECTIVITY, CPF0805B7K5E1
12	1	R44	RES., SMD, 20k Ω , 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ-3EKF2002V
13	1	R5	RES., SMD, 1 Ω , 1%, 1/8W, 0805, AEC-Q200	VISHAY, CRCW08051R00FKEA
14	3	U1, U2, U3	IC-ADI POWER CONDITIONER FOR APL FIELD DEVICES	ANALOG DEVICES, LT8440RS8E#PBF
OPTIONAL CIRCUIT COMPONENTS				
1	0	C10-C13	CAP., OPTION, 0603	
2	0	R10, R13	RES., SMD, 0 Ω , 1/8W, 0805, AEC-Q200	PANASONIC, ERJ-6GEY0R00V
3	5	R6, R9, R39-R41	RES., SMD, 0 Ω , 1/8W, 0805, AEC-Q200	PANASONIC, ERJ-6GEY0R00V
4	6	D10, D11, D16, D17, D21, D22	DIO., GEN. PURPOSE RECTIFIER, 50V, 1A	ONSEMI, S1AFL
HARDWARE – FOR DEMO BOARD ONLY				
1	2	J1, J3	CONN-PCB, 3POS, EUROSTYLE, TERM, BLK., HDR, 3.81MM PITCH	TE CONNECTIVITY, 284392-3
2	1	J2	CONN-PCB, HEADER 2 POS	SAMTEC, TSW-102-08-G-S
3	9	TP1-TP9	CONN-PCB, TEST POINT, YELLOW	KEYSTONE ELECTRONICS, 5004
4	2	TP10, TP11	CONN-PCB, SOLDER TERMINAL TURRETS FOR CLIP LEADS	MILL-MAX, 2308-2-00-80-00-00-07-0
5	4	MP1-MP4	STANDOFF, BRD. SPT. SNAP FIT 9.53MM LENGTH, EVAL BOARD MTG	KEYSTONE, 8832

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	07/24	Initial release	—

Notes

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