Evaluating the LT3077 3 A, Ultra-Low Noise, High PSRR, 85 mV Dropout Ultra-Fast Linear Regulator

FEATURES

- Input voltage range: 0.6 V to 5.5 V
- BIAS voltage range: 2.375 V to 5.5 V
- Jumpers program output voltage according to selection matrix: 0.5 V to 4.2 V
- Maximum output current: 3 A
- BNC connectors for noise and PSRR measurement
- Jumper and resistor combinations select either 3.72 A or 1.5 A output current limit or disable the programmed current limit
- Jumper turns the regulator on or off
- Terminal provides output regulation status monitoring
- Banana jacks minimize V_{IN} and V_{OUT} connection voltage drops
- VO+, VO-, and VI+ terminals for regulation and dropout monitoring
- 18-Lead (3mm × 3mm) LFCSP-RT Package

EVALUATION KIT CONTENTS

- EVAL-LT3077-AZ evaluation board

EQUIPMENT NEEDED

- DC power supplies
- Multimeters for voltage and current measurements
- Electronic or resistive load

DOCUMENTS NEEDED

- LT3077 datasheet

EVALUATION BOARD PHOTOGRAPH

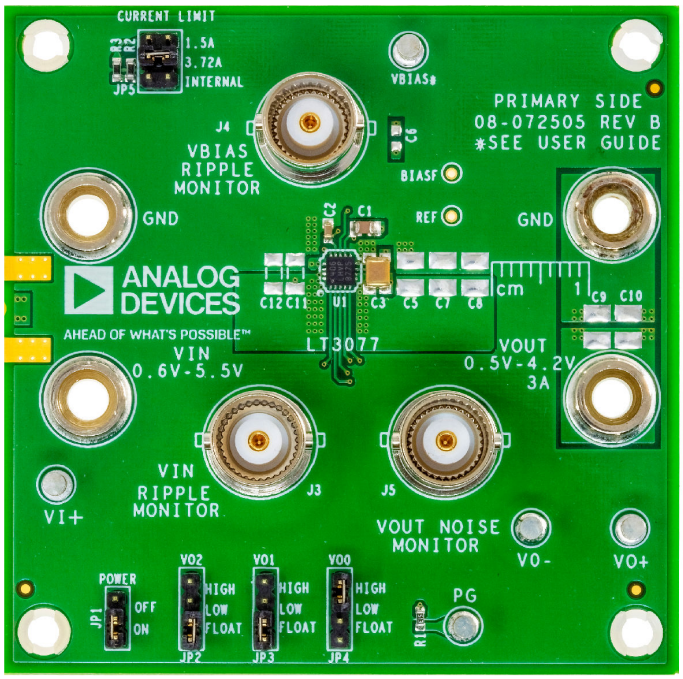

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Figure 1. Evaluation Board Photograph

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REVISION HISTORY

8/2024—Revision 0: Initial Version

GENERAL DESCRIPTION

The EVAL-LT3077-AZ evaluation board features the LT3077, a 3 A, ultra-low noise, high power-supply rejection ratio (PSRR), and 85 mV dropout ultra-fast linear regulator. The input voltage (V_{IN}) range for the V_{IN} power is from 0.6 V to 5.5 V. There are jumpers to set a 3-bit trilevel code that determines the output voltage (V_{OUT}) at pre-programmed levels that range from 0.5 V to 4.2 V. The maximum output current is 3 A. The EVAL-LT3077-AZ requires an external BIAS voltage (V_{BIAS}) that is at least 1.2 V higher than V_{OUT} and is between 2.375 V and 5.5 V.

The LT3077 of the EVAL-LT3077-AZ requires few external components, therefore, simplifying circuit design. External component choice, along with careful printed circuit board (PCB) design, helps optimize noise, PSRR, load transient response, and V_{OUT} regulation performance. The LT3077 requires capacitors for the internal reference, power input, BIASF pin, and power output. The internal reference is bypassed with a 16 V, 0805 sized, 4.7 µF capacitor to reduce output noise and program the soft-start. Larger capacitor case sizes and higher voltage ratings decrease 1/f noise for otherwise comparable capacitors. The 22 µF capacitor at the circuit output was chosen for high-frequency PSRR performance and to minimize V_{OUT} deviation during load transients.

The capacitor that bypasses the V_{IN} power for the LT3077 and the corresponding V_{IN} PCB layout can affect PSRR (see the Best PSRR Performance: PCB Layout for Input Traces section for additional information). The EVAL-LT3077-AZ decouples the V_{IN} power with a 47 µF capacitor. Less V_{IN} capacitance can improve PSRR at high frequencies (Refer to the LT3077 data sheet for the minimum capacitor value required for V_{IN}). Note that a bulk 220 µF tantalum polymer capacitor further reduces V_{IN} variation during load transients and reduces input voltage ringing that can be caused by inductive input power leads. The PCB has a footprint for an optional Subminiature Version A (SMA) connector that allows a shielded V_{IN} power connection to the PCB edge, if required.

The EVAL-LT3077-AZ bypasses the BIASF pin with a 2.2 µF capacitor instead of the V_{BIAS} supply input. Because the BIASF pin is isolated from V_{BIAS} by a resistance that is internal to the LT3077, there is less PSRR degradation when BIASF is bypassed compared to when V_{BIAS} is bypassed. Otherwise, the effect on PSRR of the V_{IN} and V_{BIAS} bypass capacitors is similar.

The EVAL-LT3077-AZ has resistors that allow a CURRENT LIMIT jumper to select output current limits of either 1.5 A or 3.72 A. The CURRENT LIMIT jumper can also disable external current-limit programming by shorting the ILIM pin to ground.

A POWER jumper (JP1) is available on the EVAL-LT3077-AZ to either connect the EN pin to V_{BIAS} to turn the output on or to ground to disable the output. There is a PG terminal that is pulled up to V_{BIAS} by a 51 kΩ resistor and pulled down by the open-drain, negative channel metal-oxide-semiconductor (NMOS) PG pin output for indication of regulator output status and other fault modes.

Banana jacks minimize voltage drops on V_{IN} and V_{OUT} connections. Bayonet Neill-Concelman (BNC) connectors provide low-noise connections to power V_{IN}, V_{BIAS}, and V_{OUT}. The EVAL-LT3077-AZ PCB design uses a split capacitor technique to Kelvin connect the ground terminal of the REF capacitor to the ground terminal of the output capacitor, and the SENSE pin to the positive terminal of the output capacitor. The VO+, VO −, and VI+ terminals Kelvin connect to V_{IN} and V_{OUT} and are the optimum place to observe output voltage regulation and dropout voltage performance. There are test points for BIASF and REF voltages.

The EVAL-LT3077-AZ has placeholders identified on the schematic as optional DNI components that make it convenient to add capacitance (see Figure 8).

For full details on the LT3077, refer to the LT3077 datasheet, which must be consulted with this user guide when using the EVAL-LT3077-AZ evaluation board.

The LT3077 of the EVAL-LT3077-AZ features an 18-Lead (3mm × 3mm) LFCSP-RT package. Proper board layout is essential for maximum thermal performance.

Design files are available on the EVAL-LT3077-AZ evaluation board page.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Table 1. Performance Summary

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE	V_{IN}					
Minimum					0.6	V
Maximum		I_{OUT} = 300 mA	5.5			V
		V_{OUT} = 1.5 V, I_{OUT} = 3 A	2[1]			V
BIAS VOLTAGE	V_{BIAS}					
Minimum		$V_{BIAS} \geq V_{OUT}$ + 1.2 V			2.375	V
Maximum			5.5			V
OUTPUT VOLTAGE	V_{OUT}	V_{OUT} = 0.5 V, 50 mA ≤ I_{OUT} ≤ 3 A, V_{IN} = 0.8 V	0.492	0.500	0.508	V
		V_{OUT} = 1.2 V, 10 mA ≤ I_{OUT} ≤ 3 A, V_{IN} = 1.5 V	1.182	1.200	1.218	V
		V_{OUT} = 3.3 V, 10 mA ≤ I_{OUT} ≤ 3 A, V_{IN} = 3.6 V	3.250	3.300	3.350	V
		V_{OUT} = 4.2 V, 10 mA ≤ I_{OUT} ≤ 3 A, V_{IN} = 4.5 V	4.137	4.200	4.263	V
OUTPUT CURRENT	I_{OUT}					
Maximum			3			A
Minimum		V_{OUT} < 0.8 V			50	mA
		V_{OUT} ≥ 0.8 V			10	mA
Limit[2]		ILIM resistor (R_{ILIM}) = 2 kΩ (1.5 A jumper position)	1.41	1.50	1.59	A
		R_{ILIM} = 806 Ω (3.72 A jumper position)	3.61	3.72	3.83	A
BIAS PIN NAP MODE CURRENT	I_{BIAS_NAP}	V_{BIAS} = 5.5 V, EN = 0 V, R1 = open			10	µA
IN PIN NAP MODE CURRENT	I_{IN_NAP}	V_{IN} = 5.5 V, EN = 0 V			500	µA

[1] The maximum power dissipation and, consequently, the maximum input voltage for an output that is programmed to 1 V with a 3 A load is set by the 60°C temperature rise of the LT3077 on the evaluation board. Higher input voltages can be reached if larger copper area or forced-air cooling is applied. In addition, consider the effect of ambient temperature and the maximum junction temperature that may occur. Refer to the LT3077 data sheet for more information.

[2] The output current limit that occurs will be the lower of either the programmable current limit or the internal current limit. The internal current limit can be less than the programmable current limit for some conditions, such as high V_{BIAS} and high temperature. Refer to the LT3077 data sheet for more information.

QUICK START PROCEDURE

To use the EVAL-LT3077-AZ to evaluate the performance of the LT3077, see Figure 2 for the proper measurement equipment setup and take the following steps:

1. With the input supplies and load off and turned down, make all the connections as shown in Figure 2. Ensure that the VO2, VO1, and VO0 jumpers to set V_{OUT} are in the proper positions for the desired V_{OUT} according to the V_{OUT} selection matrix table in the LT3077 datasheet. In addition, ensure that the POWER jumper (JP1) is in the **ON** position, and that the CURRENT LIMIT jumper (JP5) is in the 3.72 A position.
2. Turn on the input and bias supplies and increase the input supply so it is at least 200 mV above the programmed output voltage. Adjust V_{BIAS} so that it is between 2.375 V and 5.5 V and at least 1.2 V higher than the programmed V_{OUT} for proper operation. Note that when setting the input and bias voltages, a V_{IN} or V_{BIAS} that is too close to the programmed V_{OUT} (too low) can cause dropout operation and a loss of V_{OUT} regulation. Also, a V_{IN} that is too high above the output can increase power dissipation to an unacceptable level.
3. Increase the load to the desired I_{OUT}. Readjust the input supply to be at least 200 mV above the programmed output voltage. Verify that V_{OUT} is the expected voltage programmed by the jumpers. Note that if the V_{OUT} is lower than expected, the load may be set too high. Temporarily disconnect the load to ensure that it is not set too high.
4. When the proper V_{OUT} is established, adjust the input voltages and load within the operating ranges and observe the V_{OUT} regulation, load transient response, and other parameters.
5. Refer to Application Note AN83 and Application Note AN159 for measuring output noise and PSRR. Note that J3, J4, and J5 are BNC connectors that are used for noise and PSRR measurements.
6. Note that the CURRENT LIMIT jumper can additionally select a 1.5 A current limit or the INTERNAL current limit that the LT3077 provides.
7. Monitor power good at the PG terminal.

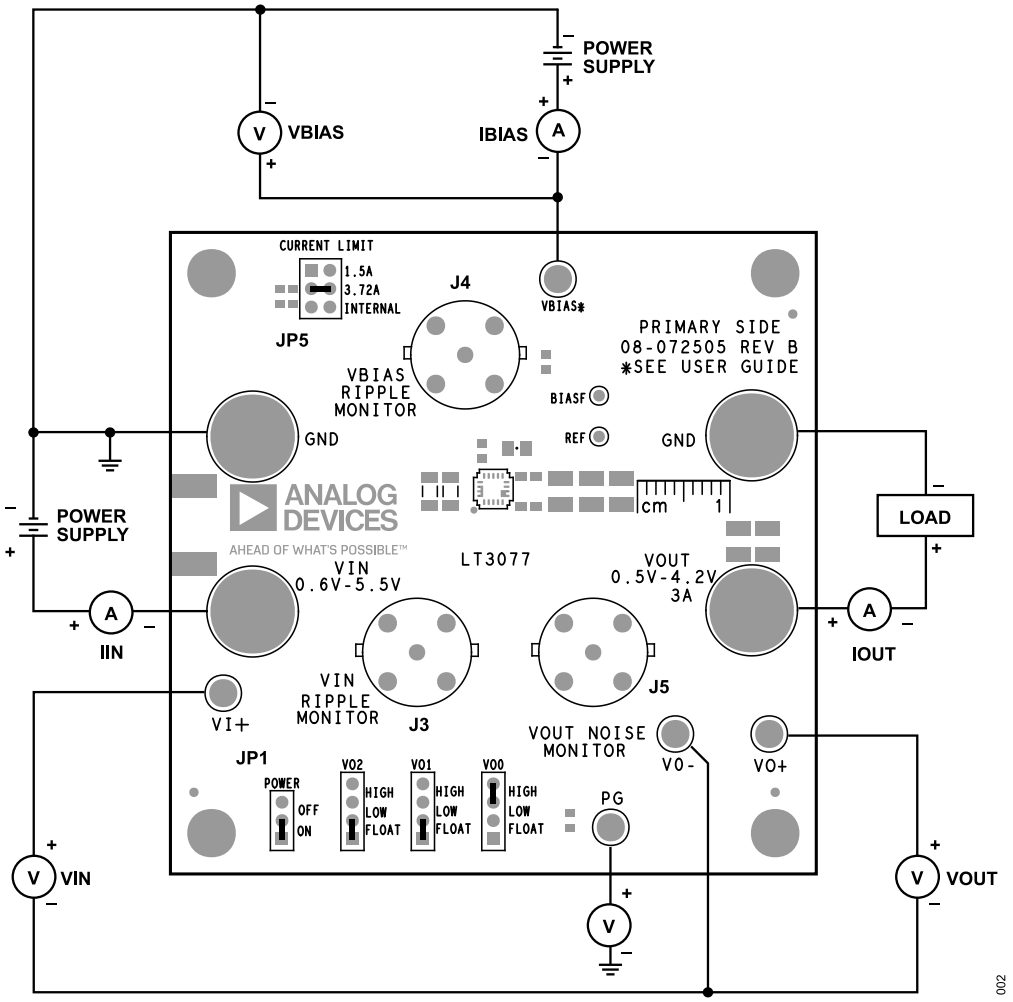

Figure 2. Proper Measurement Equipment Setup for the EVAL-LT3077-AZ

QUICK START PROCEDURE

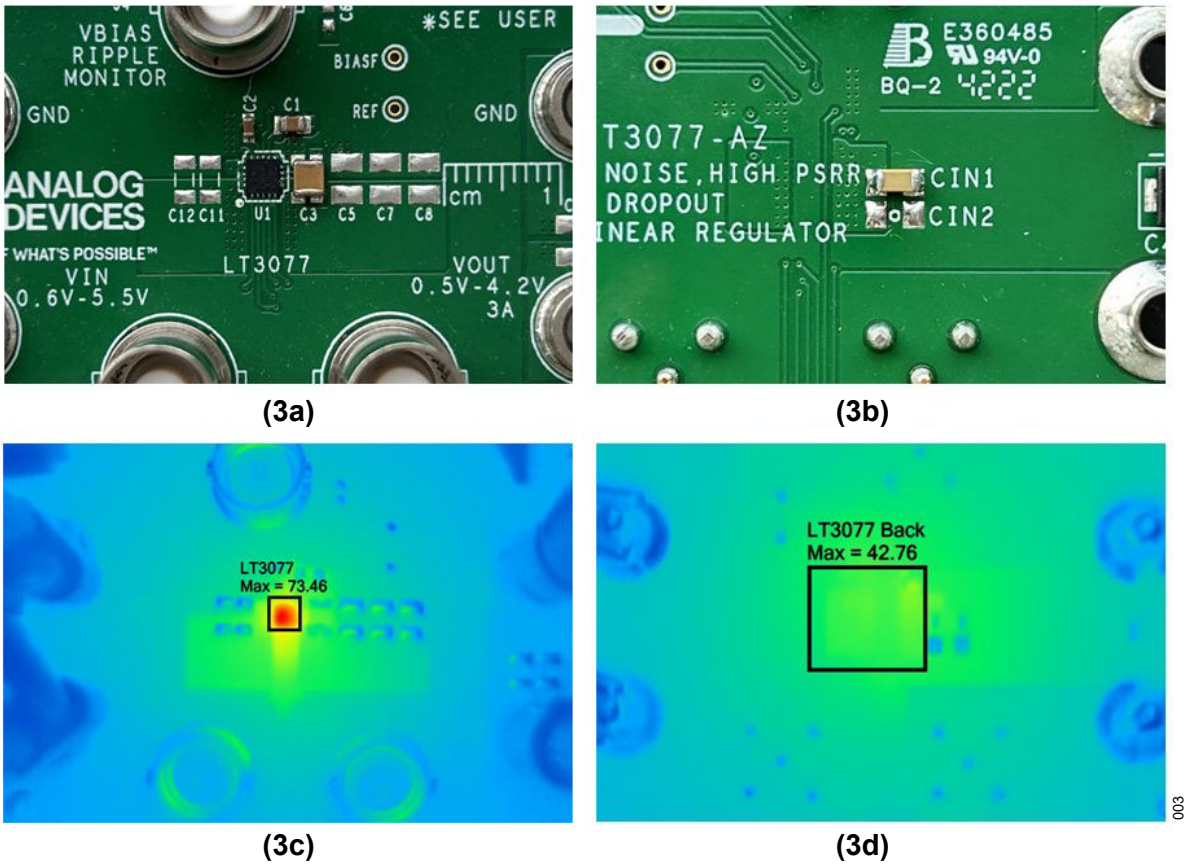

Figure 3. EVAL-LT3077-AZ Front Nonthermal (3a), Back Nonthermal (3b), Front Thermal (3c), and Back Thermal (3d) Images with 2 V_{IN}, 5 V_{BIAS}, and 1.5 V_{OUT} at 3 A, Vertical Orientation with No Forced Air

PRINTED CIRCUIT BOARD LAYOUT

BEST PSRR PERFORMANCE: PCB LAYOUT FOR INPUT TRACES

For applications using the LT3077 for post-regulating switching converters, placing a capacitor directly at the LT3077 input results in AC current (at the switching frequency) flowing near the LT3077. Without careful attention to the PCB layout, this relatively high-frequency switching current generates an electromagnetic field (EMF) that couples to the LT3077 output, degrading its effective PSRR. While highly dependent on the PCB, the switching preregulator, the input capacitor size, and among other factors, the PSRR can easily degrade at high frequencies. This degradation is present even if the LT3077 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional low PSRR low dropout (LDO) regulators, the high PSRR of the LT3077 requires careful attention to higher-order parasitics to realize the full performance offered by the regulator.

The EVAL-LT3077-AZ alleviates this degradation in PSRR by using a specialized layout technique. The V_{IN} input trace and its corresponding return path (GND) are highlighted in red in Figure 4 and Figure 5. Figure 5 also shows the location of the C1 input capacitor and the connection between the GND return path for the V_{IN} input trace and GND for the rest of the PCB. When an AC voltage is applied to the input of the EVAL-LT3077-AZ, AC current flows on the path formed through CIN1 by the input and the ground traces. Without the proper PCB layout, the AC current that flows on this path can generate EMFs that do not completely cancel and couple to the C3 output capacitor and related traces, making the PSRR appear worse than it actually is. With the input trace directly above the return path, the EMFs are in opposite directions, and consequently, cancel each other out. Ensure that these traces exactly overlap each other to maximize the cancellation effect and thus provide the maximum PSRR offered by the regulator.

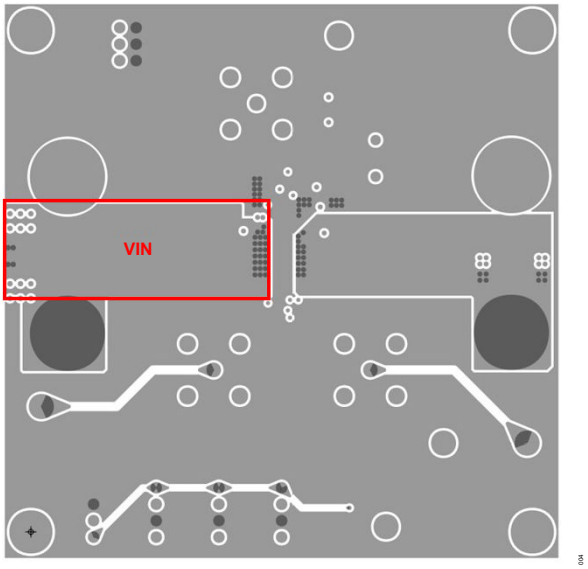

Figure 4. Layer 3 of EVAL-LT3077-AZ

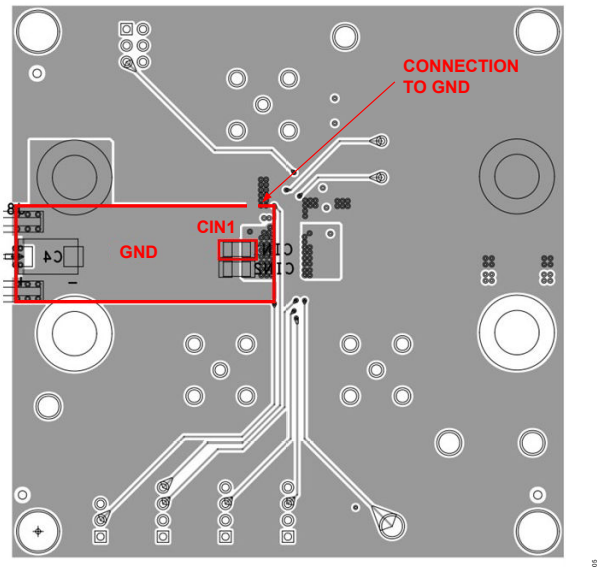

Figure 5. Layer 4 of EVAL-LT3077-AZ

PRINTED CIRCUIT BOARD LAYOUT

PCB LAYOUT FOR THE C3 OUTPUT CAPACITOR

As previously mentioned, the EVAL-LT3077-AZ PCB design uses a split-capacitor technique to Kelvin connect the ground terminal of the REF capacitor to the ground terminal of the C3 output capacitor and the SENSE pin to the positive terminal of the output capacitor (see Figure 6 and Figure 7). This Kelvin connection regulates the output voltage at the output capacitor, which in turn, optimizes noise, PSRR, load transient, and regulation performance that is all measured at the output capacitor. The split-capacitor technique is useful in this case because it makes it possible to relocate the regulation point, if desired. Regulation of the output voltage at a new location requires leaving the C3 output-capacitor location open and wiring the split-capacitor pads corresponding to the REF capacitor ground terminal and SENSE to the new output capacitor location. Additional capacitance located from SENSE to the REF ground between the regulation point and the LT3077 decreases stability. The split-capacitor technique itself does not enhance LT3077 stability because of the type of pass transistor, even though the unity-gain bandwidth of the LT3077 bandwidth is relatively high and close to the self-resonance frequency of the output capacitor.

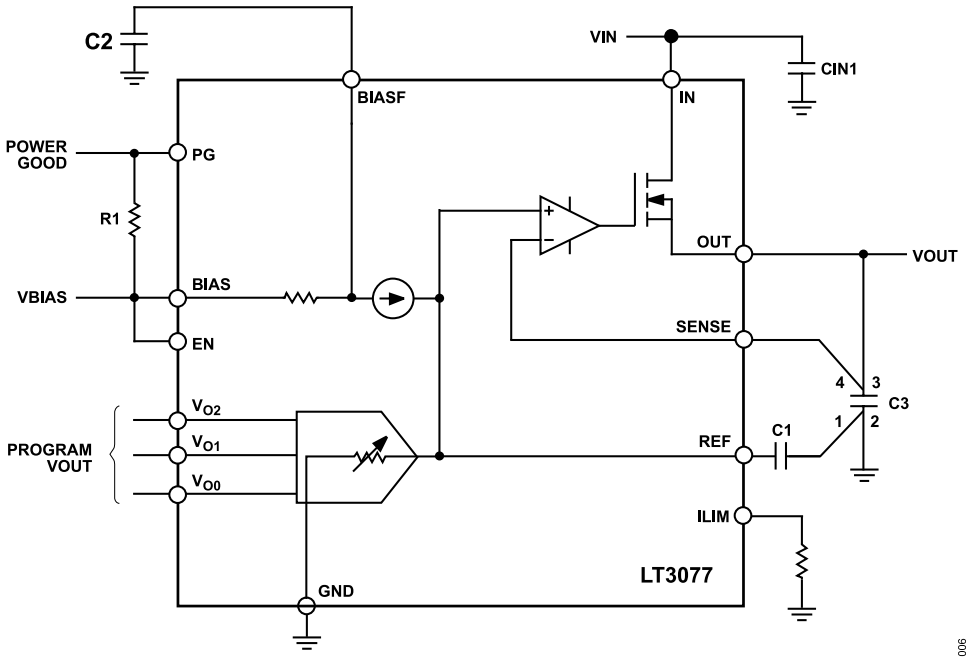

Figure 6. REF Capacitor C1 and Output Capacitor C3 Connections for Best Noise, PSRR, Load Transient, and Regulation Performance

PRINTED CIRCUIT BOARD LAYOUT

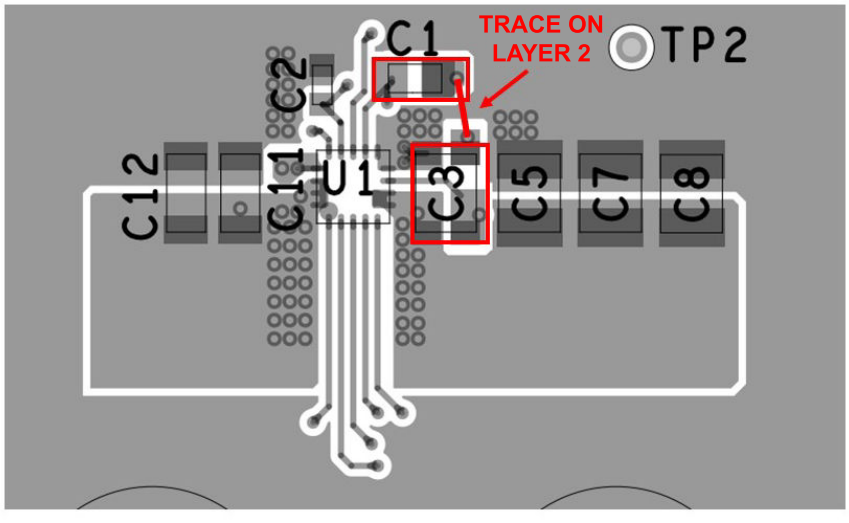

Figure 7. Split Pads for the C3 Output Capacitor on the Top Layer of EVAL-LT3077-AZ. Connect the Ground Terminal of the REF Capacitor to the Ground Terminal of the C3 Output Capacitor, and the SENSE Pin to the Positive Terminal of the Output Capacitor

EVALUATION BOARD SCHEMATIC

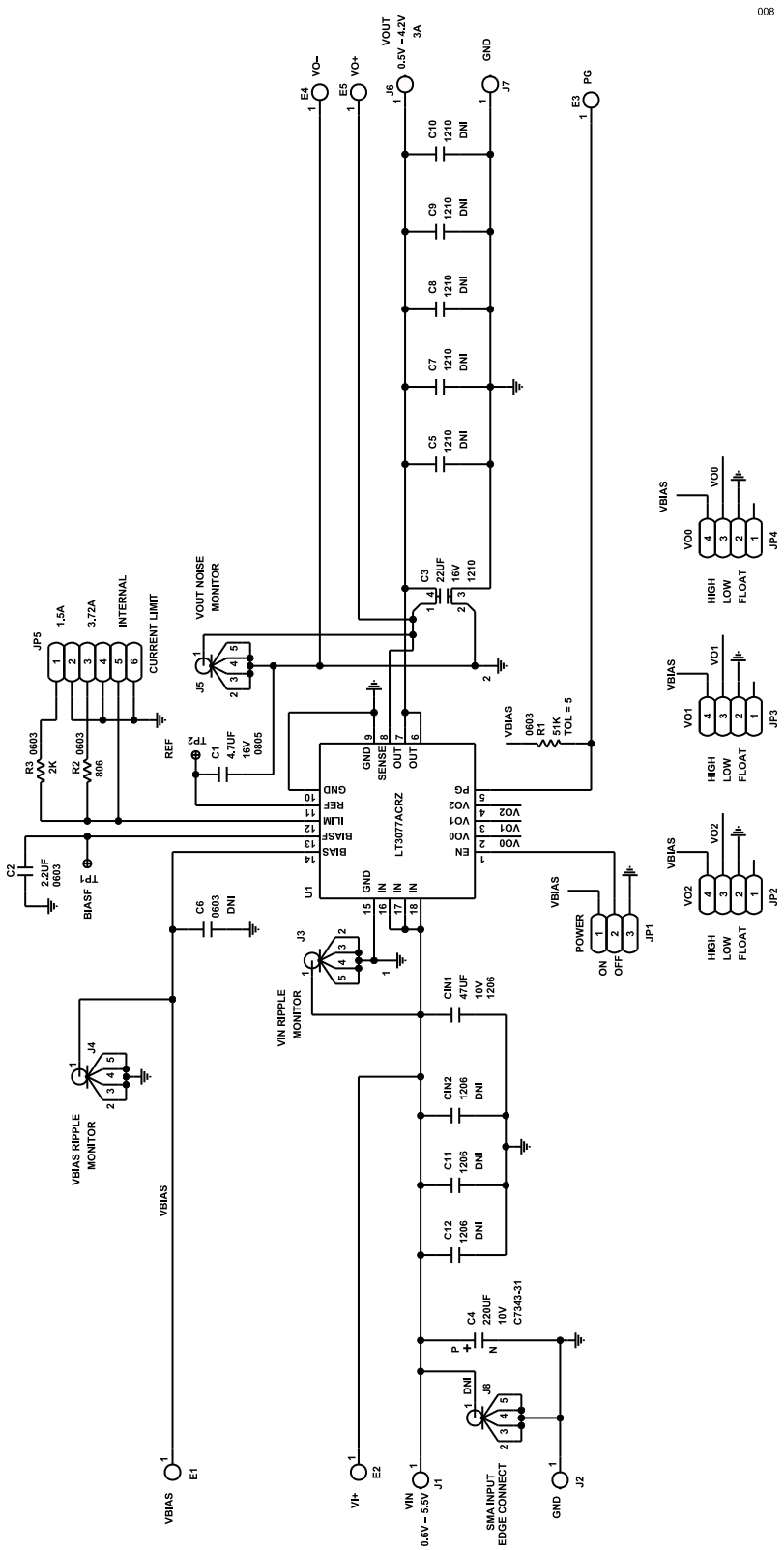

Figure 8. Evaluation Board Schematic

ORDERING INFORMATION

Table 2. Bill of Materials

Item	Quantity[1]	Reference Designator	Part Description	Manufacturer, Part Number
Required Circuit Components				
1	1	C1	4.7 µF capacitor, X7R, 16 V, 10%, 0805, soft termination	Murata, GCJ21BR71C475KA01L
2	1	C2	2.2 µF capacitor, X7R, 10 V, 10%, 0603	Murata, GRM188R71A225KE15D
3	1	C3	22 µF capacitor, X7R, 16 V, 10%, 1210, AECQ200	Murata, GCM32ER71C226KE19L
4	1	CIN1	47 µF capacitor, X5R, 10 V, 10%, 1206	Murata, GRM31CR61A476KE15L
5	1	U1	3 A, ultra-low noise, high PSRR, 85 mV dropout, ultra-fast linear regulator	Analog Devices, Inc., LT3077ACRZ
Optional Evaluation Board Components				
1	1	C4	220 µF capacitor, tantalum polymer, 10 V, 20%,7343-31, 40 mΩ ESR	AVX, TCJD227M010R0040
2		C5, C7, C8, C9, C10	Capacitors, 1210, optional	Optional
3		C11, C12, CIN2	Capacitors, 1206, optional	Optional
4		C6	Capacitors, 0603, optional	Optional
5	1	R1	51 kΩ resistor, 5%, 1/10 W, 0603, AEC-Q200	Panasonic, ERJ-3GEYJ513V
6	1	R2	806 Ω resistor, 1%, 1/10 W, 0603, AEC-Q200	Panasonic, ERJ-3EKF8060V
7	1	R3	2 kΩ resistor, 1%, 1/10 W, 0603, AEC-Q200	Panasonic, ERJ-3EKF2001V
Hardware				
1	5	E1, E2, E3, E4, E5	Test points, turret, 0.094"	Mill-Max,2501-2-00-80-00-00-07-0
2	4	J1, J2, J6, J7	Connectors, banana jack, female, through-hole,non-insulated, swage, 0.218"	Keystone, 575-4
3	3	J3, J4, J5	Connectors, RF, BNC, receptacle, jack, 5-pin,straight, through-hole, 50 Ω	Amphenol RF, 112404
4		J8	Connector, SMA jack, female, 50 Ω board edge,end launch solder tab, optional	Optional
5	1	JP1	Connector, header, male, 1 x 3, 0.079", through-hole	Würth Elektronik, 62000311121
6	3	JP2, JP3, JP4	Connector, header, male, 1 x 4, 0.079", through-hole	Würth Elektronik, 62000411121
7	1	JP5	Connector, header, male, 2 x 3, 0.079", through-hole	Würth Elektronik, 62000621121
8	4	MP1 to MP4	Standoff, nylon, snap fit, 0.500"	Würth Elektronik, 702935000
9	5	XJP1 to XJP5	Connector shunt, female, 2-position, 0.079"	Würth Elektronik, 60800213421

[1] Blank cell is for optional components.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.