Evaluating the LT3074 3A, Ultralow Noise, High PSRR, 45mV Dropout Ultrafast Linear Regulator with PMBus

FEATURES

- Input voltage range: 0.6V to 5.5V
- BIAS voltage range: 2.375V to 5.5V
- Maximum output current: 3A
- I^2C/PMBus communication
- Jumper selects bias mode of either external bias voltage or 3.3V internal logic power from the PMBus interface
- Output voltage is precisely programmed to 1.20V by two 1% resistors in series
- BNC connectors for noise and PSRR measurement
- Component placeholder can connect the PGFB pin directly to BIASAF to keep PG high
- Operates standalone without PMBus programming
- Jumper turns regulator on or off
- Jumper enables or disables the internal clocks of LT3074 for noise performance verification
- Jumper and resistor combinations select the serial bus interface address
- Stacking connectors allow PMBus communication to multiple EVAL-LT3074-AZ
- 6-pin 0.1 inch pitch connector implements Pmod Type 6 I^2C
- LED indication of POWER ON, POWER GOOD and PMBus ALERT
- Terminals provide output current and output regulation status monitoring
- The VIOC pin of the LT3074 manages power dissipation and PSRR
- Banana jacks minimize V_{IN} and V_{OUT} connection voltage drops
- VO+, VO−, and VI+ terminals for regulation and dropout monitoring
- Component footprint for an SMA connector that allows a shielded V_{IN} power connection
- 22-lead (3mm x 4mm) LQFN package

EVALUATION KIT CONTENTS

- EVAL-LT3074-AZ evaluation board

EQUIPMENT NEEDED

- DC power supplies
- Multimeters for voltage and current measurements
- Electronic or resistive load

DOCUMENTS NEEDED

- LT3074 data sheet

ADDITIONAL HARDWARE NEEDED

- DC1613A (not included, order separately) (USB-to-PMBus controller for use with LTpowerPlay®)

SOFTWARE NEEDED

- LTpowerPlay® (Microsoft Windows-based development software (download from LTpowerPlay | Analog Devices))

EVALUATION BOARD PHOTOGRAPH

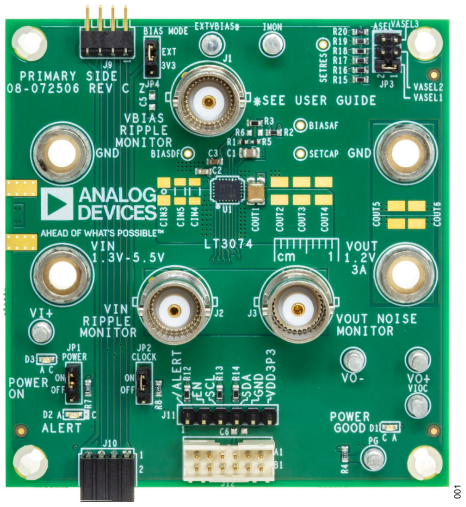

Figure 1. Evaluation Board Photograph

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REVISION HISTORY

10/2024—Revision 0: Initial Version

GENERAL DESCRIPTION

The EVAL-LT3074-AZ evaluation board features the LT3074, a 3A, ultralow noise, high power-supply rejection ratio (PSRR), 45mV dropout ultrafast linear regulator with PMBus capability. The input voltage (V_{IN}) range for the V_{IN} power is from 0.6V to 5.5V. The maximum output current is 3A. The output voltage is precisely programmed to 1.20V by two 1% resistors in series. The EVAL-LT3074-AZ requires a BIAS voltage (V_{BIAS}) that is at least 1.2V higher than V_{OUT} and is between 2.375V and 5.5V. There is a jumper (JP4), which gives an option to connect the BIAS pin to either an external bias voltage or the internal 3.3V logic power from the PMBus interface (discussed later in this section). The EVAL-LT3074-AZ can operate standalone without PMBus programming.

The LT3074 of the EVAL-LT3074-AZ requires few external components. Therefore, it simplifies circuit design. The external component choice and careful printed circuit board (PCB) design help optimize noise, PSRR, load transient response, and V_{OUT} regulation performance. The LT3074 requires capacitors for the internal reference, power input, BIASAF pin, BIASDF pin, and the power output. The internal reference is bypassed with a 16V, 0805-sized, 4.7µF capacitor, which is placed at the SETCAP pin, to reduce output noise and program the soft-start. Larger capacitor case sizes and higher voltage ratings decrease 1/f noise for otherwise comparable capacitors. The 22µF capacitor at the circuit output is chosen for high-frequency PSRR performance and to minimize V_{OUT} deviation during load transients.

The capacitor that bypasses the V_{IN} power for the LT3074 and the corresponding V_{IN} PCB layout can affect PSRR (see the Best PSRR Performance: PCB Layout for Input Traces section for additional information). The EVAL-LT3074-AZ decouples the V_{IN} power with a 47µF capacitor. Less V_{IN} capacitance can improve PSRR at high frequencies (refer to the LT3074 data sheet for the minimum capacitor value required for V_{IN}). Note that a bulk 220µF tantalum polymer capacitor further reduces V_{IN} variation during load transients and reduces input voltage ringing caused by inductive input power leads. The PCB has a footprint for an optional subminiature version A (SMA) connector that allows a shielded V_{IN} power connection to the PCB edge, if required.

The EVAL-LT3074-AZ bypasses the BIASAF pin with a 2.2µF capacitor and the BIASDF pin with a 0.47µF capacitor, instead of the V_{BIAS} supply input. Because the BIASAF and BIASDF pins are isolated from V_{BIAS} by a resistance internal to the LT3074, there is less PSRR degradation when BIASAF and BIASDF are bypassed compared to when V_{BIAS} is bypassed. A bypass capacitor at V_{BIAS} and the corresponding PCB layout input affects PSRR similar to the V_{IN} capacitor already discussed.

An IMON terminal is available for current monitoring. The IMON voltage is 1 V when the output current is 3A.

A POWER jumper (JP1) is available on the EVAL-LT3074-AZ to either connect the EN pin to V_{BIAS} to turn the output on or to ground to disable the output. EN assertion is also indicated by a green LED labeled POWER ON. There is a PG terminal pulled up to V_{BIAS} by a 51kΩ resistor and pulled down by the open-drain, negative channel metal-oxide semiconductor (NMOS) PG pin output to indicate regulator output status and other fault modes. PG assertion is also indicated by a green LED labeled PG. PGFB controls PG assertion and the PGFB pin monitors the output through a resistor divider, but there is also a component placeholder that can connect the PGFB pin directly to BIASAF to keep PG high. Note that PGFB programming does not affect fast start-up on the LT3074.

The voltage input-to-output control (VIOC) terminal allows connections for automatically controlling a preregulation voltage.

Banana jacks minimize voltage drops on V_{IN} and V_{OUT} connections. Bayonet Neill-Concelman (BNC) connectors provide low noise connections to power V_{IN}, V_{BIAS}, and V_{OUT}. The EVAL-LT3074-AZ PCB design uses a split capacitor technique to Kelvin connect the ground terminal of the SETCAP capacitor to the ground terminal of the output capacitor, and the SENSE pin to the positive terminal of the output capacitor. The VO+, VO−, and VI+ terminals Kelvin connect to V_{IN} and V_{OUT} and are the optimum place to observe output voltage regulation and dropout voltage performance. There are test points for BIASAF, BIASDF, and SETCAP voltages.

The EVAL-LT3074-AZ has placeholders identified on the schematic as optional DNI components, which make it convenient to add capacitance (see Evaluation Board Schematic).

The EVAL-LT3074-AZ supports PMBus communication for digital control, telemetry retrieval, and fault reporting. V_{OUT} margining is a control example, as are warn limit programming for output undercurrent, output overcurrent, input undervoltage, input overvoltage, output undervoltage, output overvoltage, BIAS undervoltage, BIAS overvoltage, and overtemperature. Examples of telemetry include input, output, and BIAS voltages in addition to output current and die temperature. There are many more other commands. Refer to the LT3074 data sheet for the full details of the available PMBus commands. There is a CLOCK jumper (JP2) to enable or disable the internal clocks of LT3074 for noise performance verification. An ASEL jumper (JP3) can also be used to select one of the three sequential resistor-programmed serial bus interface addresses. Additional addresses can be programmed by changing the resistors. A 12-pin connector (J12) is provided for interface to the DC1613A USB to the I^2C/SMBus/PMBus controller, and the EVAL-LT3074-AZ can be standalone programmed using DC1613A. ALERT_N assertion by the PMBus is also indicated by a red LED labeled ALERT. Connectors (J9, J10) are also present in the board to easily parallel EVAL-LT3074-AZ boards with the advantage of communicating simultaneously with multiple boards through I^2C/SMBus/PMBus. A 6-pin Pmod-type connector (J11) implements a Type 6 I^2C interface and is a 0.1 inch pitch header that allows the EVAL-LT3074-AZ to be used as a peripheral module by a wide range of embedded systems and development boards. The Pmod connector pins are labeled with the signal names. So, they can replace terminals.

Refer to the LT3074 data sheet for full details. Consult it with this user guide when using the EVAL-LT3074-AZ evaluation board. The

GENERAL DESCRIPTION

LT3074 of the EVAL-LT3074-AZ features a 22-lead, 3 mm x 4 mm LQFN package. Proper board layout is essential for maximum thermal performance.

Design files are available on the EVAL-LT3074-AZ evaluation board website page.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C, unless otherwise noted.

Table 1. Performance Summary

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE	V_{IN}	V_{OUT} = 1.2V				
Minimum					1.3	V
Maximum		I_{OUT} = 300mA	5.5			V
		I_{OUT} = 3A	1.7[1]			V
BIAS VOLTAGE	V_{BIAS}					
Minimum		$V_{BIAS} \geq V_{OUT}$ + 1.2V			2.375	V
Maximum			5.5			V
OUTPUT VOLTAGE	V_{OUT}	R1 = 10.5kΩ, R2 = 1.5kΩ, 10mA < I_{OUT} < 3A, V_{IN} = 1.5V	1.182	1.200	1.218	V
OUTPUT CURRENT	I_{OUT}					
Maximum			3			A
Minimum		V_{OUT} = 1.2V			10	mA
OUTPUT VOLTAGE WHEN PG IS INDICATED	$V_{OUT\_RISING\_PG}$	R1 = 10.5kΩ, R2 = 1.5kΩ, R3 = 383kΩ, R4 = 147kΩ, 10mA < I_{OUT} < 3A, V_{IN} = 1.5V, V_{OUT} Rising	1.06		1.10	V
BIAS PIN NAP MODE CURRENT	I_{BIAS_NAP}	V_{BIAS} = 5.5V, EN = 0V, R4 = Open			200	µA

[1] The maximum power dissipation and, consequently, the maximum input voltage for an output programmed to 1.2V with a 3A load is set by the 60°C temperature rise of the LT3074 on the evaluation board. Higher input voltages can be reached if larger copper area or forced-air cooling is applied. In addition, consider the effect of ambient temperature and the maximum junction temperature that may occur. Refer to the LT3074 data sheet for more information.

QUICK START GUIDE

To use the EVAL-LT3074-AZ to evaluate the performance of the LT3074, see Figure 2 for the proper measurement equipment setup and follow these steps:

1. With the input supplies off and turned down, and the load turned down, make all the connections shown in Figure 2. The EVAL-LT3074-AZ can operate without PMBus programming. So, standalone operation is discussed first in steps 1 to 10, and operation with PMBus communications is discussed after that. For now, just ensure that the POWER jumper (JP1) is in the ON position, the CLOCK jumper (JP2) is in the ON position, the ASEL jumper (JP3) is in the VASEL1 position, and the BIAS MODE jumper (JP4) is in the EXT position.
2. Turn on the input and bias supplies, and increase the input supply so it is at least 200mV above the programmed output voltage. Adjust V_{BIAS} so it is between 2.4V and 5.5V so BIAS is at least 1.2V higher than V_{OUT} for proper operation. Note that when setting the input and bias voltages, a V_{IN} or V_{BIAS} too close to the V_{OUT} (too low) can cause dropout operation and a loss of V_{OUT} regulation. Also, a V_{IN} too high above the output can increase power dissipation to an unacceptable level.
3. Increase the load to the desired I_{OUT}. Readjust the input supply so it is still at least 200mV above the programmed output voltage. Verify that V_{OUT} is the expected voltage. Note that if V_{OUT} is lower than expected, the load may be set too high. In that case, temporarily disconnect the load to ensure it is not set too high.
4. When the proper V_{OUT} is established, adjust the input voltages and load within the operating ranges and observe the V_{OUT} regulation, load transient response, and other parameters. Monitor V_{IN} and V_{OUT} at the VO+, VO-, and VI+ terminals.
5. Refer to Application Note AN83 and Application Note AN159 for measuring output noise and PSRR. Note that J1, J2, and J3 are BNC connectors used for noise and PSRR measurements. Use CLOCK jumper (JP2) to enable or disable the internal clocks of LT3074 for noise performance verification. The internal clocks are necessary for PMBus operation.
6. The output voltage is precisely programmed by changing the two SETRES resistors (R1 and R5) in series. Normally, the PGFB divider resistors (R2 and R3) are also changed if the SETRES resistors are changed, but PGFB programming only affects PG and not fast start-up on the LT3074. There is also a component placeholder (R6) that can connect the PGFB pin directly to BIASAF to keep PG high. Monitor power good at the PG terminal, and PG assertion is also indicated by a green LED labeled PG.
7. POWER jumper (JP1) turns the EVAL-LT3074-AZ on or off. EN assertion is also indicated by a green LED labeled POWER ON if V_{BIAS} is present.
8. Monitor the output current at the IMON terminal. Additionally, there are test points for BIASAF, BIASDF, and SETCAP voltages.
9. Refer to the LT3074 data sheet to use the VIOC terminal.
10. Occasionally, it is necessary to provide a shielded V_{IN} power connection to the PCB edge so the PCB has a footprint for an optional SMA connector that can be used in that case.

    To communicate with the LT3074 through PMBus, connect the evaluation board to the PC using the USB-PMBus controller DC1613A. See the Control With LTpower Play section for details. Make sure that the LTpower Play GUI is downloaded on the PC. It is available at **LTpowerPlay | Analog Devices.**This is discussed further in the Control With LTpower Play section.
11. When the USB-PMBus controller is connected, put the BIAS MODE jumper (JP4) in the 3V3 position to connect the BIAS pin to the internal 3.3V logic power from the PMBus interface instead of an external bias voltage, if desired. In that case, V_{OUT} programming is limited as V_{BIAS} must be 1.2 V higher than V_{OUT}. The EVAL-LT3074-AZ can be standalone programmed using DC1613A when JP4 is set to 3V3 and no other connection to the EVAL-LT3074-AZ is necessary.
12. Use the ASEL jumper (JP3) to select one of the three sequential resistor-programmed serial bus interface addresses. Additional addresses can be programmed by changing the resistors. See the LT3074 data sheet for details. The address selection is useful if multiple boards are connected to the PMBus. Parallel the PMBus communication of the EVAL-LT3074-AZ boards using "stacking" connectors J9 and J10.
13. ALERT_N assertion by the PMBus is also indicated by a red LED labeled ALERT.
14. The 6-pin Pmod-type connector (J11) is a Type 6 I^2C interface that allows the EVAL-LT3074-AZ to be used as a peripheral module by a wide range of embedded system and development boards. J11 is just a 0.1 inch pitch header and the Pmod connector pins are labeled with the signal names so they can replace terminals.

QUICK START GUIDE

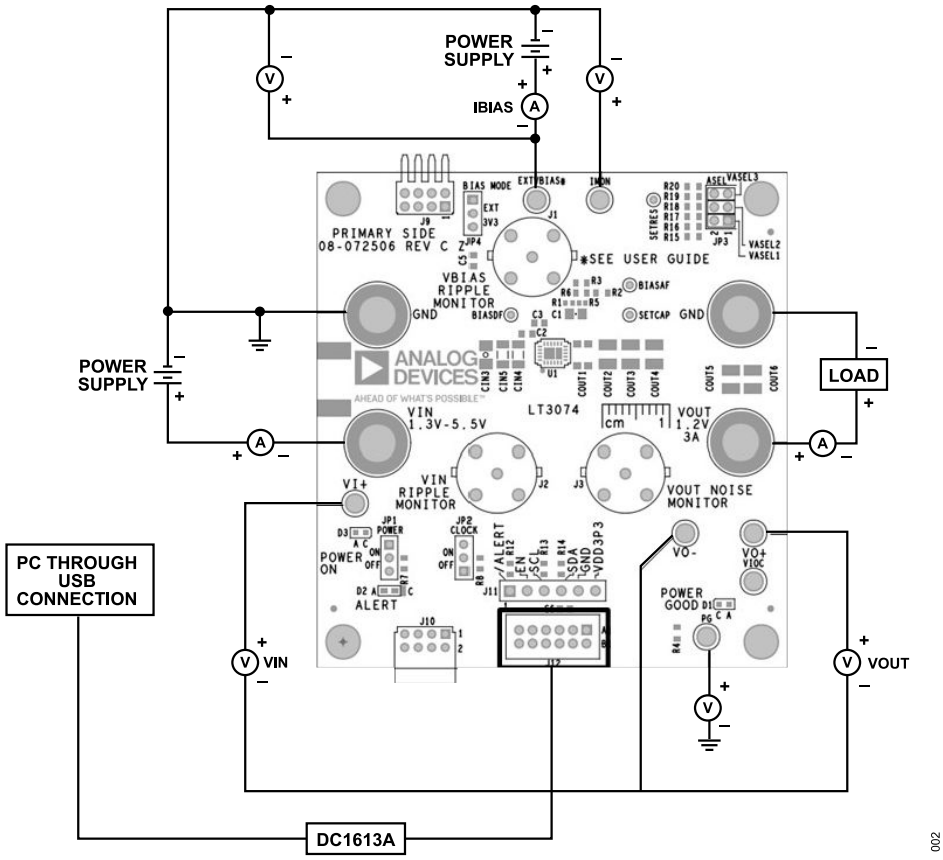

Figure 2. Proper Measurement Equipment Setup for the EVAL-LT3074-AZ

QUICK START GUIDE

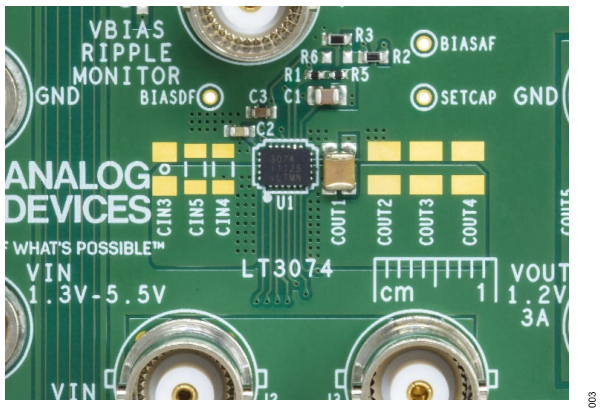

Figure 3. Front Nonthermal with a 1.5V Input Voltage, a 5V Bias Voltage, a 1.2V Output Voltage, and a 3A Load Current, Vertical Orientation with No Forced Air

Figure 4. Back Nonthermal with a 1.5V Input Voltage, a 5V Bias Voltage, a 1.2V Output Voltage, and a 3A Load Current, Vertical Orientation with No Forced Air

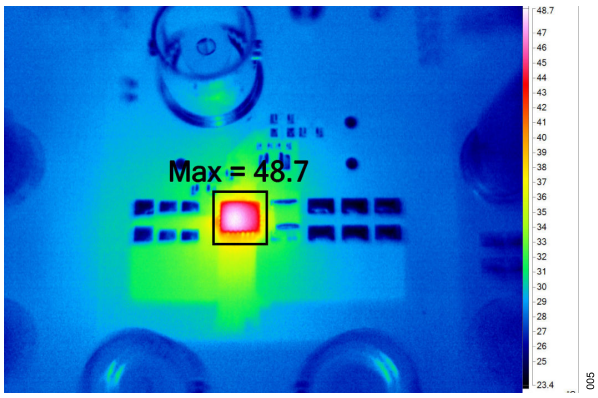

Figure 5. Front Thermal with a 1.5V Input Voltage, a 5V Bias Voltage, a 1.2V Output Voltage, and a 3A Load Current, Vertical Orientation with No Forced Air

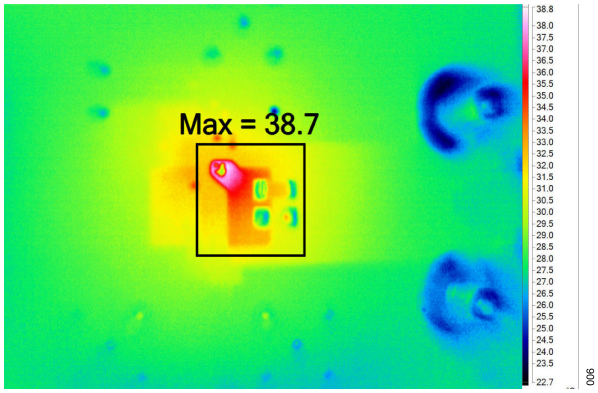

Figure 6. Back Thermal with a 1.5V Input Voltage, a 5V Bias Voltage, a 1.2V Output Voltage, and a 3A Load Current, Vertical Orientation with No Forced Air

CONTROL WITH LTPOWER PLAY

LTpowerPlay is a convenient PC graphical user interface (GUI) that gives complete access to the registers of the LT3074 and many other Analog Devices power system management devices. It can be used to configure and debug the application.

LTpowerPlay communicates using the I^2C bus in the demo system (covered in this manual) or in the real-world product environment. It provides unprecedented control over the Analog Devices chips on the I^2C bus. Use it during board bring-up to tune and optimize the power system parameters. Use it during system debug to view critical system information and troubleshoot board design or manufacturing issues. LTpowerPlay includes extensive help and documentation under the 'Help' menu. Online help includes quick-start videos and tutorials, and detailed technical documentation from the Analog Device website.

To set up and start communicating with the board using its PMBus capabilities, follow these steps:

Launch the LTpower Play GUI. The software should be able to automatically detect the EVAL-LT3074-AZ. Once the board is recognized, the LTpower Play main window interface appears, which mainly includes the PMBus address, configuration window, and telemetry pane. A message box also pops up to notify that the software is already communicating with the LT3074.

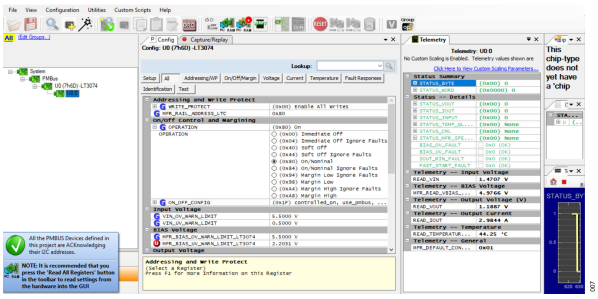

Figure 7. LTpowerPlay Main Window Interface

A telemetry pane can be seen in the interface of the LTPower Play, which allows readback of input/output voltages and currents as well as the device temperature, as shown in Figure 8. The EVAL-LT3074-AZ has the capability of monitoring V_{OUT}, I_{OUT}, V_{IN}, V_{BIAS}, and temperature. These parameters are all shown in the telemetry pane. The green statuses show that all parameters are met and that there are no limits. The telemetry pane also shows warning limits during I_{OUT} overcurrent and undercurrent, V_{OUT}, V_{IN}, and V_{BIAS} overvoltage and undervoltage warning limits, and lastly, overtemperature warning limits. The status changes to red once these limits are triggered. The LT3074 is also capable of margining the output voltage in discrete steps from 1% to 30% through PMBus.

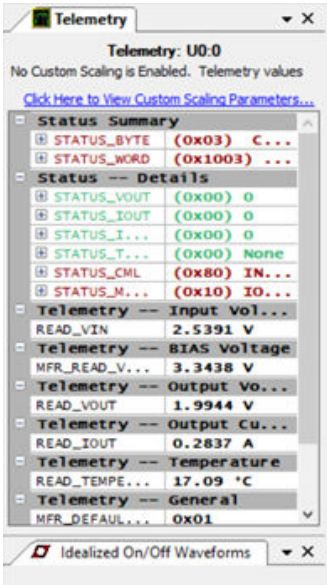

Figure 8. LTpowerPlay Telemetry Pane

TEST PLOTS

The following test plots show scope captures, which demonstrate the response of the pins to the following commands:

ON - Operation Command (Minimum Load)

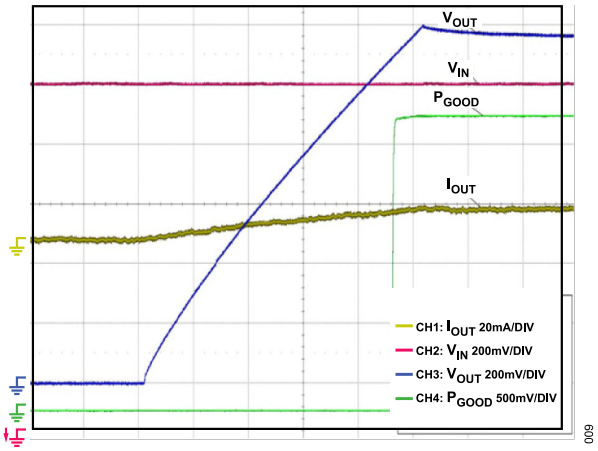

Figure 9. Scope Capture of the Behavior of V_{IN}, V_{OUT}, P_{GOOD}, and I_{OUT} After Sending ON Command at Minimum Load

- V_{IN} = 1.4 V
- V_{BIAS} = 2.5 V
- V_{OUT} = 1.2 V
- I_{OUT} = 10 mA
- T_{BASE} = 500 µs/div

ON - Operation Command (Maximum Load)

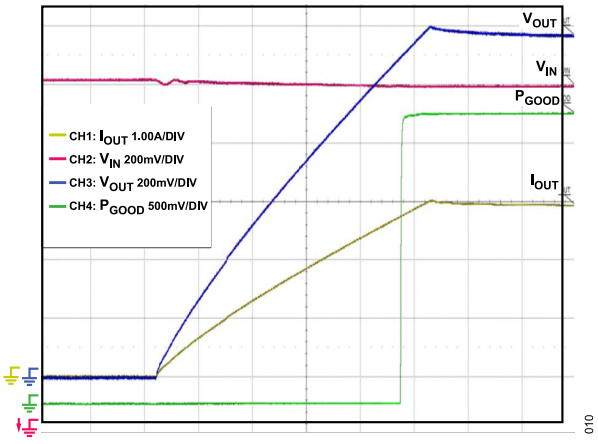

Figure 10. Scope Capture of the Behavior of V_{IN}, V_{OUT}, P_{GOOD}, and I_{OUT} After Sending ON Command at Maximum Load

- V_{IN} = 1.4 V
- V_{BIAS} = 2.5 V
- V_{OUT} = 1.2 V
- I_{OUT} = 3 A
- T_{BASE} = 500 µs/div

MFR_MARGIN - Margin Low Command

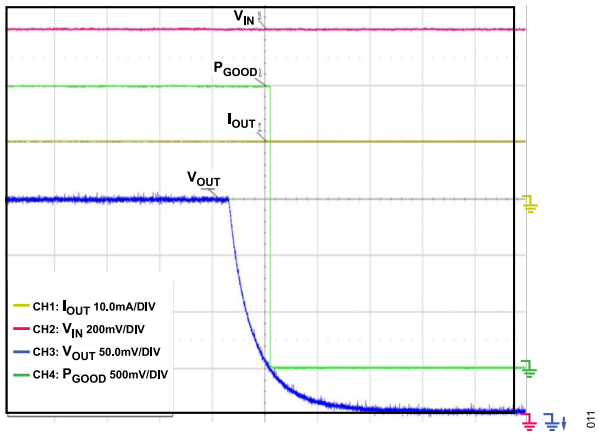

Figure 11. Scope Capture of the Behavior of V_{IN}, V_{OUT}, P_{GOOD}, and I_{OUT} After Sending Margin Low Command with a 15% Margin Percentage

- V_{IN} = 1.4 V
- V_{BIAS} = 2.5 V
- V_{OUT} = 1.2 V
- I_{OUT} = 10 mA
- Margin Percentage = 15%
- T_{BASE} = 100 ms/div

MFR_MARGIN - Margin High Command

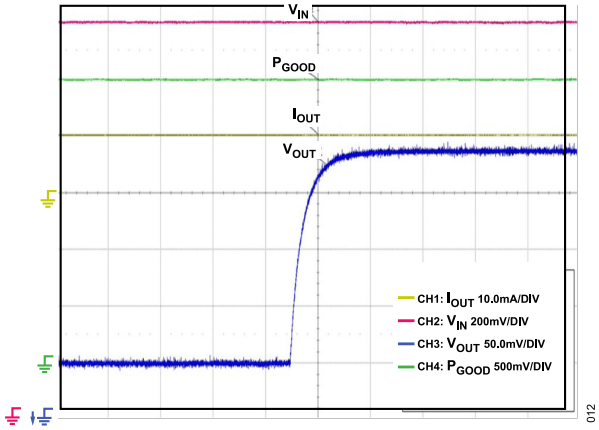

Figure 12. Scope Capture of the Behavior of V_{IN}, V_{OUT}, P_{GOOD}, and I_{OUT} After Sending Margin High Command with a 15% Margin Percentage

- V_{IN} = 1.4 V
- V_{BIAS} = 2.5 V
- V_{OUT} = 1.2 V
- I_{OUT} = 10 mA
- Margin Percentage = 15%
- T_{BASE} = 200 ms/div

TEST PLOTS

OFF - Operation Command (Minimum Load)

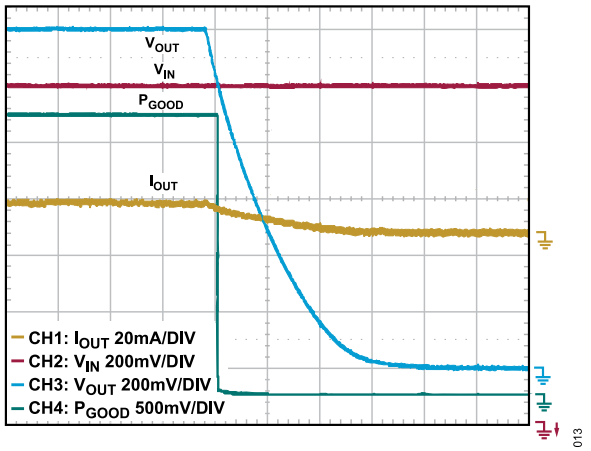

Figure 13. Scope Capture of the Behavior of V_{IN}, V_{OUT}, P_{GOOD}, and I_{OUT} After Sending OFF Command at Minimum Load

- V_{IN} = 1.4 V
- V_{BIAS} = 2.5 V
- V_{OUT} = 1.2 V
- I_{OUT} = 10 mA
- T_{BASE} = 500 µs/div

OFF - Operation Command (Maximum Load)

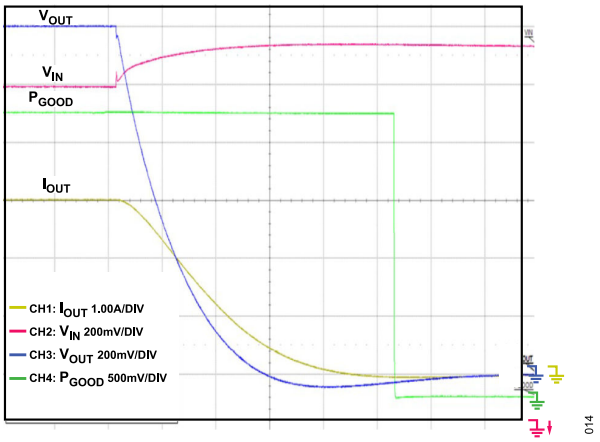

Figure 14. Scope Capture of the Behavior of V_{IN}, V_{OUT}, P_{GOOD}, and I_{OUT} After Sending OFF Command at Maximum Load

- V_{IN} = 1.4 V
- V_{BIAS} = 2.5 V
- V_{OUT} = 1.2 V
- I_{OUT} = 3 A
- T_{BASE} = 500 µs/div

PRINTED CIRCUIT BOARD (PCB) LAYOUT

BEST PSRR PERFORMANCE: PCB LAYOUT FOR INPUT TRACES

For applications using the LT3074 for post-regulating switching converters, placing a capacitor directly at the LT3074 input results in alternating current (AC) (at the switching frequency) to flow near the LT3074. Without careful attention to the PCB layout, this relatively high-frequency switching current generates an electromagnetic field (EMF) that couples to the LT3074 output, degrading its effective PSRR. While highly dependent on the PCB, switching preregulator, input capacitor size, among other factors, the PSRR can easily degrade at high frequencies. This degradation is present even if the LT3074 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional low PSRR low dropout (LDO) regulators, the high PSRR of the LT3074 requires careful attention to higher-order parasitics to realize the full performance offered by the regulator.

The EVAL-LT3074-AZ alleviates this degradation in PSRR by using a specialized layout technique. The V_{IN} input trace and its corresponding return path (GND) are highlighted in red in Figure 15 and Figure 16. Figure 16 also shows the location of the C1 input capacitor and the connection between the GND return path for the V_{IN} input trace and GND for the rest of the PCB. When an AC voltage is applied to the input of the EVAL-LT3074-AZ, AC flows on the path formed through CIN1 by the input and ground traces. Without the proper PCB layout, the AC that flows on this path can generate EMFs that do not completely cancel and couple to the COUT1 output capacitor and related traces, making the PSRR appear worse than it actually is. With the input trace directly above the return path, the EMFs are in opposite directions, and consequently, cancel each other out. Ensure these traces exactly overlap each other to maximize the cancellation effect and thus provide the maximum PSRR offered by the regulator.

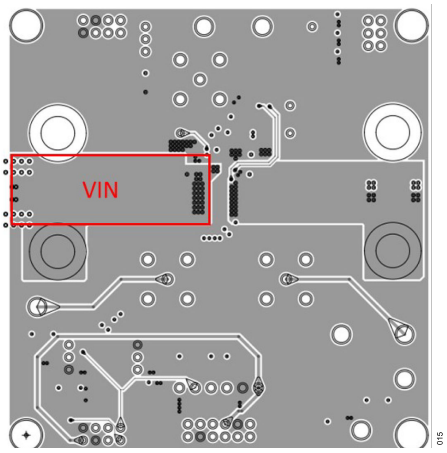

Figure 15. Layer 3 of the EVAL-LT3074-AZ

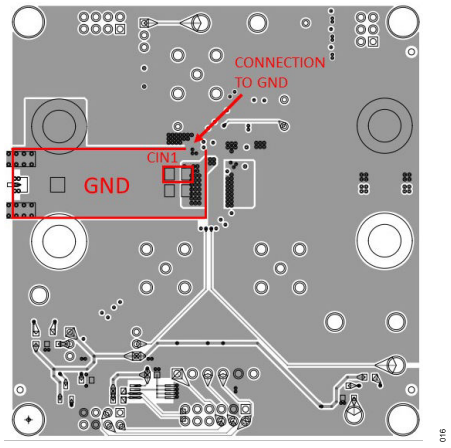

Figure 16. Layer 4 of the EVAL-LT3074-AZ

PCB LAYOUT FOR THE COUT1 OUTPUT CAPACITOR

As previously mentioned, the EVAL-LT3074-AZ PCB design uses a split-capacitor technique to Kelvin connect the ground terminal of the SETCAP capacitor to the ground terminal of the COUT1 output capacitor and the SENSE pin to the positive terminal of the output capacitor (see Figure 17 and Figure 18). This Kelvin connection regulates the output voltage at the output capacitor, which in turn, optimizes noise, PSRR, load transient, and regulation performance, all measured at the output capacitor. The split-capacitor technique is useful in this case because it makes it possible to relocate the regulation point, if desired. Regulation of the output voltage at a new location requires leaving the COUT1 output-capacitor location open and wiring the split-capacitor pads corresponding to the SETCAP capacitor ground terminal and SENSE to the new output capacitor location. Additional capacitance located from SENSE to the SETCAP ground between the regulation point and the LT3074 decreases stability. The split-capacitor technique itself does not enhance LT3074 stability because of the type of pass transistor, even though the unity-gain bandwidth of the LT3074 bandwidth is relatively high and close to the self-resonance frequency of the output capacitor.

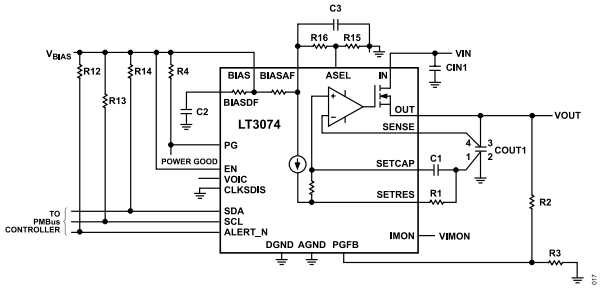

Figure 17. SETCAP Capacitor (C1) and Output Capacitor (COUT1) Connections for Best Noise, PSRR, Load Transient, and Regulation Performance

PRINTED CIRCUIT BOARD (PCB) LAYOUT

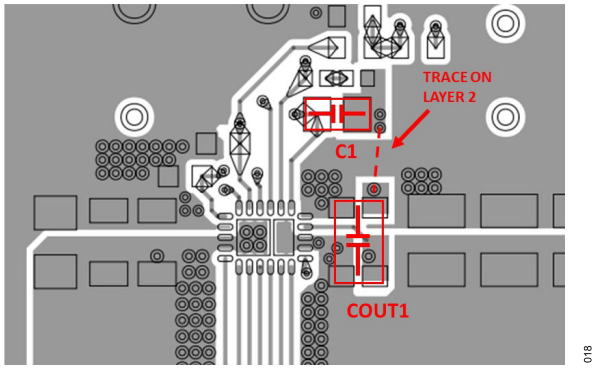

Figure 18. Split Pads for the Output Capacitor (COUT1) on the Top Layer of EVAL-LT3074-AZ. Connect the Ground Terminal of the SETCAP Capacitor (C1) to the Ground Terminal of COUT1 and the SENSE Pin to the Positive Terminal of COUT1

EVALUATION BOARD SCHEMATIC

EVALUATION BOARD SCHEMATIC 1

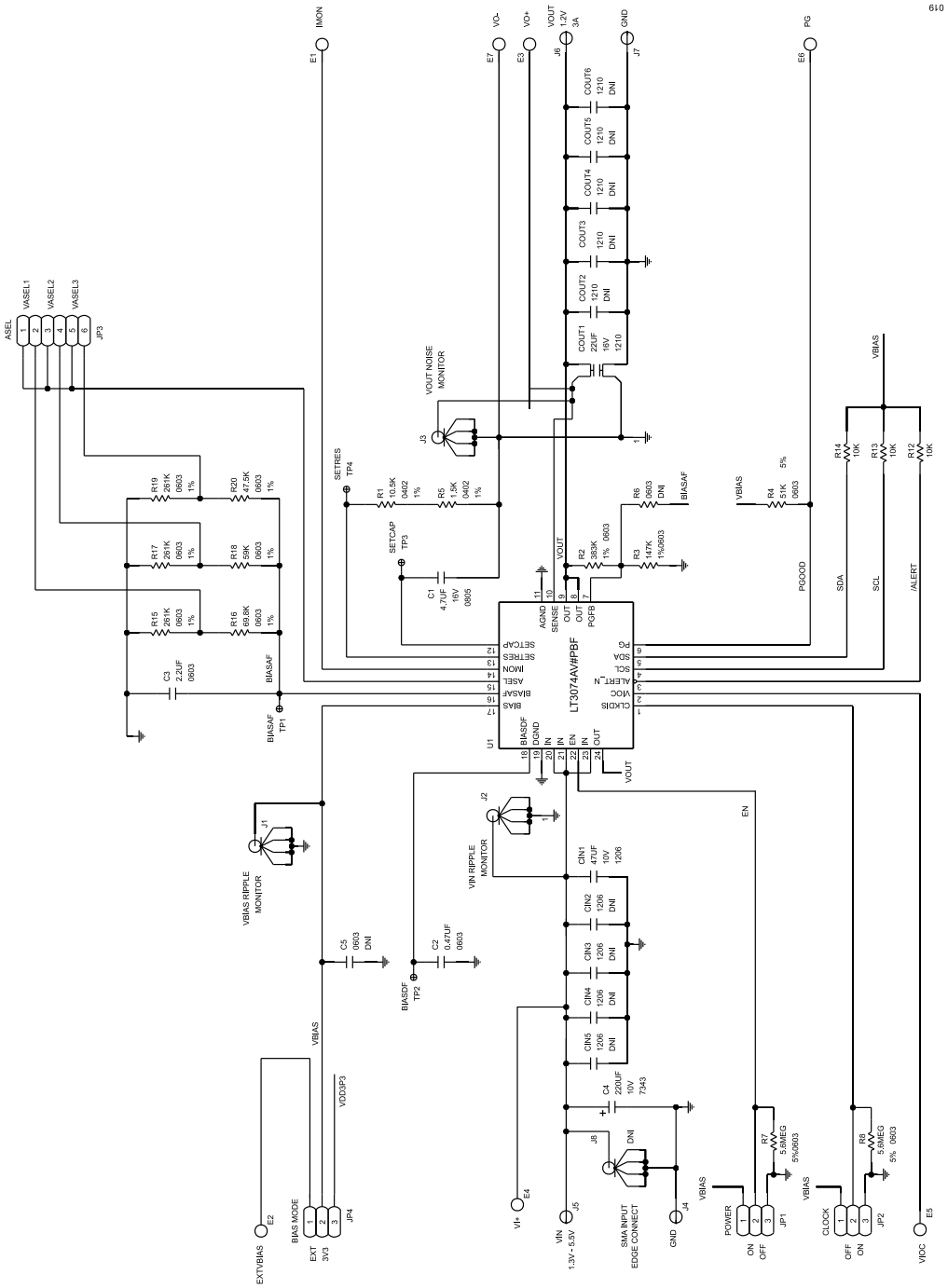

Figure 19. Evaluation Board Schematic 1

EVALUATION BOARD SCHEMATIC

EVALUATION BOARD SCHEMATIC 2

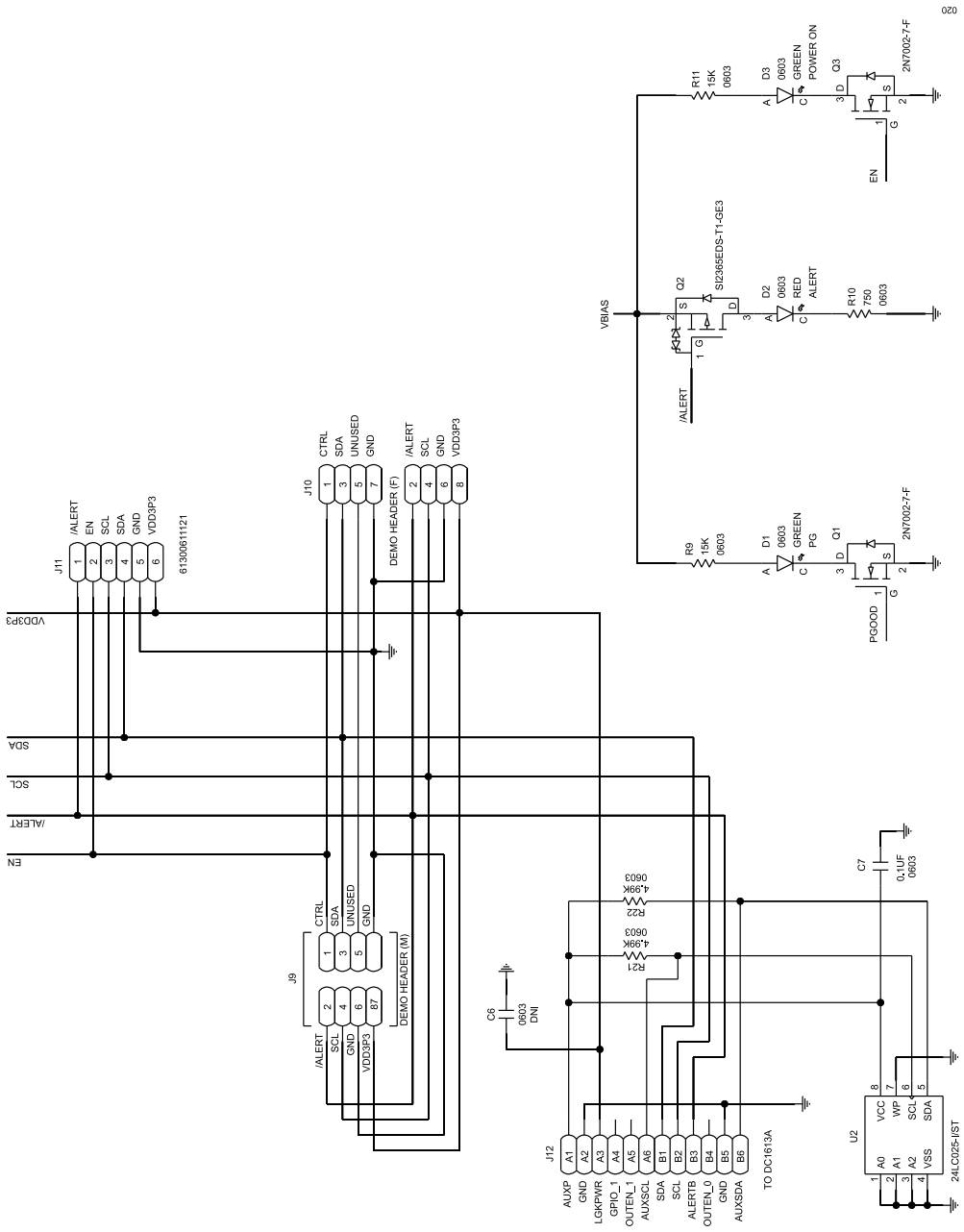

Figure 20. Evaluation Board Schematic 2

ORDERING INFORMATION

BILL OF MATERIALS

Item	Quantity	Reference Designator	Part Description	Manufacturer, Part Number
Required Circuit Components				
1	1	C1	4.7µF capacitor, X7R, 16 V, 10%, 0805, AEC-Q200	Murata, GCJ21BR71C475KA01L
2	1	C2	0.47µF capacitor, X7R, 10V, 10%, 0603	AVX, 0603ZC474KAT2A
3	1	C3	2.2µF capacitor, X7R, 10V, 10%, 0603	Murata, GRM188R71A225KE15D
4	1	CIN1	47µF capacitor, X5R, 10V, 10%, 1206	Murata, GRM31CR61A476KE15L
5	1	COUT1	22µF capacitor, X7R, 16V, 10%, 1210, AEC-Q200	Murata, GCM32ER71C226KE19L
6	1	R1	10.5kΩ resistor, 1%, 1/10W, 0402, AEC-Q200	Panasonic, ERJ-2RKF1052X
7	1	U1	3A, ultralow noise, high PSRR, 45mV dropout, ultrafast linear regulator with PMBus	Analog Devices, Inc., LT3074AV#PBF
Optional Evaluation Board Components				
1	1	C4	220µF capacitor, tantalum polymer, 10V, 20%, 7343-31, 40Ω ESR	AVX, TCJD227M010R0040
2		C5, C6	Capacitors, 0603, optional	Optional
3	1	C7	0.1µF capacitor, X8L, 50 V, 10%, 0603, AEC-Q200	Murata, GCM188L81H104KA57D
4		CIN2, CIN3, CIN4, CIN5	Capacitors, 1206, optional	Optional
5		COUT2, COUT3, COUT4, COUT5, COUT6	Capacitors, 1210, optional	Optional
6	2	D1, D3	Green, 520nm, LED Indication - Discrete, 3.2V, 0603	Wurth Elektronik, 150060GS75000
7	1	D2	Red, 630nm, LED Indication - Discrete, 1.9V, 0603	Wurth Elektronik, 150060SS75000
8	2	Q1, Q3	N-Channel, MOSFET, 60V, 370mW, surface mount, SOT-23-3	Diodes Incorporated, 2N7002-7-F
9	1	Q2	P-Channel, MOSFET, 20V, 1W, surface mount, SOT-23-3	Vishay, SI2365EDS-T1-GE3
10	1	R2	383kΩ resistor, 1%, 1/10W, 0603, AEC-Q200	Panasonic, ERJ-3EKF3833V
11	1	R3	147kΩ resistor, 1%, 1/10W, 0603, AEC-Q200	Panasonic, ERJ3EKF1473V
12	1	R4	51kΩ resistor, 5%, 1/10W, 0603, AEC-Q200	Panasonic, ERJ3GEYJ513V
13	1	R5	1.5kΩ resistor, 1%, 1/10W, 0402, AEC-Q200	Panasonic, ERJ-2RKF1501X
14	1	R6	Resistor, 0603, optional	Optional
15	2	R7, R8	5.6MΩ resistor, 5%, 1/10W, 0603, AEC-Q200	Panasonic, ERJ3GEYJ565V
16	2	R9, R11	15kΩ resistor, 1%, 1/10W, 0603, AEC-Q200	Vishay, CRCW060315K0FKEB
17	1	R10	750Ω resistor, 1%, 1/10W, 0603, AEC-Q200	Vishay, CRCW0603750RFKEA
18	3	R12, R13, R14	10kΩ resistor, 1%, 1/10W, 0603, AEC-Q200	Panasonic, ERJ-3EKF1002V
19	3	R15, R17, R19	261kΩ resistor, 1%, 1/10W, 0603, AEC-Q200	Panasonic, ERJ-3EKF2613V
20	1	R16	69.8kΩ resistor, 1%, 1/10W, 0603, AEC-Q200	Panasonic, ERJ-3EKF6982V
21	1	R18	59kΩ resistor, 1%, 1/10W, 0603, AEC-Q200	Panasonic, ERJ-3EKF5902V
22	1	R20	47.5kΩ resistor, 1%, 1/10W, 0603, AEC-Q200	Vishay, CRCW060347K5FKEA
23	2	R21, R22	4.99kΩ resistor, 1%, 1/10W, 0603, AEC-Q200	Panasonic, ERJ-3EKF4991V
24	1	U2	EEPROM IC, 2Kb, I^2C, 500kHz, 900ns, 8-TSSOP	Microchip Technology, 24LC025-I/ST
Hardware				
1	7	E1, E2, E3, E4, E5, E6, E7	Test points, turret 0.094"	Mill-Max, 2501-2-00-80-00-00-07-0
2	3	J1, J2, J3	BNC connector jack, female, 50Ω, through-hole	Amphenol RF, 112404
3	4	J4, J5, J6, J7	Banana jack connector, female, non-insulated, swage	Keystone, 575-4
4		J8	SMA connector jack, female, 50Ω board edge, end launch solder tab, optional	Cinch, 142-0701-851
5	1	J9	Connector, header, male, through-hole, right angle, 8-position, 0.079"	Molex, 87760-0816
6	1	J10	Connector, header, female, through-hole, right angle, 8-position, 0.079"	Sullins, NPPN042FJFN-RC
7	1	J11	Connector, header, male, through-hole, 6-position, 0.100"	Wurth Elektronik, 61300611121

ORDERING INFORMATION

Item	Quantity	Reference Designator	Part Description	Manufacturer, Part Number
8	1	J12	Connector, header, male, through-hole, 12-position, 0.079"	Amphenol ICC, 98414-G06-12ULF
9	3	JP1, JP2, JP4	Connector, header, male, through-hole, 3-position, 0.079"	Wurth Elektronik, 62000311121
10	1	JP3	Connector, header, male, through-hole, 6-position, 0.079"	Sullins, NRPN032PAEN-RC
11	4	MP1 to MP4	Standoff, nylon, snap fit, 0.500"	Wurth Elektronik, 702935000
12	4	XJP1 to XJP4	Connector shunt, female, 2-position, 0.079"	Wurth Elektronik, 60800213421

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.