

ADRV903x Evaluation System User Guide**INTRODUCTION**

The ADRV903x family evaluation system enables customers to evaluate an ADRV903x device without having to develop custom hardware or software. The system is comprised of an ADRV903x customer evaluation (CE) board and an [ADS10-V1EBZ](#) motherboard with accompanying wall adapter power supplies for both. The evaluation software uses the [Analysis | Control | Evaluation \(ACE\)](#) software developed by Analog Devices, Inc., extended by an ADRV903x specific board plugin. This plugin can be run with ACE on a Windows® host PC communicating with the ADS10-V1EBZ motherboard using Ethernet. The ADS10-V1EBZ functions as a baseband processor running an application (ADRV903x command server) for controlling and communicating with the ADRV903x device.

This document also serves as a quick startup guide for the **ADRV903x Configurator**, which is built into the ADRV903x board plugin for ACE. The **ADRV903x Configurator** allows the user to explore various configurations of an ADRV903x device to arrive at a desired use case configuration. The **ADRV903x Configurator** also provides an overview of the frequency responses of the receiver (Rx), transmitter (Tx), and the observation receiver (ORx) datapaths for a chosen configuration.

This user guide details the steps required to install the ADRV903x evaluation software, program an existing use case, and evaluate the ADRV903x transmitter, receiver, and observation receiver datapaths. The **ADRV903x Configurator** sections of this user guide enable the user to generate a new use case and view its corresponding datapath configurations and filter graphs for the ADRV903x. Note that this document updates as the **ADRV903x Configurator** development progresses and as additional functions are added to the tool.

INITIAL SETUP

The ACE GUI is the graphical user interface (GUI) used to communicate with the evaluation platform. The GUI can run with or without evaluation hardware connected. When ACE runs without the hardware connected, the GUI can be fully configured for a particular operating mode. If the evaluation hardware is connected, the desired operating parameters can be setup with ACE and then the software can program the evaluation hardware. When the transceiver is configured, the evaluation software can be used to transmit waveforms generated from the internal numerically controlled oscillator (NCO) block or using custom waveform files as well as to observe signals received on one of the receiver or observation input ports.

TABLE OF CONTENTS

Introduction.....	1	Tx Init.....	37
Initial Setup.....	1	Post MCS Init.....	38
Hardware Kit.....	3	Calibration.....	39
Quick Start Guide.....	4	AD9528 Clock Settings.....	40
Software Requirements.....	4	Runtime.....	41
Hardware Setup.....	4	Transmitter Vectors.....	41
Software Setup.....	6	Rx (Capture).....	45
ACE Core Installation.....	6	ORx (Capture).....	47
ADRV903x Plugin Installation.....	7	TDD View.....	48
Hardware Connection.....	8	FFT Analysis.....	49
ADS10-V1EBZ Platform Files Update.....	8	Software Resource Files.....	57
ADRV903x Plugin Overview.....	11	Resource File Generation Using ACE.....	58
Use Case Selector.....	13	IronPython Scripting.....	59
Device Programming.....	15	Appendix.....	60
Programming Errors.....	16	Uninstalling Older ACE.....	60
ADRV903x Configurator.....	17	Uninstalling Older Plug-In Using Plug-In	
Top Level Configuration.....	17	Manager.....	61
LO Configuration.....	18	Installing the ADRV903x Plugin Using the	
Transmitter Configuration.....	21	ACE Plug-in Manager.....	62
Receiver Configuration.....	23	Disconnecting ACE from ADS10-V1EBZ	
Observation Receiver Configuration.....	25	Command Server.....	63
JESD Configuration.....	27	Reconnecting ACE to the ADS10-V1EBZ	
Power Analysis.....	33	Command Server.....	64
Init Pages.....	37		

REVISION HISTORY**1/2025—Revision 0: Initial Version**

HARDWARE KIT

The ADRV903x evaluation system consists of the following hardware:

- ▶ One (1) ADRV903x CE board with a field programmable gate array mezzanine card (FMC) connector
- ▶ One (1) 12 V, 1.5 A wall connector power supply cable for the CE board
- ▶ One (1) [ADS10-V1EBZ](#) motherboard with an FMC connector
- ▶ One (1) 12 V, 16.6 A power supply for powering the ADS10-V1EBZ
- ▶ One (1) FMC adapter for ADS10-V1EBZ
- ▶ Two (2) secure digital (SD) cards along with the evaluation kit
 - ▶ ADS10-V1EBZ transmitter V1.0 SD card (used for booting Linux on the ADS10-V1EBZ and running the ADRV903x command server application)
 - ▶ SD card type, 16 GB size, Class 10

Note that the ADRV903x CE board can be any of the ADRV903X-MB/PCBZ, ADRV903X-HB/PCBZ, ADRV903X-LB/PCBZ, and ADRV903X-UB/PCBZ evaluation boards. The ADS10-V1EBZ motherboard is not included with the purchase of the ADRV903x evaluation board and must be purchased separately.

QUICK START GUIDE

SOFTWARE REQUIREMENTS

The host PC running the [ACE](#) evaluation software must meet the following requirements:

- ▶ The operating system on the controlling PC must be Windows 10 (x86 and x64).
- ▶ The PC must have a free Ethernet port to establish a dedicated connection over the following ports:
 - ▶ Port: 22—secure shell (SSH) protocol.
 - ▶ Port: 5000—for communicating with the command server on [ADS10-V1EBZ](#).

If the Ethernet port is occupied by another local area network (LAN) connection, a USB to Ethernet adapter can be used.

- ▶ ADRV903x customer software package—contact your [Analog Devices Sales Representative](#) to obtain access to this software.
- ▶ The user must have administrative privileges.
- ▶ The PC must have access to the internet to run automatic software updates.

If internet access is restricted, a manual software update can be performed. Do not upgrade to newer ACE versions as this may cause issues.

HARDWARE SETUP

To setup the evaluation hardware, follow these steps in conjunction with [Figure 1](#):

1. Insert the SD card that comes with the evaluation kit into the ADS10-V1EBZ MicroZED MicroSD card slot (J6).
2. Mount the FMC adapter on the ADS10-V1EBZ. This step is to protect the ADS10-V1EBZ FMC connector from multiple reinsertions.
3. Connect the ADRV903x customer evaluation board and the ADS10-V1EBZ motherboard together. Use the high pin count (HPC) FMC connector (P1001/P2), ensuring the connectors are properly aligned.
4. On the ADRV903x evaluation board, provide a reference clock source (122.88 MHz is the default, or use Reference A (REFA) frequency from AD9528 clock settings), at a 7 dBm power level to the J901 connector. This signal drives the reference clock into the [AD9528](#) clock generation chip on the board. The REFA/REFA_N pins of the AD9528 generate the DEV_CLK for the device and REF_CLK for the FPGA on the ADS10-V1EBZ platform.
5. Connect the included 12 V, 16.6 A power supply to the ADS10-V1EBZ motherboard through the P2 header.
6. Connect the ADS10-V1EBZ to the host PC with an Ethernet cable (connect to P3). No driver installation required.

A USB to Ethernet adapter can be used if no Ethernet port is available on the host PC.

- ▶ On the Ethernet connection dedicated to the ADS10-V1EBZ platform, the user must manually configure the IP address (see [Figure 2](#)):
 - ▶ IPv4 address: 192.168.1.xyz, where xyz can be assigned such that no other device on the user local network uses the same IP address. Note that xyz must not be equal to 10 because 192.168.1.10 is used by the ADRV903x command server on the ADS10-V1EBZ.
 - ▶ IPv4 subnet mask: 255.255.255.0.
- ▶ The user must ensure that the following ports are not blocked by the host PC firewall:
 - ▶ Port: 22
 - ▶ Port: 5000
- ▶ Power up the CE board using the included 12 V, 3 A wall connector power supply.

QUICK START GUIDE

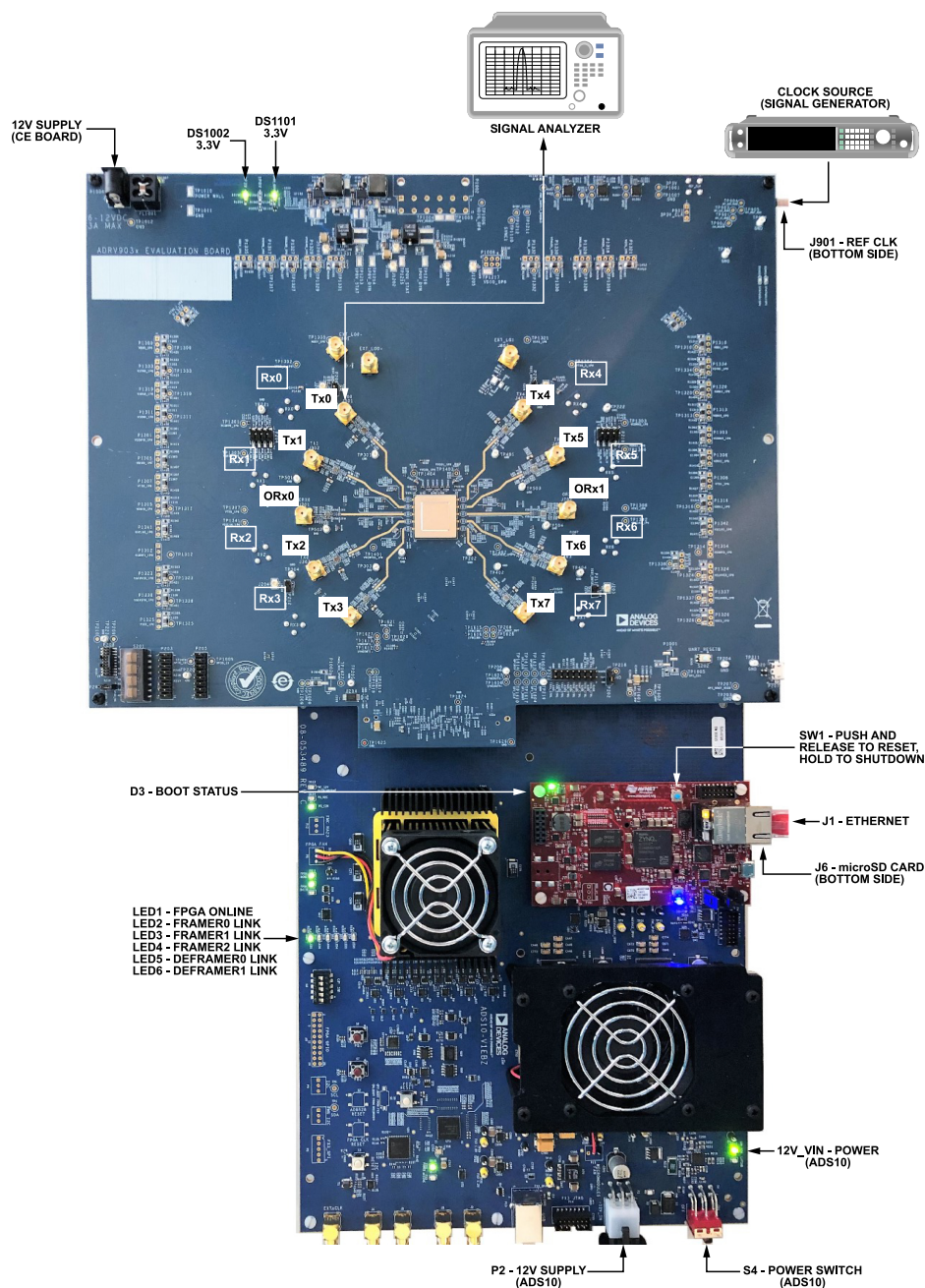


Figure 1. ADRV903x CE Board and ADS10-V1EBZ Motherboard with Instruments Required for Transmitter Testing

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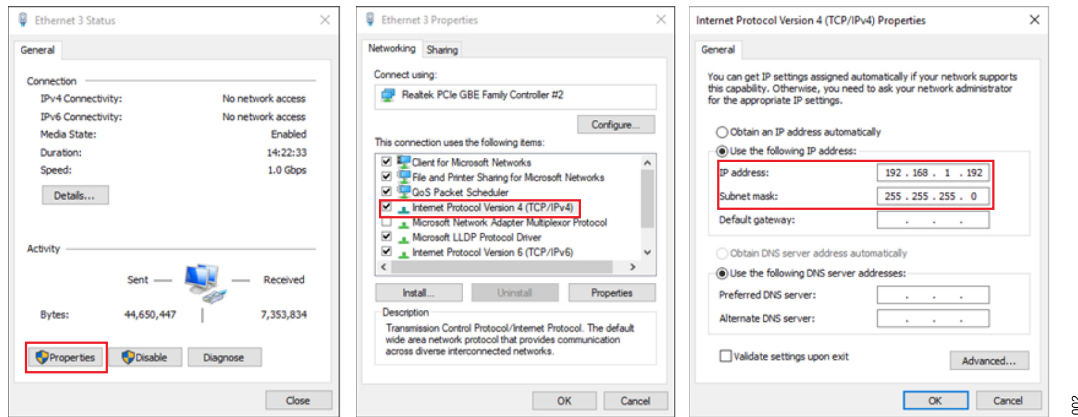


Figure 2. IP Settings for Ethernet Port Dedicated to ADS10-V1EBZ Motherboard (Note the Last Number in the IP Address Must Be Chosen by the User.)

SOFTWARE SETUP

The ADRV903x configurator uses the [ACE](#) software, which is a desktop application that allows the evaluation and control of various products from across the Analog Devices portfolio. ACE consists of a common framework (core) that can be extended by plugins for evaluating products such as the ADRV903x. ACE is designed to educate the user in the functional operation of a product and to enable access to the product evaluation system at a higher level of abstraction.

The ADRV903x evaluation software can be set up and updated to use the latest customer software package provided by Analog Devices. This update process requires the user to perform the following steps:

1. Install (or update) ACE on the host Windows PC.
2. Install (or update) the ADRV903x board plugin.
3. Update the ADS10-V1EBZ platform files. This step requires setting up a hardware connection.

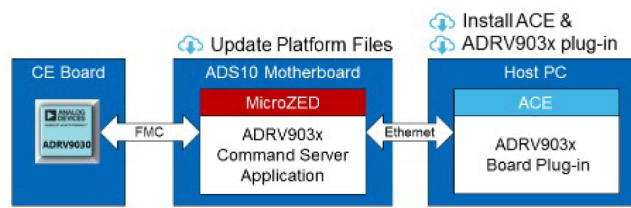


Figure 3. ADRV903x Evaluation Software Components

ACE CORE INSTALLATION

The ADRV903x evaluation software consists of an ACE core (shared framework) and an ACE plugin unique to the ADRV903x. The ACE core can be installed by running the ACE installer included in the customer software package provided by Analog Devices.

The installer consists of a single executable file with the ACE core version number included in the file name. The user can start ACE installation by double clicking on the installer and going through the recommended settings to install ACE. Administrator privileges are required for this installation.

If an older version of ACE was previously installed on the host PC, installing the included ACE version is strongly recommended to get the latest features and bug fixes. In case installation errors are seen, see the [Uninstalling Older ACE](#) section to start from a fresh install. Additional ACE documentation is available on wiki.analog.com/resources/tools-software/ace/user-guide.

QUICK START GUIDE

ADRV903x PLUGIN INSTALLATION

The ADRV903x [ACE](#) plugin is also included with the customer software package as a **Board.ADRV903x.acezip** file.

Once ACE is installed, the ADRV903x plugin can be installed by double clicking on the included **.acezip** file. This launches ACE with the ADRV903x plugin listed in the **Explore Without Hardware** section as **ADRV903x Board** (see [Figure 4](#)). The plugin may take a moment to load on ACE first launch. Alternatively, **ACE Plug-in Manager** can be used for installing the plugin as described in the [Installing the ADRV903x Plugin Using the ACE Plug-in Manager](#) section. The uninstallation process for plugins is also described in the [Appendix](#) section.

With the ADRV903x plugin installed, the search bar on ACE **Start** page can be used to navigate to the plugin with the ID **ADRV903x Board**. The user can then verify that the installed plugin version number matches the version in the **.acezip** file name. Once the desired ADRV903x plugin version is installed in ACE, it can be run either:

- ▶ Without hardware. Double click on the ADRV903x plugin row under **Explore Without Hardware** or select the plugin row and click on **Add Selected Subsystem(s)** to start as shown in [Figure 4](#).
- ▶ With hardware. Configure a hardware connection between ACE and the ADRV903x command server running on the ADS10-V1EBZ motherboard and update platform files, then double click the **ADRV903x Board** icon.

Important: if the host PC already has an ADRV904x board plugin installed, the user may need to uninstall this ADRV904x plugin before the ADRV903x plugin can be run (see the [Appendix](#) section). This issue will be resolved in upcoming releases such that the ADRV904x and ADRV903x plugins can coexist within ACE as needed.

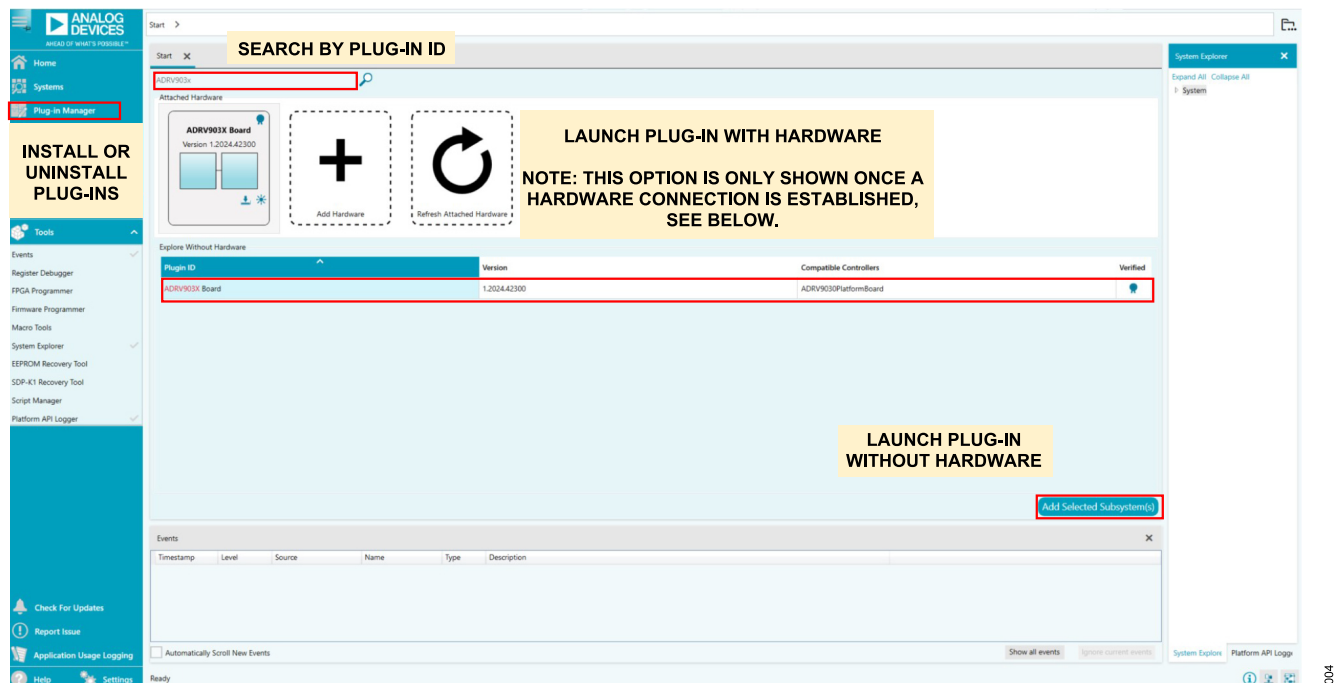


Figure 4. ACE Startup Screen Showing the Installed ADRV903x Plugin That Can Be Double Clicked to Start the Configurator Without Any Hardware

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HARDWARE CONNECTION

The ADRV903x plugin can be used standalone (without hardware) as a use case configurator for the ADRV903x family. See the [ADRV903x Configurator](#) section to explore the plugin without connecting to ADS10-V1EBZ/CE board evaluation hardware.

If the user is evaluating with hardware, [ACE](#) must first be configured to connect to the ADRV903x command server application running on the [ADS10-V1EBZ](#) motherboard. By default, the ADRV903x command server listens for incoming connections from the host PC on the IP address 192.168.1.10 and port 5000. The same IP address and port information can be provided to ACE by taking the following steps:

1. Open ACE **Settings** and navigate to the **Ethernet Boards** tab.
2. Click on **+** to make a new server connection.
3. Enter server settings as shown in [Figure 5](#). **ADRV903x Platform** must be selected for platform.
4. Click **OK** to connect ACE to the ADRV903x server running on ADS10-V1EBZ.

Setting up this connection allows ACE to update the ADRV903x command server running on ADS10-V1EBZ. This process can take a moment, and the user must monitor events associated with updating and starting the ADRV903x command server by displaying the **Events** panel from **Tools** then **Events** on the left panel of ACE.

Once the command server has been started successfully, the **Start** page updates to list the **ADRV903x Board** under **Attached Hardware** ([Figure 6](#)). In case the **ADRV903x Board** does not show under **Attached Hardware**, refer to the [Hardware Setup](#) section to ensure that the hardware is powered properly. Verify the command server IP address configured under **ACE Settings > Ethernet Boards** and ensure that no other software application (or ACE instance) is accessing the IP address 192.168.1.10:5000.

The [Appendix](#) section additionally covers disconnecting from and reconnecting ACE back to the command server application running on ADS10-V1EBZ.

ADS10-V1EBZ PLATFORM FILES UPDATE

The [ADS10-V1EBZ](#) platform files must be updated to use the platform files included with the ADRV903x plugin. The user may then click the **Update Platform Files** button on the **ADRV903x Board** icon to update the ADS10-V1EBZ to use the platform files included with the plugin. A loading screen is shown while the update is in progress. This process takes about a minute.

If the loading screen is not seen, the user can attempt to update the platform files again. In case issues persist, the user may navigate to **Tools > System Explorer > Debug**, and read back FPGA Address 0x43000000 to compare against a good setup.

QUICK START GUIDE

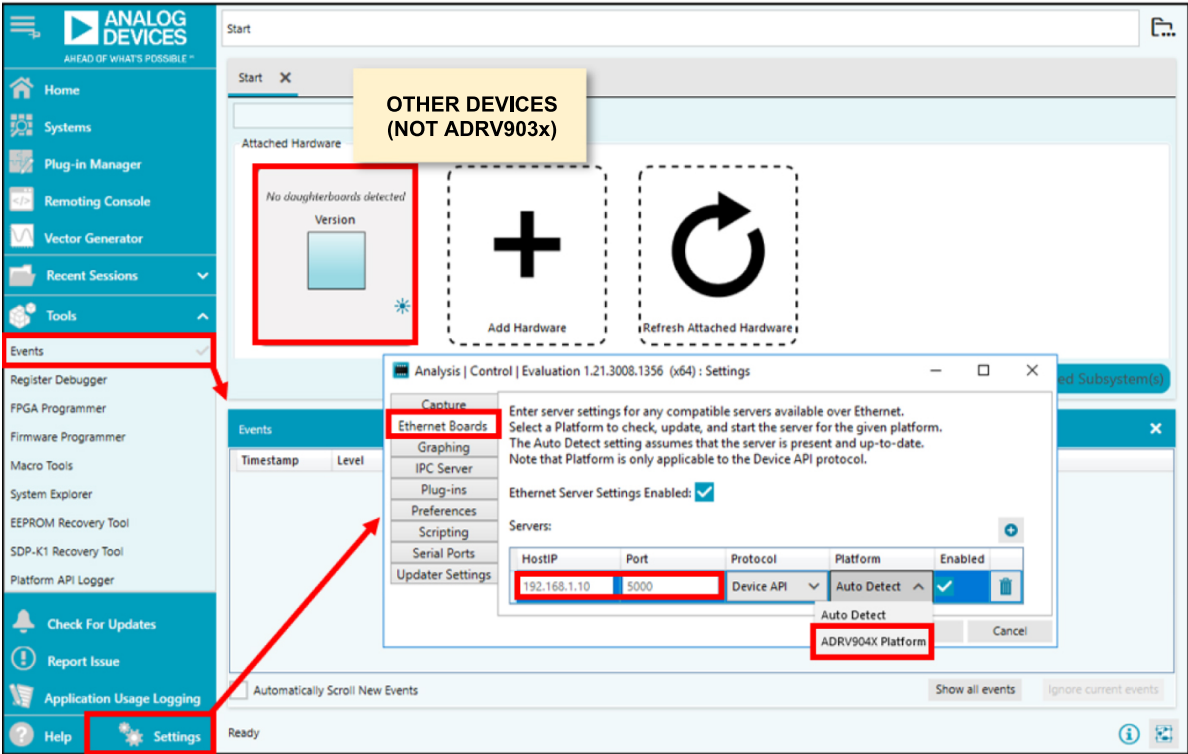


Figure 5. Providing ADRV903x Command Server Application IP Address, Port, and Platform Type to ACE

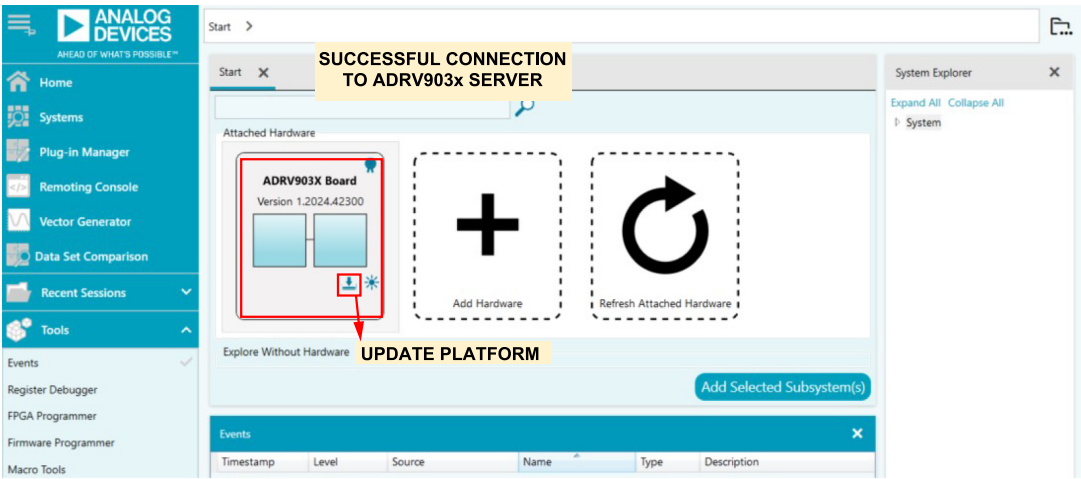


Figure 6. ADRV903X Board Gets Populated Under Attached Hardware When ACE Successfully Interfaces to ADS10-V1EBZ

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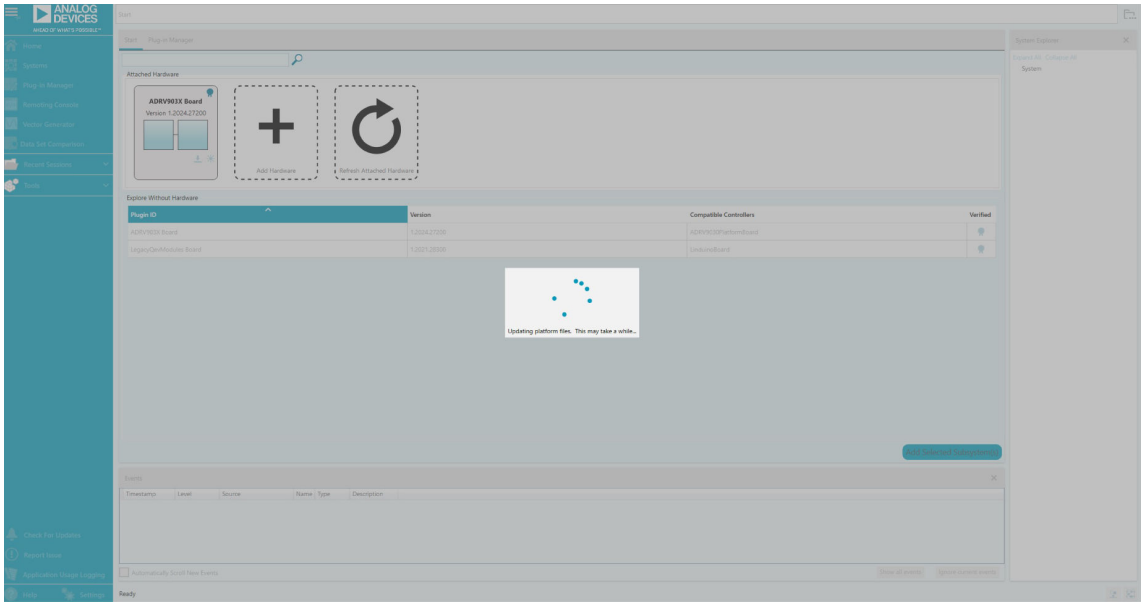


Figure 7. Loading Screen While Updating Platform Files

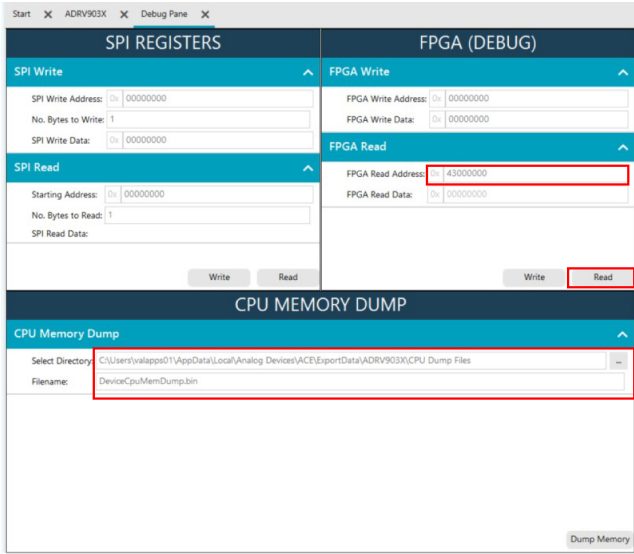


Figure 8. Platform Files Version Can Be Verified by Reading Back FPGA Address 0x43000000 from the Debug Page

CPU memory dump can be taken for analysis as shown in Figure 8. Browse to the directory. Once the directory is selected, the memory dump automatically gets saved.

ADRV903x PLUGIN OVERVIEW

The ADRV903x plugin can be launched with a hardware connection from the **Start** page by double clicking the **ADRV903x Board** icon under **Attached Hardware**. It can also be run in configuration only mode, without hardware, to explore various ADRV903x configurations. The plugin looks and feels the same when launched with or without hardware, but a hardware connection is essential for programming the ADRV903x device and evaluating performance through runtime pages.

The **Tools** menu on the **ACE** panel can be used to display **System Explorer** for navigating the different pages included with the ADRV903x plugin. These pages are briefly described, and can be navigated as follows:

- ▶ Configuration pages: create, modify, program, and export ADRV903x use cases by setting up the following:
 - ▶ **Top Level Config** (see [Figure 10](#)): maps various **Tx/Rx Profile Assignment** and **ORx Profile Assignment** channels to profiles, export the current state of the configuration as a JSON use case, view the device **Open Help File**, and access the configuration pages.
 - ▶ Subsequent configuration pages can be used to configure the local oscillator (LO), carrier digital up conversion (DUC), transmitter, carrier digital down conversion (DDC), receiver, observation receiver, and JESD settings to arrive at and validate a desired ADRV903x use case.
 - ▶ **Power Analysis**: estimate power consumption in time division duplex (TDD) and frequency division duplex (FDD) modes for a configured use case.
- ▶ **Use Case Selector**: load and program a previously generated ADRV903x use case. This page allows the following:
 - ▶ Loading the configuration pages above with an existing use case as a starting point, and then the user modifies settings as needed to derive a new use case.
 - ▶ Bypassing the configuration pages and programming an existing use case as is.
- ▶ **AD9528 Clock Settings**: generate the desired ADRV903x device clock using the [AD9528](#) clock chip on the CE board.
- ▶ **Init Pages**: set ADRV903x initialization parameters including the following:
 - ▶ **Tx Init** and **Rx Init** settings, calibrations, post multichip synchronization (MCS) init TRX_CTRL pin assignments, and transmitter to observation receiver mappings.
- ▶ Program the ADRV903x (if connected with hardware) from the following:
 - ▶ **Use Case Selector**: if running the selected use case default settings, refer to [Figure 11](#). If running a modified use case, use a **ADRV903x Configurator** at the top level as shown in [Figure 11](#).
 - ▶ Track the ADRV903x device programming phases through the ACE **Events** window, as shown in [Figure 11](#).
- ▶ **Program Settings**: enable exporting software resource files for the chosen configuration and init parameters. These files can then be integrated into the user application code.
- ▶ **Runtime**: evaluate the ADRV903x device performance through the following:
 - ▶ Transmitting JESD data or NCO tones using the **Tx Vectors** page.
 - ▶ Capturing receiver data using either on-chip random access memory (RAM) or JESD through the **Rx (Capture)** page.
 - ▶ Capturing observation receiver data using on-chip RAMs or JESD through the **ORx (Capture)** page.

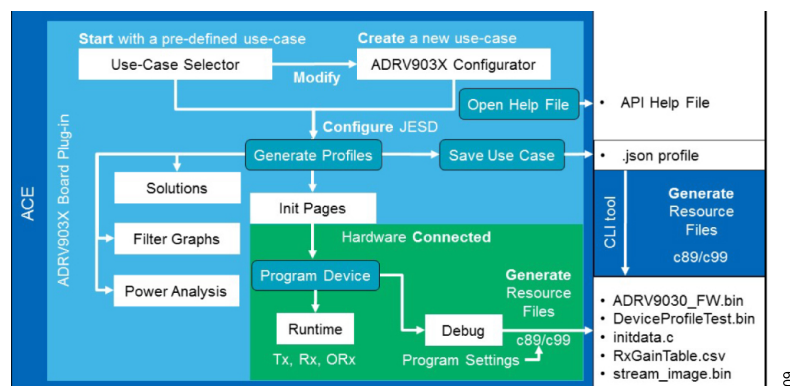


Figure 9. A Typical ADRV903x Programming Flow Where the User Programs a Use Case and Generates Software Resource Files

ADRV903x PLUGIN OVERVIEW

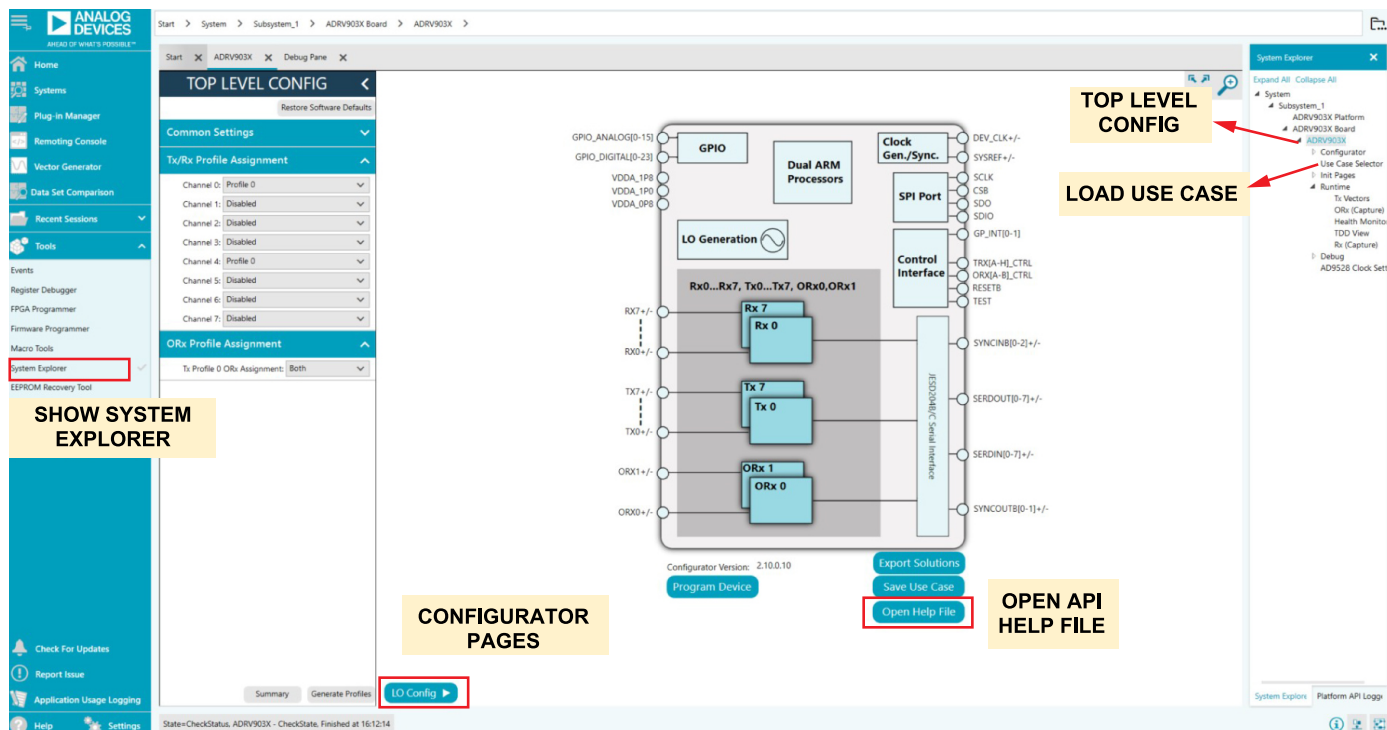


Figure 10. Launching the ADRV903x Plugin Opens the ADRV903x Configurator Top Level Config Page

ADRV903x PLUGIN OVERVIEW

USE CASE SELECTOR

This page allows the user to load the **ADRV903x Configurator** pages with a predefined use case by taking the following steps:

1. Select the desired use case from the **Use Case Selector** as shown in [Figure 11](#).
2. Click **Generate Profiles** to load the selected use case settings into the **ADRV903x Configurator** pages, or click **Program** to program the ADRV903x device using the default settings from the selected use case. By clicking **Program**, it automatically generates profiles, overriding any previous user inputs to the **ADRV903x Configurator** pages.

Note that new use cases can also be added to the **Use Case Selector** page by either providing a directory to load multiple **.json** files from or by providing direct paths to each **.json** file to be added. To add new use cases, take the following steps:

1. Navigate to **System Explorer > Use Case Selector**.
2. Click **Add Use Case Source** to add a new directory to the use case list. This directory is then displayed as a new tab.
3. Alternatively, the user can add one **.json** file at a time by selecting **Load Use Case**. This creates a new **Misc. Files** tab and multiple use cases can be added to this tab as well.

Once the **ADRV903x Configurator** pages are loaded by generating profiles, the user must then modify the selected use case default settings as shown in [Figure 11](#). Such a modified use case must be programmed from the ADRV903x **Top Level Config** page as previously shown in the [ADRV903x Plugin Overview](#) section. The modified use case can also be exported as a **.json** file from the ADRV903x **Top Level Config** page.

Note that the ADRV903x device can be programmed from two different pages within the plugin. Programming behavior changes between these two buttons, and care must be taken to retain and program any configuration changes intended by the user. The two different pages are as follows:

- ▶ **Use Case Selector** page > **Program**
 - ▶ Click the **Program** button to program the ADRV903x with the default configuration for a selected use case.
 - ▶ Clicking this button reloads the **ADRV903x Configurator** pages, which overrides any changes made by the user.
- ▶ ADRV903x **Top Level Config** page > **Program** device
 - ▶ Click the **Program** button to program the current state of the **ADRV903x Configurator** pages (as modified by the user).

ADRV903x PLUGIN OVERVIEW

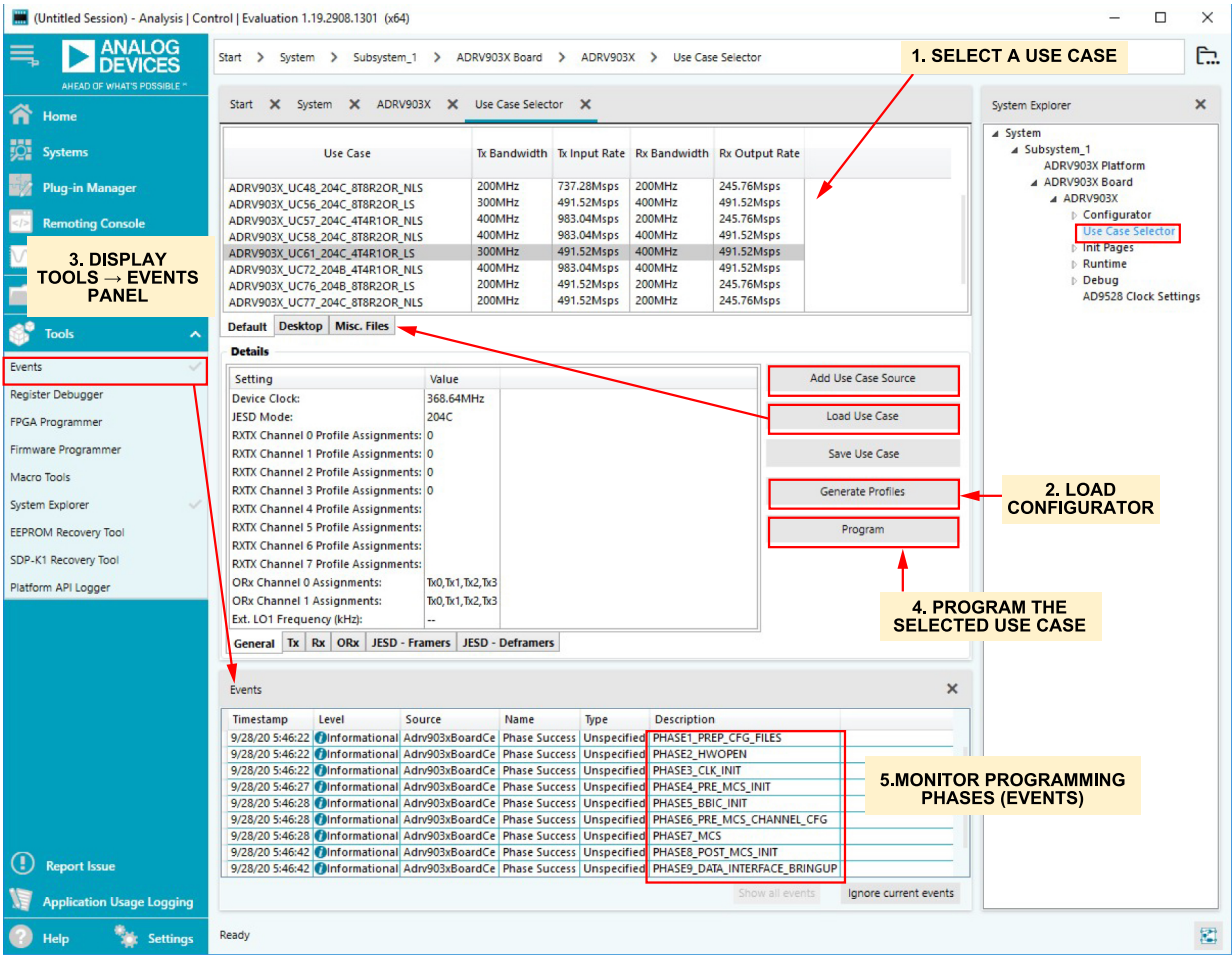


Figure 11. Loading a Predefined Use Case from Use Case Selector Page

ADRV903x PLUGIN OVERVIEW

DEVICE PROGRAMMING

Clicking either of the **Program** button from the **Top Level Config** page or the **Use Case Selector** page, which executes the 10 programming phases tabulated in [Table 1](#).

Table 1. Description of ADRV903x Programming Phases and Order of Execution

Phase	Description
PHASE1_PREP_CFG_FILES	This phase generates stream, central processing unit (CPU), digital front end (DFE), and profile binaries. This phase also copies resource files to a location available to the application processor interface (API) for the remainder of the program sequence.
PHASE2_HWOPEN	This phase calls open on the available devices on the board.
PHASE3_CLK_INIT	This phase sets up and initializes the AD9528 clock chip on the board.
PHASE4_PRE_MCS_INIT	This phase calls the ADRVGen6 PreMcsInit broadcast API function. This includes loading the CPU, stream, and profile binaries, along with the Rx gain tables.
PHASE5_BBIC_INIT	This phase sets up and initializes the available baseband processor (ADS10-V1EBZ FPGA).
PHASE6_PRE_MCS_CHANNEL_CFG	This phase calls the ADRVGen6 PreMcsInit non broadcast API function.
PHASE7_MCS	This phase calls the ADRVGen6 Multi-Chip Sync (MCS) API sequence.
PHASE8_POST_MCS_INIT	This phase calls the ADRVGen6 PostMcsInit API function and initializes calibrations.
PHASE9_DATA_INTERFACE_BRINGUP	This phase initializes the data interface on the board (JESD204B/C).
PHASE10_ENABLE_TRACKING_CALS	This phase enables tracking calibrations after full initialization and post data interface bring up.

ADRV903x PLUGIN OVERVIEW

PROGRAMMING ERRORS

Setup issues with the evaluation system, such as the CE board missing a power or clock input can cause the ADRV903x device programming to error out. [ACE Tools > Events](#) window allows the user to monitor programming progress across multiple phases and identify a phase that may have triggered an error event as shown in [Figure 12](#). Detailed error messages can be accessed from ACE **AppTrace.log** file: **C:\Users\%USERPROFILE%\AppData\Local\Analog Devices\ACE\AppTrace.log**.

Note that this log gets overwritten every time the user restarts ACE. Occasionally, multiple **AppTrace.log** files may be generated, and the most recently modified log file contains error information from the last programming attempt.

ACE **Report Issue** can be used for accessing **AppTrace.log** and reporting any unclear errors to Analog Devices for support.

Table 2. Common Programming Errors and Error Resolution

Programming Error	Resolution
There was a problem programming the device (Phase: PHASE3_CLK_INIT). See the trace log for more information.	Check the REFA clock input to AD9528 . Also verify that the REFA input from the clock source matches the REFA clock frequency set on the AD9528 clock settings page.
There was a problem programming the device (Phase: PHASE5_BBIC_INIT). See the trace log for more information.	Verify that platform files are up to date, see the ADS10-V1EBZ Platform Files Update section.
There was a problem programming the device (Phase: PHASE6_PRE_MCS_CHANNEL_CFG). See the trace log for more information.	Ensure that the CE board is powered up.

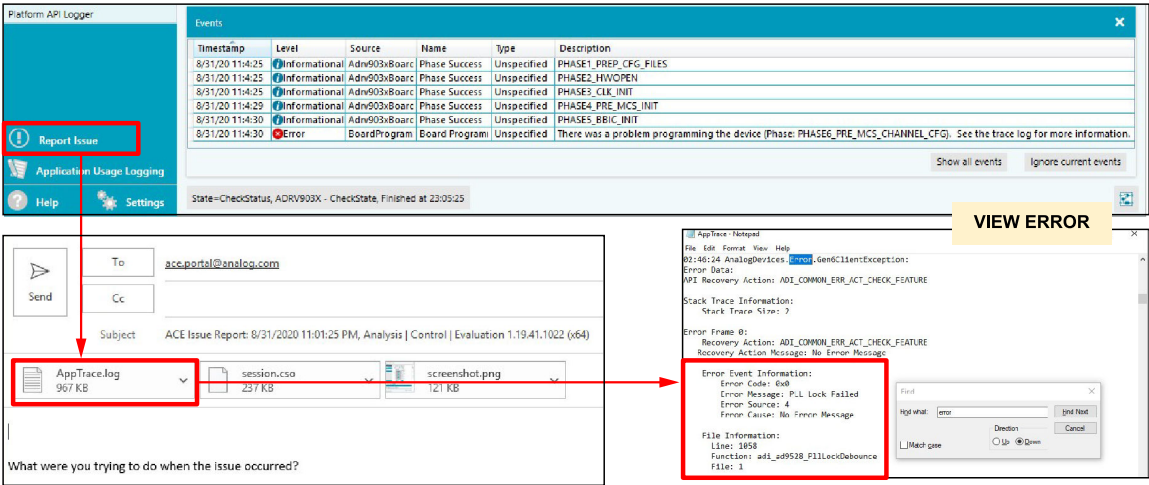


Figure 12. Procedure for Viewing Error Messages from ACE AppTrace.log File

ADRV903x CONFIGURATOR

The **ADRV903x Configurator** pages enable the user to arrive at a desired use case configuration by exploring different options available for configuring various subsystems of the ADRV903x, including the following:

- ▶ Setup of the carrier digital upconversion (CDUC), transmitter, carrier digital downconversion (CDDC), receiver, and observation receiver datapaths.
- ▶ Preview of the frequency graphs (analog, digital, and composite) for the receiver, transmitter, and observation receiver.
- ▶ JESD data interface parameters for the framers and deframers.
- ▶ LO settings.

The user must start from a known state by loading a use case from the **Use Case Selector** page and clicking on **Generate Profiles** to load the **ADRV903x Configurator** pages with a desired configuration. This function generates the transmitter, receiver, and observation receiver datapath configurations along with their corresponding filter responses for each enabled profile, as described in the following sections. Alternatively, the user can start from the default state of the configuration pages (as preloaded when the ADRV903x plugin is launched) and then provide inputs to the various configuration pages.

TOP LEVEL CONFIGURATION

On the **Top Level Config** page, the user can assign profiles for each of the transmitter, receiver, and observation receiver channels as shown in [Figure 13](#). The **ADRV903x Configurator** pairs receiver and transmitter channels together for profile assignment. For example, the user can assign Tx0/Rx0 to one profile and Tx1/Rx1 to a different profile. However, each ORx channel can be assigned separate profiles as needed. This grouping of channels for profile assignment is not a hardware constraint but it is a consequence of the current **ADRV903x Configurator** format. Profile assignment flexibility allows an 8T8R ADRV903x device configuration to be split in various ways, such as two 4T4R configurations.

Note that the term profile is not the same as a use case. A use case refers to an ADRV903x device configuration, which consists of one or more profiles, where profiles are a set of configuration parameters applied to a group of transmitter/receiver/observation receiver datapaths. This grouping by profile minimizes the time needed to set up a use case as each datapath is not configured individually.

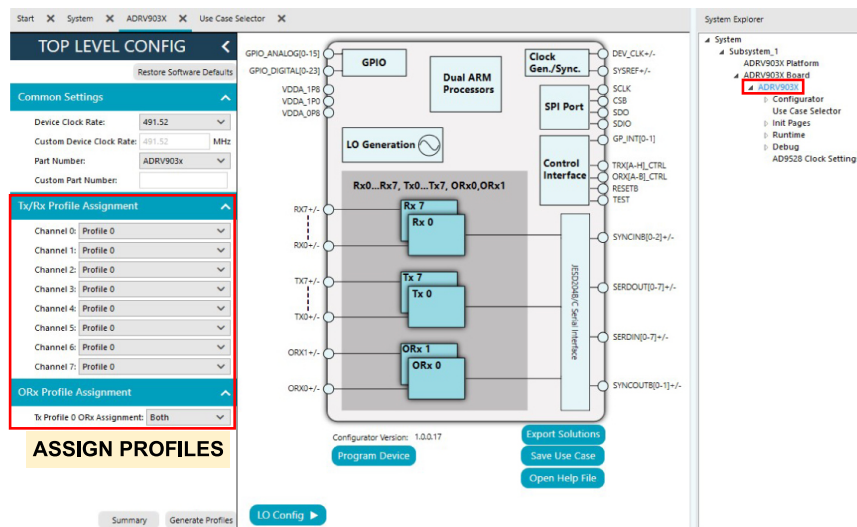


Figure 13. Top Level Config Page Showing All Tx/Rx/ORx Assigned to Profile 0

ADRV903x CONFIGURATOR

LO CONFIGURATION

After setting the desired profile mappings on the **Top Level Config** page, the user can navigate to the **LO Config** page. Click the **LO Config** button at the bottom of the **Top Level Config** page as shown in [Figure 14](#).

On the **LO Config** page, the user can set the LO frequency for each of the receiver and transmitter channels per profile, as assigned on the **Top Level Config** page. The LO selection dropdown boxes allow the user to select between **RF PLL0** and **RF PLL1** as the source of each LO. The accompanying block diagram is then updated when the user clicks on **Generate Profiles**.

Note that profile generation requires all the **ADRV903x Configurator** pages to be set up correctly, otherwise errors might occur. An error is also displayed if the user selects an out of range or invalid setting for any of the available parameters. These error messages can be accessed from the left panel of the **ACE** under **Tools > Events**. If at any point the **ADRV903x Configurator** is put into a bad state, the user can click the **Restore Software Defaults** button to return to a known good state as shown in [Figure 14](#).

Once profiles are generated without error, the LO diagram updates to show a high-level view of the LO generation setup inside the ADRV903x device for all assigned profiles, which includes the mux connections, RF phase locked loop (PLL) and voltage-controlled oscillator (VCO) frequencies, and the dividers used per receiver and transmitter channels. [Figure 14](#) shows the **LO Config** page with the LO set to **3.75 GHz**.

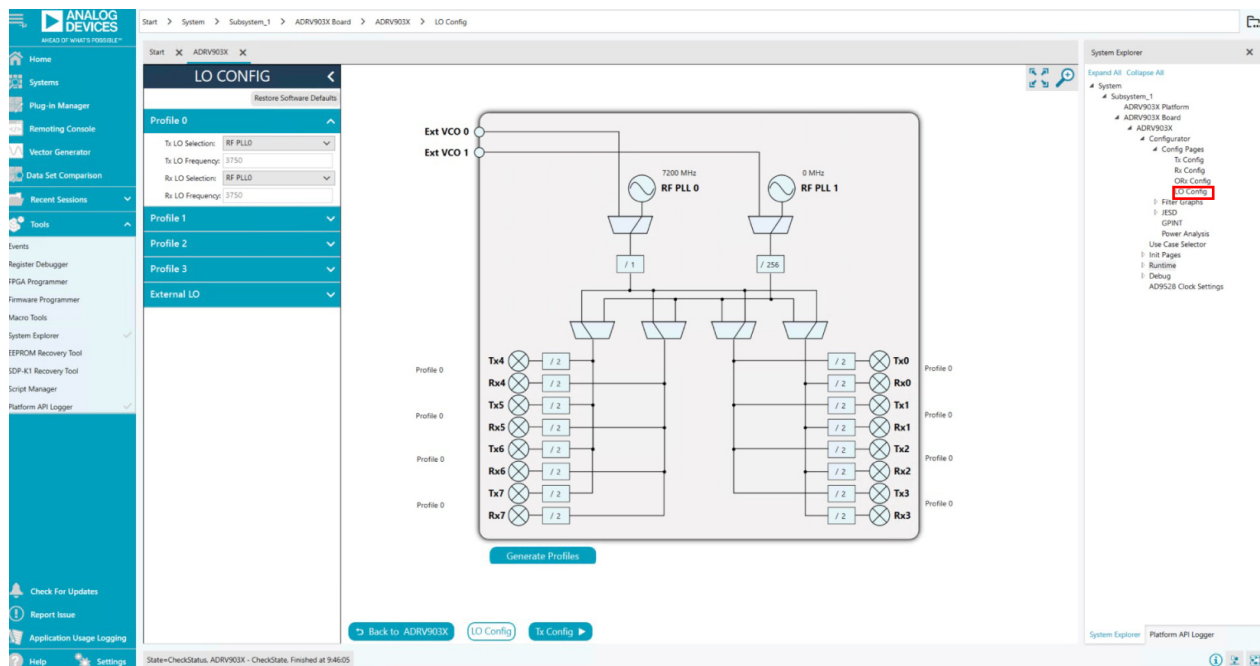


Figure 14. LO Config Page Showing ADRV903x LO Generation Setup for Given LO Frequency

ADRV903x CONFIGURATOR

LO Frequency Change Steps

The following steps describe the LO frequency change and other procedures associated with configuration changes:

1. Select the desired use case from the **Use Case Selector** and click **Generate Profiles** as shown in Figure 15.

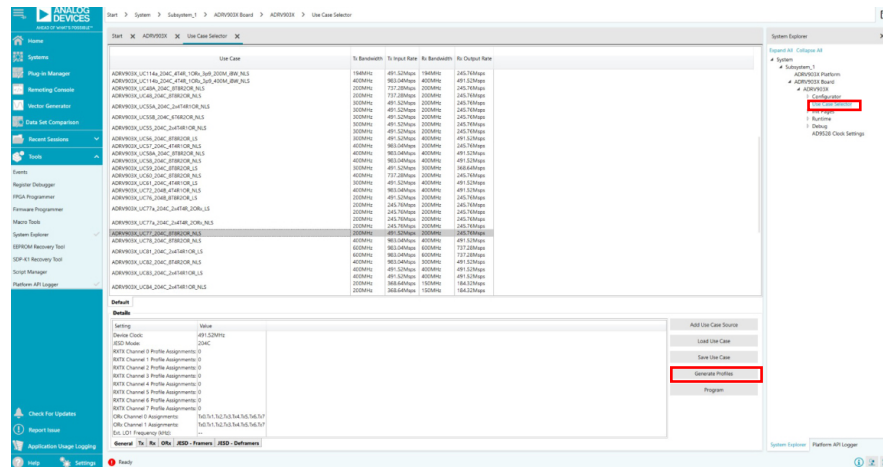


Figure 15. Generate Profiles

2. Update the RF PLL frequencies under the **LO Config** are as shown in Figure 16.

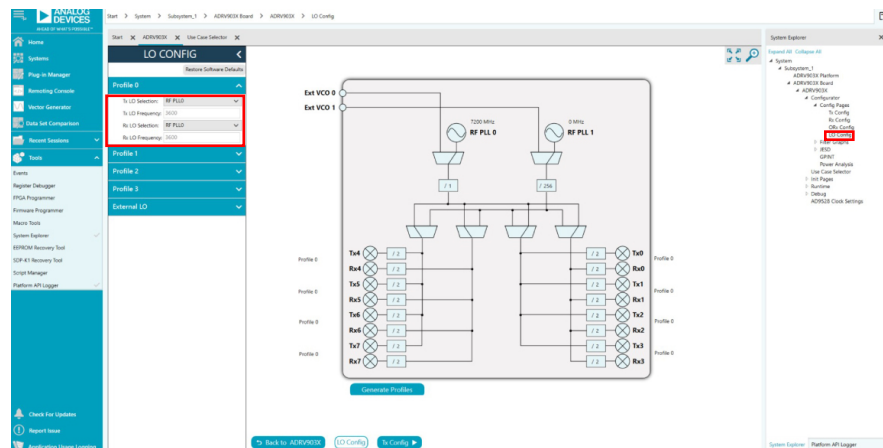


Figure 16. LO Config Page

3. Update the Tx Synthesis BW Upper Edge and Tx Synthesis BW Lower Edge boxes under the Tx Config area as shown in Figure 17.

ADRV903x CONFIGURATOR

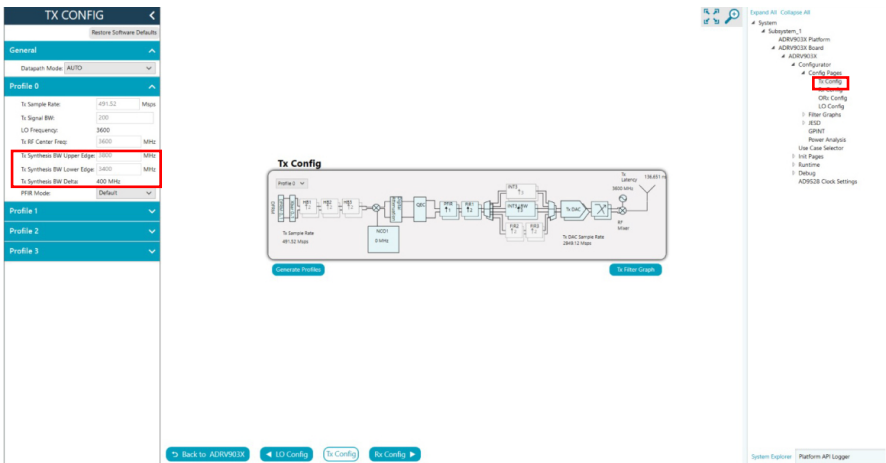


Figure 17. Tx Config Page

4. Click the **Program Device** button as shown in Figure 18. Once the device is programmed successfully, the updated LO frequency is ready to use.

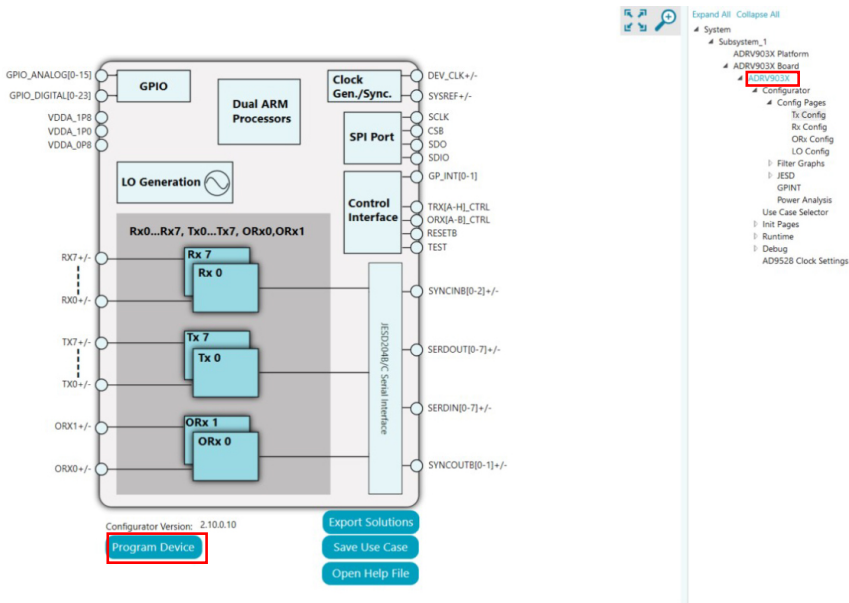


Figure 18. Top Level Program Page

ADRV903x CONFIGURATOR

TRANSMITTER CONFIGURATION

Transmitter Datapath Configuration

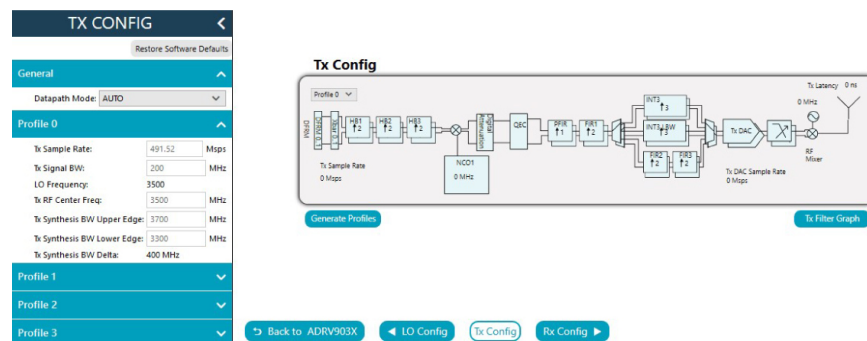
After configuring the **LO Config** page as desired, click **Tx Config** to navigate to the **Tx Config** page as shown in [Figure 19](#). **Tx Config** can also be accessed from under the configuration pages in System Explorer.

On the **Tx Config** page, the user can assign the following parameters for different profiles as mapped to transmitter channels on the top level configuration page as follows:

- **Datapath Mode** to set the data path interpolation rate, effectively selecting the transmitter digital-to-analog converter (DAC) rate
- **Tx Sample Rate** to input the data rate for data coming over JESD in MSPS
- **Tx RF Center Freq.** is the Tx band RF center. This input allows the user to displace the Tx band from LO as needed
- **Tx Synthesis BW Upper Edge** and **Tx Synthesis BW Lower Edge** to set the DPD correction bandwidth as specified by the upper and lower edge user inputs

The **ADRV903x Configurator** solved outputs populate correctly only after all the **ADRV903x Configurator** pages have been setup and the user clicks **Generate Profiles**, which is accessible from various pages. Once generated, the **Tx Config** figure updates to show the transmitter datapath configuration for the profile selected as shown in [Figure 19](#). Blocks colored blue are enabled, and blocks that remain opaque are bypassed. Calculated datapath latencies are also shown.

Note that an error displays if the user selects an out of range or invalid setting for any of the available parameters. The error message can be accessed under the **Tools** section (on the left) under the **Events** tab. If at any point the **ADRV903x Configurator** is put into a bad state, the user can click **Restore Software Defaults** at the top of the page to return to a known good state.



ADRV903x CONFIGURATOR

Transmitter Filter Graph

Corresponding transmitter filter graphs for the profile selected on the **Tx Config** page can be viewed by clicking the **Tx Filter Graph** button, which helps the user understand the frequency response of the selected transmitter profile. An example is shown in [Figure 20](#).

The transmitter filter graph includes the digital composite response, Tx DAC response, analog response, and the full composite response. The user can change the profile selection on the **Tx Config** page to display the filter graphs corresponding to the selected profile.

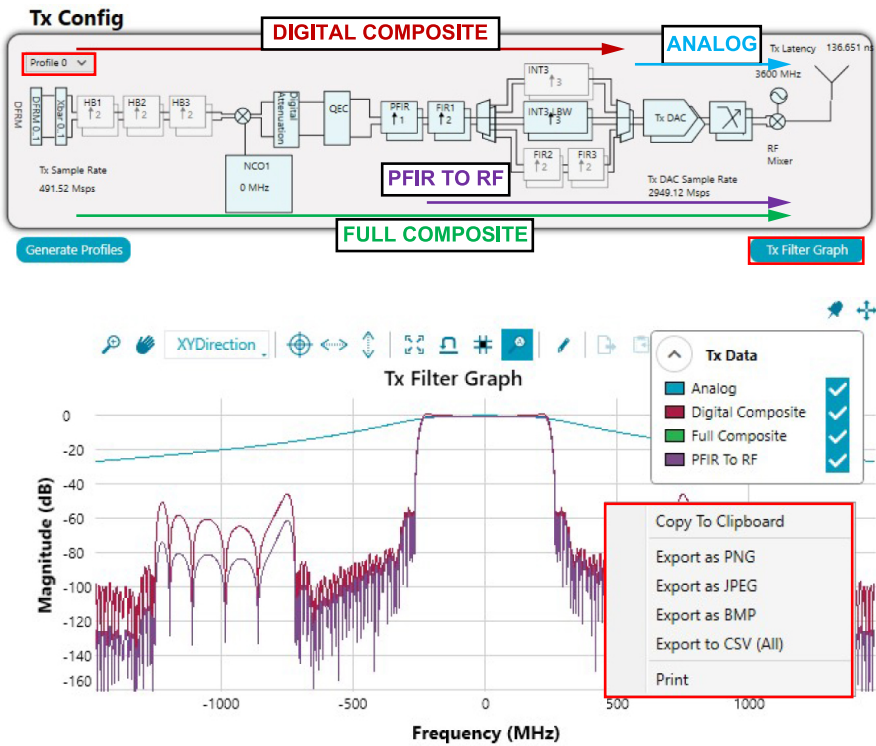


Figure 20. Transmitter Datapath Filter Graphs

ADRV903x CONFIGURATOR

RECEIVER CONFIGURATION

Receiver Datapath Configuration

The user can navigate to the **Rx Config** page found under the **Carrier DDC Config** page or by using the **ACE** system explorer. The **Rx Config** page allows the user to change the Rx datapath decimation to select a different analog-to-digital converter (ADC) rate through the datapath mode dropdown menu.

The user can input receiver parameters for different profiles in the use case by expanding the input list for each profile mapped on the top level config page. On this page, the user must set the following:

- **Datapath Mode** to set the data path decimation rate, effectively selecting the transmitter ADC rate
- **Rx Output Sample Rate** to input the data rate for data coming over JESD in MSPS
- **Rx RF Center Frequency** is the Rx band RF center that allows the user to displace the Rx band from DC as needed

The **Rx Config** page updates to show the receiver datapath configuration and latencies as shown in [Figure 21](#). Note that the profiles can only be generated successfully after all **ADRV903x Configurator** pages have been setup. A dropdown box on the top left corner of the **Rx Config** page allows the user to view **ADRV903x Configurator** solutions for different profiles as defined from the [Top Level Configuration](#) section. Blocks that are colored blue are enabled and blocks that remain opaque are bypassed.

Note that an error displays if the user selects an out of range or invalid setting for any of the available parameters. The error message can be accessed under the **Tools** section (on the left) under the **Events** tab. If at any point the **ADRV903x Configurator** is put into a bad state, the user can click **Restore Software Defaults** in the top of the page to return to a known good state.

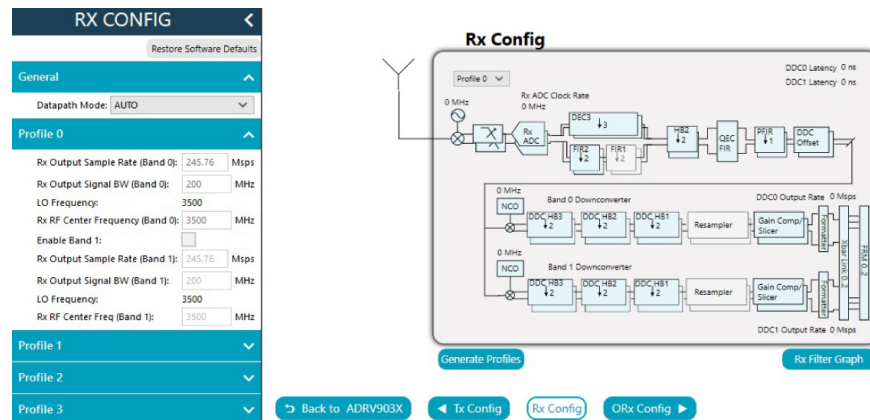


Figure 21. Receiver Configuration Wizard and Datapath Diagram Updated After Generating Profiles

ADRV903x CONFIGURATOR

Receiver Filter Graph

A corresponding receiver filter graph of the profile can be viewed via the **Rx Filter Graph** button, which helps the user understand the frequency response of the selected receiver profile. An example is shown in [Figure 22](#). The Rx filter graph includes the digital composite response, Rx ADC response, and the analog composite response. The user can change the profile selection on the **Rx Config** page to see the corresponding filter response for the selected profile.

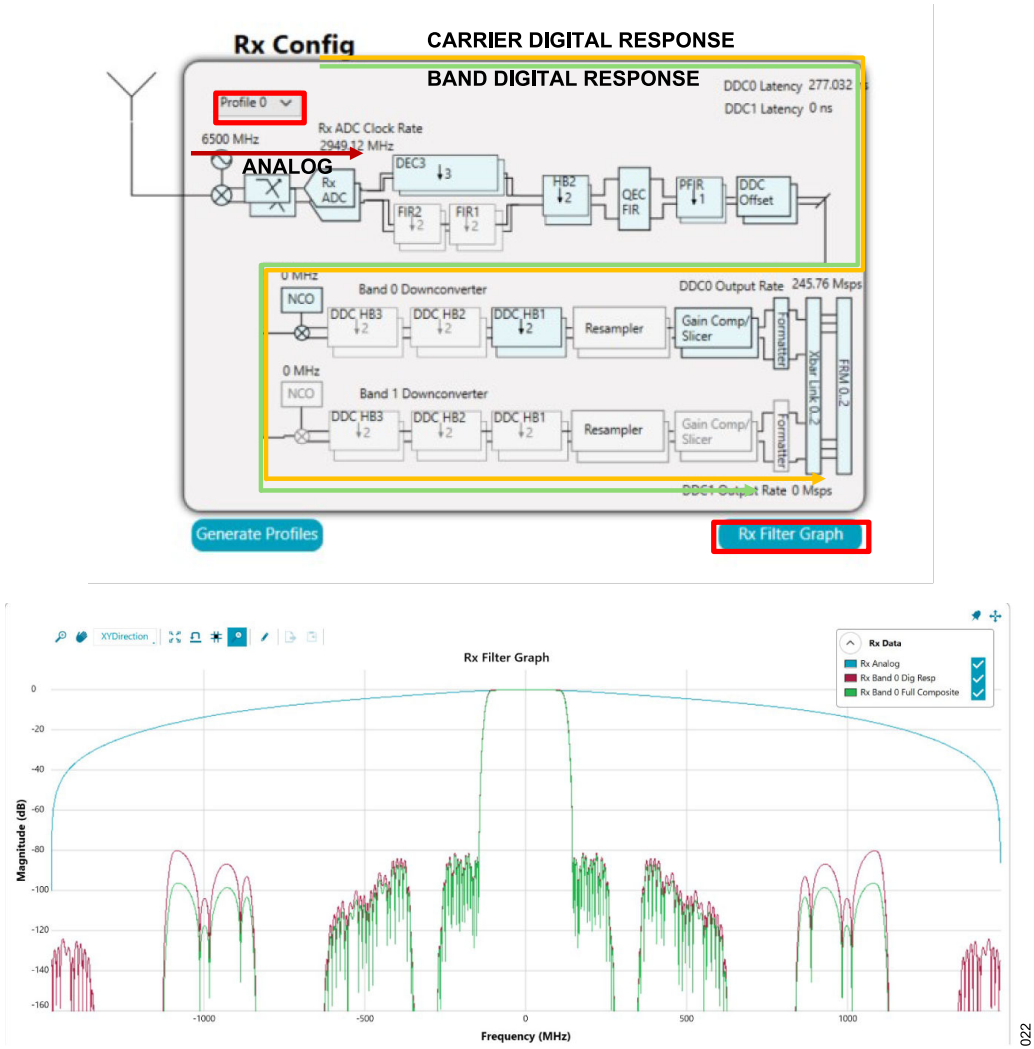


Figure 22. Receiver Datapath Filter Graphs

ADRV903x CONFIGURATOR

OBSERVATION RECEIVER CONFIGURATION

Observation Receiver Datapath

On the **ORx Config** page, the user can set the following:

- ▶ **ORx ADC CLK Rate Mode** to switch between ADC rates
- ▶ **ORx Enabled** for ORx0/ORx1
- ▶ **ORx Output Sample Rate** for the enabled ORx channels

Figure 23 shows the **ORx Config** input fields on the left panel. After configuring the remaining **ADRV903x Configurator** pages and clicking **Generate Profiles**, which can be accessed from multiple **ADRV903x Configurator** pages, the observation receiver datapath figure is updated. Switch the displayed parameters of the figure between different profiles and ORx configurations via the dropdown boxes at the top left corner of the datapath figure. Blocks that are colored blue are enabled and blocks that remain opaque are bypassed.

Note that an error generates if the user selects an out of range or invalid setting for any of the available parameters. This error can be accessed under the **Tools** section (on the left) under the **Events** tab. If at any point the **ADRV903x Configurator** is put into a bad state, the user can click on the **Restore Software Defaults** button at the top of the page.

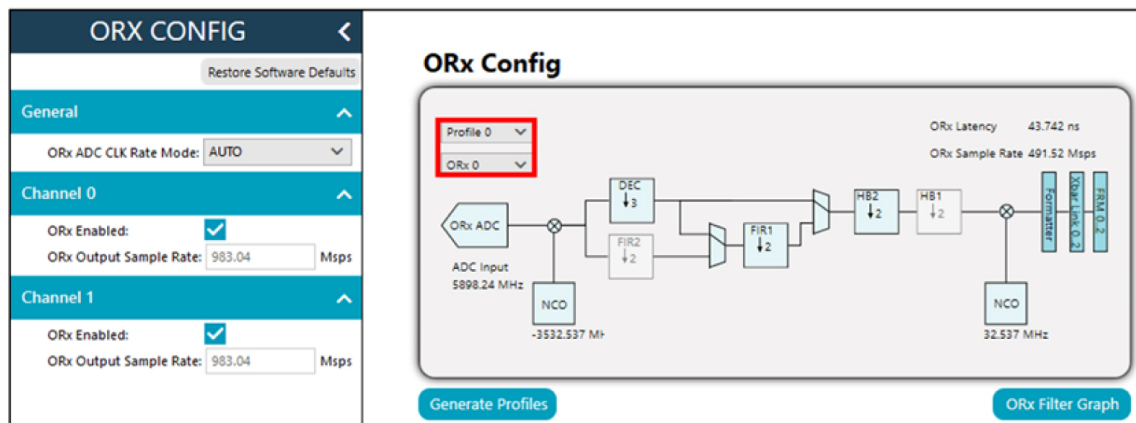


Figure 23. Observation Receiver Configuration Setup Diagram

023

ADRV903x CONFIGURATOR

Observation Receiver Filter Graph

A corresponding observation receiver filter graph of the profile can be viewed via the **ORx Filter Graph** button, which helps the user understand the frequency response of the selected observation receiver profile. An example is shown in [Figure 24](#).

In the current **ADRV903x Configurator** version, only the digital composite response of the observation receiver datapath is displayed, but analog filter contributions are not included. The user can change the profile selection on the **ORx Config** page to see the corresponding filter response for a selected profile.

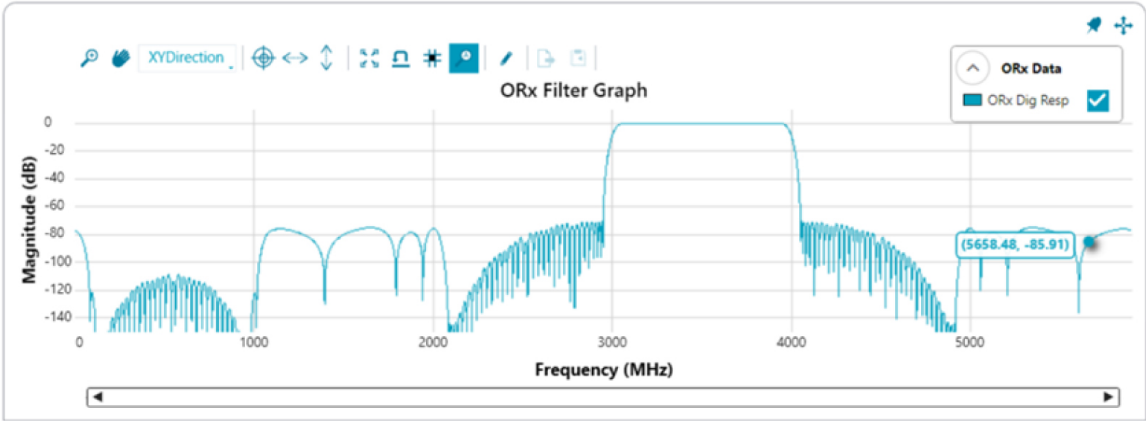


Figure 24. Observation Receiver Digital Filter Composite Frequency Response

ADRV903x CONFIGURATOR

JESD CONFIGURATION

The ADRV903x transceiver supports JESD interface standards for the serializer/deserializer (SERDES) link between the baseband unit and the transceiver to facilitate high-speed high bandwidth data transfer. The JESD interface on the ADRV903x transceiver supports JESD204B and JESD204C standards and SERDES lane rates of up to 24.3 Gbps over eight serial lanes.

The JESD configuration pages can be accessed by expanding the menu under **ADRV903x > Configurator > JESD** in the system explorer window. The user can configure the **Framer** and **Deframer** pages. The JESD configuration inputs required from the user are listed in [Table 3](#) and [Table 4](#).

Table 3. ADRV903x JESD Deframer Configuration Parameters

JESD Deframer (Tx Side) Configuration Parameters	Description
M	Number of virtual DACs on the transmitter side. Each carrier is mapped to a virtual pair of DACs. For example, if there are eight receiver channels enabled, there are 16 DACs, one converter per I and one converter per Q sample.
NP	DAC sample bit width.
L	Number of input lanes at the ADRV903x deserializer input.
F	Number of DAC bytes per frame of data.

Table 4. ADRV903x JESD Framer Configuration Parameters

JESD Framer (Rx Side) Configuration Parameters	Description
Framer Lane Crossbar	Lane crossbars settings between the framer and the serializer in the Rx path.
ADC Sample Crossbar	Sample crossbar settings between the ADC output and framer input.
M	Number of virtual ADCs on the receiver side. Each carrier is mapped to a virtual pair of ADCs. For example, if there are eight receiver channels enabled, there are 16 ADCs, one converter per I and one converter per Q sample.
NP	ADC sample bit width.
L	Number of output lanes at the ADRV903x serializer output.
F	Number of ADC bytes per frame of data.

ADRV903x CONFIGURATOR

JESD204B/C Deframer

On the **JESD204B/C Deframer** page, the user can set up the different deframers for the transmitter datapath. A snapshot of the **JESD204B/C Deframer** page is shown in [Figure 25](#).

On this page, the **ADRV903x Configurator** divides up the deframer settings as mandatory inputs, optional inputs, and crossbar selection (deframer selectors) on the left-hand side. A visual image of the deframer set up with the crossbar and lane selection is shown in the center. Note that the block diagram updates only after all other pages are configured. At the top of this block diagram, the user can switch between different deframers. A typical workflow for setting up the deframer configuration wizard follows these steps:

1. Setting up the **Mandatory Inputs**. [Figure 26](#) shows the mandatory input section of the **JESD204B/C Deframer**. Depending on the user application, the NP (converter resolution) and L (number of lanes used) parameters for each of the deframers can be setup. Note that there are a maximum of eight lanes for the ADRV903x.
2. **Optional Inputs**. [Figure 27](#) shows the optional input section of the deframer wizard. In this section, the user has the option to set up the JESD parameters E, K, and S per deframer. Typically, these values are auto calculated based on the other mandatory JESD inputs. The auto calculated values are displayed in the block diagram in the center of the page. Note that these values display only when the other **ADRV903x Configurator** pages are configured and the profiles are generated.
3. Setting up **Deframer 0 SYSREF and SYNCB** or **Deframer 1 SYSREF and SYNCB**. [Figure 28](#) shows the SYSREF and SYNCB configuration options for Deframer0. If JESD204B mode is used, then SYNCBOUT pins can be mapped to each deframer through **SYNCB Out Select**. LVDS or CMOS output pads can be enabled through **SYNCB Out LVDS Mode**, with the option to **SYNCB Out LVDS Pin Invert**. If using CMOS output, CMOS drive strength can be set by using the drive level. **SYSREF For Startup** prevents the assertion of SYNCB (for initializing link) until SYSREF has occurred. **SYSREF N Shot Enable** and **SYSREF N Shot Count** can be used to ignore possible runt pulses, such that the Nth SYSREF rising edge resets the LMFC phase. When the link is up and valid, **SYSREF Ignored When Linked** ignores any subsequent SYSREF pulses.

Once the user sets up all the sections along with selecting all the lanes on the deframer block diagram (for each of the deframers), the deframer configuration is complete. The user can now click the **Configure JESD** button at the bottom of the deframer block diagram to run the **ADRV903x Configurator**.

Note that an error generates if the user selects an out of range or invalid setting for any of the available parameters. This error list can be accessed under the **Tools** section (on the left) within the **Events** tab. If at any point the **ADRV903x Configurator** is put into a bad state, the user can click the **Restore Software Defaults** button on the top of the page.

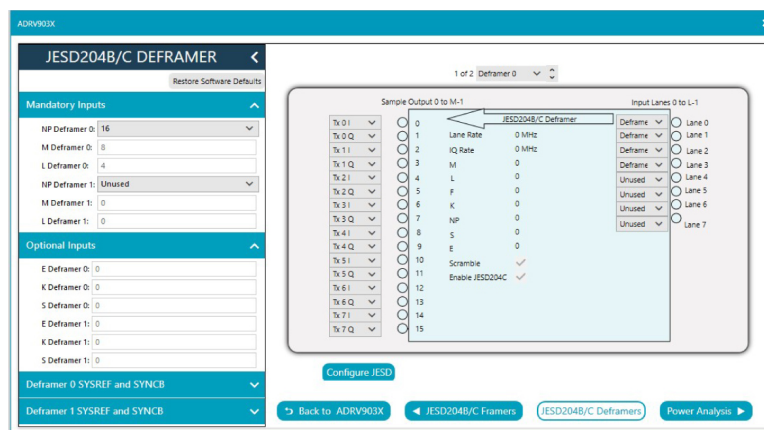


Figure 25. JESD204B/C Deframer Page

ADRV903x CONFIGURATOR

Mandatory Inputs ^

NP Deframer 0:	16	▼
M Deframer 0:	16	
L Deframer 0:	8	
NP Deframer 1:	16	▼
M Deframer 1:	0	
L Deframer 1:	0	

Figure 26. JESD204B/C Deframer Wizard Page—Mandatory Inputs

Optional Inputs ^

E Deframer 0:	0
K Deframer 0:	0
S Deframer 0:	0
E Deframer 1:	0
K Deframer 1:	0
S Deframer 1:	0

Figure 27. JESD204B/C Deframer Wizard Page—Optional Inputs

Deframer 0 SYSREF and SYNCB ^

SYNCB Out Select:	SYNCB OUT Disabled	▼
SYNCB Out LVDS Mode:	LVDS Output	▼
SYNCB Out LVDS Pin Invert:	☐	
SYNCV Out CMOS Slew Rate:	0	
SYNCB Out Drive Level:	0	
New SYSREF On Relink:	☐	
SYSREF For Startup:	☐	
SYSREF N Shot Enable:	☐	
SYSREF N Shot Count:	0	
SYSREF Ignore When Linked:	☐	

Figure 28. JESD204B/C Deframer Wizard Page—SYSREF and SYNCB Settings

ADRV903x CONFIGURATOR

JESD204B/C Framer

On the **JESD204B/C Framer** page, the user can setup the different framers for Rx and ORx datapaths. A snapshot of the **JESD204B/C Framer** page is shown in [Figure 29](#)

On this page, the **ADRV903x Configurator** separates the framer settings into three categories: mandatory inputs, optional inputs, and SYSREF-SYNCB selections, which can all be entered on the left panel. Dropdown menus for assigning the framer inputs to converter samples and the framer outputs to physical lanes are embedded in the framer figure itself. The user can switch between different framers by using the dropdown at the top of this block diagram.

Note that the values in the block diagram only get updated after setting the remaining **ADRV903x Configurator** pages and clicking **Generate Profiles** from any of the pages or by clicking **Update JESD** from the **JESD204B/C Framers** or **JESD204B/C Deframers** pages.

A typical workflow for setting up the framer configuration wizard follows these steps:

1. Setting up the **Mandatory Inputs**. [Figure 30](#) shows the mandatory input section of the **JESD204B/C Framer**. Depending on the user application, the NP (converter resolution, or N') and L (number of lanes used) for each of the framers can be adjusted. Note that there are a maximum of eight lanes for the ADRV903x. The user can enable or disable the JESD204C mode using this section. If the **Enable JESD204C** checkbox is disabled, JESD204B mode is enabled. The user can enable link sharing mode for both the framers in this section as well. This mode can be used for TDD applications where the receiver and observation receiver can use the same lanes during operation, which helps in reducing power consumption. After enabling link sharing mode, the user can set the NP parameter to be used when switching to observation receiver mode. This parameter is then added to the mandatory inputs once either **Enable Link Sharing Framer 0** or **Enable Link Sharing Framer 1** is selected.
2. **Optional Inputs**. [Figure 31](#) shows the optional input section of the **JESD204B/C Framer Wizard**. In this section, the user has the option to set up the E, K, and S JESD parameters per framer. Typically, these values are automatically calculated based on the other mandatory JESD inputs. The automatically calculated values are displayed in the block diagram in the center of the page. Note that these values display only after all **ADRV903x Configurator** pages are configured and the profiles are generated.
3. Setting up **Framer 0 SYSREF and SYNCB** or **Framer 1 SYSREF and SYNCB**. [Figure 32](#) shows the SYSREF and SYNCB selections available for Framer 0. If using JESD204B mode, **SYNCB In Select** can be used to select a SYNCB input source for each framer. **SYNCB In LVDS Mode** enables either an LVDS input pad (with an 100 Ω internal termination) or a CMOS input pad. LVDS PN can be inverted by checking off the **SYNCB in LVDS Invert Framer** checkbox. **SYSREF For Startup** requires a SYSREF before CGS is output from the serializer. **SYSREF N Shot Enable** and **SYSREF N Shot Count** can be used to ignore possible runt pulses, such that the Nth SYSREF rising edge resets the LMFC phase. When the link is up and valid, the **SYSREF Ignored When Linked** checkbox ignores any subsequent SYSREF pulses.
4. Sample inputs and framer outputs. The user can assign sample inputs and framer outputs for the framer selected using the dropdown menu in the top of the page. If the user intends to start from a blank slate, click the **Clear Inputs** and **Clear Outputs** buttons to set all sample inputs and framer outputs to **Unused**, respectively.

Once the user sets up all the sections along with selecting all the sample inputs and lane outputs on the framer block diagram (for all enabled framers), the framer configuration is complete.

Note that an error displays if the user selects an out of range or invalid setting for any of the available parameters. This error message can be accessed under the **Tools** section (on the left) under the **Events** tab. If at any point the **ADRV903x Configurator** is put into a bad state, the user can click **Restore Software Defaults** at the top of the page.

ADRV903x CONFIGURATOR

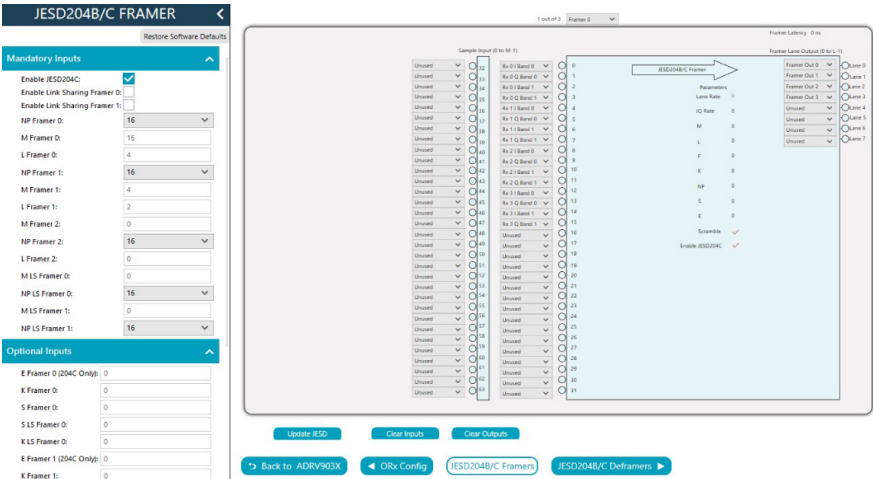


Figure 29. JESD204B/C Framer Page Showing Framer0 Block Diagram in Nonlink Sharing Mode

Mandatory Inputs

Enable JESD204C:

☒

Enable Link Sharing Framer 0:

☐

Enable Link Sharing Framer 1:

☐

NP Framer 0:

16

M Framer 0:

16

L Framer 0:

4

NP Framer 1:

16

M Framer 1:

4

L Framer 1:

2

M Framer 2:

0

NP Framer 2:

16

L Framer 2:

0

M LS Framer 0:

0

NP LS Framer 0:

Unused

M LS Framer 1:

0

NP LS Framer 1:

Unused

Figure 30. JESD204B/C Framer—Mandatory Inputs

ADRV903x CONFIGURATOR

Optional Inputs ^

E Framer 0:	0
K Framer 0:	0
S Framer 0:	0
S LS Framer 0:	0
K LS Framer 0:	0
E Framer 1:	0
K Framer 1:	0
S Framer 1:	0
S LS Framer 1:	0
K LS Framer 1:	0
E Framer 2:	0
K Framer 2:	0
S Framer 2:	0

031

Figure 31. JESD204B/C Framer—Optional Inputs

Framer 0 SYSREF and SYNCB ^

Sync In SPI Mode:	Pin Mode
SYNCB In Select:	SYNCB IN D
SYNCB In LVDS Mode:	LVDS Outp
SYNCB In LVDS Invert Framer:	☐
SYSREF On Relink:	☐
SYSREF For Startup:	☒
SYSREF N Shot Enable:	☐
SYSREF N Shot Count:	0
SYSREF Ignored When Linked:	☐

032

Figure 32. JESD204B/C Framer—SYSREF and SYNCB Settings

ADRV903x CONFIGURATOR

POWER ANALYSIS

A separate **Power Analysis** page provides power estimates for the ADRV903x configuration set using the preceding **ADRV903x Configurator** pages. The user can navigate to this page from the **Power Analysis** button under the **General Sample Crossbar** or by using the **ACE** System Explorer.

Figure 33 shows a snapshot of the **Power Analysis** page.

The **Power Analysis** page displays the current draw and power consumed per voltage supply rail, as split between the transmitter, receiver, observation receiver, and common blocks. The common block shows the combined power consumed by the VCOs, dividers, JESD blocks, general-purpose input and output (GPIO) blocks, and certain digital blocks.

In the left panel, the user can switch between configuration options to compare the associated power consumption as follows:

- **Datapath Mode** to set the transmitter and receiver datapath interpolation and decimation ratios to select different transmitter DAC and receiver ADC rates.
- **ORx ADC CLK Rate Mode** to select between observation receiver ADC clock rates.
- **Tx Attenuation** to set transmitter attenuation per channel, or copy the Channel 0 attenuation setting to all channels by checking off the **Use Shared Tx Attenuation Value** checkbox. **Tx Attenuation** is set to 6 dB by default.

In the **Power Analysis** page, the user can enter the TDD duty cycle for the transmitter, receiver, and observation receiver channels to get an estimate of the power consumed in TDD mode. Check off the **Use FDD Mode** checkbox to get the total power consumed when all transmitter, receiver, and observation receiver channels are enabled, which essentially sets the duty cycle to 100% for receiver, transmitter, and observation receiver modes. The user must click **Generate Profiles** to update the power numbers.

A typical use for the **Power Analysis** page is to get an estimate of the power consumed in different states of the ADRV903x as shown in Figure 34 to Figure 38. The displayed power numbers can also be exported to a .csv file by using the **Export** button to the top left of the **Power Analysis** page.

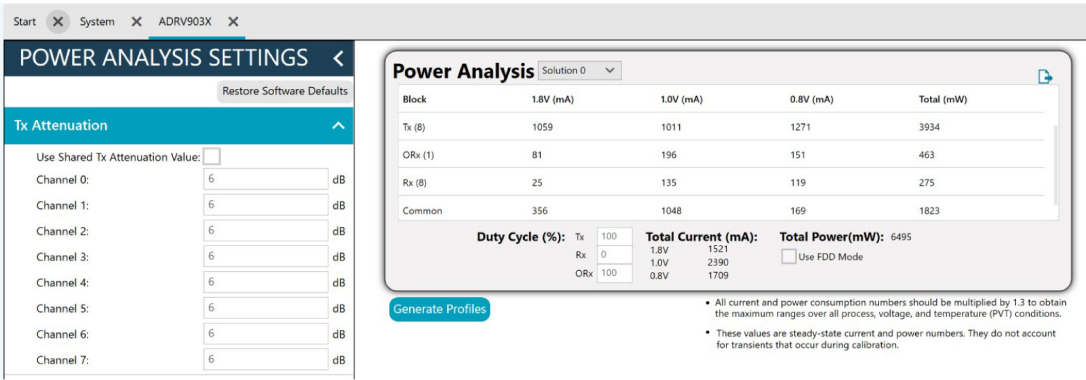


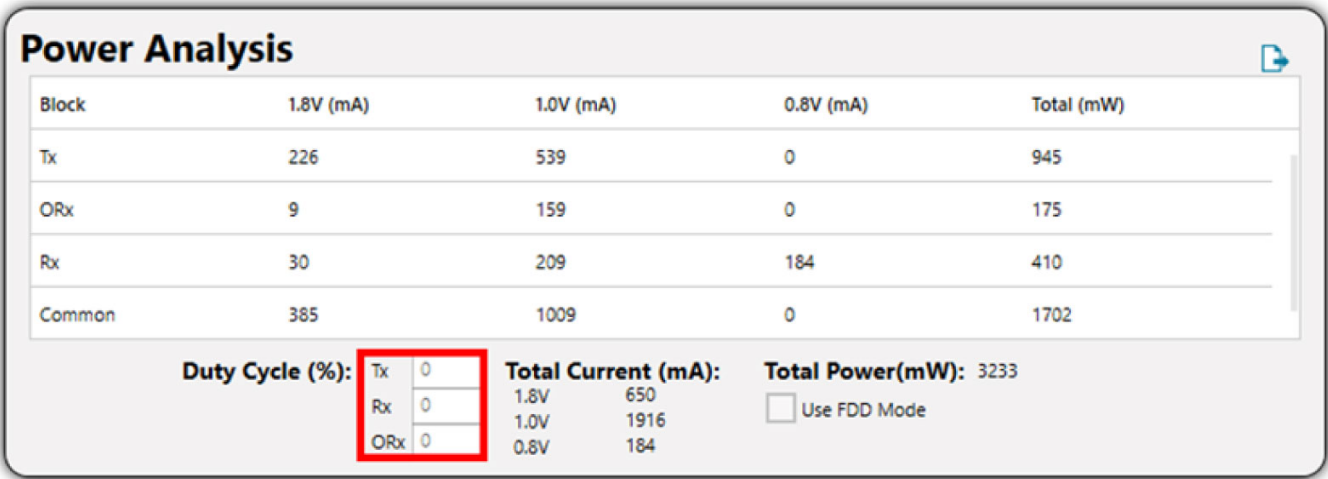
Figure 33. Power Analysis Settings and Estimates

033

ADRV903x CONFIGURATOR

Standby Mode

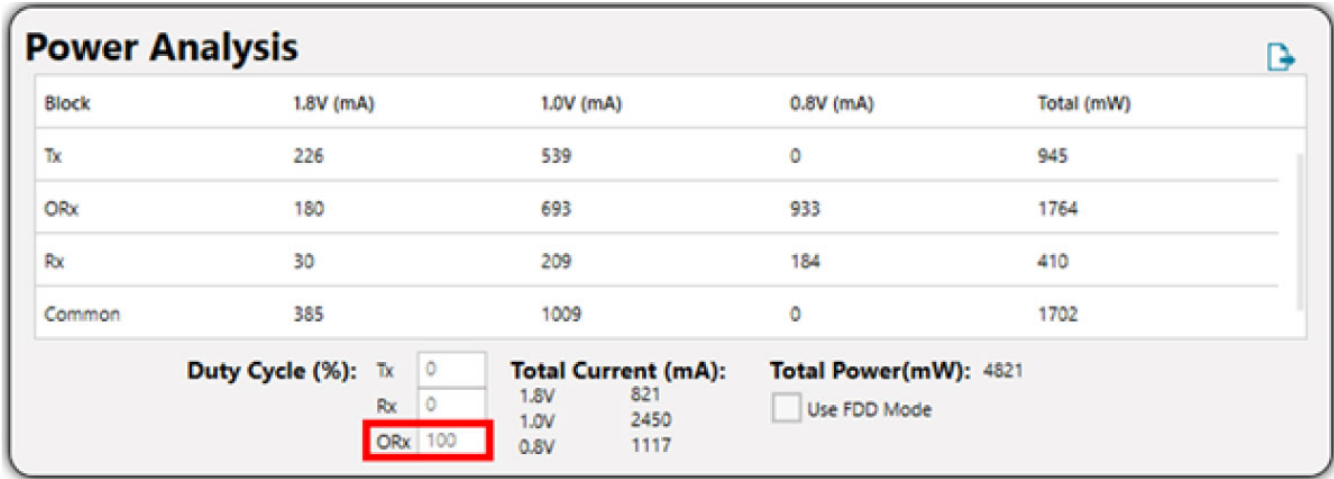
This mode represents the total standby current consumed when all transmitter, receiver, and observation receiver channels are in the off state.



ADRV903x CONFIGURATOR

Observation Receiver Only Mode

Observation receiver only mode represents the total current consumed when only observation receive channel/s are enabled. All transmit and receive channels are in the off state.

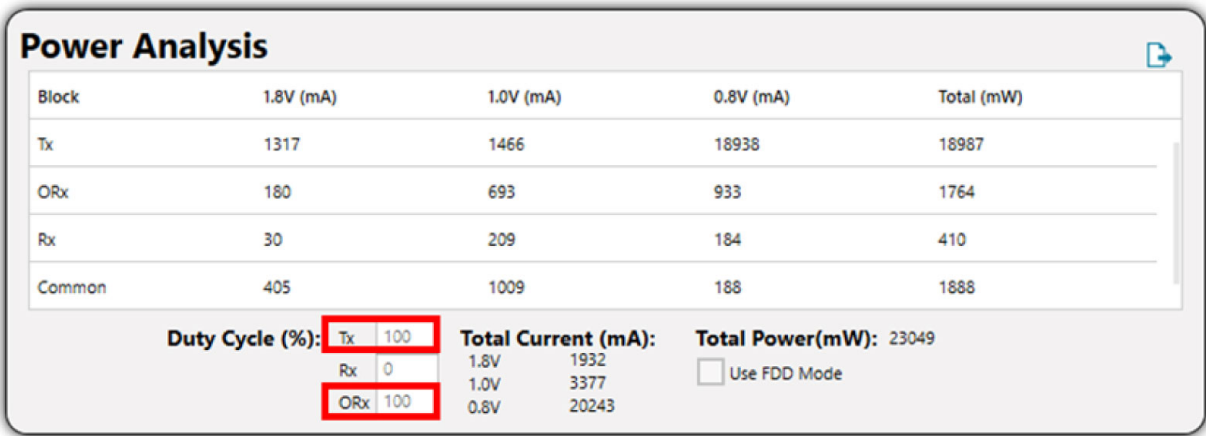


042

Figure 36. Current Consumed in ORx Only Mode

Transmitter and Observation Receiver Only Mode

Transmitter and observation receiver only mode represents the total current consumed when only the transmit channel and observation receive channel(s) are enabled. All receive channels are in the off state.



043

Figure 37. Current Consumed in Tx and ORx Only Mode

ADRV903x CONFIGURATOR

Receiver Only Mode

Receiver only mode represents the total current consumed when only receive channels are enabled. All transmit and observation receive channels are in the off state.

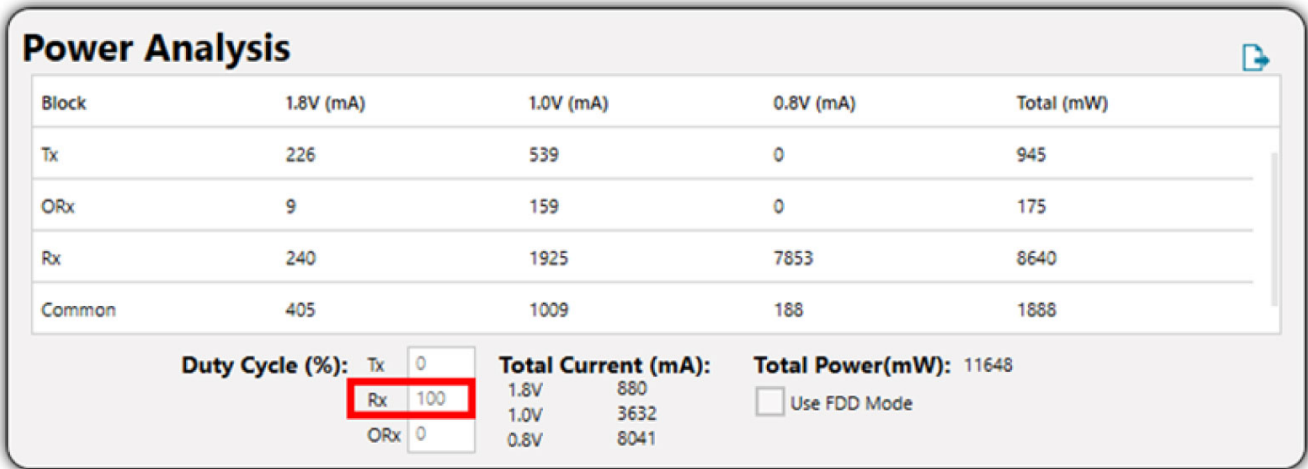


Figure 38. Current Consumed in Rx Only Mode

It is recommended that the user must estimate the TDD power by configuring ACE into the transmitter and observation receiver only mode as shown in Figure 37 and record the total power. Then, the user can configure ACE in receiver only mode as shown in Figure 38 and record the total power. Finally, the user can take a weighted average of the two to get to the correct TDD power consumed for different receiver, transmitter, and observation receiver duty cycles.

Note that the values reported are steady state current and power numbers. These numbers do not account for the transients that occur during calibration.

It is also important to note that the power numbers reported are only an estimate. Analog Devices, does not run exhaustive testing to cover all cases that can be set up using the ADRV903x Configurator. The user must contact Analog Devices Technical Support for any issues with the power consumption numbers reported by the tool.

INIT PAGES

The **Init Pages** can be used to set initialization parameters for ADRV903x device datapaths.

TX INIT

The **Tx Init** page allows users to set the initialization parameters for various Tx subsystem features .

Table 5. Tx Subsystem Features Can Be Set on the Tx Init Page (Refer to the [UG-2278 ADRV903x System Development User Guide](#) for further details)

Tx Subsystem Feature	Description
Attenuation	This feature allows user to configure Tx attenuation index and simultaneous update functions.
Ramp	This feature allows user to configure attenuation ramping. It can be used to prevent the power amplifier from damage. Tx power can be ramp down in case of average power error, peak power error, slew rate detector error, PLL unlock, and deframer IRQs.
Power Monitor	This feature can be used to configure the peak power monitor and average power monitor blocks. A peak error can be asserted if the signal power ($I^2 + Q^2$) exceeds the user-defined threshold more than the user-defined count values within the configured time window. Similarly, the signal power ($I^2 + Q^2$) is averaged over the user-defined time period, and if this average value is exceeded, the average power error flag asserts. These error flags can be used to ramp down Tx power to prevent the power amplifier from damage.
Slew Rate Detector	This feature allows users to configure the slew rate detector. Calculate the slew rate by $(I(n) - I(n - 1))^2 + (Q(n) - Q(n-1))^2$, where n is the latest sample index of both I and Q samples. If the calculated slew is greater than the user-defined threshold, a slew rate error asserts. This error flag can be used to ramp down Tx power to prevent the power amplifier from damage.

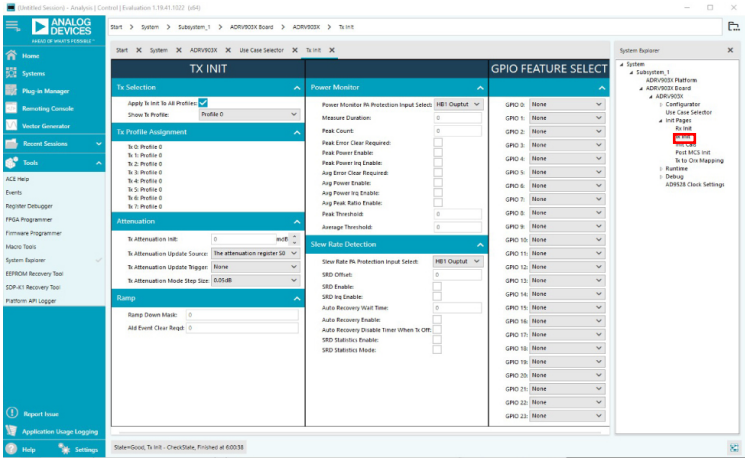


Figure 39. Tx Init Page Showing Initialization Parameters that Can Be Set by the User

INIT PAGES

POST MCS INIT

If using pin mode, the **Post MCS Init** page can be used to assign TRXx_CTRL (TRX[A-H]_CTRL) pins as enables for various ADRV903x transmitter and receiver channels through user-specified channel masks as shown in [Figure 40](#). In addition, refer to the following steps:

1. Set the **Pin Select** bit mask to 1 for each TRXx_CTRL pin to be configured as an enable. For instance, setting **Pin Select** to 0x3 selects TRXA_CTRL and TRXB_CTRL to be used as channel enables.
2. Set the **Config Select** bits to select whether pin controls are updated for transmitter, transmitter alt, receiver, and receiver alt settings.
3. If configuring transmitter enables, map the transmitter channel mask to be enabled per the TRXx_CTRL pin. For example, mapping 0xFF to TRXA_CTRL allows all eight transmitter channels to be enabled by TRXA_CTRL.
4. If configuring receiver enables, map the receiver channel mask to be enabled per TRXx_CTRL pin. For example, mapping 0xFF to TRXC_CTRL allows all eight receiver channels to be enabled by TRXC_CTRL.
5. Transmitter alt and receiver alt pin mappings can be assigned in the same way.
6. The user can program these TRXx_CTRL mappings by clicking on program device from the **Top Level Config** page. Alternatively, click **Configure Mappings** to apply the pin mappings after initialization.

TRX[A-H]_CTRL MAPPINGS

Current Mappings

Shows the channels mapped to each TRX Enable Pin.

TRXA_CTRL: Tx1, Tx2, Tx1, Tx0
 TRXB_CTRL: Rx1, Rx2, Rx1, Rx0
 TRXC_CTRL:
 TRXD_CTRL:
 TRXE_CTRL:
 TRXF_CTRL:
 TRXG_CTRL:
 TRXH_CTRL:

Selectors

Mask of pins to be configured. Unset pins will take a default value:

Pin Select:

Select whether configuration settings should be applied for Tx, Rx or both:

Config. Select:

Tx Mappings

Configure channel mappings using bit mask. High = driven by current pin.

TRXA_CTRL Tx Mask:

TRXB_CTRL Tx Mask:

TRXC_CTRL Tx Mask:

TRXD_CTRL Tx Mask:

TRXE_CTRL Tx Mask:

TRXF_CTRL Tx Mask:

TRXG_CTRL Tx Mask:

TRXH_CTRL Tx Mask:

Rx Mappings

Configure channel mappings using bit mask. High = driven by current pin.

TRXA_CTRL Rx Mask:

TRXB_CTRL Rx Mask:

TRXC_CTRL Rx Mask:

TRXD_CTRL Rx Mask:

TRXE_CTRL Rx Mask:

TRXF_CTRL Rx Mask:

TRXG_CTRL Rx Mask:

TRXH_CTRL Rx Mask:

System
 Subsystem_1
 ADRV903x Platform
 ADRV903x Board
 ADRV903x
 Configuration
 User Case Selector
 Init Pages
 Rx Init
 Tx Init
 Init Calc
 Post MCS Init
 Tx to Rx Mapping
 Runtime
 Tx Vectors
 CRx (Capture)
 Health Monitoring
 TDD View
 Rx (Capture)
 Debug
 ADRV903x Clock Settings

040

Figure 40. TRXA_CTRL to TRXH_CTRL Pins Mapped as Tx/Rx Datapath Enables on Post MCS Init Page

INIT PAGES

CALIBRATION

Device calibrations to be run during ADRV903x initialization can be enabled or disabled from the **Init Pages > Init Cals**. Refer to the release notes accompanying the given customer software package for more information regarding supported calibrations.

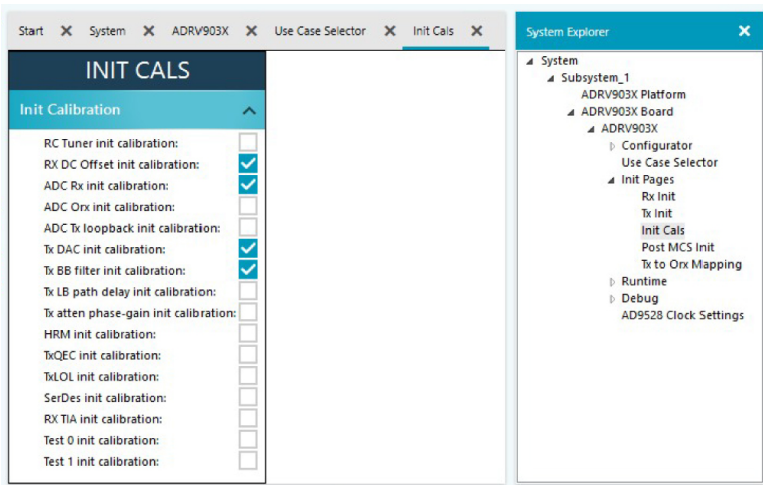


Figure 41. Calibration Page Used to Update the Init Calibration Mask Run During Initialization

INIT PAGES

AD9528 CLOCK SETTINGS

The CE board comes with an [AD9528](#) clock generator that takes a **Ref A Clock** input and generates the ADRV903x device clock and the FPGA device clock as outputs. The CE board includes a voltage-controlled crystal oscillator (VCXO) running at 122.88 MHz.

The **AD9528 Clock Settings** page can be used to program the ADRV903x using a clock input different from the default. After configuring this page, the user must program the ADRV903x from the **Top Level Config** page, the **ADRV903x**.

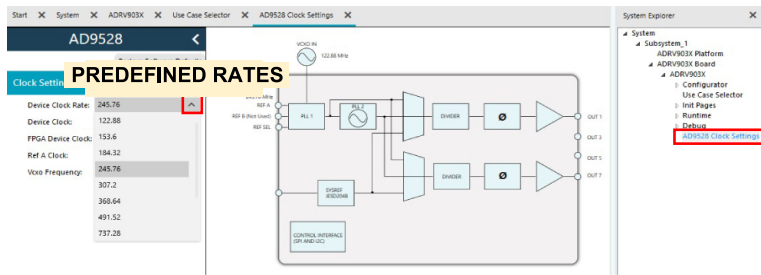


Figure 42. AD9528 Clock Settings Page for Changing Clock Generator Settings

RUNTIME

Once programmed, the runtime pages can be used for testing the performance of different ADRV903x datapaths. These runtime pages provide data sourcing capability for the transmitters, and capturing functionality for the receivers and observation receivers.

TRANSMITTER VECTORS

Transmitter performance can be evaluated by sending data over the JESD link, or by generating test tones using ADRV903x on-chip NCO in each baseband of a transmitter datapath. The vector generator of [ACE](#) can be used for creating new data vectors or importing vectors from existing data files, and can also be used to change attenuation settings for each enabled transmitter.

Generating JESD Data Vectors

For illustration, a single tone vector was generated using the following steps:

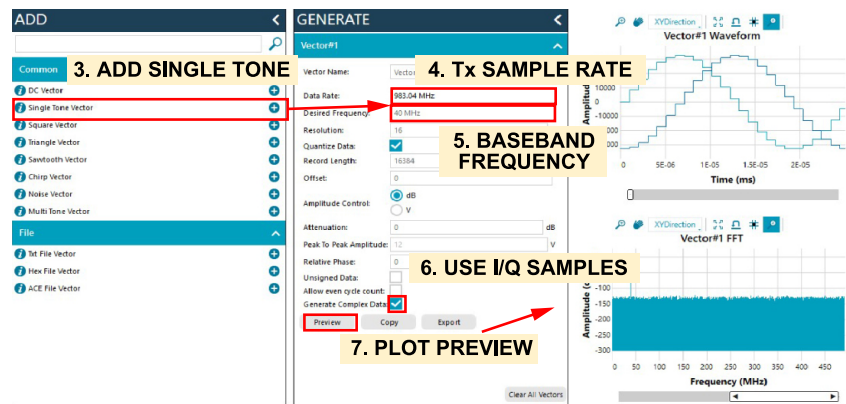
1. Launch **Tx Vectors** from **System Explorer > Runtime > Tx Vectors** as shown in [Figure 43](#).
2. Click on **Vectors** to open the vector generator of ACE.
3. Create a new single tone vector by clicking on **+** besides the **Single Tone Vector** under **Common > Waveforms** as shown in [Figure 44](#).
4. Set the data rate of the vector to match the transmitter sample rate (as configured in the [Use Case Selector](#) section or the [LO Frequency Change Steps](#) section).
 - ▶ Data rate must match the carrier sample rate for CDUC and CDDC profiles.
 - ▶ For FDD, the play length (time) must be equal for each carrier. For example, the record length of a 122.88 MHz carrier should be four times the record length of a 30.72 MHz carrier.
 - ▶ Change the record length of the vector as per the sample rate.
5. Set the desired baseband frequency of the tone.
6. Select **Generate Complex Data** to generate a data vector containing I and Q samples.
7. Preview the vector to verify parameters. If needed, this vector can be exported to a text file by clicking **Export**.
8. Switch back to the **Tx Vectors** page. However, do not close the **Vector Generator** tab completely by pressing **x**. The **Vector Generator** must remain open as a background tab for the vectors to be selectable on the **Tx Vectors** page.
9. Enable the desired transmitter channel(s) and transmitter observability from the **Tx Vectors** page.
10. Configure each transmitter channel data input to the intended vector, as named and defined on the **Vector Generator**.
 - ▶ For profiles with CDUC or CDDC enabled, users can map a specific vector to each carrier as shown in [Figure 45](#).
11. Update the **Tx Attenuation** (dB) field as needed.
12. Enable the quadrature error correction (QEC) and local oscillator leakage (LOL) tracking calibrations.
13. **Play** transmitter data continuously over JESD to update the waveform and fast Fourier transform (FFT) plots to preview the loaded vectors. The transmitter RF output can then be captured using a spectrum analyzer as shown in [Figure 45](#).
14. Click **Stop** to halt the data transmission.

RUNTIME



043

Figure 43. Tx Vectors Page is Used to Enable Tx Channels, Map Vectors to Each Enabled Tx, and Plot the Baseband Vectors



044

Figure 44. Steps for Generating a Complex Single Tone Vector Using ACE Vector Generator

RUNTIME

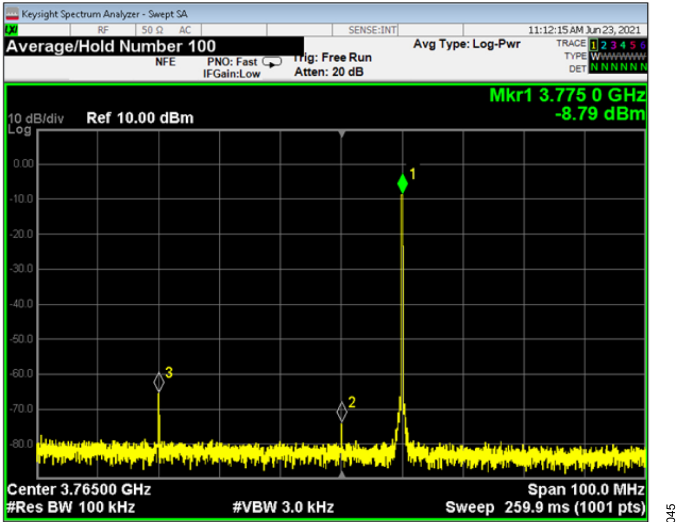


Figure 45. Tx0 Single Tone Spectrum as Captured by a Spectrum Analyzer

RUNTIME

Exporting and Importing JESD Data Vectors

The **Vector Generator** page also allows exporting and importing of vectors. The user can export a vector from **Vector Generator** by clicking on **Export** from the **Generate** panel as shown in [Figure 46](#). This writes the vector out to a **.txt** file in the **ACE** export data directory **C:\Users\%USERPROFILE%\AppData\Local\Analog Devices\ACE\ExportData**.

This vector can be imported back into the **Vector Generator** as follows:

1. Click **+** to add a **.txt** file vector.
2. Select **Complex – Interleaved**. ACE generated **.txt** vectors are a single column with I- and Q-samples interleaved.
3. Match data rate to the transmitter sample rate (as configured by in the [Use Case Selector](#) section or [LO Frequency Change Steps](#) section).
4. Click on **Preview** to confirm the vector parameters.

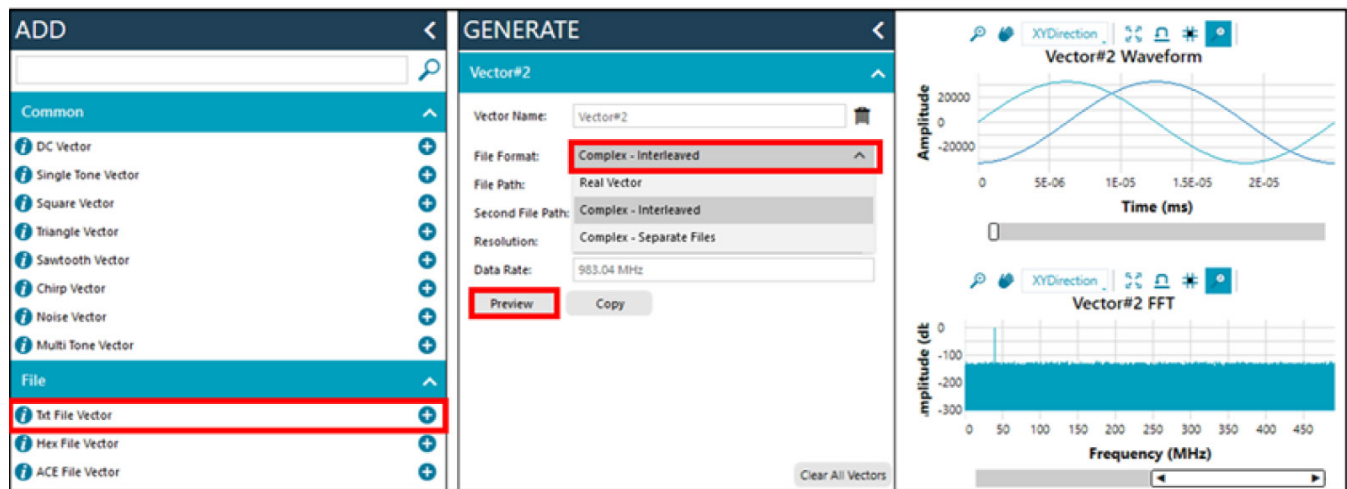


Figure 46. Importing a .txt File Vector into a Vector Generator

Setting Transmitter Attenuation

Transmitter attenuation can be set in dB for each enabled transmitter channel individually.

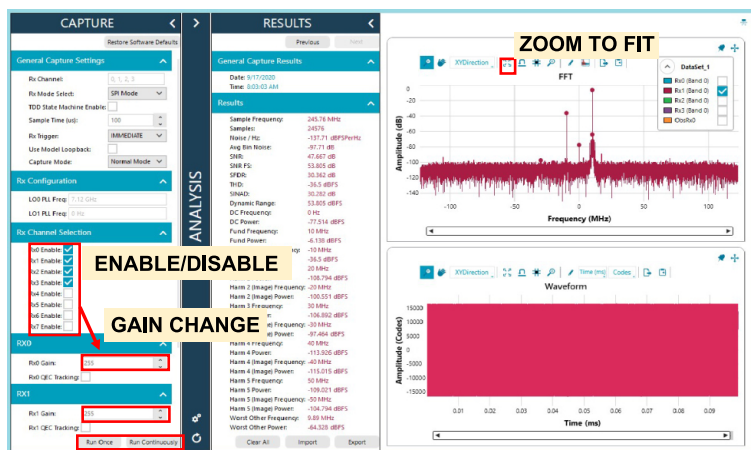
Note that transmitter attenuation changes are only applied when the user clicks **Play**.

RUNTIME

Rx (CAPTURE)

Receiver data can be captured over JESD and analyzed using the **Rx (Capture)** page as shown in [Figure 47](#). The user must do the following:

1. Navigate to **System Explorer > Runtime > Rx (Capture)**.
2. Confirm that the desired receiver channels are enabled. If using a link sharing profile, ensure that no observation receiver channels are enabled at this time. Observation receiver channels can be disabled from the **System Explorer > Runtime > ORx (Capture)** page.
3. Click **Run Once** or **Run Continuously** to capture data.



047

Figure 47. Rx (Capture) Used to Capture and Analyze Receiver Outputs over JESD

Setting Receiver Gain

The gain index for any enabled receiver channel can be changed by either entering a new gain index or by using the arrowheads to increment/decrement the gain index in steps of one. Gain changes are applied to the ADRV903x as soon as the values are updated, regardless of the data capture state whether halted or running continuously.

RUNTIME

Enabling Receiver QEC Tracking

The user can additionally enable QEC (receiver QEC tracking) calibration for each enabled receiver as shown in [Figure 48](#).



Figure 48. Rx Capture Performed after Enabling Rx QEC Tracking for Rx0

It is important to take note of the following if using a link sharing profile:

- ▶ Only receiver channels must be enabled when attempting to capture receiver data.
- ▶ Currently, the user must disable any additionally enabled observation receiver channels from the **ORx (Capture)** page before receiver data can be captured over the shared JESD link.
- ▶ The user can click the **Zoom to Fit** icon to correctly rescale the FFT plot when switching between receiver and observation receiver.

RUNTIME

ORx (CAPTURE)

The process for capturing observation receiver data is similar to the **Rx (Capture)** process as shown in Figure 49. The process is as follows:

1. Navigate to **System Explore > Runtime > ORx (Capture)**.
2. Confirm that the desired observation receiver channels are enabled. Note that when using a link sharing profile, ensure that no receiver channels are enabled at this time. Receiver channels can be disabled from the **System Explore > Runtime > Rx (Capture)** as shown in Figure 49.
3. Under **Capture Mode**, select **Normal Mode**, which captures the observation receiver data over the JESD link.
4. Click **Run Once** or **Run Continuously** to capture the data.



Figure 49. ORx0 and ORx1 Data Captured over JESD Link with Tx LO and 10MHz Input Tone Applied to ORx0

Setting Observation Receiver Attenuation

Observation receiver attenuation can be entered in dB for each observation receiver channel. Attenuation changes are applied to the ADRV903x as soon as the user clicks on **Enter** in data capture state (halted or running continuously).

Setting ORx1 attenuation through the **ORx (Capture)** page might not work as expected. This is expected to be addressed in the upcoming releases of the ADRV903x plugin.

RUNTIME

TDD VIEW

The setup TDD timings for each TRXx_CTRL pin configured on the **Post MCS Init** is detailed in this section. The procedure follows:

1. Enter start and stop times to specify a time range for driving each TRXx_CTRL pin. Four start and stop time ranges can be specified per pin. LTE presets can also be applied to each TRXx_CTRL pin from under **LTE Presets**. [Figure 50](#) applies **4G LTE 0 (Tx)** preset to **TRXA_CTRL LTE** and **4G LTE 0 (Rx)** preset to **TRXB_CTRL LTE**.
2. Click **Apply** to plot the TDD timings for review, which only updates the plot but does not enable the TDD.
3. Click **Configure** to configure the TDD state machine using the specified timings, which enables the TDD state machine (the **Enable TDD FSM** checkbox). To perform data sourcing and capture in TDD mode, the user must additionally modify capture settings on the **Runtime** pages, as illustrated in [Figure 51](#).

Delay Settings on the **TDD View** page can be used to add delays per the JESD link between the enable inputs and data outputs.

Miscellaneous settings can be used to loop the TDD frame timings continuously.

TDD can be disabled by unselecting the **Enable TDD FSM** checkbox. Note that clicking **Configure** is not required for disabling TDD FSM because **Configure** reselects the **Enable TDD FSM** checkbox.

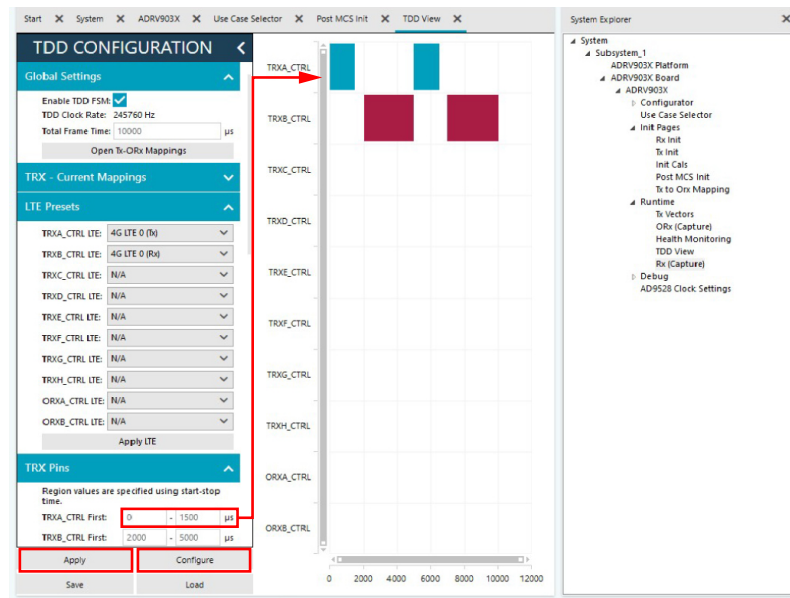


Figure 50. TDD Configuration Page Used to Specify the Enable Timing for Each TRXx_CTRL Pin and Configure the TDD State Machine

RUNTIME

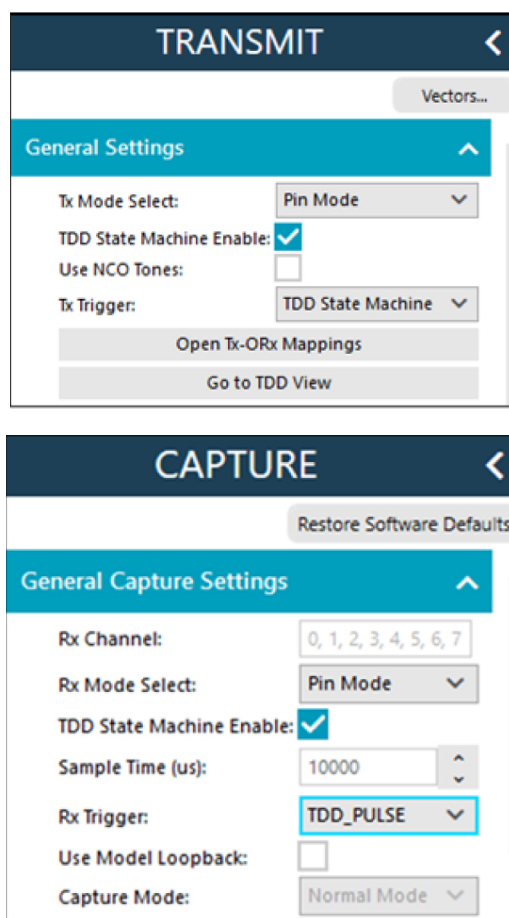


Figure 51. Runtime Pages Updated to Trigger Data Source and Capture Using the TDD State Machine for Rx

FFT ANALYSIS

On the **Rx (Capture)** and **ORx (Capture)** pages (see [Figure 48](#) and [Figure 49](#)), each provides data analysis tab that allows the user to manipulate the FFT calculations to best fit their requirements. The user can configure FFT analysis settings, manipulate FFT durations, and perform simple spur analysis. On both **Rx (Capture)** and **ORx (Capture)** pages, the **Analysis** tab provides information about the received signal. This tab is directly related to the **Results** tab, such that the selections determine the information presented to the user.

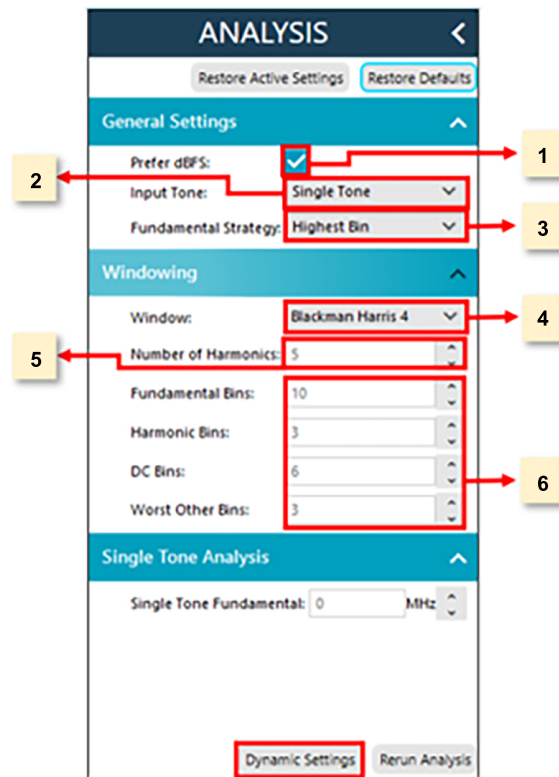
Analysis Settings

Users can select their preference on how results of the FFT analysis are generated and determine what is presented in the **Results** tab. The following are the key options available to users:

- ▶ Select preference tones power measurements in dBc or dBFS.
- ▶ Specify a 1-tone or 2-tone analysis for information on harmonics or intermodulation.
- ▶ Select options for the strategy used to find the fundamental tones, such as the following:
 - ▶ Highest bin
 - ▶ Mirror image
 - ▶ Fixed
- ▶ Select the type of windowing used in FFT spectrum generation, such as the following:
 - ▶ Blackman Harris 4 (default)
 - ▶ Blackman Harris 7
 - ▶ Blackman Harris 7 scaled
 - ▶ Hann

RUNTIME

- ▶ None
- ▶ Specify the number of harmonics reported, such as the following:
 - ▶ Harmonics; single-tone analysis
 - ▶ Intermodulations; two-tone analysis
- ▶ Specify the number of bins used during the FFT analysis power calculations for the following:
 - ▶ Fundamental tones
 - ▶ DC components
 - ▶ Worst other (spurs)



052

Figure 52. Analysis Tab with Default Parameters

RUNTIME

FFT Ranges

For some operations, the user does not need the FFT analysis to cover the full capture duration, especially during TDD operations where the duration of capture is much larger than the duration of the desired signal. The rest of this section explains how to use this feature through the framework of a TDD operation outlined in [Figure 53](#). For this example, the Tx0 and Tx4 outputs tones of 10 MHz and 30 MHz delta from LO, respectively. The two transmitters are then combined using a splitter, and the resulting signal is sent into another splitter, which is then fed to ORx0 and Rx1.

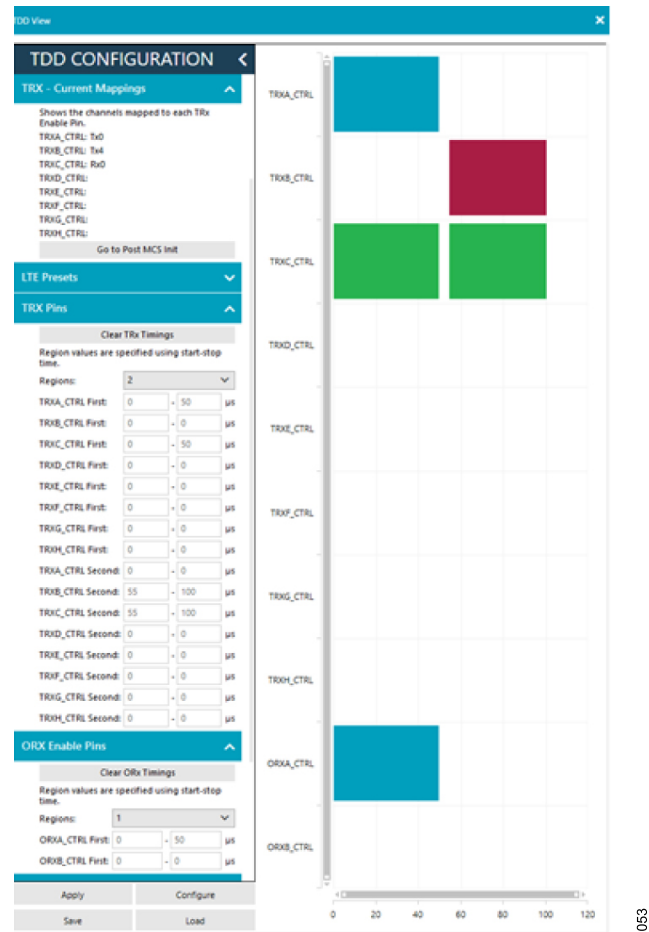


Figure 53. Example TDD Configuration to Demonstrate Dynamic FFT Duration Feature

RUNTIME

Adding an FFT Range

On the **ORx (Capture)** page with a capture period equal to the TDD frame of 100 μ s, a regular capture does not produce a true FFT representation of the signal received during the slot seen in [Figure 54](#). Therefore, it is essential to use the FFT duration feature available through the **Dynamic Settings** available on the **Analysis** tab as shown in [Figure 52](#).

Upon clicking **Dynamic Settings**, a pop-up window, as shown in [Figure 55](#), appears. To add an FFT range, take the following steps:

- 1. Click on **+** to create an instance of the FFT range.
- 2. Select the appropriate channel.
- 3. Set the starting sample index in reference to the capture period.
- 4. Set the number of samples used for analysis.

Take note of the following:

- All numerical inputs involved with adding an FFT range is in terms of samples.
- The **Startindex** and **MaxSampleCount** values define the range of the FFT analysis.
- For each channel, only one FFT range is allowed.
- Each FFT range addition or update must be followed by clicking **Rerun Analysis** in the **Analysis** tab.

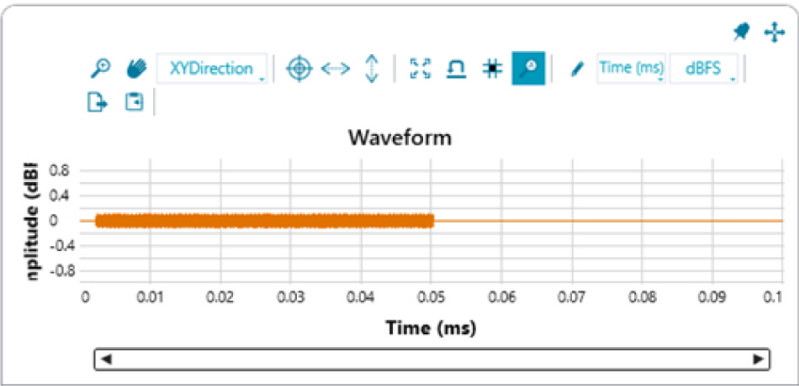


Figure 54. ORx Capture for FFT Duration Example

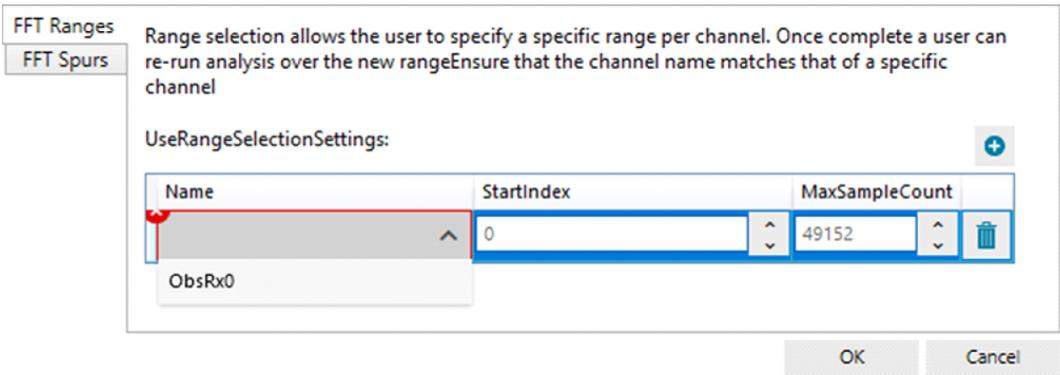
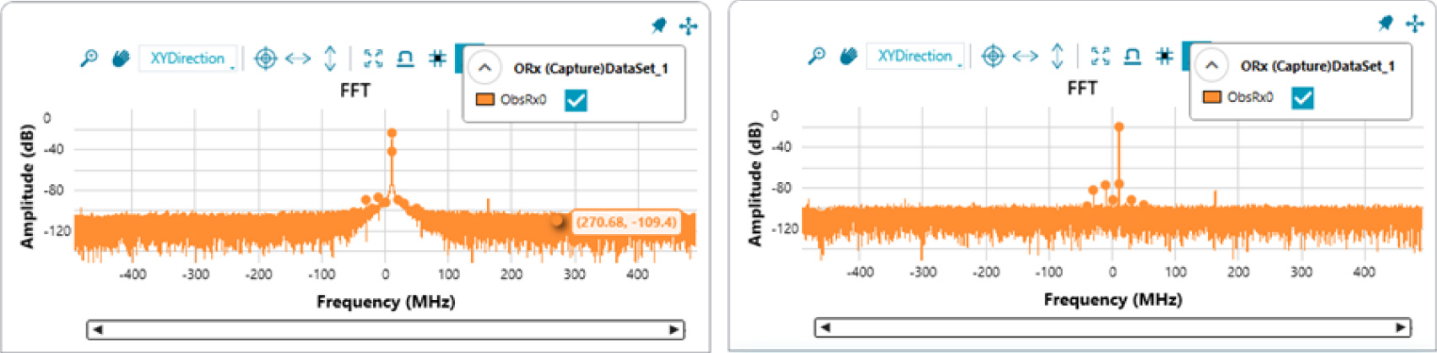


Figure 55. FFT Range Settings Window

RUNTIME



(A) BEFORE FFT RANGE

(B) AFTER FFT RANGE

Figure 56. ORx Capture FFT Plot Before and After Applying FFT Range

056

RUNTIME

Inserting Spur

The user can perform simple spur analysis by inserting spurs to track the power measurements of a specific spur. This feature can be accessed through the **Dynamic Settings** as shown in Figure 52. The following outlines the use of this feature.

For this demonstration, the ORx is used to capture a 20 MHz tone. Because of the direct conversion from the RF, there is a significant spur at approximately 153 MHz. The following steps are recommended for adding a spur:

- 1. Upon clicking **Dynamic Settings**, a pop-up window appears.
- 2. Select the **FFT Spurs** tab and the window in Figure 57 appears.
- 3. Set the following parameters:
 - a. Provide a **Name** for administrative purposes.
 - b. Set **Frequency** in MHz.
 - c. Set spur **SingleSideBand** (SSB).
 - d. Select **Units** of SSB.
 - e. Specify whether spur is considered in noise calculations.
 - f. Enable or disable spur.
- 4. Click **OK** followed by clicking **Rerun Analysis** in the **Analysis** tab.

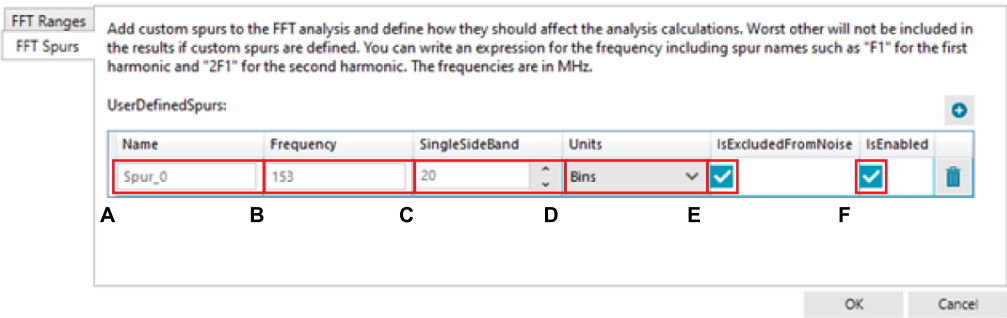
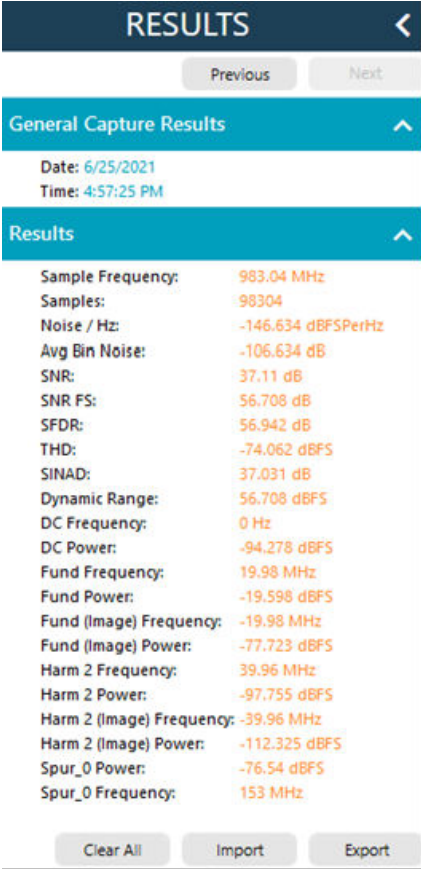
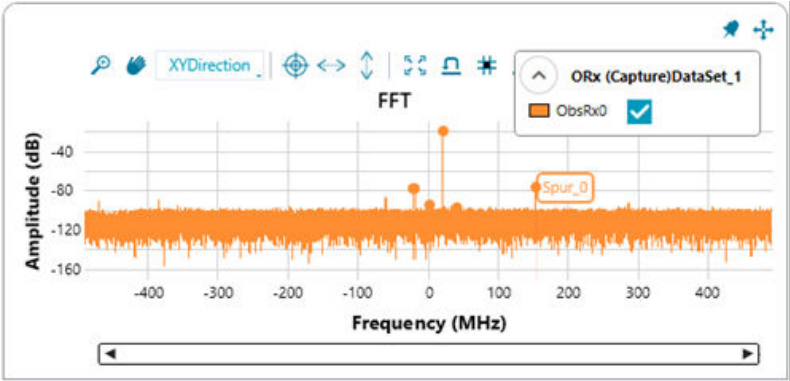


Figure 57. FFT Spur Configuration Window

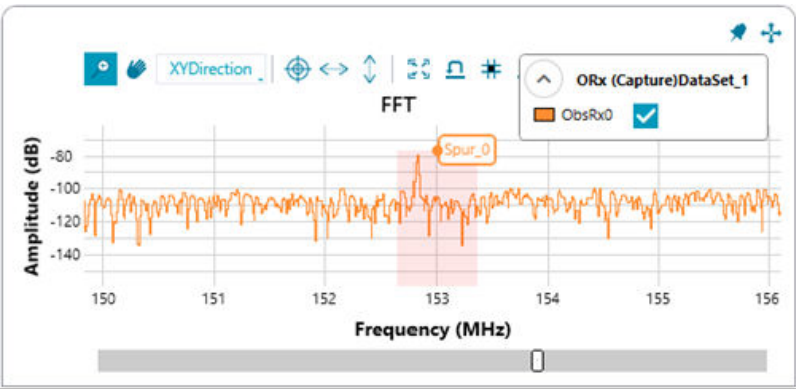
RUNTIME



(A) RESULTS TAB WITH INSERTED SPUR



(B) FFT PLOT WITH INSERTED SPUR



(C) FFT PLOT ZOOMED ONTO INSERTED SPUR

Figure 58. Results and FFT Plot After Spur Inserted at 153 MHz

RUNTIME

Exporting Captured Data

This section explains the exporting captured data feature. The user can perform nonnative measurements or operations on the received signal. Found on both the **Rx (Capture)** and **ORx (Capture)** pages, the **Results** tab provides the ability to export data via the **Export** button as shown in Figure 59. The process is as follows:

1. Upon clicking **Export**, a pop-up window prompts the user to save an XML file.
 - ▶ Note that the name of the file is the base name of the generated files in .csv format.
 - ▶ Default naming convention is **[CapturePage]DataSet_#_DDMonthYYY_HH_MM_SS**.
 - ▶ Default path is as follows: **C:\Users\%UserFolder%\AppData\Local\Analog Devices\ACE\ExportData\ADRV903x**.
2. The total number of additional files generated depends on the number of active channels during the capture.
 - ▶ Key files and brief descriptions follow:
 - ▶ **.fft** file with FFT plot data with additional summary information.
 - ▶ **Raw sample**. Raw data in an interleaving format of I and Q samples. Each column corresponds to a different channel. This file is used for importing data to the **Results** tab.
 - ▶ **Waveform**. File with waveform plot data with additional summary data, including the following:
 - ▶ Samples are interleaved by I and Q samples.
 - ▶ Multiple waveform files are generated depending on number of active channels during capture.
 - ▶ File name follows as **[CapturePage]DataSet_#_waveform_[Channel]_DDMonthYYY_HH_MM_SS**.



Figure 59. ORx (Capture) Page Results Tab with Plots

SOFTWARE RESOURCE FILES

The resource files required for programming the ADRV903x device are listed in [Table 6](#).

These include the **DeviceProfileTest.bin** and **initdata.c** files, which must be generated by the user for the desired ADRV903x configuration and initialization settings. These files can be generated using [ACE](#) with the attached hardware. The ADRV903x can be programmed using ACE for generating these resource files.

Note that ACE needs a hardware connection to the [ADS10-V1EBZ](#) board system for generating the resource files during programming.

Table 6. Resource Files Essential for Programming the ADRV903x

Resource File	Purpose
ADRV9030_FW.bin	Precompiled firmware binary for the embedded dual core ARM processors in the ADRV903x.
DeviceProfileTest.bin	Profile binary consisting of filter coefficients, clock rates, and signal processing resources to be enabled or disabled for a particular use case.
initdata.c	Initialization data structures for setting up the ADRV903x subsystems. It can be generated with either C89 or C99 compatibility to integrate with the user application code base. The difference between a C89- and C99-compatible data structure is illustrated in Table 7 .
RxGainTable.csv	The front-end gain lookup table (LUT) for the ADRV903x receiver.
stream_image.bin	Binary file for the stream co processor in the ADRV903x, which is mainly used for setting up and controlling the Tx/Rx datapaths when certain events occur, such as Tx/Rx enable.

Table 7. Member Representations Compared Between C99-Compatible and C89-Compatible Data Structures

C99 Data Structure Example	C89 Data Structure Example
<pre>adi_adrv903x_Version_t initStructApiVersion = {2, 10, 0, 6}; adi_adrv903x_CpuFwVersion_t initStructArmVersion = { {2, 10, 0, 6} , ADI_ADRV903X_CPU_FW_BUILD_RELEASE}; adi_adrv903x_Version_t initStructStreamVersion = {2, 10, 0, 6}; adi_adrv903x_Init_t deviceInitStruct = {spiOptionsInit = {allowSpiStreaming = 1, allowAhbAutoIncrement = 1, allowAhbSpiFifoMode = 1,},</pre>	<pre>adi_adrv903x_Version_t initStructApiVersion = {2, 10, 0, 6}; adi_adrv903x_CpuFwVersion_t initStructArmVersion = { {2, 10, 0, 6} , ADI_ADRV903X_CPU_FW_BUILD_RELEASE}; adi_adrv903x_Version_t initStructStreamVersion = {2, 10, 0, 6}; adi_adrv903x_Init_t deviceInitStruct = { { // spiOptionsInit 1, // allowSpiStreaming 1, // allowAhbAutoIncrement 1, // allowAhbSpiFifoMode},</pre>

SOFTWARE RESOURCE FILES

RESOURCE FILE GENERATION USING ACE

ACE can be used to generate the resource files needed for programming the ADRV903x by connecting and programming the evaluation hardware using the ADRV903x plugin. ACE outputs the resource files to the resource folder path **C:\Users\%USERNAME%\AppData\Local\Analog Devices\ACE\PluginFiles\Board.ADRV9030\Local\resources** as shown in Figure 60.

Note that ACE clears the contents of the resource folder with every program before writing new resource files. Any resource files required by the user must be copied to a different location before attempting to program the ADRV903x again.

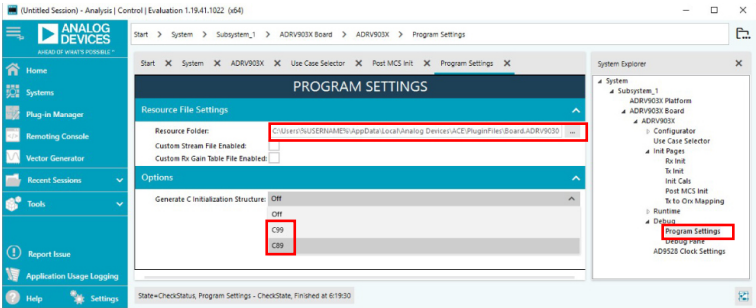


Figure 60. Resource File Generation Using the ACE Software, C89 or C99 Compatibility Can Be Selected for Initdata.c

IRONPYTHON SCRIPTING

ACE enables the user to interface with the ADRV903x evaluation system using a scripting language such as IronPython. To run scripts from within ACE, the user must refer to the following steps:

- 1. Provide the following path to the host PC IronPython installation under ACE: **Settings > Scripting > Path** as shown in Figure 61. This step must only be completed after installing ACE.

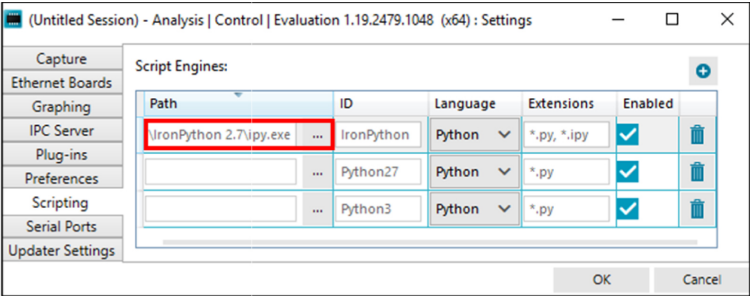


Figure 61. Providing IronPython Path to ACE for Enabling Script Execution

- 2. Open a script from **Tools > Platform API Logger > Open Script** as shown in Figure 62. A template script for interfacing with the ADRV903x device is included with the plugin and can be opened from **Create New**. Note that scripts open as new tabs in ACE.

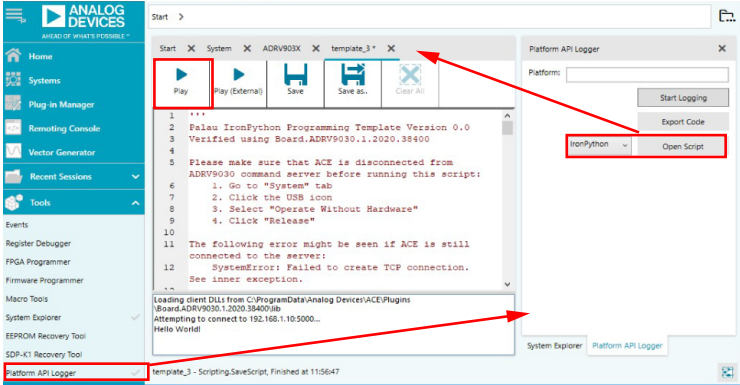


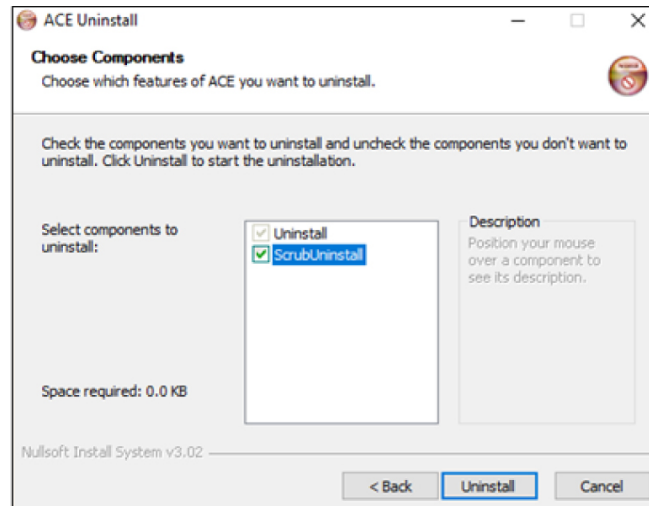
Figure 62. Using Platform API Logger to Open and Execute IronPython Scripts from Within ACE

APPENDIX

UNINSTALLING OLDER ACE

Uninstalling [ACE](#) is not necessary to update the ACE core to a newer release. However, if errors are seen during the installation of a new ACE core version, any previous versions of ACE core can be removed from the host PC as outlined as follows. Note that administrator privileges are required for the following steps:

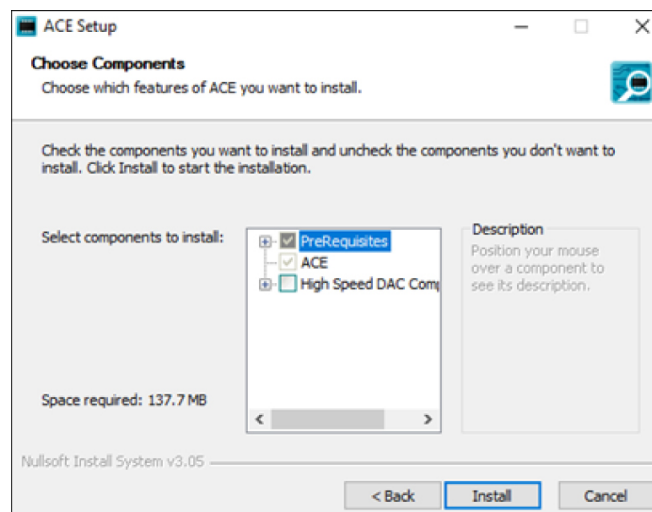
1. Close any running instances of ACE. Task manager can be used to confirm that no background ACE processes are running.
2. Navigate to Windows **Start > Add or Remove Programs > ACE > Uninstall**.
3. Select **ScrubUninstall** in the ACE uninstall wizard as shown in [Figure 63](#), which is necessary to remove any older ACE plugin versions; however, it also removes any custom files, settings, and data exports previously stored by the user. Note that this step must only be performed as a fallback option if the ACE installation appears corrupted, and it is necessary to start from a clean slate.



063

Figure 63. ScrubUninstall Used to Troubleshoot Erroneous ACE Installation

4. When prompted, select **No** to additionally uninstall system demonstration platform (SDP) drivers, LRF drivers, and ADIThon from the previous ACE installation.
5. Attempt to reinstall ACE by running the included ACE installer with the default components selections as shown in [Figure 64](#).



064

Figure 64. Component Selections Used when Attempting a New Installation of ACE

More information about the ACE uninstallation process is available on the ACE wiki <https://wiki.analog.com/resources/tools-software/ace/installscrub>.

APPENDIX

UNINSTALLING OLDER PLUG-IN USING PLUG-IN MANAGER

Any previously installed [ACE](#) plugin, such as an ADRV903x plugin, can be uninstalled using the ACE **Plug-In Manager** as shown in [Figure 65](#). The steps are as follows:

1. Open the **Plug-In Manager** from the ACE left panel.
2. Select **Plug-ins** from the list of installed packages. Find the plugin to be uninstalled via the search bar.
3. Click **Uninstall Selected**, and then restart ACE to complete this step.

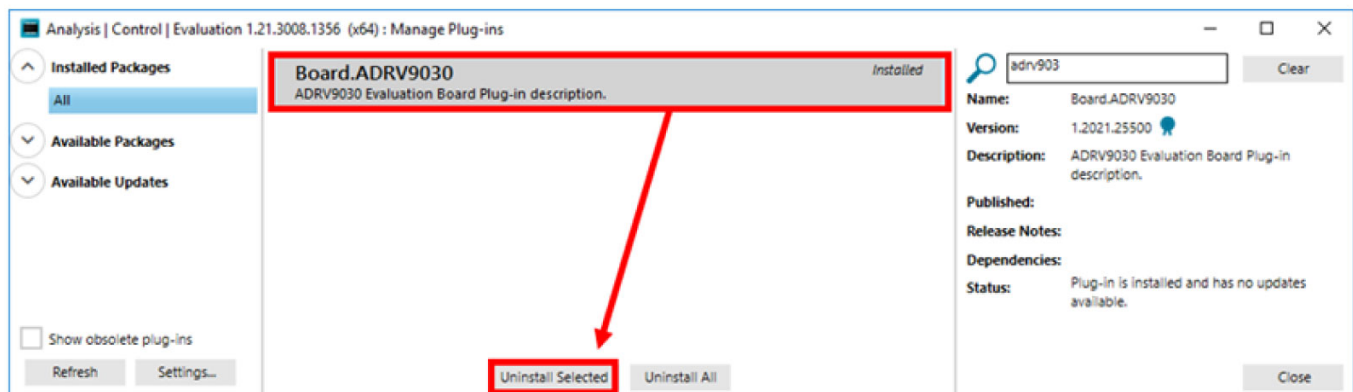


Figure 65. Using ACE Plug-In Manager to Uninstall Older Version of the ADR903x Plugin (Board [ADRV9010](#))

APPENDIX

INSTALLING THE ADRV903X PLUGIN USING THE ACE PLUG-IN MANAGER

The user can install the ADRV903x plugin by providing the plugin .acezip file path to ACE under **Settings** as shown in Figure 66. The steps are as follows:

1. Open ACE **Settings**.
2. Select the **Plug-ins** tab.
3. Add a new plugin by clicking on the **+** button under **Zipped Plug-in Sources** as shown in Figure 66.

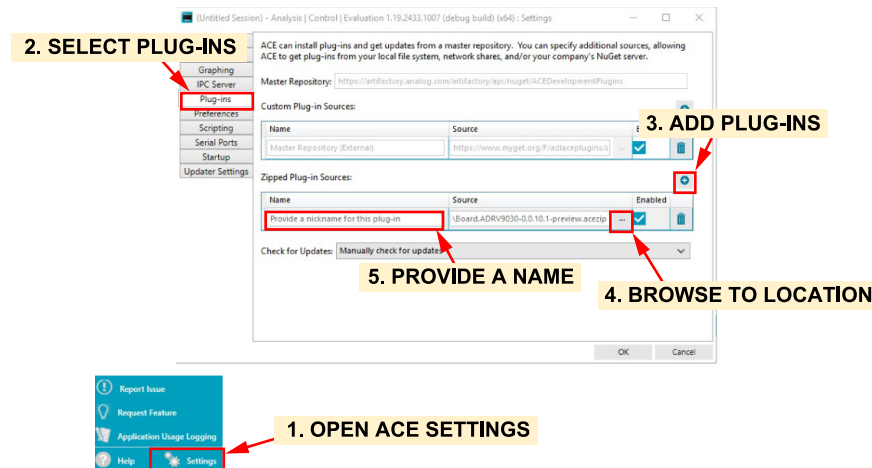


Figure 66. Adding ADRV903x Plugin as a Zipped Source in ACE Settings, Once Added, Run ACE Plug-in Manager to Install the Plugin

4. Click on ... to navigate to the **Board.ADRV903x.acezip** file location to populate the source field.
5. Provide a name for this plugin source. The name choice is arbitrary and can be chosen by the user.
6. Launch the **Plug-in Manager** and then select and install **Board.ADRV9030** from the list of **Available Packages** as shown in Figure 67.

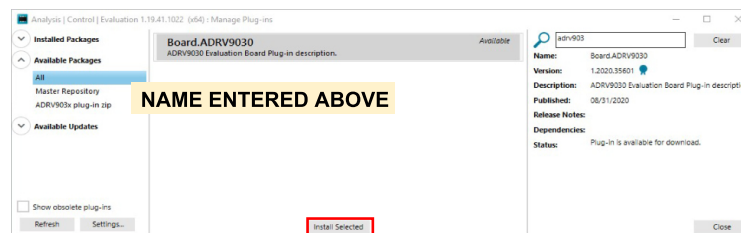


Figure 67. ADRV903x Plugin Installed Using ACE Plug-in Manager

APPENDIX

DISCONNECTING ACE FROM ADS10-V1EBZ COMMAND SERVER

The user may disconnect ACE from the ADS10-V1EBZ command server to enable other applications to communicate with the evaluation hardware. ACE can be disconnected from the ADS10-V1EBZ as shown in Figure 68. The steps to disconnect ACE from the ADS10-V1EBZ command server are as follows:

1. Navigate to the **System** tab for ACE.
2. Click the **USB** icon on the **ADRV903x Platform Controller** to open the **Acquire/Release Hardware** dialog box.
3. Check off the **Operate without hardware** box within the **Acquire/Release Hardware** dialog box. This selection updates the buttons in the dialog box to show the **Release** button.
4. Click **Release**. This step disconnects ACE from the evaluation hardware. The status of the ACE connection to the hardware can be checked from either of the following:
 - Go to **System > ADRV903x Platform Controller** and ensure the **USB** icon turned from green for connected to gray for disconnected.
 - See the **ADRV903x Board** connection indicator, its green light turns red once the board is disconnected.

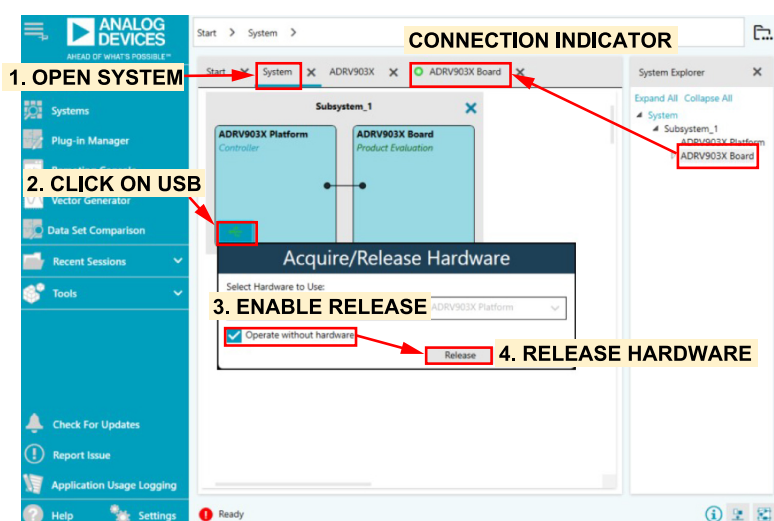


Figure 68. Steps for Disconnecting ACE from the Evaluation Hardware

APPENDIX

RECONNECTING ACE TO THE ADS10-V1EBZ COMMAND SERVER

The process for reconnecting **ACE** to the evaluation hardware is similar to the disconnecting procedure as shown in [Figure 69](#). The steps to reconnect ACE to the **ADS10-V1EBZ** command server are as follows:

1. Navigate to the **System** tab of ACE.
2. Click on the **USB** icon on the **ADRV903x Platform Controller** to open the **Acquire/Release Hardware** dialog box.
3. Uncheck the **Operate without hardware** box in the **Acquire/Release Hardware** dialog box to update the buttons in the dialog box to show **Acquire**.
4. Click **Acquire** to reestablish the hardware connection. This step connects ACE to the evaluation hardware. The status of the ACE connection to the hardware can be checked from either of the following:
 - ▶ Go to **System > ADRV903x Platform Controller** and verify that the **USB** icon is green.
 - ▶ See the **ADRV903x Board** tab to verify the connection indicator is green.

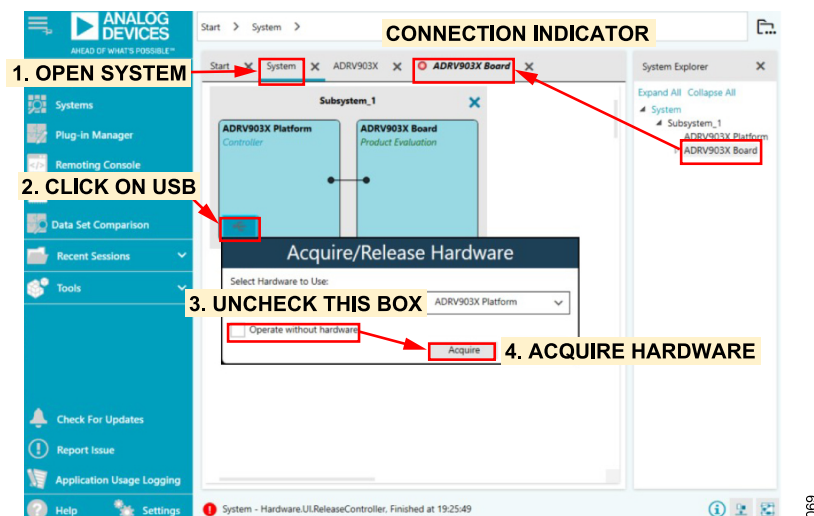


Figure 69. Steps for Reconnecting ACE to the Evaluation Hardware



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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