Evaluating the ADRF5703 Silicon Digital Attenuator, 0.25 dB LSB, 7-Bit, 9kHz to 20GHz

FEATURES

- Full featured evaluation board for the ADRF5703
- Easy connection to the test equipment
- Additional through line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5703 is a 7-bit digital attenuator with an 31.75dB attenuation range manufactured in the silicon on insulator (SOI) process.

This user guide describes the ADRF5703-EVALZ evaluation board, which is designed to simply evaluate the features and performance of the ADRF5703. A photograph of the ADRF5703-EVALZ is shown in Figure 1.

A full description and complete specifications for the ADRF5703 are provided in the data sheet and should be consulted in conjunction with this user guide when using the ADRF5703-EVALZ evaluation board.

ADRF5703-EVALZ EVALUATION BOARD PHOTOGRAPH

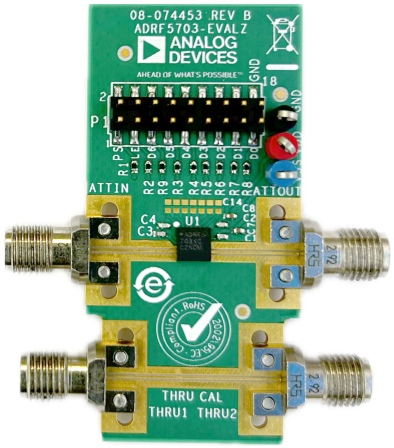

Figure 1. ADRF5703-EVALZ Evaluation Board Photograph

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REVISION HISTORY

9/2025—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5703-EVALZ is a connectorized board, assembled with the ADRF5703 and its application circuitry. All components are placed on the primary side of ADRF5703-EVALZ. An assembly drawing for the ADRF5703-EVALZ is shown in Figure 9, and an evaluation board schematic is shown in Figure 8.

BOARD LAYOUT

The ADRF5703-EVALZ is designed using RF circuit design techniques on a 4-layer printed circuit board (PCB). The PCB stackup is shown in Figure 2.

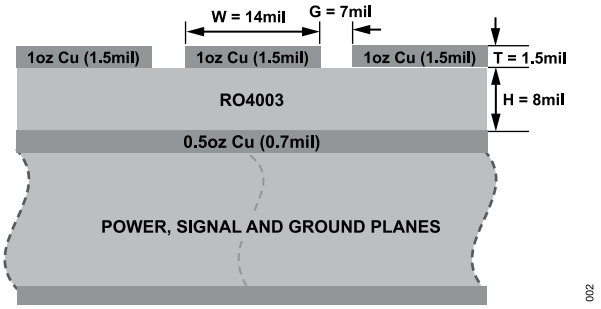

Figure 2. Evaluation Board Stackup

The outer copper layers are 1oz (1.5mil) thick, and the inner layers are 0.5oz (0.7mil) thick.

The top dielectric material is 8mil Rogers 4003, which provides 50Ω-controlled impedance and optimizes the high frequency performance. All RF traces are routed on the top layer, and the second layer is used as the ground plane for RF transmission lines. The remaining two layers are also ground planes filled with FR4 material to manage the thermal rise during high power operations and are supported with dense and filled vias to the PCB bottom for thermal relief. The overall board thickness is approximately 62mil for mechanical strength.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14mil and ground spacing of 7mil to have a characteristic impedance of 50Ω. Ground via fences are arranged on both sides of the CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5703, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled, through vias to provide the lowest possible thermal resistance path from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

POWER SUPPLY AND CONTROL INPUTS

The ADRF5703-EVALZ has two-supply pins, nine control inputs, and a ground, as shown in Table 1. The DC test points are populated on VDD, VSS, D0 to D6, LE, PS, and GND. A +3.3V supply is connected to the DC test points on VDD and a −3.3 supply is connected to the DC test point on VSS. The ground reference can be connected to GND. Connect D0 to D6, LE, and PS to 3.3V or 0V. The typical total current consumption for the ADRF5703 is 0.7mA for +3.3V VDD and 0.6mA for −3.3V VSS.

The VDD and VSS supply pins of the ADRF5703 are decoupled with 0.1µF capacitor.

Table 1. Power Supply and Control Inputs

Test Point	Description
VDD	+3.3V supply voltage
VSS	−3.3V supply voltage
D0 to D6	Control Input 0 to Control Input 6
PS	Parallel serial control
LE	Latch enable
GND	Ground

EVALUATION BOARD HARDWARE

RF INPUTS AND OUTPUTS

The ADRF5703-EVALZ has four edge-mounted, 2.92mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

SMA Connector	Description
ATTIN	Attenuator input
ATTOUT	Attenuator output
THRU1	Thru line input and output
THRU2	Thru line input and output

The ADRF5703-EVALZ is shipped together with a thru line that calibrates out the board loss effects from the measurements determining the device performance at the pins of the IC. Figure 3 shows the typical board loss (through line) for the ADRF5703-EVALZ at room temperature, as well as the non-de-embedded and de-embedded insertion loss for ADRF5703.

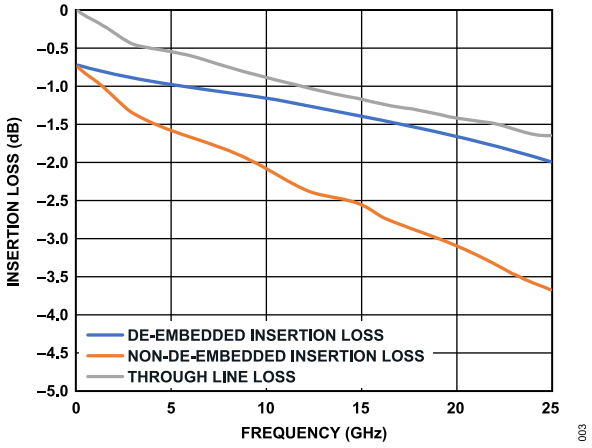

Figure 3. Insertion Loss vs. Frequency

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5703-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the D0 to D6, PS, and LE test points.
4. Apply an RF input signal.

The ADRF5703-EVALZ is shipped fully assembled and tested. Figure 4 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Perform the following steps to complete the test setup and to verify the operation of the ADRF5703-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage output terminal of the +3.3V supply.
3. Connect the VSS test point to the voltage output terminal of the −3.3V supply. Note that the current from the VDD test point is around 0.7mA and from the VSS test point is around 0.6mA.
4. Connect the D0 to D6, EN, and LS test points to the voltage output terminal of the 3.3V or 0V supply. The ADRF5703 can be configured in different modes by connecting the control test points to 3.3V or 0V.
5. Connect a calibrated network analyzer to the ATTIN and ATTOUT 2.92mm connectors. If the network analyzer port count is not enough, terminate the unused RF ports with 50Ω. Sweep the frequency from 9kHz to 20GHz and set the power to 10dBm.
6. The ADRF5703-EVALZ is expected to have an insertion loss of 1.7dB at 20GHz. See the expected results in Figure 5.

Additional test equipment is needed to fully evaluate the device functions and performance.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is also recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

Note that the measurements performed at the 2.92mm connectors of the ADRF5703-EVALZ include the losses of the 2.92mm connectors and the PCB. The thru line must be measured to calibrate out the effects on the ADRF5703-EVALZ. The thru line is the summation of an RF input line and an RF output line that are connected to the device and equal in length.

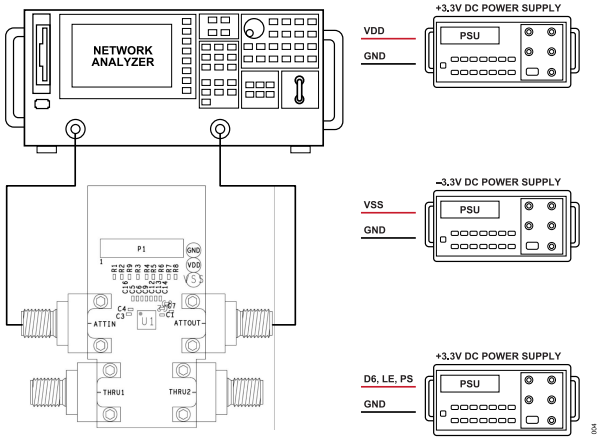

Figure 4. Test Setup Diagram

Table 3. Truth Table

Digital Control Input[1]							
D6	D5	D4	D3	D2	D1	D0	Attenuation State (dB)
Low	Low	Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	Low	Low	High	0.25
Low	Low	Low	Low	Low	High	Low	0.50
Low	Low	Low	Low	High	Low	Low	1.0
Low	Low	Low	High	Low	Low	Low	2.0
Low	Low	High	Low	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	High	31.75

[1] Any combination of the states within this table provides an attenuation equal to the sum of the bits selected.

TEST PROCEDURE

EXPECTED RESULTS

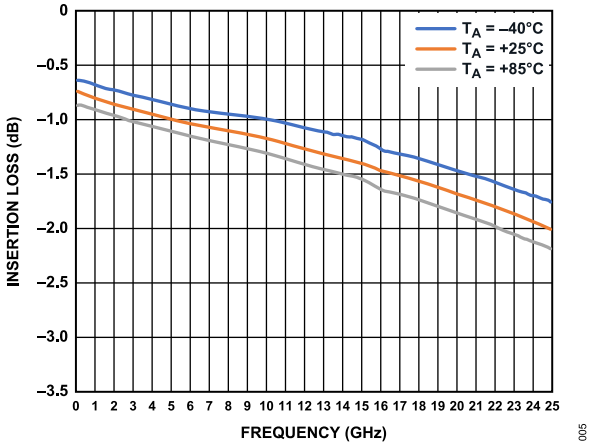

Figure 5. Insertion Loss vs. Frequency for Various Temperatures

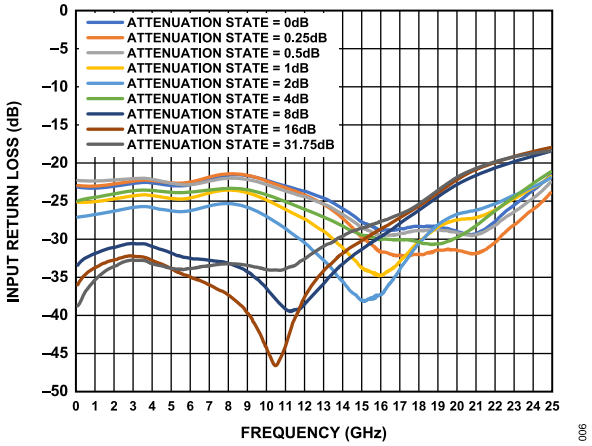

Figure 6. Input Return Loss vs. Frequency for Major Attenuation States

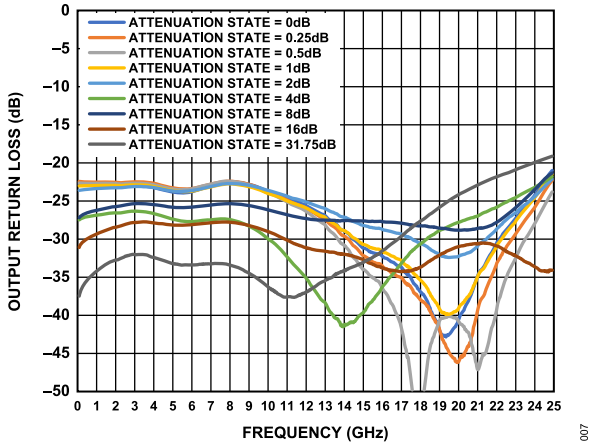

Figure 7. Output Return Loss vs. Frequency for Major Attenuation States

EVALUATION BOARD SCHEMATIC AND ARTWORK

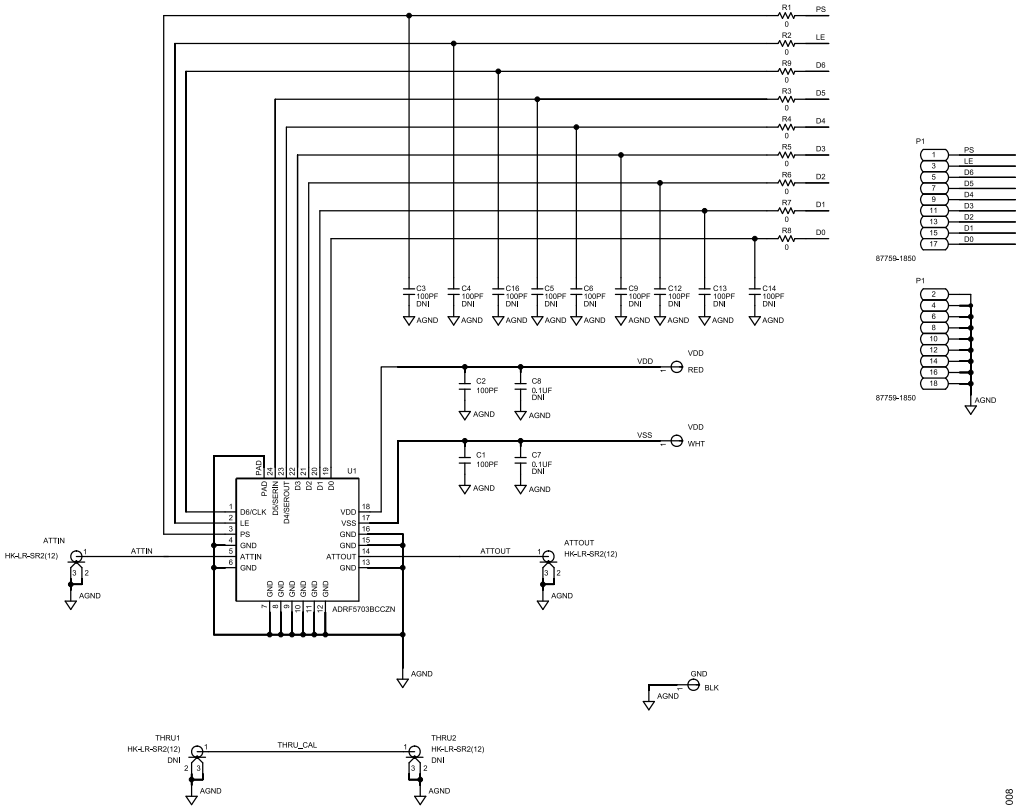

Figure 8. ADRF5703-EVALZ Evaluation Board Schematic

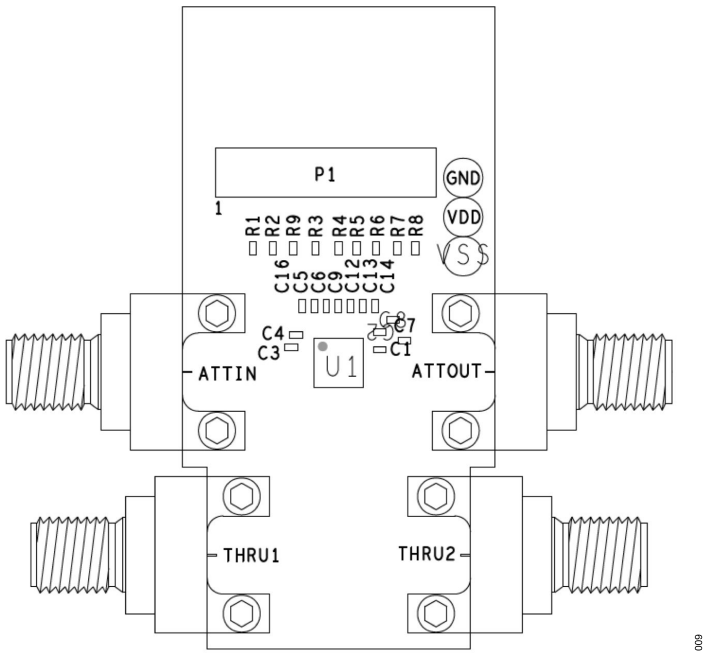

Figure 9. ADRF5703-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

EVALUATION BOARDS

Table 4. Evaluation Boards

Model[1]	Description
ADRF5703-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

BILL OF MATERIALS

Table 5. Bill of Materials for ADRF5703-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
1	C1, C2	Capacitors, 100pF, 50V, C0402 package	Murata	GCM1555C1H101JA16D
10	R1 to R9	Resistors, 0Ω, 1/16W, R0402 package	Yageo	RC0402JR-070RL
2	ATTIN and ATTOUT	Edge-mount 2.92mm connectors	Hirose Electronic Co.	HK-LR-SR2(12)
1	P1	18-position male header	Molex	87759-1850
5	VDD, VSS, GND	Surface-mount test points	Components Corporation	TP-104-01-0X
1	U1	Silicon digital attenuator, 0.25dB LSB, 7-bit, 9kHz to 20GHz	Analog Devices, Inc.	ADRF5703
1	PCB	ADRF5703 evaluation board	Analog Devices	ADRF5703-EVALZ

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.