Evaluating the ADRF5702 Silicon Digital Attenuator, 0.125dB LSB, 8-Bit, 50MHz to 20GHz

FEATURES

- Full featured evaluation board for the ADRF5702
- Easy connection to test equipment
- Additional through line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5702 is a 8-bit digital attenuator with 31.875dB attenuation range manufactured in the silicon on insulator (SOI) process.

This user guide describes the ADRF5702-EVALZ evaluation board, which is designed to simply evaluate the features and performance of the ADRF5702. A photograph of the evaluation board is shown in Figure 1.

ADRF5702-EVALZ EVALUATION BOARD PHOTOGRAPH

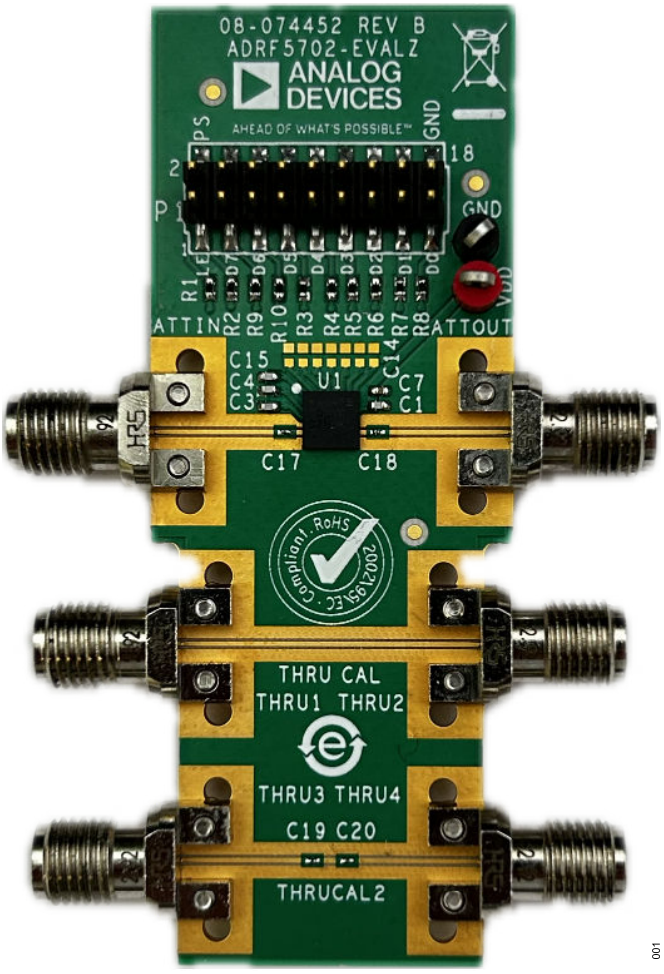

Figure 1. ADRF5702-EVALZ Evaluation Board Photograph

TABLE OF CONTENTS

REVISION HISTORY

6/2025—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5702-EVALZ is a connectorized board, assembled with the ADRF5702 and its application circuitry. All components are placed on the primary side of ADRF5702-EVALZ. An assembly drawing for the ADRF5702-EVALZ is shown in Figure 8, and an evaluation board schematic is shown in Figure 7.

BOARD LAYOUT

The ADRF5702-EVALZ is designed using RF circuit design techniques on a 4-layer printed circuit board (PCB). The PCB stack-up is shown in Figure 2.

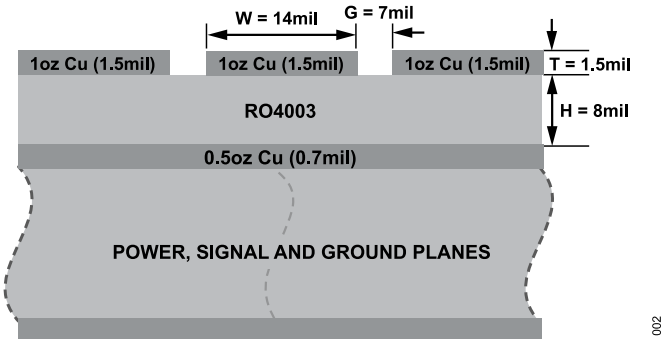

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 1oz (1.5mil) thick and the inner layers are 0.5oz (0.7mil) thick.

The top dielectric material is 8mil Rogers 4003, which provides 50Ω controlled impedance and optimizes the high frequency performance. All RF traces are routed on the top layer, and the second layer is used as the ground plane for RF transmission lines. The remaining two layers are also ground planes filled with FR4 material to manage the thermal rise during high power operations and are supported with dense and filled vias to the PCB bottom for thermal relief. The overall board thickness is approximately 62mil for mechanical strength.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14mil and ground spacing of 7mil to have a characteristic impedance of 50Ω. Ground via fences are arranged on both sides of the CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5702, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled, through vias to provide the lowest possible thermal resistance path from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

POWER SUPPLY AND CONTROL INPUTS

The ADRF5702-EVALZ has one power-supply input, ten control inputs, and a ground, as shown in Table 1. The DC test points are populated on VDD, D0 to D7, LE, PS, and GND. A 5V or 3.3V supply is connected to the DC test points on VDD. Ground reference can be connected to GND. Connect D0 to D7, LE, and PS to 3.3V or 0V. The typical total current consumption for the ADRF5702 is 3.50mA for 5V VDD or 1.75mA for 3.3V VDD.

The VDD supply pin of the ADRF5702 is decoupled with 100pF capacitor.

Table 1. Power Supply and Control Inputs

Test Point	Description
VDD	5V or 3.3V supply voltage
D0 to D7	Control Input 0 to Control Input 7
PS	Parallel serial control
LE	Latch enable
GND	Ground

RF INPUTS AND OUTPUTS

The ADRF5702-EVALZ has four edge-mounted, 2.92mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

SMA Connector	Description
ATTIN	Attenuator input
ATTOUT	Attenuator output
THRU1	Thru line input and output
THRU2	Thru line input and output

The ADRF5702-EVALZ is shipped together with a thru line that calibrates out the board loss effects from the measurements determining the device performance at the pins of the IC.

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5702-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the D0 to D7, PS, and LE test points.
4. Apply an RF input signal.

The ADRF5702-EVALZ is shipped fully assembled and tested. Figure 3 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Perform the following steps to complete the test setup and to verify the operation of the ADRF5702-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage output terminal of the 5V or 3.3V supply. Note that the current from VDD test point is around 3.50mA for 5V VDD or 1.75mA for 3.3V VDD.
3. Connect the D0 to D7, EN, and LS test points to the voltage output terminal of the 3.3V supply. The ADRF5702 can be configured in different modes by connecting the control test points to 3.3V or 0V.
4. Connect a calibrated network analyzer to the ATTIN and ATTOUT 2.92 mm connectors. If the network analyzer port count is not enough, terminate unused RF ports with 50Ω. Sweep the frequency from 100MHz to 20GHz and set the power to 10dBm.
5. The ADRF5702-EVALZ is expected to have an insertion loss of 2.6dB at 20GHz. See the expected results in Figure 4.

Additional test equipment is needed to fully evaluate the device functions and performance.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is also recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

Note that the measurements performed at the 2.92mm connectors of the ADRF5702-EVALZ include the losses of the 2.92mm connectors and the PCB. The thru line must be measured to calibrate out the effects on the ADRF5702-EVALZ. The thru line is the summation of an RF input line and an RF output line that are connected to the device and equal in length.

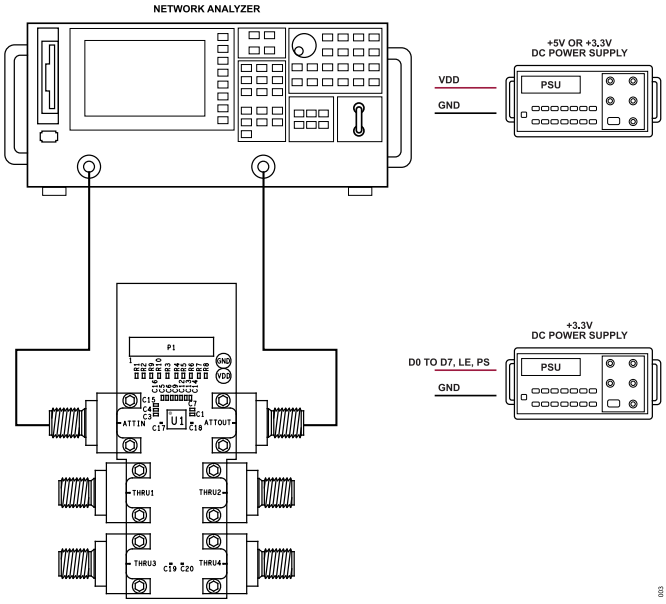

Figure 3. Test Setup Diagram

Table 3. Truth Table

Digital Control Input[1]								
D7	D6	D5	D4	D3	D2	D1	D0	Attenuation State (dB)
Low	Low	Low	Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	Low	Low	Low	High	0.125
Low	Low	Low	Low	Low	Low	High	Low	0.25
Low	Low	Low	Low	Low	High	Low	Low	0.5
Low	Low	Low	Low	High	Low	Low	Low	1.0
Low	Low	Low	High	Low	Low	Low	Low	2.0
Low	Low	High	Low	Low	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	High	High	31.875

[1] Any combination of the states within this table provides an attenuation equal to the sum of the bits selected.

TEST PROCEDURE

EXPECTED RESULTS

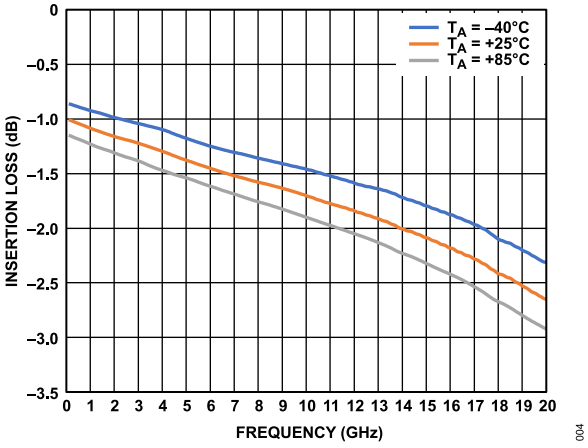

Figure 4. Insertion Loss for RFC to RFx On vs. Frequency

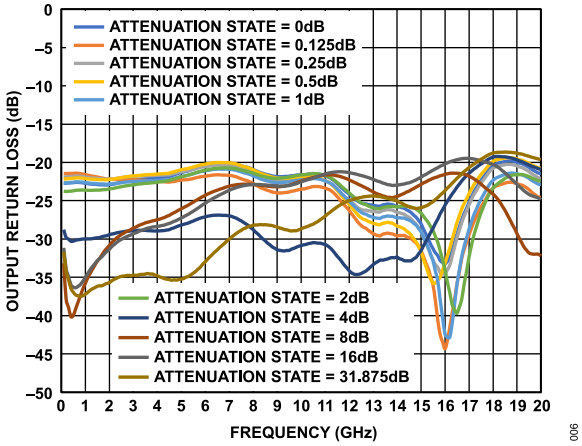

Figure 6. Output Return Loss vs. Frequency

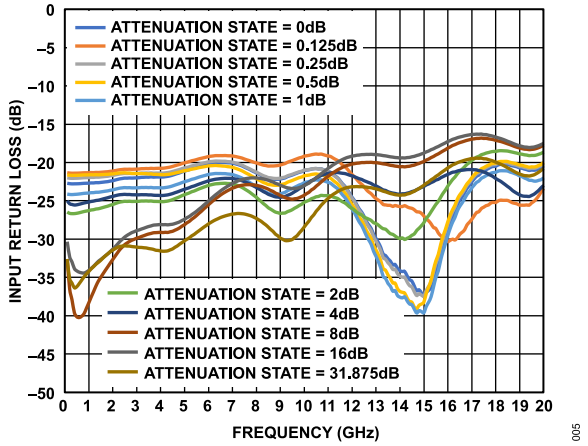

Figure 5. Input Return Loss vs. Frequency

EVALUATION BOARD SCHEMATIC AND ARTWORK

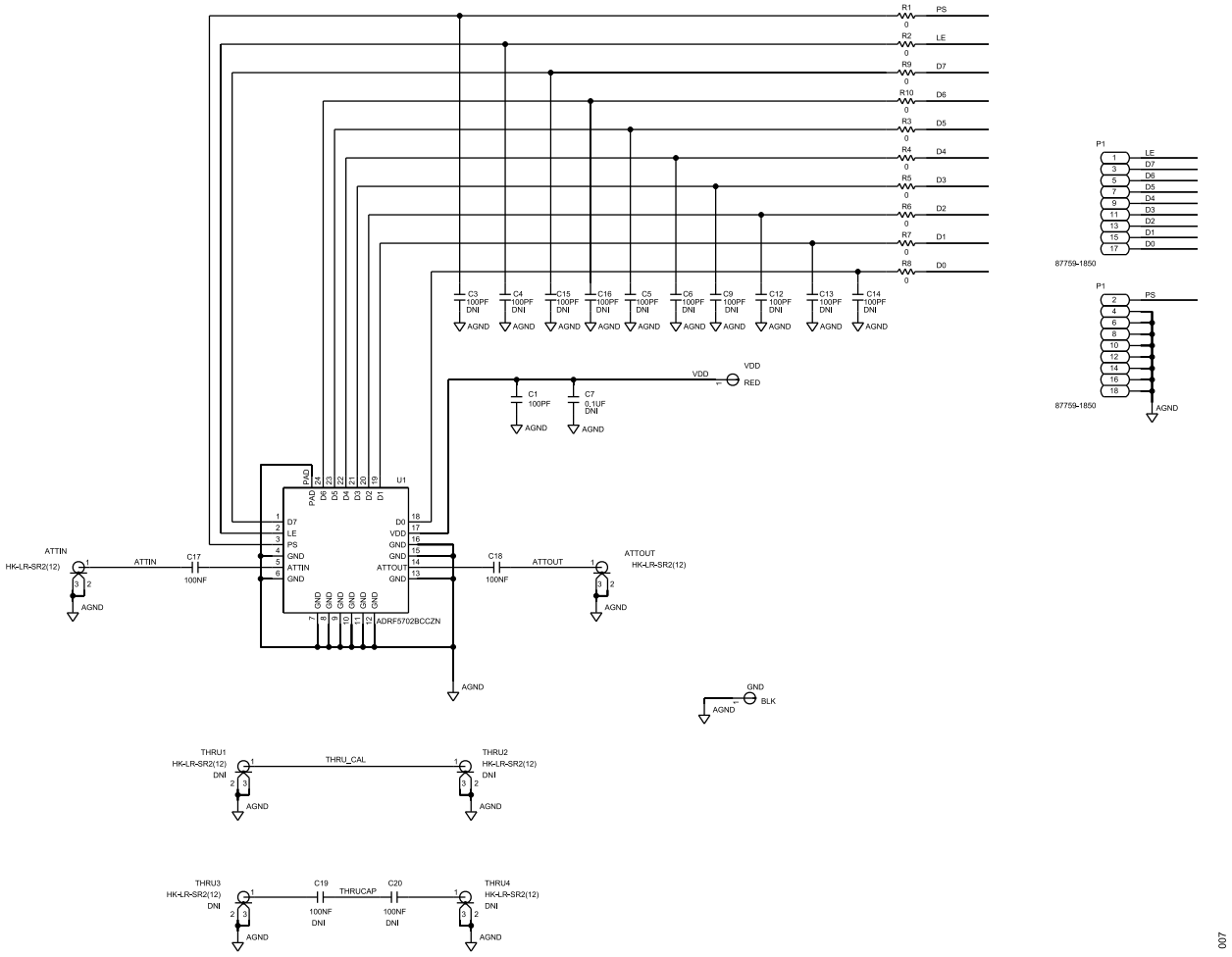

Figure 7. ADRF5702-EVALZ Evaluation Board Schematic

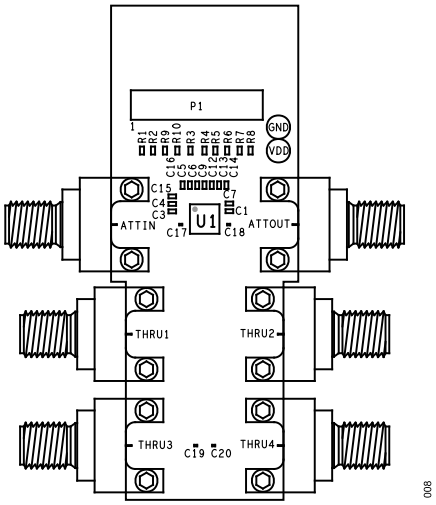

Figure 8. ADRF5702-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

EVALUATION BOARDS

Table 4. Evaluation Boards

Model[1]	Description
ADRF5702-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

BILL OF MATERIALS

Table 5. Bill of Materials for ADRF5702-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
1	C1	Capacitors, 100pF, 50V, C0402 package	Murata	GCM1555C1H101JA16D
2	C17, C18	Capacitors, 100nF, 6.3V, C01005	Passive Plus Inc.	01005BB104-MW6R3
10	R1 to R10	Resistors, 0Ω, 1/16W, R0402 package	Yageo	RC0402JR-070RL
2	ATTIN and ATTOUT	Edge-mount 2.92mm connectors	Hirose Electronic Co.	HK-LR-SR2(12)
1	P1	18 position male header	Molex	87759-1850
5	VDD, GND	Surface-mount test points	Components Corporation	TP-104-01-0X
1	U1	Silicon digital attenuator, 0.125dB LSB, 8-bit, 100MHz to 20GHz	Analog Devices, Inc.	ADRF5702
1	PCB	ADRF5702 evaluation board	Analog Devices	ADRF5702-EVALZ

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.