Evaluating the ADRF5063 9 kHz to 13 GHz, Differential SPDT Switch

FEATURES

- Full-featured evaluation board for the ADRF5063
- Easy connection to the test equipment
- Thru line for calibration

EVALUATION KIT CONTENTS

- ADRF5063-EVALZ evaluation board

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

DOCUMENTS NEEDED

- ADRF5063 data sheet

GENERAL DESCRIPTION

The ADRF5063 is a differential SPDT switch manufactured in the silicon on insulator (SOI) process.

This user guide describes the ADRF5063-EVALZ evaluation board, which was designed to evaluate the features and performance of the ADRF5063. Figure 1 shows a photograph of the ADRF5063-EVALZ.

The ADRF5063-EVALZ uses the same evaluation board as ADRF5062-EVALZ.

Full specifications on the ADRF5063 are available in the ADRF5063 data sheet from Analog Devices, Inc. Consult the data sheet with this user guide when using the ADRF5063-EVALZ evaluation board.

EVALUATION BOARD PHOTOGRAPH

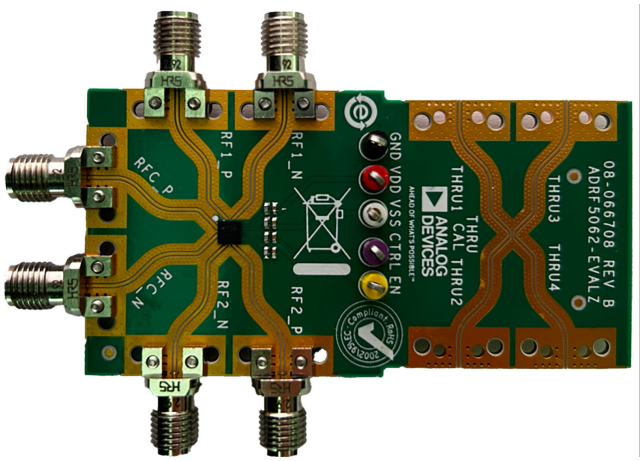

Figure 1. ADRF5063-EVALZ Evaluation Board Photograph

TABLE OF CONTENTS

REVISION HISTORY

10/2024—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5063-EVALZ is a connectorized board, assembled with the ADRF5063 and its application circuitry. All components are placed on the primary side of the ADRF5063-EVALZ evaluation board. Figure 6 shows an assembly drawing for the ADRF5063-EVALZ, and Figure 5 shows an ADRF5063-EVALZ schematic.

BOARD LAYOUT

The ADRF5063-EVALZ evaluation board is designed using RF circuit design techniques on a four-layer printed circuit board (PCB). Figure 2 shows the PCB stack-up.

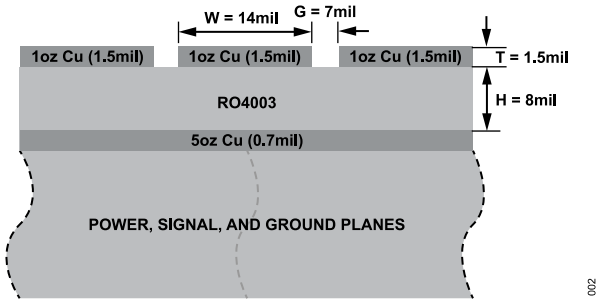

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 1.5 mil thick, and the inner layers are 0.7 mil thick.

All RF and DC traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers RO4003, offering optimal high-frequency performance. The middle and bottom dielectric materials provide mechanical strength. The total board thickness is 62 mil, which allows 2.92 mm RF edge launch connectors to be placed at the board edges.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14 mil and ground spacing of 7 mil to have a characteristic impedance of 50 Ω. Ground via fences are arranged on both sides of a CPWG to improve isolation between nearby RF lines and other signal lines.

POWER-SUPPLY AND CONTROL INPUTS

The ADRF5063-EVALZ evaluation board has two power-supply inputs, two control inputs, and a ground, as shown in Table 1. The DC test points are populated on VDD, VSS, CTRL, EN, and GND. A 3.3 V supply is connected to the DC test points on VDD, and a −3.3 V supply is connected to the DC test points on VSS. Ground reference can be connected to GND. Connect the CTRL and EN inputs to 3.3 V or 0 V. The typical total current consumption for the ADRF5063 is 650 µA.

The V_{DD} and V_{SS} supply pins of the ADRF5063 are decoupled with 100 pF capacitors.

Table 1. Power-Supply and Control Inputs

Test Points	Description
VDD	Positive supply voltage
VSS	Negative supply voltage
CTRL	Control input voltage
EN	Enable input voltage
GND	Ground

EVALUATION BOARD HARDWARE

RF INPUTS AND OUTPUTS

The ADRF5063-EVALZ evaluation board has 10 edge-mounted, 2.92 mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

2.92 mm Connectors	Description
RFC_P	RF common positive port
RFC_N	RF common negative port
RF1_P	RF Throw 1 positive port
RF1_N	RF Throw 1 negative port
RF2_P	RF Throw 2 positive port
RF2_N	RF Throw 2 negative port
THRU1	Thru line input positive
THRU2	Thru line output positive
THRU3	Thru line input negative
THRU4	Thru line output negative

The through calibration line, connecting the THRU1, THRU3, THRU2, THRU4 RF connectors, calibrates out the board loss effects from the measurements of the ADRF5063-EVALZ evaluation board to determine the device performance at the pins of the IC. Figure 3 shows the typical board loss for the ADRF5063-EVALZ evaluation board at room temperature, as well as the embedded and de-embedded insertion loss for the ADRF5063.

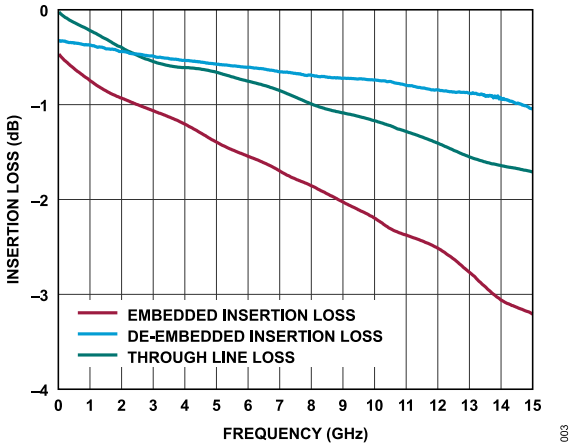

Figure 3. Differential Insertion Loss vs. Frequency

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5063-EVALZ, take the following steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the VSS test point.
4. Bias up the CTRL test point.
5. Bias up the EN test point.
6. Apply an RF input signal.

The ADRF5063-EVALZ is shipped fully assembled and tested. Figure 4 provides a basic test setup diagram to evaluate the S-parameters using a network analyzer. Follow these steps to complete the test setup and to verify the operation of the ADRF5063-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage-output terminal of the 3.3 V supply.
3. Connect the VSS test point to the voltage-output terminal of the −3.3 V supply.
4. Connect the CTRL test point to the voltage-output terminal of the 3.3 V supply. The ADRF5063 can be configured in different modes by connecting the CTRL test point to 3.3 V or 0 V, as shown in Table 3.
5. Connect the EN test point to the voltage-output terminal of the 3.3 V supply. The ADRF5063 can be configured in different modes by connecting the EN test point to 3.3 V or 0 V, as shown in Table 3.
6. Connect a calibrated network analyzer to the 2.92 mm connectors of RFC_P, RFC_N, RF1_P, RF1_N, RF2_P, RF2_N. If the network analyzer port count is not enough, terminate unused RF ports with 50 Ω. In addition, sweep the frequency from 9 kHz to 15 GHz and set the power to −10 dBm.

Additional test equipment is needed to fully evaluate the functions and performance of the ADRF5063.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high-isolation balun and power combiner is also recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

Note that the measurements performed at the 2.92 mm connectors of the ADRF5063-EVALZ include the losses of the 2.92 mm connectors and the PCB. The thru line must be measured to calibrate out the effects on the ADRF5063-EVALZ. The thru line is the summation of an RF input line and an RF output line connected to the ADRF5063 and equal in length.

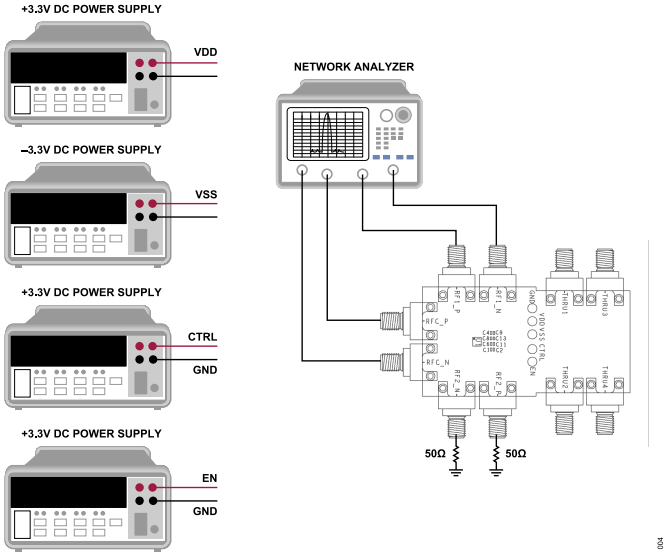

Figure 4. Test Setup Diagram

Table 3. Control Voltage Truth Table

Digital Control Inputs		RF Paths	
EN	**CTRL**	**RF1_x to RFC_x**	**RF2_x to RFC_x**
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)
High	High	Isolation (off)	Isolation (off)

EVALUATION BOARD SCHEMATIC AND ASSEMBLY DIAGRAM

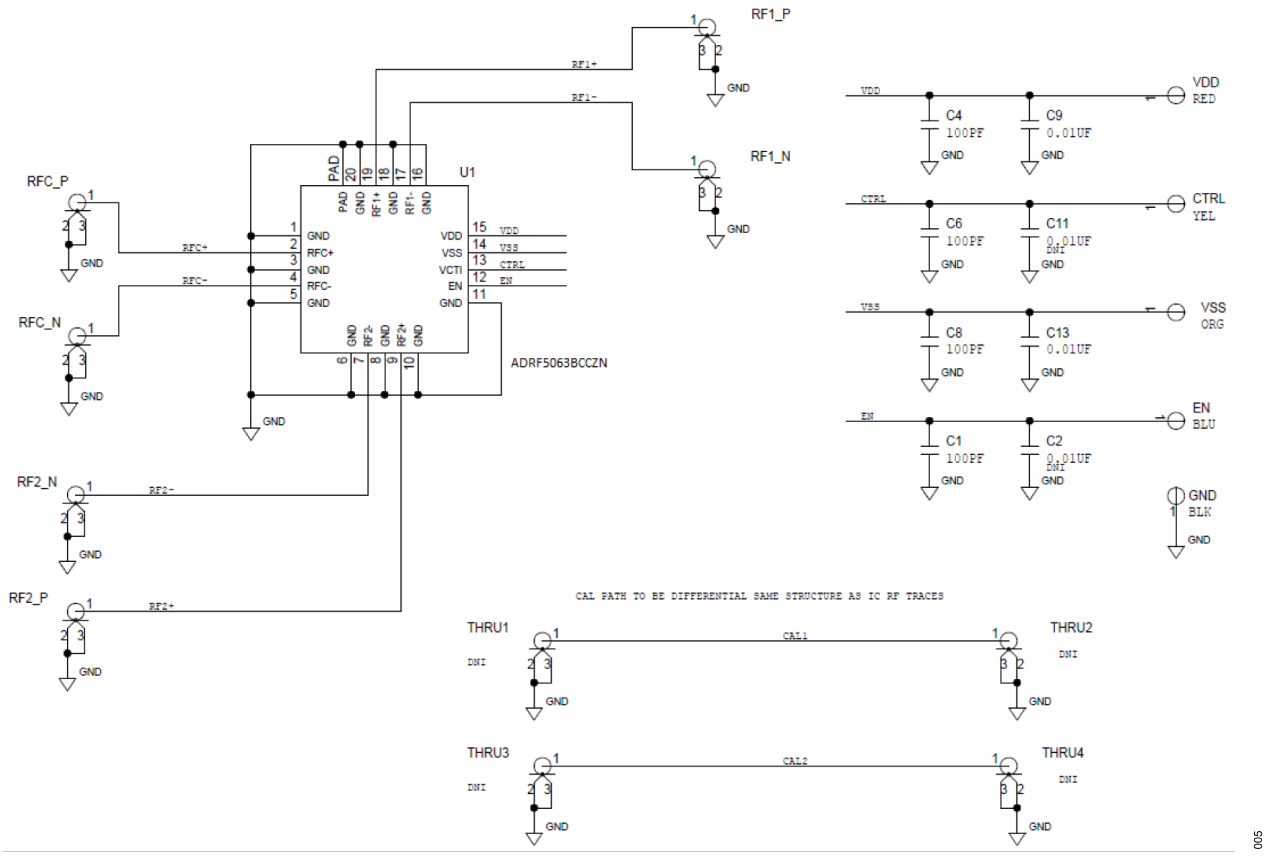

Figure 5. ADRF5063-EVALZ Evaluation Board Schematic

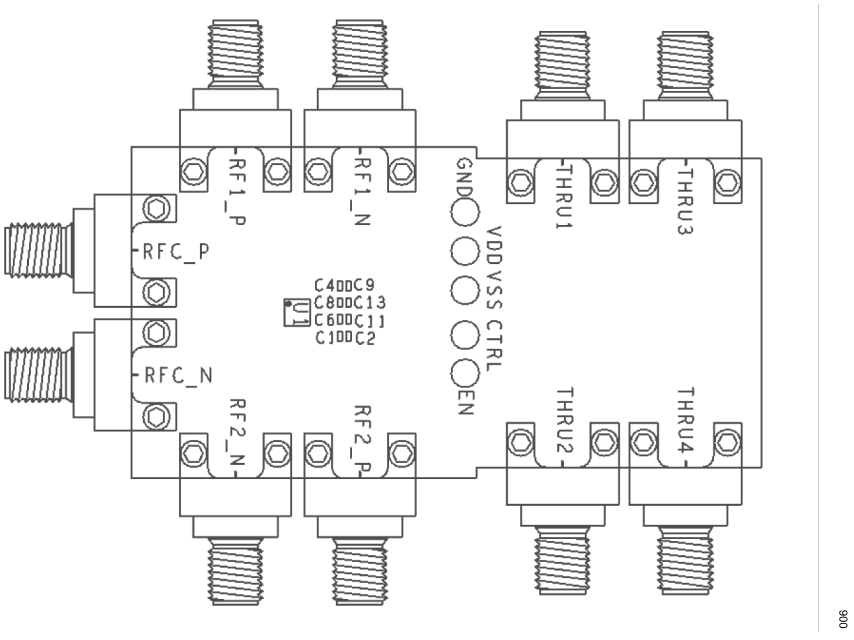

Figure 6. ADRF5063-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for ADRF5063-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
4	C1, C4, C6, C8	100 pF ceramic capacitors, 50 V, 5%, C0G, 0402	Murata	GCM1555C1H101JA16D
2	C9, C13	0.01 µF ceramic capacitors, 50 V, 10%, X7R, 0402	Murata	GCM155R71H103KA55D
6	RFC_P, RFC_N, RF1_P, RF1_N, RF2_P, RF2_N	Edge-mount 2.92 mm connectors	Hirose Electric CO.	HK-LR-SR2(12)
5	GND, CTRL, EN, VDD, VSS	Surface-mount test points	Components Corporation	TP-104-01-0x
1	U1	9 kHz to 13 GHz, differential SPDT switch	Analog Devices	ADRF5063BCCZN
1	PCB	ADRF5063-EVALZ	Analog Devices	BR-066708
2	C2, C11	0.01 µF ceramic capacitors, 50 V, 10%, X7R, 0402, do not install (DNI)	Murata	GCM155R71H103KA55D
4	THRU1, THRU2, THRU3, THRU4	Edge-mount 2.92 mm connectors (DNI)	Hirose Electric CO.	HK-LR-SR2(12)

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.