Evaluating the ADRF5060 Nonreflective RF Path Selector SP3T with Bypass, 100MHz to 20GHz

FEATURES

- Full-featured evaluation board for the ADRF5060
- Easy connection to the test equipment
- Thru line for calibration

EVALUATION KIT CONTENTS

- ADRF5060-EVALZ evaluation board

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

DOCUMENTS NEEDED

- ADRF5060 data sheet

GENERAL DESCRIPTION

The ADRF5060 is a SP3T switch with bypass, manufactured in a silicon on insulator (SOI) process.

This user guide describes the ADRF5060-EVALZ evaluation board, designed to evaluate the features and performance of the ADRF5060. Figure 1 shows a photograph of the evaluation board.

Full specifications on the ADRF5060 are available in the ADRF5060 data sheet from Analog Devices. Consult the ADRF5060 data sheet with this user guide when using the ADRF5060-EVALZ evaluation board.

EVALUATION BOARD PHOTOGRAPH

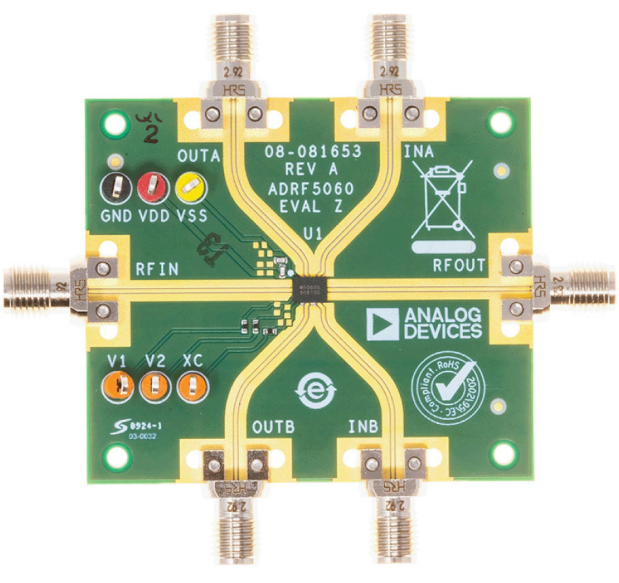

Figure 1. ADRF5060-EVALZ Evaluation Board Photograph

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REVISION HISTORY

5/2025—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5060-EVALZ is a connectorized board, assembled with the ADRF5060 and its application circuitry. All components are placed on the primary side of the ADRF5060-EVALZ evaluation board. Figure 6 shows an assembly drawing for the ADRF5060-EVALZ and Figure 5 shows an evaluation board schematic.

BOARD LAYOUT

The ADRF5060-EVALZ evaluation board is designed using RF circuit design techniques on a four-layer printed circuit board (PCB). Figure 2 shows the PCB stack-up.

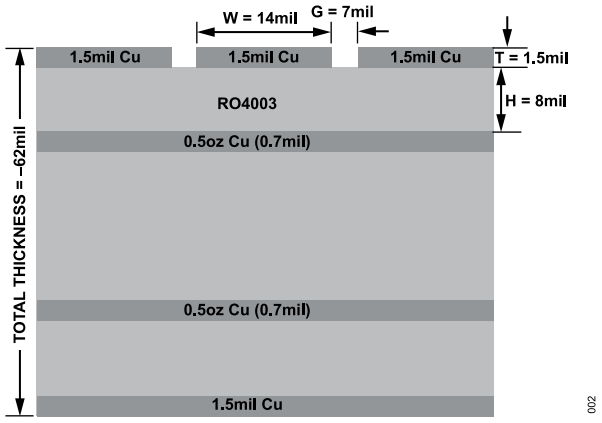

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 1.5mil thick and the inner layers are 0.7mil thick.

All RF and DC traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 8 mil Rogers RO4003, offering optimal high-frequency performance. The middle and bottom dielectric materials provide mechanical strength. The total board thickness is 62mil, which allows 2.4mm RF edge launch connectors to be placed at the board edges.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14mil and ground spacing of 7mil to have a characteristic impedance of 50Ω. Ground via fences is arranged on both sides of a CPWG to improve isolation between nearby RF lines and other signal lines.

POWER-SUPPLY AND CONTROL INPUTS

The ADRF5060-EVALZ evaluation board has two power-supply inputs, three control inputs, and a ground, as shown in Table 1. The DC test points are populated on VDD, VSS, V1, V2, XC, and GND. A 3.3V supply is connected to the DC test points on VDD, and a −3.3V supply is connected to the DC test points on VSS. Ground reference can be connected to GND. Connect the control inputs, V1, V2, and XC, to 3.3V or 0V. The typical total current consumption for the ADRF5060 is 660µA.

The VDD and VSS supply pins of the ADRF5060 are decoupled with 100pF capacitors.

Table 1. Power-Supply and Control Inputs

Test Points	Description
VDD	Positive supply voltage
VSS	Negative supply voltage
V1	Control Input Voltage 1
V2	Control Input Voltage 2
XC	Cross port control voltage
GND	Ground

RF INPUTS AND OUTPUTS

The ADRF5060-EVALZ evaluation board has eight edge-mounted, 2.92mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

2.92mm Connectors	Description
RFIN	RF Input
OUTB	Output path for External Path B
INB	Input path for External Path B
OUTA	Output path for External Path A
INA	Input path for External Path A
RFOUT	RF output
THRU1	Thru line input and output
THRU2	Thru line input and output

The through calibration line, connecting the THRU1 and THRU2 RF connectors, calibrates out the board loss effects from the measurements of the ADRF5060-EVALZ evaluation board to determine the device performance at the pins of the IC. Figure 3 shows the typical board loss for the ADRF5060-EVALZ evaluation board at room temperature, as well as the embedded and de-embedded insertion loss for the ADRF5060.

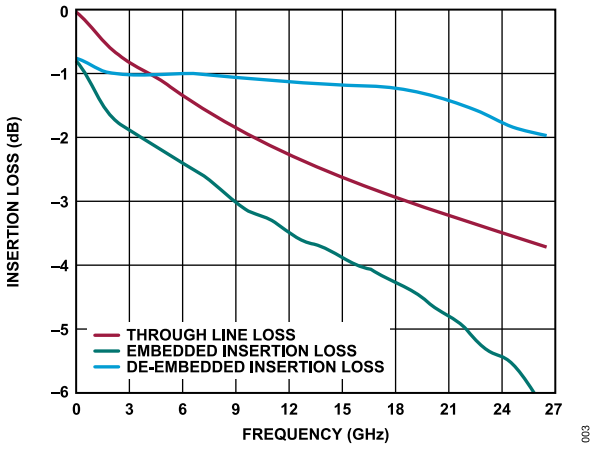

Figure 3. Insertion Loss vs. Frequency

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5060-EVALZ evaluation board, follow these steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the VSS test point.
4. Bias up the digital control test points.
5. Apply an RF input signal.

The ADRF5060-EVALZ evaluation board is shipped fully assembled and tested. Figure 4 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Follow these steps to complete the test setup and verify the operation of the ADRF5060-EVALZ evaluation board:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage-output terminal of the 3.3V supply.
3. Connect the VSS test point to the voltage-output terminal of the −3.3V supply.
4. Connect the V1, V2, and XC test points to the voltage-output terminal of the 3.3V supply(if needed). The ADRF5060 can be configured in different modes by connecting the CTRL test point to 3.3V or 0V, as shown in Table 3.
5. Connect a calibrated network analyzer to the RFIN, RFOUT 2.92mm connectors. If the network analyzer port count is not enough, terminate unused RF ports with 50Ω. Sweep the frequency from 10MHz to 30GHz and set the power to –10dBm.

Additional test equipment is needed to fully evaluate the functions and performance of the device.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high-isolation power combiner is also recommended.

For power compression and power handling evaluations, use a two-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

Note that the measurements performed at the 2.92mm connectors of the ADRF5060-EVALZ evaluation board include the losses of the 2.92mm connectors and the PCB. The thru line must be measured to calibrate out the effects on the ADRF5060-EVALZ evaluation board. The thru line is the summation of an RF input line and an RF output line connected to the device and equal in length.

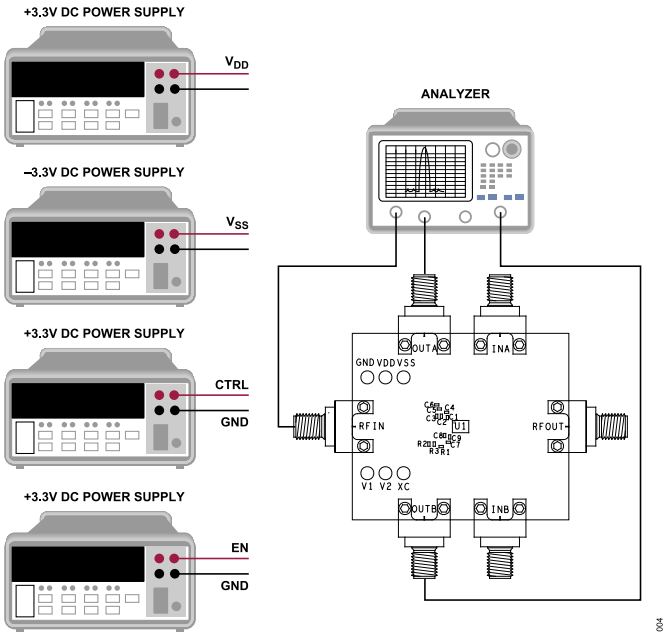

Figure 4. Test Setup Diagram

Table 3. Control Voltage Truth Table

RF Path Selection	XC	V1	V2
Through	Don't care	Low	Low
External Path B	Low	Low	High
External Path A	Low	High	Low
All Off (Isolation)	Don't care	High	High
Through	Don't care	Low	Low
Out A and In B	High	Low	High
Out B and In A	High	High	Low
All Off (Isolation)	Don't care	High	High

EVALUATION BOARD SCHEMATIC AND ASSEMBLY DIAGRAM

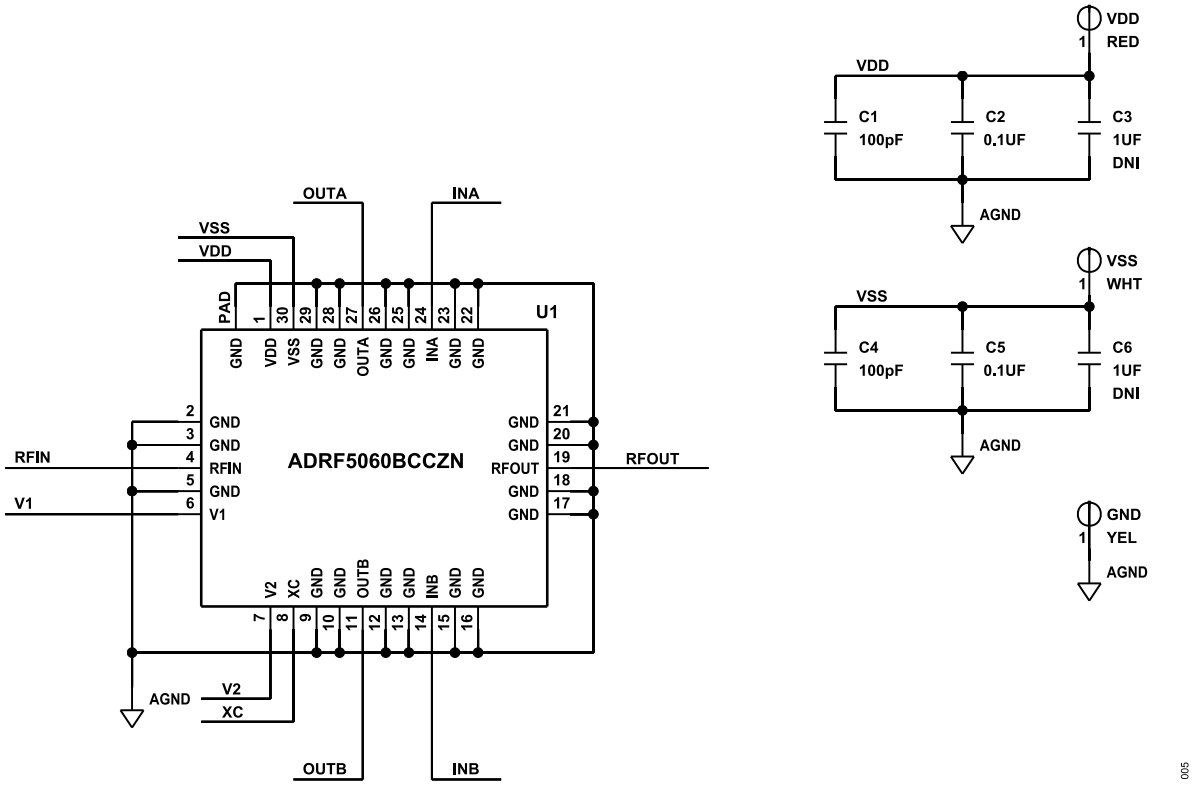

Figure 5. ADRF5060-EVALZ Evaluation Board Schematic

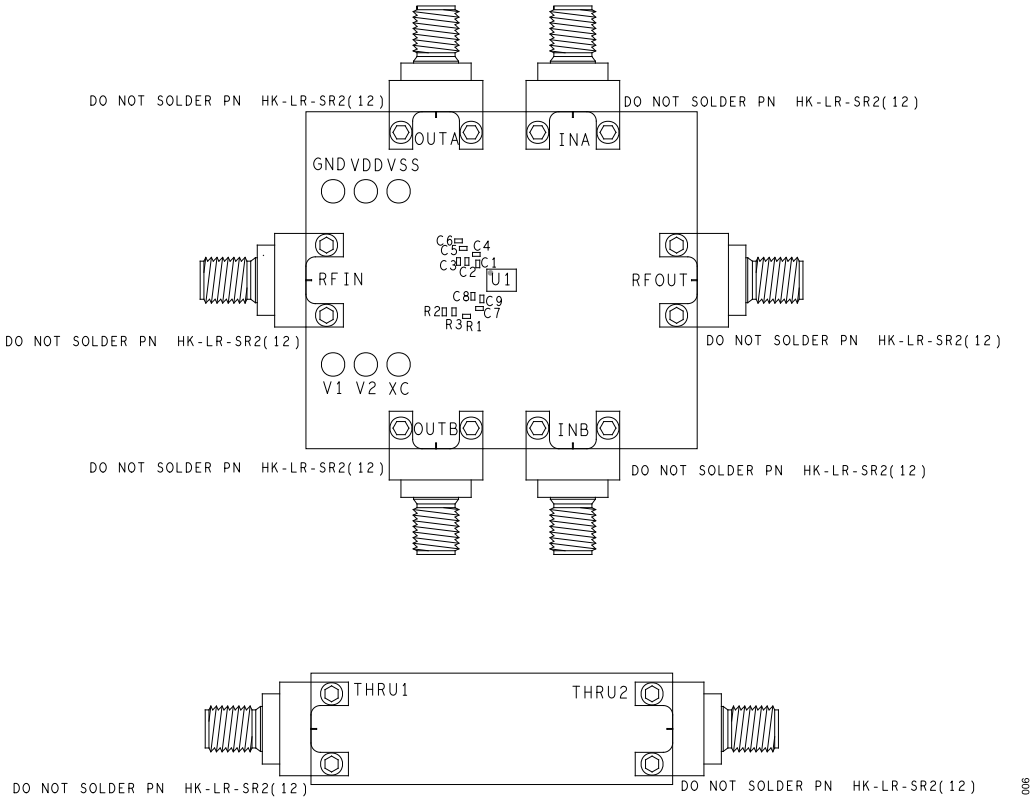

Figure 6. ADRF5060-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

EVALUATION BOARDS

Model[1]	Description
ADRF5060-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.

BILL OF MATERIALS

Table 4. Bill of Materials for ADRF5060-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
2	C1, C4	Capacitors, 100pF, 50V, 5%, C0G, C0402 package	Samsung	CL05C101JB5NNNC
2	C2, C5	Capacitors, 0.1µF, 50V, 10%, X7R, C0402 package	Murata	GRM155R71H104KE14J
2	C3, C6	Ceramic capacitors, 1µF, 10V, 10%, X7R, 0402 (do not install (DNI))	Murata	GRM155Z71A105KE01D
3	C7, C8, C9	Ceramic capacitors, 100pF, 50V, 5%, C0G, 0402 (DNI)	Samsung	CL05C101JB5NNNC
2	R1, R2, R3	Resistors, surface-mounted device (SMD) 0Ω, Jumper, 1/8W, 0402, AEC-Q200	Vishay	RCC04020000Z0ED
5	RFIN, OUTA, INA, OUTB, OUTA, RFOUT, THRU1, and THRU2	Connectors, PCB, 2.92mm, 50Ω, 40GHz	Hirose Electric Co.	HK-LR-SR2(12)
5	GND, VDD, VSS, V1, V2, and XC	Surface-mount test points	Components Corporation	TP104-01
1	U1	Nonreflective RF path selector SP3T with bypass, 100MHz to 20GHz	Analog Devices, Inc.	ADRF5060BCCZN
1	PCB	ADRF5060-EVALZ	Analog Devices	BR-081653

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.