Evaluating the ADRF5051 Silicon SP4T Switch, Nonreflective, 9kHz to 20GHz

FEATURES

- Full feature availability for the ADRF5051
- Easy connection to test equipment
- Additional through line for calibration
- Dual- and single-supply operation support

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

This user guide describes the ADRF5051-EVALZ evaluation board, which is designed to simply evaluate the features and performance of the ADRF5051. A photograph of the evaluation board is shown in Figure 1. Note that ADRF5051-EVALZ is shared with ADRF5050.

The ADRF5051 is a silicon SP4T switch, nonreflective, manufactured in the silicon on insulator (SOI) process. Refer to the ADRF5051 data sheet with this user guide when using the ADRF5051-EVALZ.

ADRF5051-EVALZ EVALUATION BOARD PHOTOGRAPH

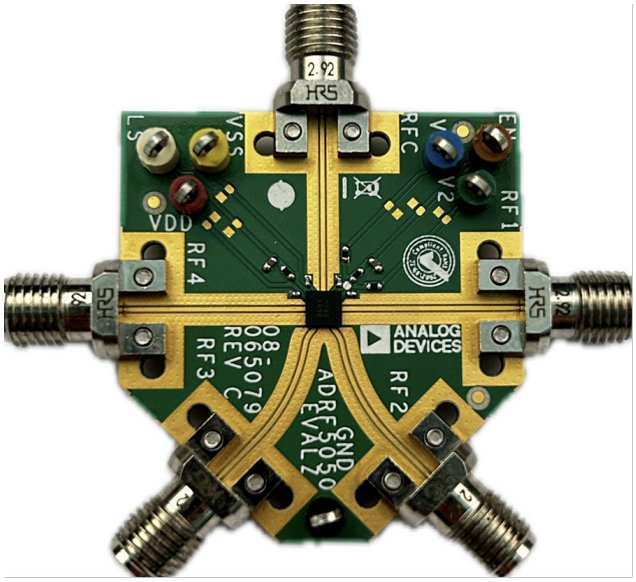

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Figure 1. ADRF5051-EVALZ Evaluation Board Photograph

TABLE OF CONTENTS

REVISION HISTORY

3/2025—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5051-EVALZ is a connectorized board, assembled with the ADRF5051 and its application circuitry. All components are placed on the primary side of ADRF5051-EVALZ. The evaluation board schematic is shown in Figure 10, and the assembly drawing for the ADRF5051-EVALZ is shown in Figure 11.

BOARD LAYOUT

The PCB stack-up for the ADRF5051-EVALZ is shown in Figure 2.

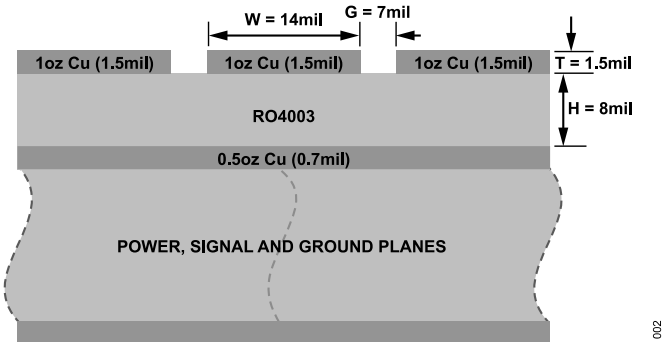

Figure 2. Evaluation Board Stack-Up

The PCB stack-up has four layers. The outer copper layers are 1oz (1.5mil) thick and the inner layers are 0.5oz (0.7mil) thick.

The top dielectric material is 8mil Rogers 4003, which provides 50Ω-controlled impedance and optimizes the high frequency performance. All RF traces are routed on the top layer, and the second layer is used as the ground plane for the RF transmission lines. The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14mil and ground spacing of 7mil to have a characteristic impedance of 50Ω. Ground via fences are arranged on both sides of the CPWG to improve isolation between nearby RF lines and other signal lines.

The bottom two layers are also ground planes filled with FR4 material to manage the thermal rise during high power operations and are supported with dense and filled vias to the PCB bottom for thermal relief. The exposed ground pad of the ADRF5051, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The total board thickness is approximately 62mil for mechanical strength.

POWER SUPPLY AND CONTROL CONNECTIONS

The ADRF5051-EVALZ has two power supply pins (VDD and VSS), four control pins (V1, V2, EN, and LS), and a ground pin (GND) that are all connected with DC test points. The VDD and VSS supply pins and control pins of the ADRF5051 are decoupled with 100pF capacitors.

Table 1. Power Supply and Control Connections

Test Point	Description
VDD	+3.3V supply voltage
VSS	−3.3V supply voltage
V1	Control Input 1
V2	Control Input 2
EN	Enable
LS	Logic select
GND	Ground

EVALUATION BOARD HARDWARE

RF CONNECTIONS

The ADRF5051-EVALZ has five edge-mounted, 2.92mm connectors for the RF ports, as detailed in Table 2.

Table 2. RF Inputs and Outputs

SMA Connector	Description
RFC	RF common port
RF1	RF Throw Port 1
RF2	RF Throw Port 2
RF3	RF Throw Port 3
RF4	RF Throw Port 4

The ADRF5051-EVALZ is shipped together with a through line that is used for de-embedding the board loss effects from the measurements, which are enabled to determine the device performance at the pins of the ADRF5051. Figure 3 shows the typical board loss (through line) for the ADRF5051-EVALZ at room temperature, as well as the nonde-embedded and de-embedded insertion loss for the ADRF5051.

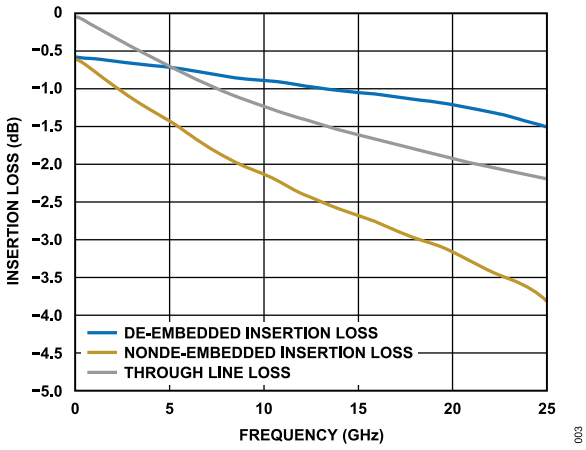

Figure 3. Insertion Loss vs. Frequency

TEST PROCEDURE

BIASING SEQUENCE

The ADRF5051-EVALZ is shipped fully assembled and tested. Figure 4 provides a basic test setup diagram to evaluate the S-parameters using a network analyzer. Take the following steps to complete the test setup and to verify the operation of the ADRF5051-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage output terminal of the 3.3V supply.
3. Connect the VSS test point to the voltage output terminal of the −3.3V supply. Note that the current from the VDD test point is approximately 160µA and from the VSS test point is approximately 540µA.
4. Connect the V1, V2, EN, and LS test points to the voltage output terminal of the 3.3V supply. The ADRF5051 can be configured in different modes by connecting the control test points to 3.3V or 0V, as detailed in Table 3.
5. Connect a calibrated network analyzer to the RFC, RF1, RF2, RF3, and RF4 2.92mm connectors. If the network analyzer port count is not enough, terminate unused RF ports with 50Ω (see Figure 4). Set the power to –5dBm and sweep the frequency from 9kHz to 20GHz.
6. The ADRF5051-EVALZ is expected to have an insertion loss of 1.20dB at 20GHz. See Figure 3 for the nonde-embedded and de-embedded insertion loss. See Figure 5 to Figure 9 for the de-embedded results.

Additional test equipment is required to fully evaluate the device functions and performance.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is also recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

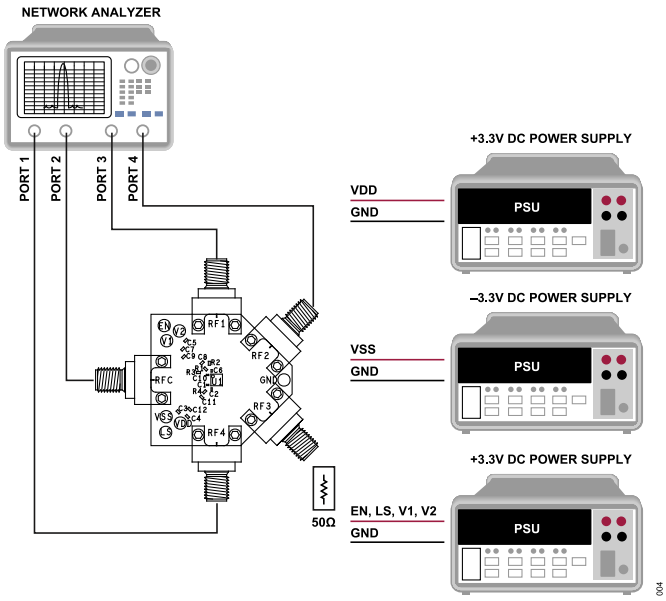

Figure 4. Test Setup Diagram

Table 3. Control Voltage Truth Table

Digital Control Inputs				RFx Paths			
EN	LS	V1	V2	RF1 to RFC	RF2 to RFC	RF3 to RFC	RF4 to RFC
Low	Low	Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	Low	High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	Low	Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	High	Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low or high	Low or high	Low or high	Isolation (off)	Isolation (off)	Isolation (off)	Isolation (off)

TEST PROCEDURE

EXPECTED RESULTS

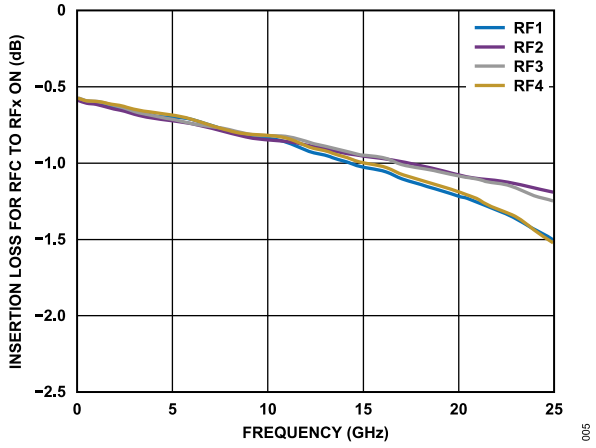

Figure 5. Insertion Loss for RFC to RFx (On) vs. Frequency

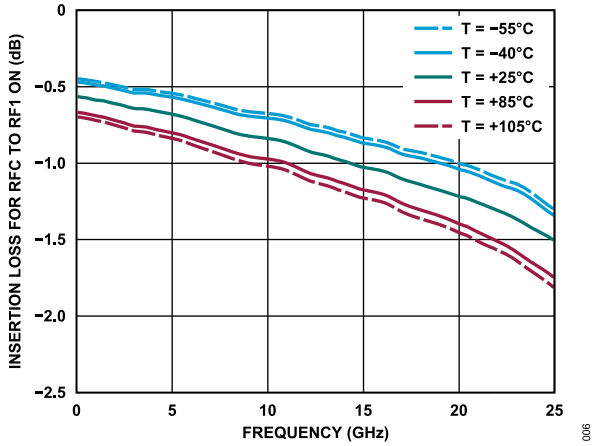

Figure 6. Insertion Loss for RFC to RF1 (On) vs. Frequency over Temperature

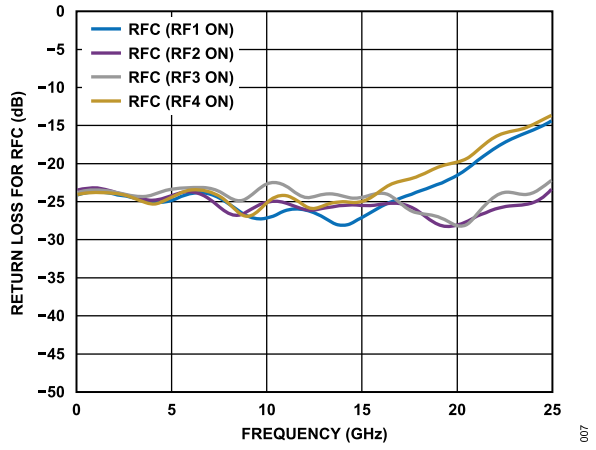

Figure 7. Return Loss for RFC vs. Frequency

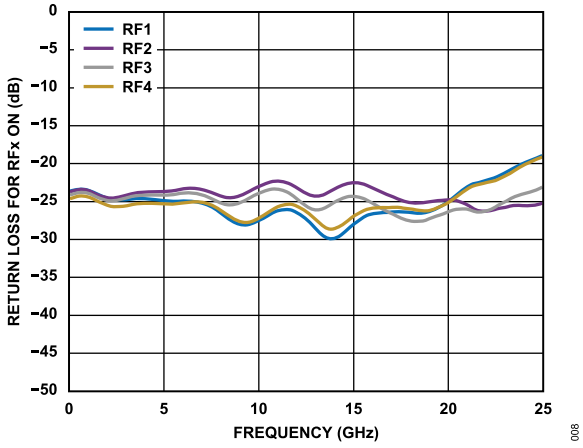

Figure 8. Return Loss for RFx (On) vs. Frequency

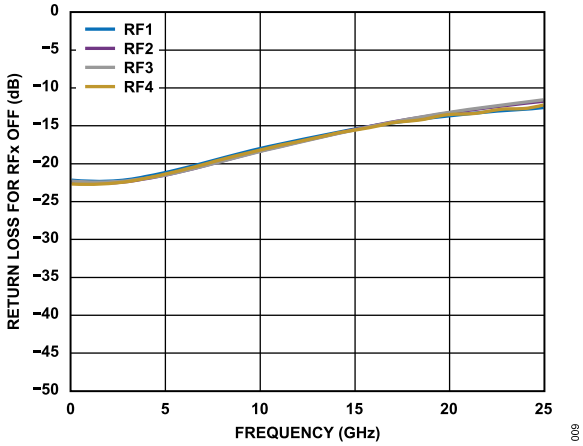

Figure 9. Return Loss for RFx (Off) vs. Frequency

EVALUATION BOARD SCHEMATIC AND ARTWORK

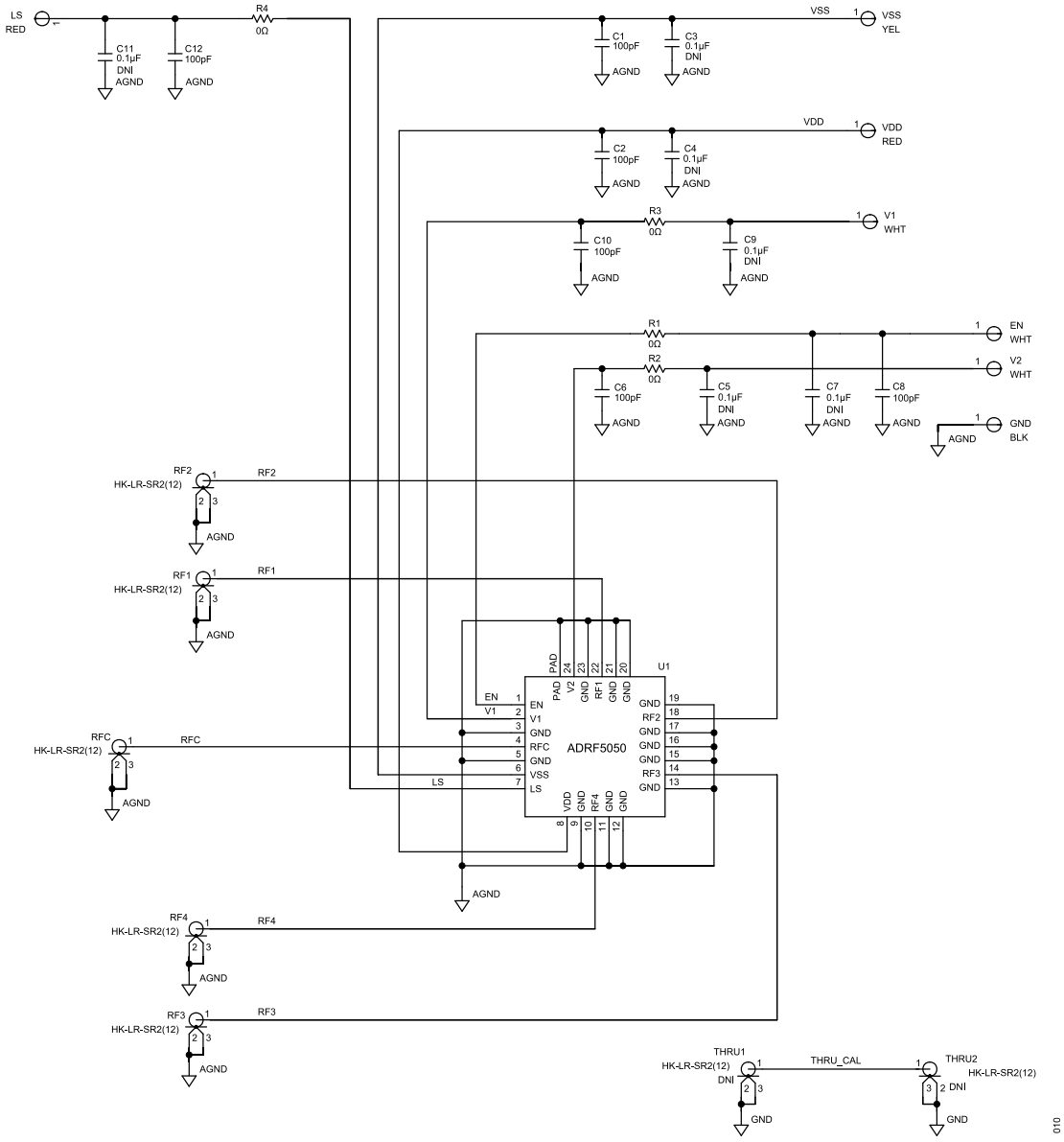

Figure 10. ADRF5051-EVALZ Evaluation Board Schematic

EVALUATION BOARD SCHEMATIC AND ARTWORK

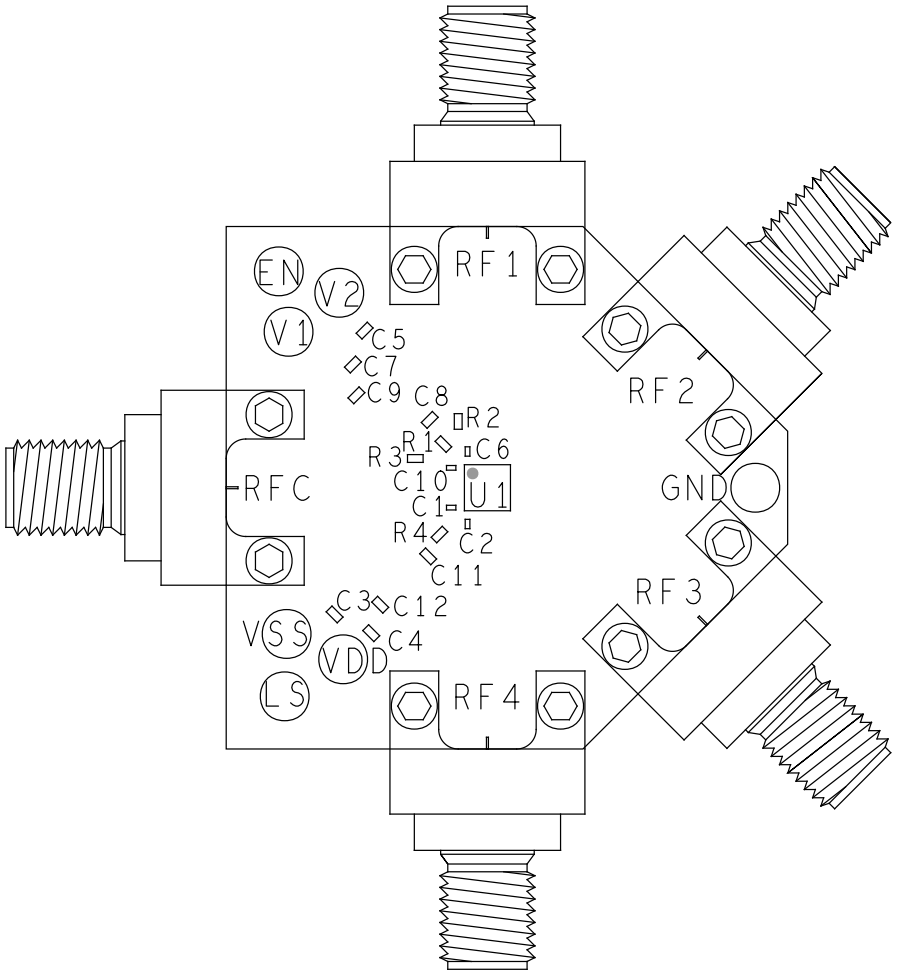

Figure 11. ADRF5051-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for ADRF5051-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
4	C1, C2, C6, C10	Capacitors, 100pF, 25V, C0201 package	Murata	GRM033R71E101KA01D
2	C8, C12	Capacitors, 100pF, 50V, C0402 package	Murata	GCM1555C1H101JA16D
4	R1, R2, R3, R4	Resistors, 0Ω, 1/10W, R0402 package	Panasonic	ERJ-2GE0R00X
5	RF1, RF2, RF3, RF4, RFC	Edge-mount 2.92mm connectors	Hirose Electronic Co.	HK-LR-SR2(12)
7	EN, V1, V2, GND, LS, VDD, VSS	Surface-mount test points	Keystone Electronics	500x
1	U1	Silicon SP4T switch, nonreflective, 9kHz to 20GHz	Analog Devices, Inc.	ADRF5051
1	PCB	Evaluation board	Analog Devices	ADRF5051-EVALZ

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.