Evaluation Board User Guide

ADPL83200 Evaluation Board

Evaluates: ADPL83200

General Description

Evaluation board EVAL-ADPL83200-IZ features the ADPL83200IS6, low-loss PowerPath™ controller. The controller is capable of automatically switching between primary and auxiliary power sources for a single output. The ADPL83200 circuit is intended for lower current loads.

The input supply voltage ranges from 2.5V to 36V. As initially configured with the default MOSFET, the ADPL83200 circuit's maximum input voltage is 18V. The ADPL83200 circuit current limit is 2A.

The primary power paths can be controlled with external logic applied to the CTL pins. PowerPath status can be monitored using the STAT pins. Evaluation of higher current or more complex sourcing systems can be accomplished by installing additional ICs, as well as paralleling the inputs and/or outputs using the optional supplied pads. Multiple standard Metal-oxide-semiconductor field-effect transistor (MOSFET) package options are also available on each circuit for evaluation convenience.

Ordering Information ***appears at end of data sheet***

Quick Start Procedure

Evaluation board EVAL-ADPL83200-IZ is easy to set up to evaluate the performance of ADPL83200. See *Figure 1* for the proper measurement equipment setup of both circuits, use the following procedures.

ADPL83200 Circuit

1. With all power off, connect the auxiliary (V_{AUX}) and primary (V_{IN}) power supplies, each capable of 2A, to the system load and meters as shown in *Figure 1*.
2. Preset the system load to 0A and the input supplies to 0V, 0A current limit.
3. Connect the system load to the output terminals, V_{OUT} and GND.
4. Turn on the supplies, setting the current limit up to 2A. Adjust the voltages to the desired value, up to 18V. The higher voltage of the two supplies should appear at the output.
5. Turn the load on and adjust as necessary.
6. Adjust the supplies and observe how the output switches over to follow the higher voltage of the two sources.

Optional

7. For improved current handling, install additional MOSFETs, select from different package footprints, or shunt the circuits at V_{IN}, V_{OUT}, and GND.
8. For source-load back-to-back isolation, remove jumpers JMP3 and JMP4, then install additional MOSFETs back-to-back as shown in *Figure 2*.
9. For external control of the primary source power path, remove the 0Ω jumper on the CTL pin, R2. Apply the logic-control signal on CTL as necessary.

Performance Summary

PARAMETER	CONDITIONS	VALUE
Minimum ADPL83200 Input Voltage	V_{IN}	2.5V
Maximum ADPL83200 Input Voltage	V_{IN} and V_{AUX}	18V
ADPL83200 Maximum Current	MOSFET Limited	2A

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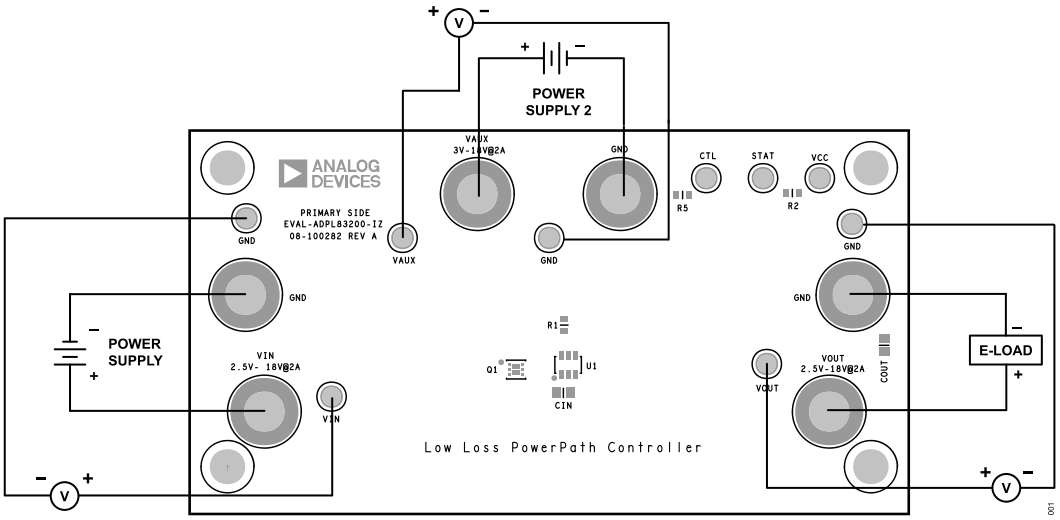

Figure 1. Test Setup of EVAL-ADPL83200-IZ

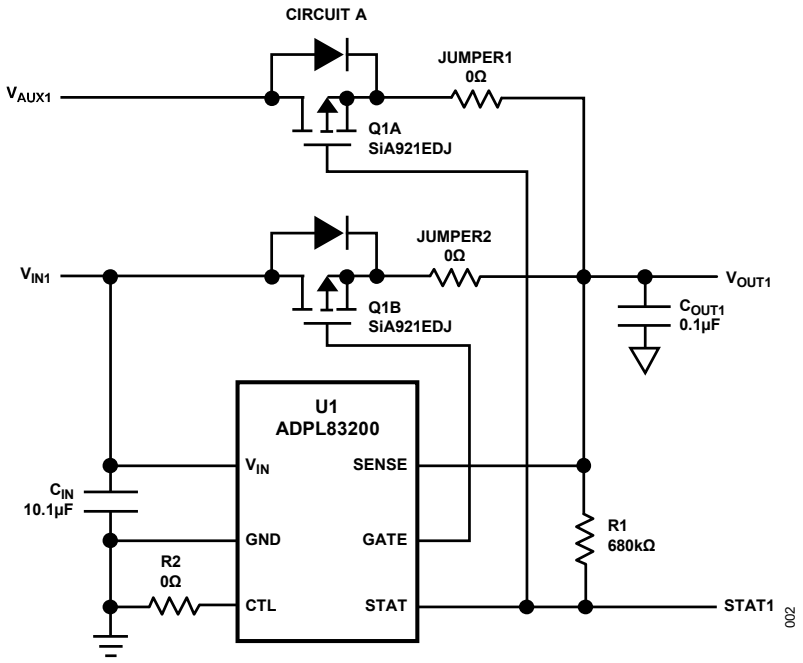

Figure 2. Standard Configurations with Automatic Switchover between Sources

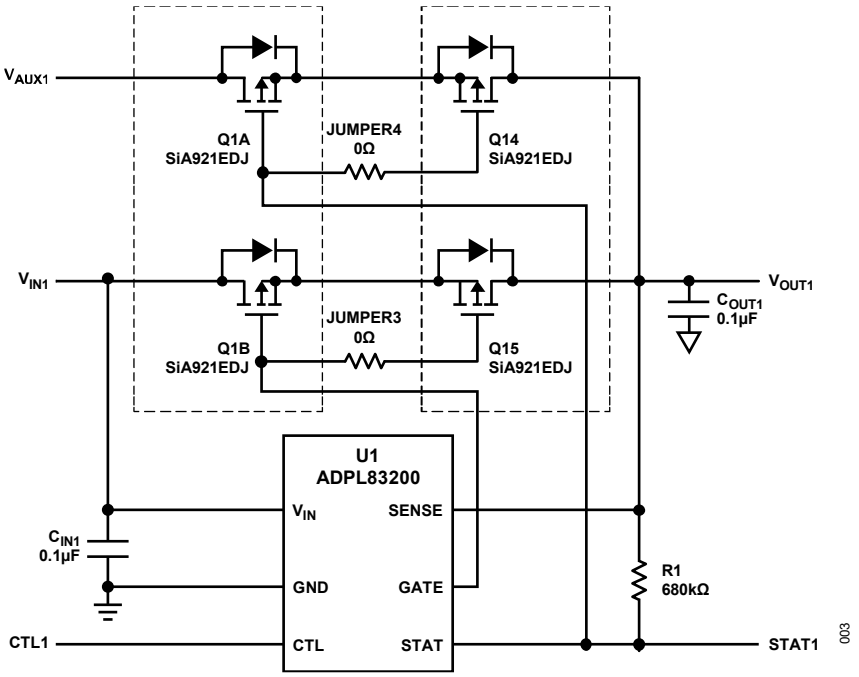

Figure 3. Optional, Fully-Isolated Configurations with External Logic Control

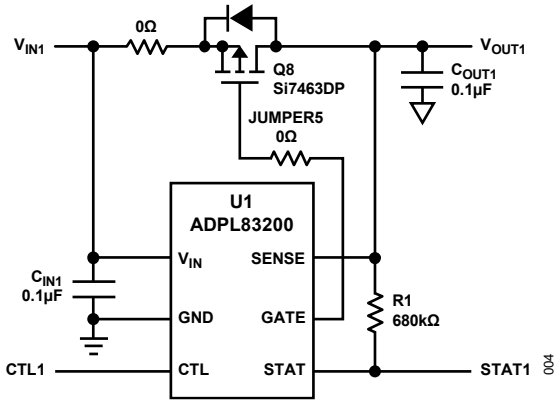

Figure 4. Optional, High Side Switch with Logic Control and Status Output (Requires 0Ω Jumper Across Drain-Source Pins of Q7)

Note: Diodes shown are body diodes of their respective MOSFETs. Do not install extra diodes, or the operation of the power paths may be compromised.

Ordering Information

MODEL[1]	DESCRIPTION
EVAL-ADPL83200-IZ	Evaluation board

[1]*Z = RoHS Compliant Part*

EVAL-ADPL83200-IZ Evaluation Board Bill of Materials

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	2	C_{OUT}, C_{IN}	CAP, X7R, 0.1µF 50V 10%, 0805	AVX, 08055C104KAT4A
2	1	Q1	DUAL P-CHANNEL, 20V/4.5A	VISHAY, SiA921EDJ-T1-E3
3	1	R1	RES., CHIP 698kΩ, 1%, 0603	VISHAY, ERJ-3EKF6983
4	1	R2	RES., CHIP 560kΩ, 1%, 0603	PANASONIC, ERJ-3EKF5603V
5		R5	RES., CHIP 0Ω, 0603	VISHAY, CRCW06030000Z0EA
6	1	U1	I.C., ADPL83200IS6	Analog Devices, Inc., ADPL83200IS6#PBF
ADDITIONAL CIRCUIT COMPONENTS				
1	0	Q12, Q13	OPTIONAL	VISHAY, SiA921EDJ-T1-E3
2	0	Q14, Q15	OPTIONAL	VISHAY, Si7463DP-T1-E3
3	0	Q16, Q17	OPTIONAL	VISHAY, Si7905DN-T1-E3
4	2	JMP3, JMP4	JUMPER, 1206	TEPRO, RN6087
6	0	JMP7, JMP8	RES., 0603 OPT	
8	0	U2	I.C., ADPL83200IS6 OPT	Analog Devices, Inc., ADPL83200IS6#PBF
HARDWARE-FOR EVALUATION BOARD ONLY				
1	9	E1, E2, E3, E4, E9, and E10	TEST POINT TURRET 0.095"	MILL-MAX, 2501-2-00-80-00-00-07-0
		E13, E14, and E15	TEST POINT TURRET 0.095"	MILL-MAX, 2501-2-00-80-00-00-07-0
2	6	J1, J2, J3, J4, J9, and J10	BANANA JACK	KEYSTONE, 575-4
3	4	(STAND OFF)	STAND OFF, NYLON 0.25"	KEYSTONE, 8831 (SNAP ON)

EVAL-ADPL83200-IZ Schematic Diagrams

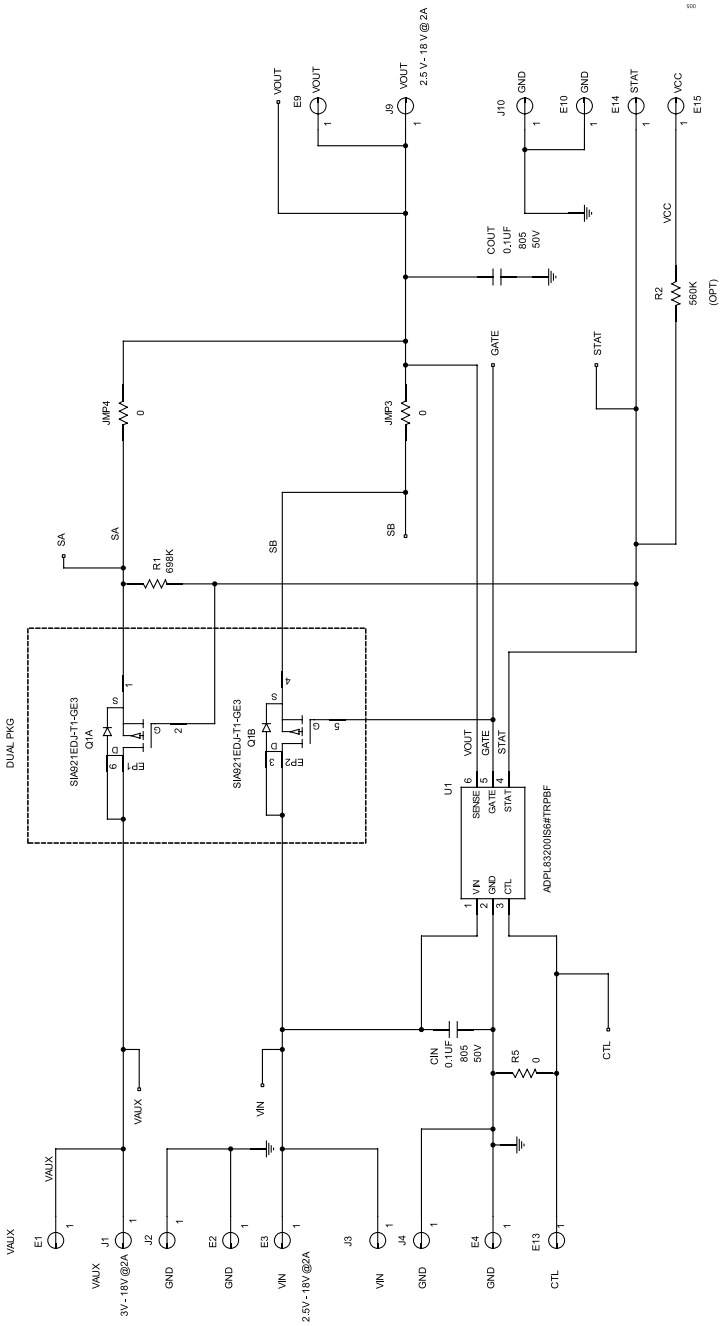

Figure 5. Top Circuit Schematic Diagram

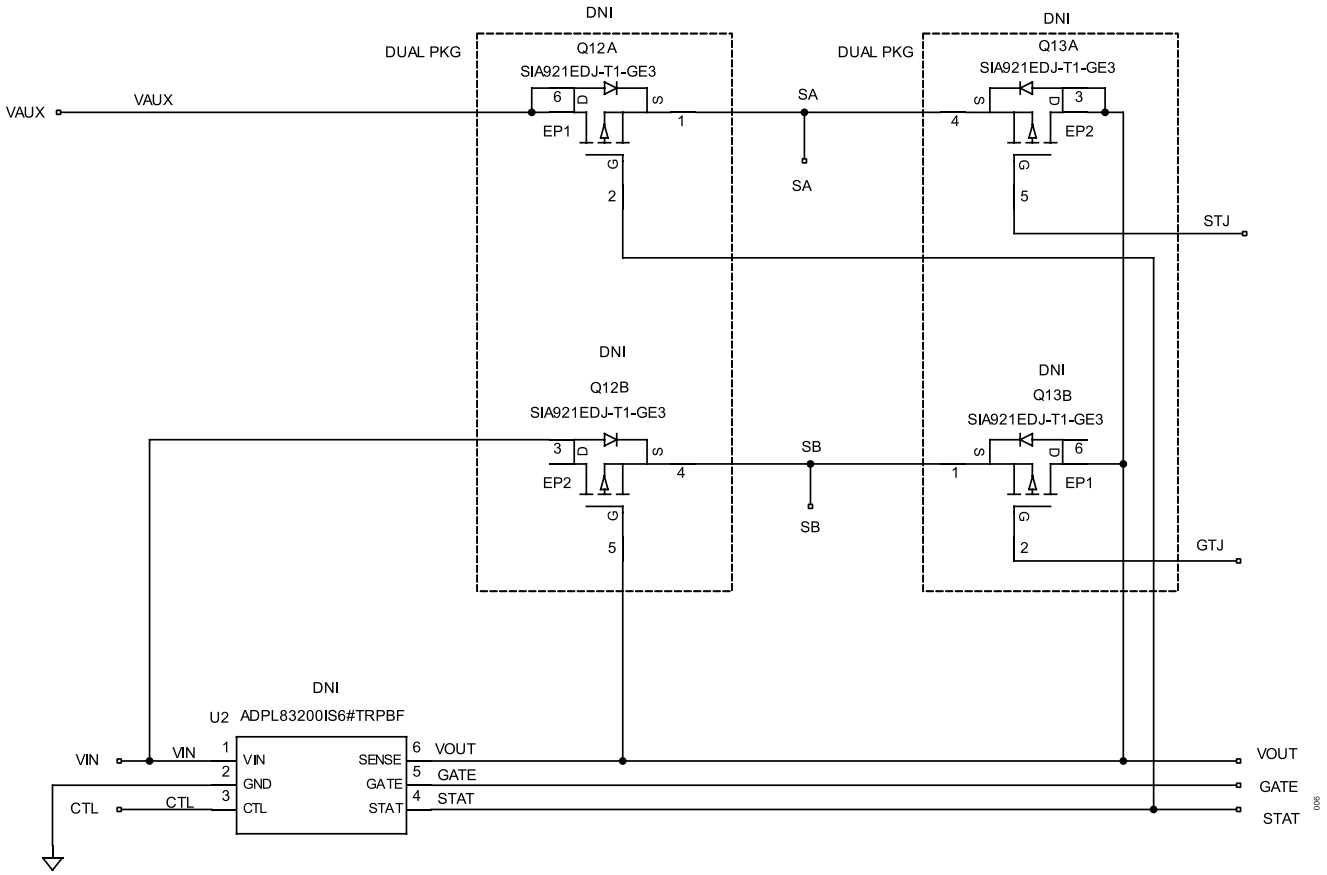

Figure 6. Optional Circuit #1

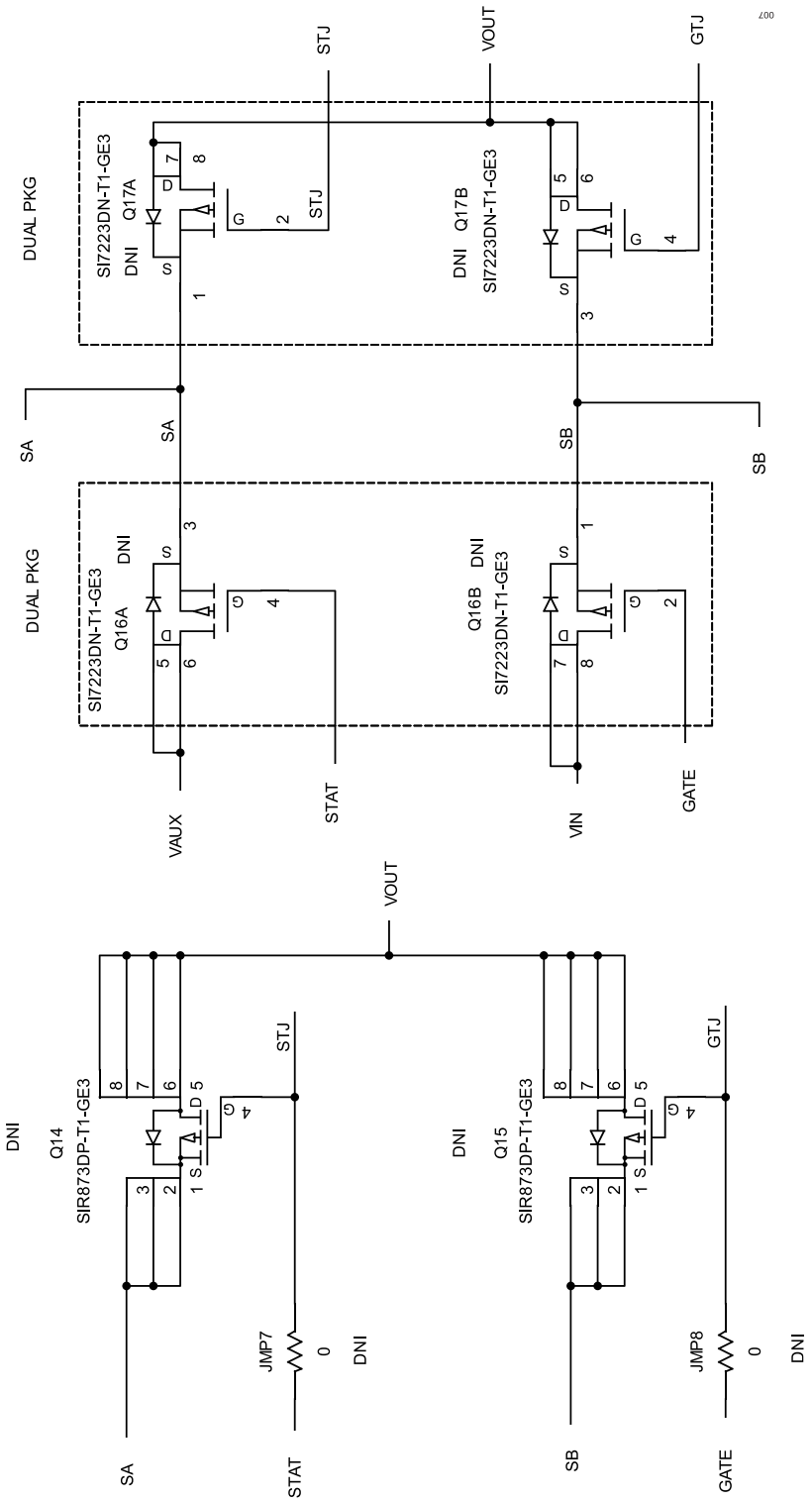

Figure 7. Optional Circuit #2

Evaluation Board PCB Layouts

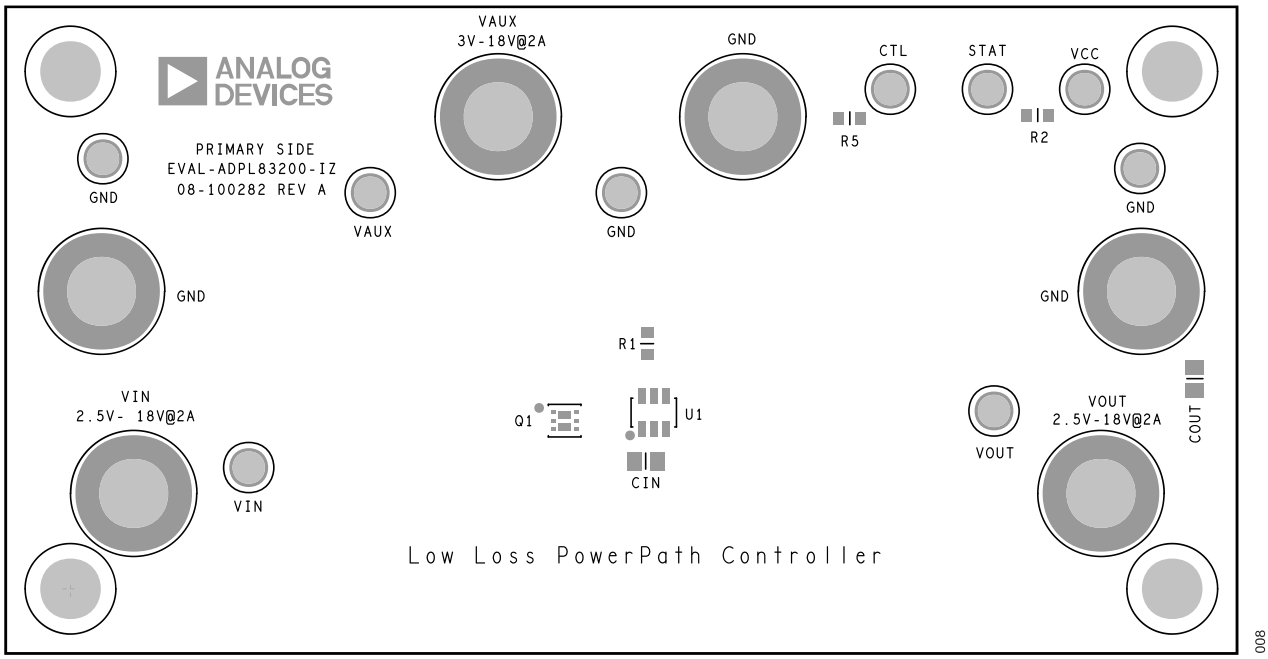

Figure 8. ADPL83200 Evaluation Board Component Placement Guide—Top Silkscreen

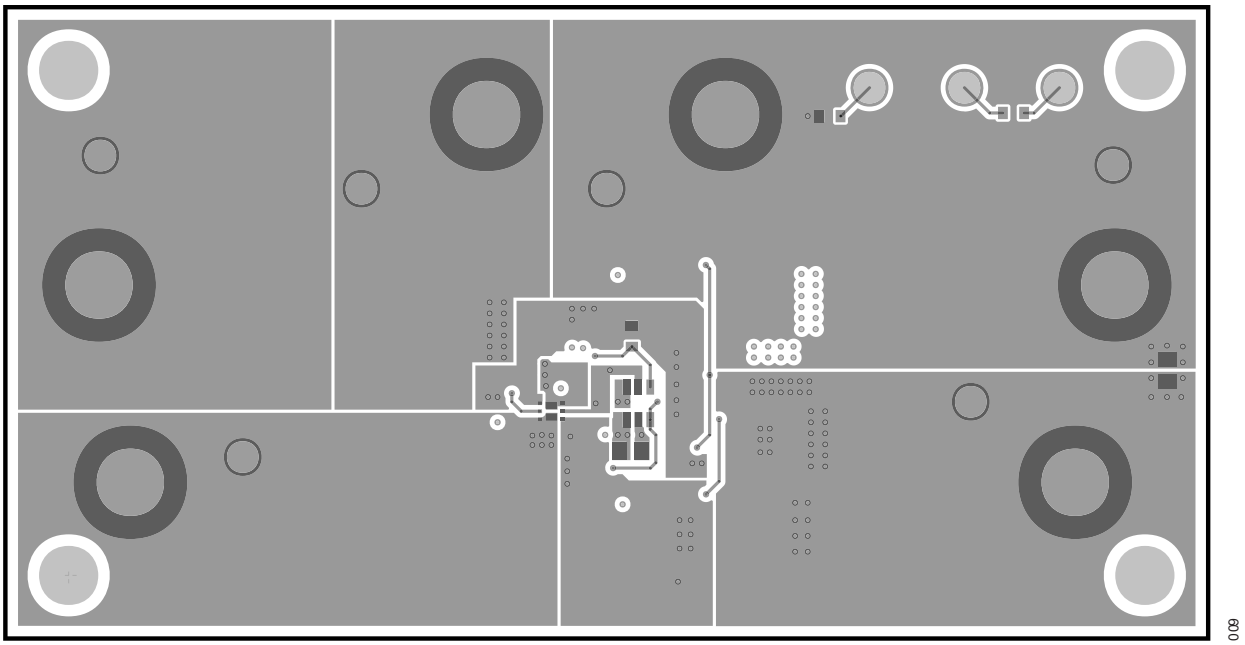

Figure 9. ADPL83200 Evaluation Board PCB Layout—Top View

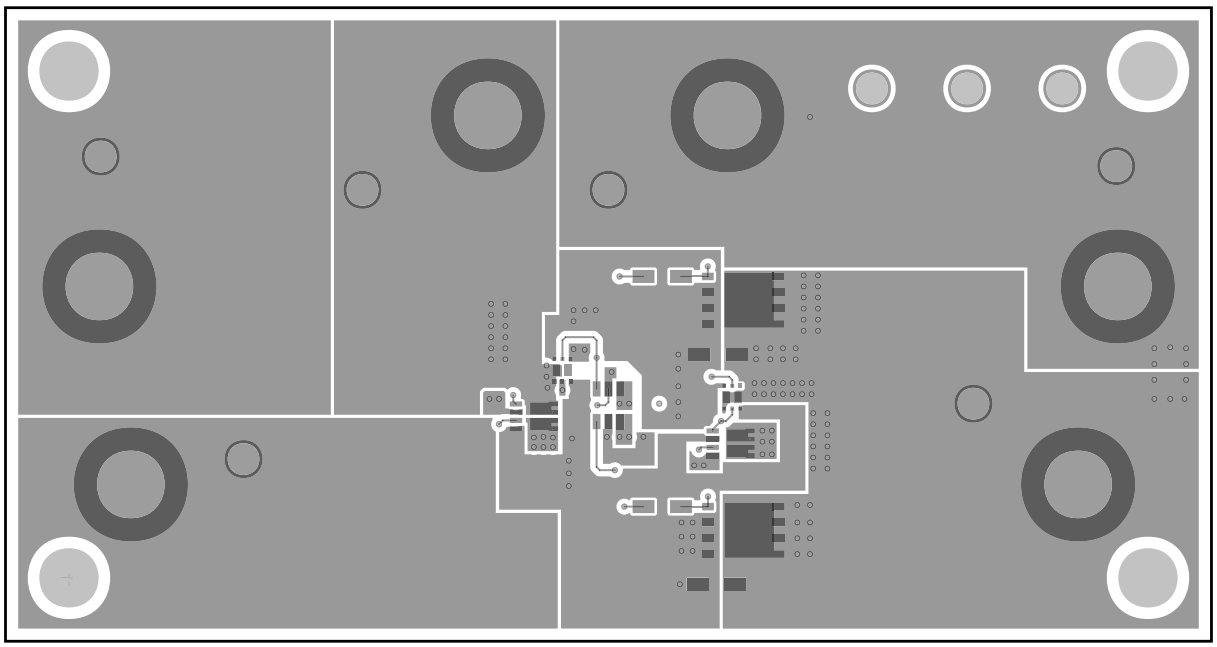

Figure 10. ADPL83200 Evaluation Board PCB Layout—Bottom View

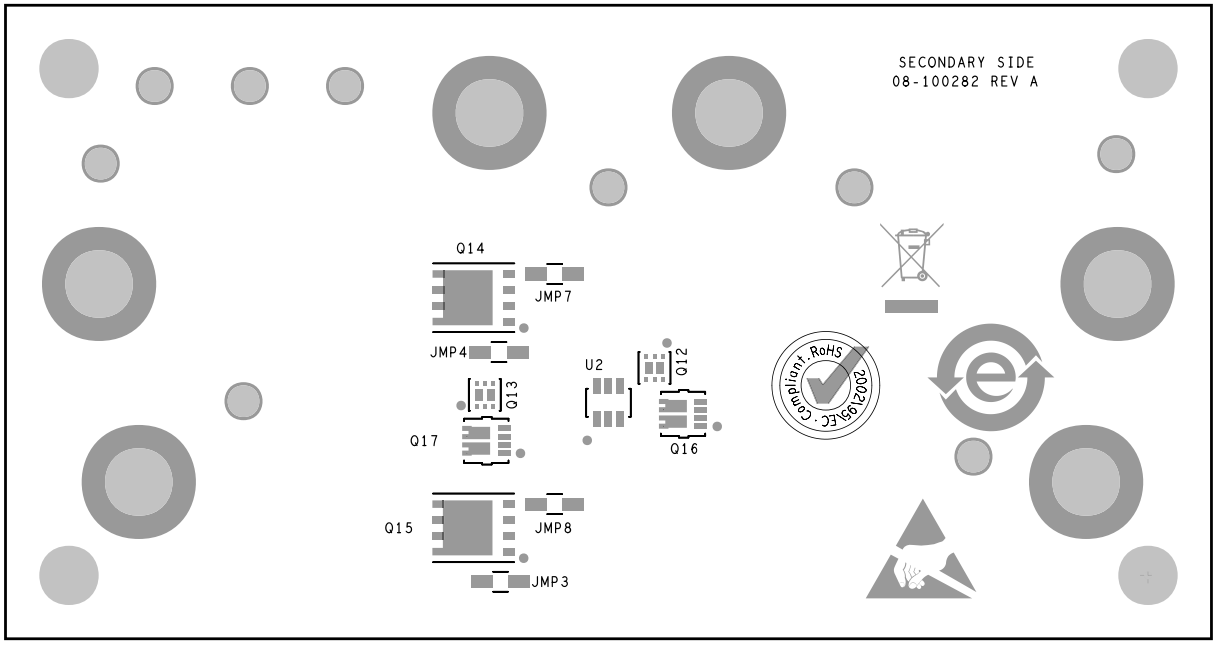

Figure 11. ADPL83200 Evaluation Board Component Placement Guide—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/25	Initial release	—

Notes