Evaluation Board User Guide

EVAL-ADPL42010AZ

Evaluating the ADPL42010A, 20V, 1A, Fast Transient Response LDO Regulator

General Description

The EVAL-ADPL42010AZ evaluation board evaluates the ADPL42010A, a 20V, 1A low dropout linear regulator that is optimized for fast transient response. Circuits designed with the ADPL42010A are used primarily in voltage-controlled oscillators, RF power supplies, and in larger systems, as local regulators. The ability to tolerate a wide variety of output capacitors makes the ADPL42010A ideal in space- and cost-sensitive systems.

Features and Benefits

- Evaluates the ADPL42010A in an 8-Lead SO Package
- Maximum Output Current: 1A
- Jumper programs output voltage according to the resistors set for the output voltage options: **1.2V, 1.5V, 1.8V, 2.5V, 3V, 3.3V,** and **5V**
- Jumper turns the regulator on by connecting the $\overline{SHDN}$ pin to the INPUT pin or connecting the pin to a external supply to turn the regulator on or off
- V_{IN}, V_{OUT}, and GND Test Points for Regulation and Dropout Voltage Monitoring
- Component placeholder for a resistor connected to J2 that can modify the required output voltage of the user when the SENSE/ADJ pin connects to the output through a resistor divider

Quick Start

Required Equipment

- A DC Power Supply
- Multimeters for Voltage and Current Measurements
- Electronic or Resistive Loads

***Ordering Information* appears at end of data sheet.**

Procedure

The EVAL-ADPL42010AZ evaluation board is simple to set up to evaluate the performance of the ADPL42010A. For the evaluation board connections, do the following steps (see *Figure 1*):

1. Connect the load between the V_{OUT} and GND terminals.
2. With the input power supply off and turned down, connect the input supply to the V_{IN} and GND terminals. Ensure that the shunt of JP1 connects $\overline{SHDN}$ to V_{IN}. Also ensure that the shunt of JP2 allows the resistor divider to program the output as per the requirement of the user. The default connection of the shunt gives a 1.21V output voltage.
3. With the load turned down, turn the input power supply on and increase the voltage to 2.5V or higher.
4. Vary V_{IN} from 2.5V to 20V and the load current from 0A to 1A. Observe conservative power dissipation limits and note the following when setting V_{IN} and the load current:
   a. An input voltage that is too close to the programmed output voltage (too low) can cause dropout operation and a loss of output-voltage regulation.
   b. The amount of output current combined with an input voltage that is too high above the output can increase power dissipation to an unacceptable level.
5. Monitor regulation and dropout voltage at the V_{IN}, V_{OUT}, and GND test points.
6. To apply a $\overline{SHDN}$ signal externally, remove the shunt on JP1 and apply the $\overline{SHDN}$ signal to the $\overline{SHDN}$ test point.
7. If an output voltage other than 1.21V is required, change the JP2 connection according to the output voltage options that is programmed through the resistor divider.
8. A resistor can be installed in the component placeholder location on the USER SELECT resistor option in JP2, which enables the output voltage to be modified according to the required output needed by the user that is not included in the default values on the board.

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Evaluation Board Photo

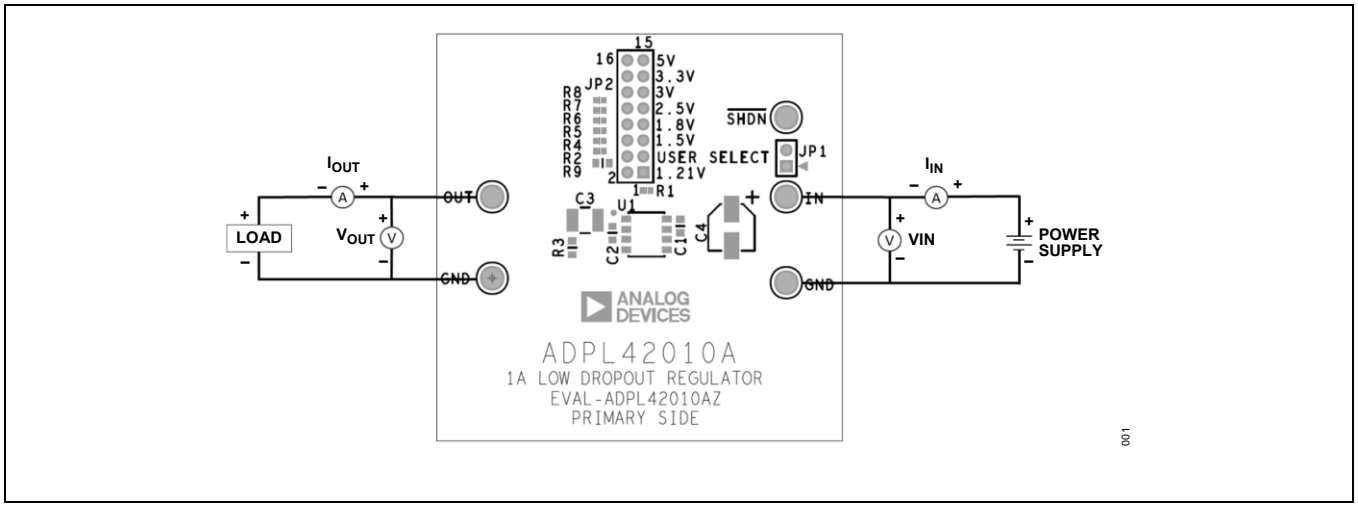


Figure 1. EVAL-ADPL42010AZ Board Connection

Table 1. Jumper Connection Guide

JUMPER	DEFAULT CONNECTION	FEATURE
JP1	Pin 1-2	Turns regulator on.
JP2	Pin 1-2	Connects the SENSE/ADJ pin to the output through a resistor divider.

Detailed Description of Hardware

Full specifications on the *ADPL42010A* are available in the ADPL42010A data sheet available from Analog Devices, Inc., and must be consulted with this user guide when using the EVAL-ADPL42010AZ evaluation board.

This EVAL-ADPL42010AZ evaluation board evaluates the ADPL42010A. The EVAL-ADPL42010AZ evaluation board uses the ADPL42010ABRCZ, the adjustable version of the ADPL42010A. The EVAL-ADPL42010AZ evaluation board operates over an input voltage range of 2.5V to 20V. The EVAL-ADPL42010AZ evaluation board's output voltage is set through JP2, which connects the SENSE/ADJ pin to the resistor divider that programs the output voltage to either 1.21V, 1.5V, 1.8V, 2.5V, 3V, 3.3V, or 5V. There is also a resistor placeholder for the USER SELECT configuration, which provides option to modify the output voltage that are not included in the default configuration of J2.

Table 2. Performance Summary

T_A = 25°C, V_{IN} = 2.5V, $V_{\overline{SHDN}}$ = 5V, I_{LOAD} = 1mA, V_{OUT} = 1.21V (JP2 set on Pins 1-2), unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.5		20	V
Output Voltage		1.192	1.210	1.228	V
Output Voltage (Note 1)	V_{IN} = 2.5V, JP2 on Pin 5-6	1.469	1.500	1.535	V
Output Voltage (Note 1)	V_{IN} = 2.8V, JP2 on Pin 7-8	1.759	1.803	1.856	V
Output Voltage (Note 1)	V_{IN} = 3.5V, JP2 on Pin 9-10	2.417	2.491	2.585	V
Output Voltage (Note 1)	V_{IN} = 4V, JP2 on Pin 11-12	2.890	2.995	3.130	V
Output Voltage (Note 1)	V_{IN} = 4.3V, JP2 on Pin 13-14	3.171	3.280	3.420	V
Output Voltage (Note 1)	V_{IN} = 6V, JP2 on Pin 15-16	4.810	5.020	5.190	V
Line Regulation	ΔV_{IN} = 2.5V to 20V		2	10	mV
Quiescent Current	ΔI_{LOAD} = 0mA		1	1.5	mA
Load Regulation	ΔI_{LOAD} = 1mA to 1A		0.2	1	%
$\overline{SHDN}$ Pin Threshold	On-to-Off	0.25	0.75		V
	Off-to-On, I_{LOAD} = 1mA		0.90	2	V
Output Voltage Noise	I_{LOAD} = 1A, BW = 10Hz to 100kHz		70		µVRMS

[1] *0utput voltage variations include ±1% tolerance of feedback divider network. For tighter voltage range, use lower tolerance resistors or use fixed voltage output devices.*

Printed Circuit Board (PCB) Layout

The printed circuit boards (PCBs) for this evaluation boards are 0.062inches thick and 2inches square. There are four copper layers, and the finishes copper thickness for the top and bottom layer is 2ounces. The input and output capacitors are placed near the ADPL42010A with their ground terminals connected to the lower half side of the board. The two middle layers and the bottom side of the PCB is a solid ground plane that connects to the ground on the top PCB layer by thermal vias under or near the ADPL42010A and at other points. Layout may significantly affect circuit electrical performance and reliability.

Ordering Information

MODEL[1, 2]	PACKAGE DESCRIPTION
EVAL- ADPL42010AZ	8-Lead SO Package Evaluation Board

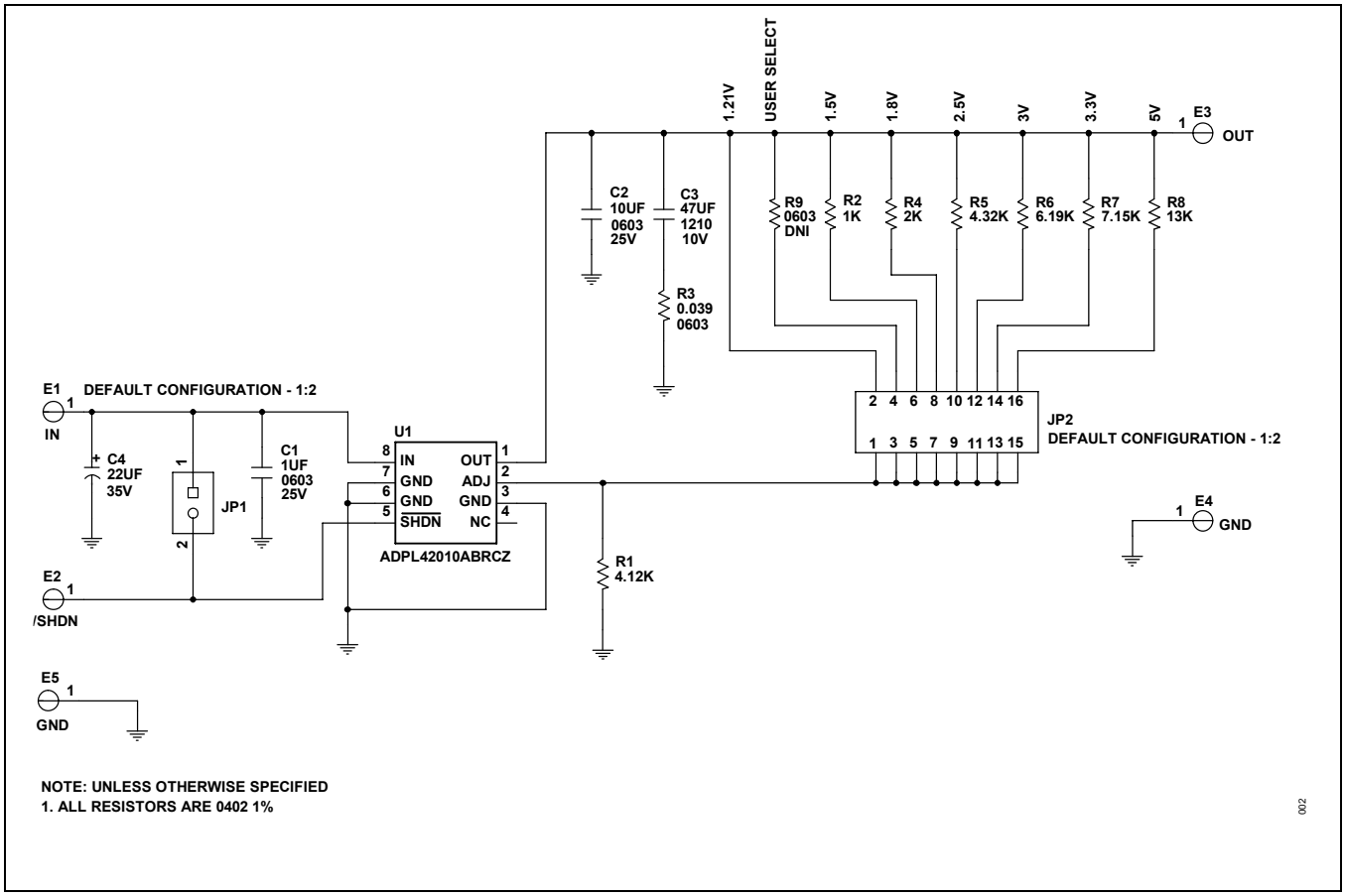
[1] *Z = RoHS Compliant Part.*

[2] *The evaluation boards are preconfigured with an adjustable ADPL42010A.*

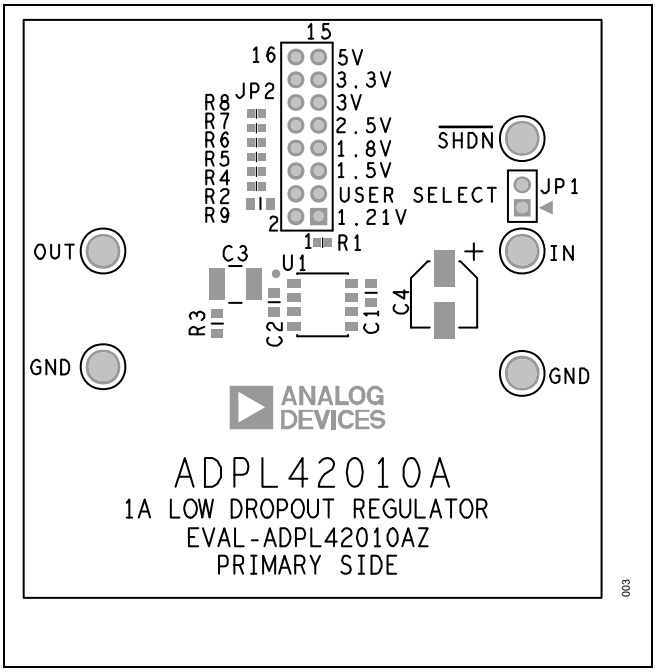
EVAL-ADPL42010AZ Bill of Materials

ITEM	QTY	REF_DES	DESCRIPTION	MANUFACTURER, PART NUMBER
Required Circuit Components				
1	1	C1	Capacitor, 1µF, 25V, 10%, X5R, 0603	Kyocera AVX, 06033D105KAT2A
2	1	C2	Capacitor, 10µF, 25V, 10%, X5R, 0603	Murata, GRM188R61E106KA73D
3	1	C3	Capacitor, 47µF,10V, 10%, X5R, 1210	Kyocera AVX, KGM32LR51A476KU
4	1	C4	Aluminum-electrolytic capacitor, 22µF, 35V, 20%	Kemet, EDK226M035A9DAA
5	1	R1	Resistor, 4.12kΩ, 1%, 1/16W, 0402	Venkel, CR0402-16W-4121FT
6	1	R2	Resistor, 1kΩ, 1%, 1/16W, 0402, AEC-Q200	Vishay, CRCW04021K00FKED
7	1	R3	Resistor, 0.039Ω, 1%, 1/3W, 0603, AEC-Q200	Panasonic, ERJ-3BWFR039V
8	1	R4	Resistor, 2kΩ, 1%, 1/16W, 0402	Bourns Inc., CR0402-FX-2001GLF
9	1	R5	Resistor, 4.32kΩ, 1%, 1/16W, 0402, AEC-Q200	Vishay, CRCW04024K32FK
10	1	R6	Resistor, 6.19kΩ, 1%, 1/16W, 0402, AEC-Q200	Vishay, CRCW04026K19FKED
11	1	R7	Resistor, 7.15kΩ, 1%, 1/16W, 0402	Vishay, CRCW04027K15FK
12	1	R8	Resistor, 13kΩ, 1%, 1/16W, 0402	Venekel, CR0402-16W-1302FT
13	1	U1	20V, 1A, fast transient response LDO regulator	Analog Devices, Inc., *ADPL42010ABRCZ*
Optional Evaluation Board Component				
1	1	R9	Resistor, 0603, optional	
Hardware				
1	5	E1,E2,E3,E4,E5	Test points, turrets, 0.094in	Mill-Max, 2501-2-00-80-00-00-07-0
2	1	JP1	Connector, header, male, through hole, 2-position, 0.079in	Sullins, NRPN021PAEN-RC
3	1	JP2	Connector, header, male, through hole, 16-position, 0.079in	Wurth Elektronik, 62001621121
4	2	XJP1, XJP2	2 (1 x 2) position, shunt connectors, 0.079in	Wurth Elektronik, 60800213421

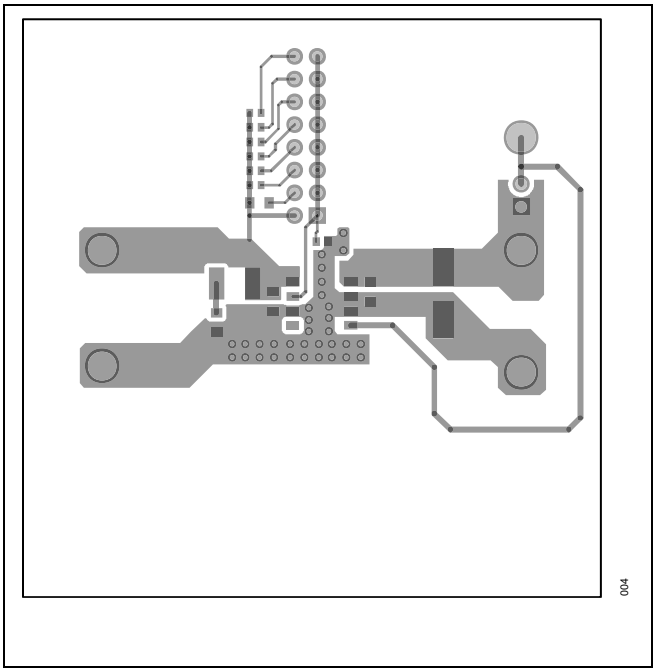
EVAL-ADPL42010AZ Schematic



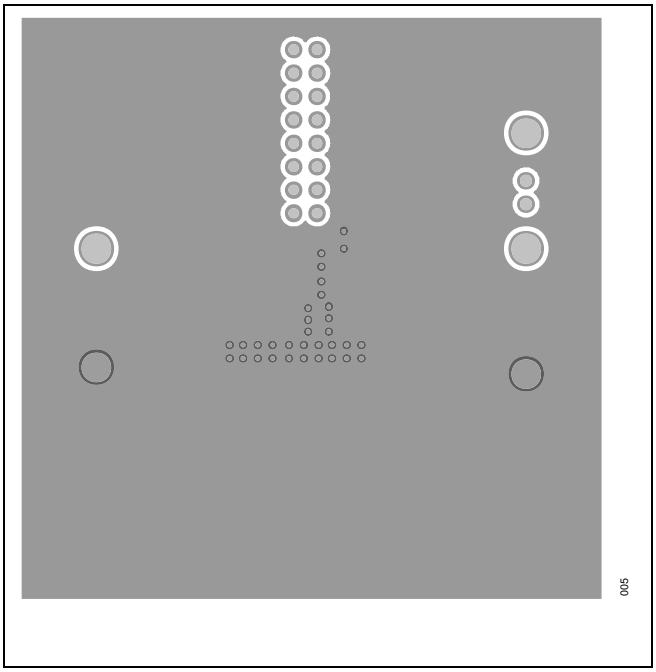
EVAL-ADPL42010AZ PCB Layout



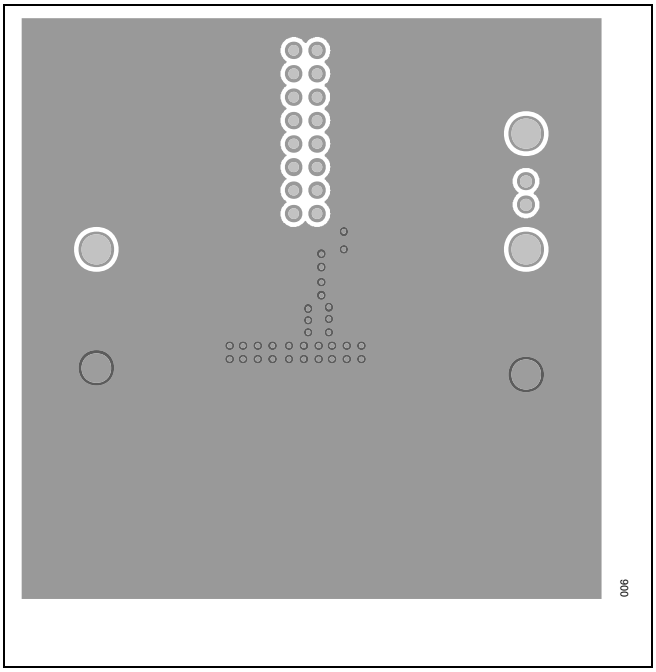
EVAL-ADPL42010AZ Component Placement Guide—Top Silkscreen



EVAL-ADPL42010AZ PCB Layout—Top Layer

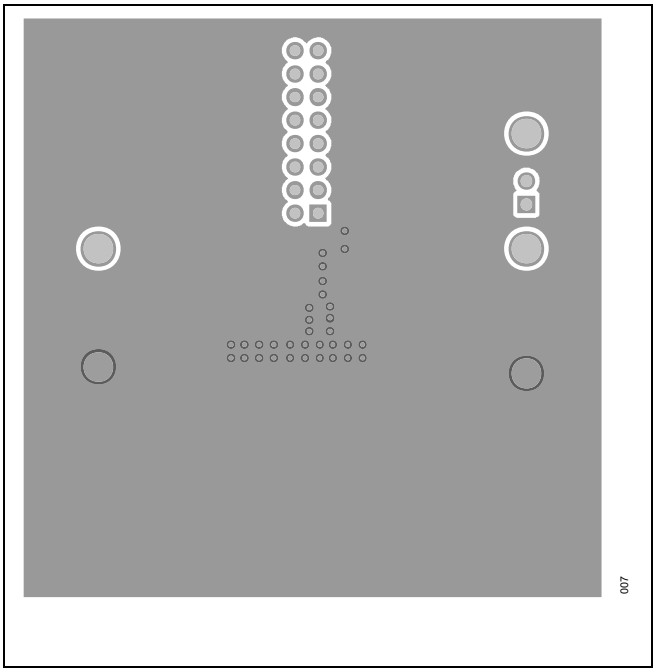


EVAL-ADPL42010AZ PCB Layout—Layer 2

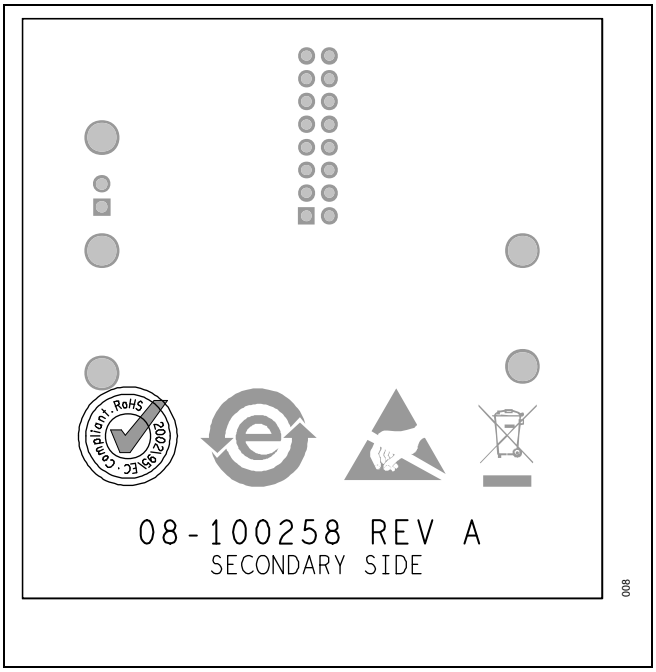


EVAL-ADPL42010AZ PCB Layout—Layer 3

EVAL-ADPL42010AZ PCB Layout (continued)



EVAL-ADPL42010AZ PCB Layout—Bottom Layer



EVAL-ADPL42010AZ Component Placement Guide—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/25	Initial release	—

Notes