

Evaluates: ADPL21504 in a 20V Output Voltage Application

General Description

The [EVAL-ADPL21504-AZ](#) evaluation board features the [ADPL21504](#), a micropower step-up DC/DC converter in a ThinSOT™ package.

The ADPL21504 is designed for higher power systems with a 350mA current limit. A current-limited, fixed off-time control scheme conserves operating current, resulting in high efficiency over a broad range of load current.

The ADPL21504's low off-time of 400ns permits the use of tiny, low-profile inductors and capacitors to minimize footprint and cost in space-conscious portable applications.

The EVAL-ADPL21504-AZ evaluation board features an application circuit with a 20V output voltage, operating within an input voltage range of 2.5V to 4.2V and a load current upto 20mA.

The ADPL21504 data sheet must be read in conjunction with this user guide to properly use or modify the evaluation board.

Features and Benefits

- $V_{OUT} = 20V$, V_{IN} Range = 2.5V to 4.2V, I_{OUT} = upto 20mA
- Resistor Programmable Output Voltage
- Features a Current-Limited, Fixed Off-Time control scheme
- Internal Compensation and Soft-Start
- Proven PCB Layout
- Fully Assembled and Tested

Quick Start

Required Equipment

- One 10V, 1A DC Power Supply
- Digital Multimeters (DMM)
- Load Resistors Capable of Sinking up to 20mA at 20V output

Procedure

The evaluation board is fully assembled and tested. Use the following steps to verify the board operation.

Note: Do not turn on the power supply until all connections are completed.

1. Ensure that the JP1 jumper is in the ON position.
2. Disable the power supply and set the input power supply at a voltage between 2.5V to 4.2V.
3. Connect the positive terminal of the power supply to the VIN PCB pad and the negative terminal to the nearest GND PCB pad.
4. Connect the positive terminal of the load to the VOUT pad and the negative terminal to the nearest GND PCB pad.

Caution: Do not enable the Load until the power supply is turned on.

5. Connect the DMM across the VOUT PCB pad and the nearest GND PCB pad.
6. Ensure that the JP1 jumper is in the ON position.
7. Turn on the input power supply.
8. Enable the load.
9. Verify that the DMM displays the expected terminal voltage with respect to GND.

[Ordering Information](#) appears at end of data sheet.

EVAL-ADPL21504-AZ Evaluation Board Configuration

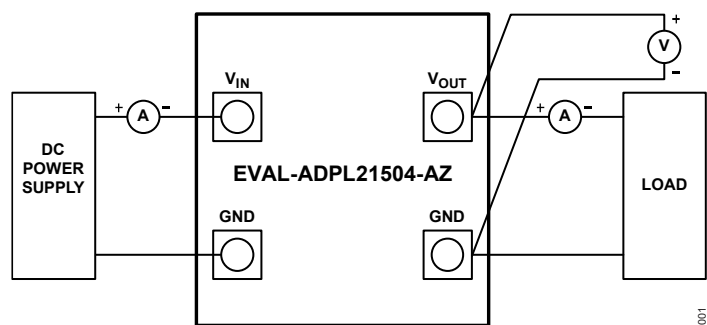


Figure 1. EVAL-ADPL21504-AZ Evaluation Board Connections

Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, all measurements are in reference to [EVAL-ADPL21504-AZ Evaluation Board Schematic Diagram](#), unless otherwise noted.

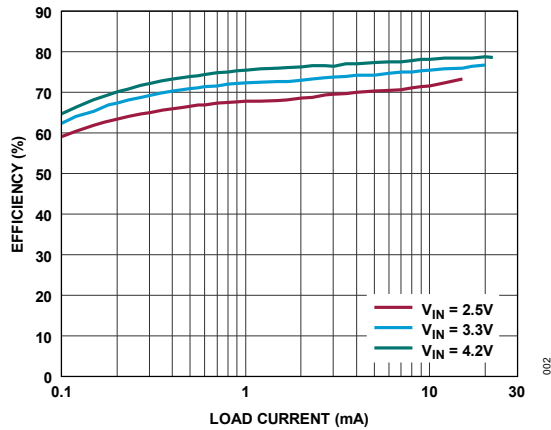


Figure 2. Efficiency vs. Output Current

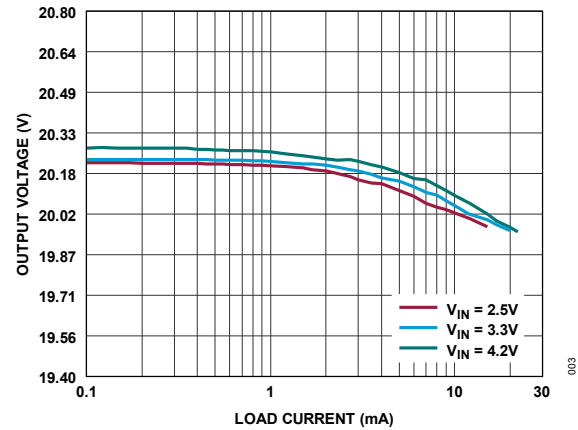


Figure 3. Output Voltage vs. Output Current

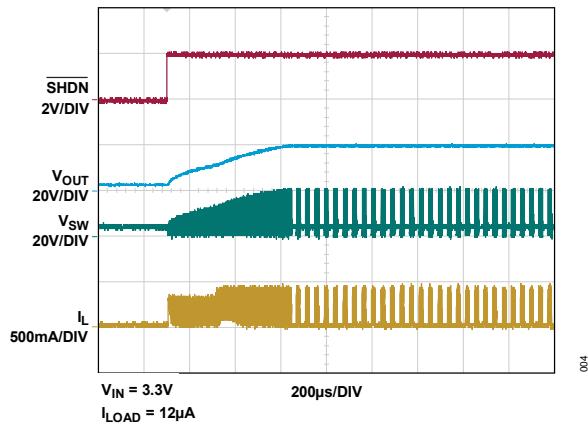


Figure 4. Start-up Waveform

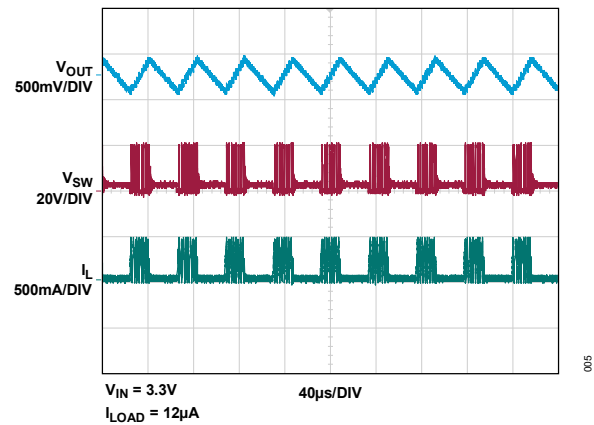


Figure 5. Steady-state Waveforms at Full Load

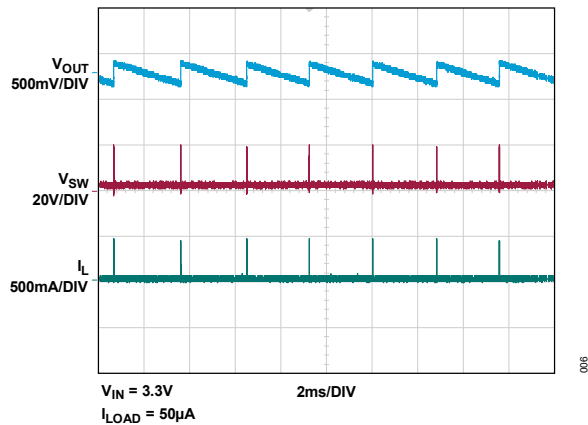


Figure 6. Steady-state Waveform at Light Load

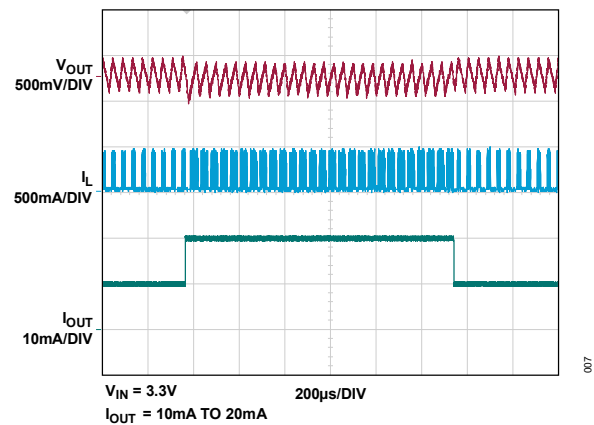


Figure 7. Transient Response 10mA to 20mA

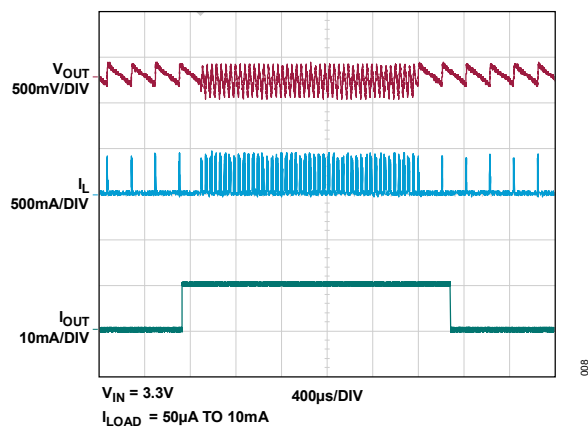


Figure 8. Transient Response Light Load to 10mA

Detailed Description

The EVAL-ADPL21504-AZ evaluation board is designed to demonstrate the salient features of ADPL21504, a micropower step-up DC/DC converter in a ThinSOT. The evaluation board is preset for 20V output from 2.5V to 4.2V input and can deliver load current up to 20mA.

SHDN Programming

The EVAL-ADPL21504-AZ evaluation board offers a jumper JP1 for the $\overline{\text{SHDN}}$ pin feature. When Jumper JP1 is connected across pins 2-3, the EVAL-ADPL21504-AZ is enabled. To disable, install the shunt across pins 1-2 on Jumper J1. See [Table 1](#) for Jumper settings.

Table 1. Jumper Connection Guide (JP1)

SHUNT POSITION	$\overline{\text{SHDN}}$ PIN	OUTPUT
1-2	Connected to the GND	OFF
2-3*	Connected to VIN	ON

*Default position.

Adjusting Output Voltage

The ADPL21504 supports an adjustable output voltage of up to 20V. EVAL-ADPL21504-AZ evaluation board is configured to 20V output. The output voltage is programmed using the resistor dividers R1 and R2. Refer to the [ADPL21504 data sheet](#) for more details.

Input Capacitor Selection

The input capacitor, C2, reduces current peaks drawn from the input power supply and reduces the switching frequency ripple at the input. Refer to the *Capacitor Selection* section in the [ADPL21504 data sheet](#) for more details. The input capacitor is chosen to be 4.7 μ F.

Output Capacitor Selection

The output capacitor C3 is chosen as 1 μ F/100V. Refer to the *Capacitor selection* section in the [ADPL21504 data sheet](#) for more details.

Diode Selection

The EVAL-ADPL21504-AZ evaluation board circuit uses a low-leakage rectifier diode to further minimize input current at light loads and no load. Refer to the *Diode Selection* section in the [ADPL21504 data sheet](#) for more details.

Hot Plug-In and Long input cables

The EVAL-ADPL21504-AZ evaluation board provides an electrolytic capacitor to dampen input voltage peaks and oscillations that can arise during hot-plug-in and/or due to long input cables. These capacitors limit the peak voltage at the input of the DC-DC converters when the evaluation board is powered directly from a precharged capacitive source or an industrial backplane Printed circuit board (PCB). Long input cables between an input power source and the evaluation board circuit can cause input voltage oscillations due to the inductance of the cables. The Equivalent series resistance (ESR) of the electrolytic capacitor helps damp out the oscillations caused by long input cables.

Ordering Information

PART	TYPE
EVAL-ADPL21504-AZ	Evaluation Board

Z = RoHS-compliant part.

Component Suppliers

SUPPLIER	WEBSITE
Murata Americas	www.murata.com
Coilcraft	www.coilcraft.com
Würth Elektronik	www.we-online.com
Panasonic	www.industrial.panasonic.com
Vishay	www.vishay.com
Onsemi	www.onsemi.com

Note: When contacting these component suppliers, indicate that the ADPL21504 is used.

EVAL-ADPL21504-AZ Evaluation Board Bill of Materials

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER, PART NUMBER
1	1	C1	CAP, ALUM 33 μ F 25V 20%	Panasonic, 25SVPK33M
1	1	C2	CAP CER, X7R 4.7 μ F 16V 10% 0805	Murata, GRM21BR71C475KE51L
2	1	C3	CAP CER X7R 1 μ F 100V 10% 1206	Murata, GRM31CR72A105KA01K
3	1	L1	IND, 10 μ H 20% 1.25A 0.51OHM DCR	Wurth Electronik, 74438335100
4	1	D1	Diode, Schottky 30V 0.5A	Onsemi, MBR0530T1G
5	1	R1	Res, 2Meg Ω 1% 1/16W 0402	Vishay, CRCW04022M00FKED
6	1	R2	Res, 130k Ω 1% 1/16W 0402	Vishay, CRCW0402130KFKED
7	5	J1-J5	Turret	MILL-MAX 2501-2
8	1	JP1	HEADER,3PIN	Sullins, PBC03SABN
9	1	U1	ADPL21504 IC	Analog Devices IC, ADPL21504IS5#TRPBF
10	1	C4	OPEN: Capacitor (0402)	—

EVAL-ADPL21504-AZ Evaluation Board Schematic Diagram

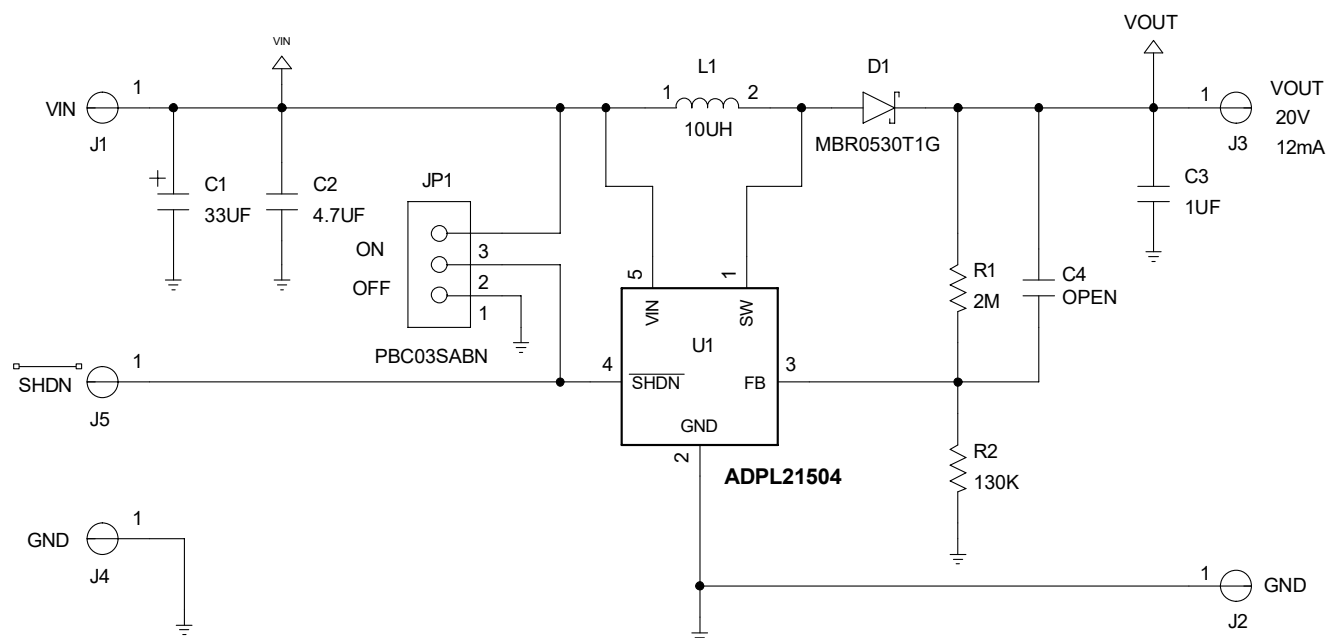


Figure 9. EVAL-ADPL21504-AZ Evaluation Board Schematic Diagram

EVAL-ADPL21504-AZ Evaluation Board PCB Layout Diagrams

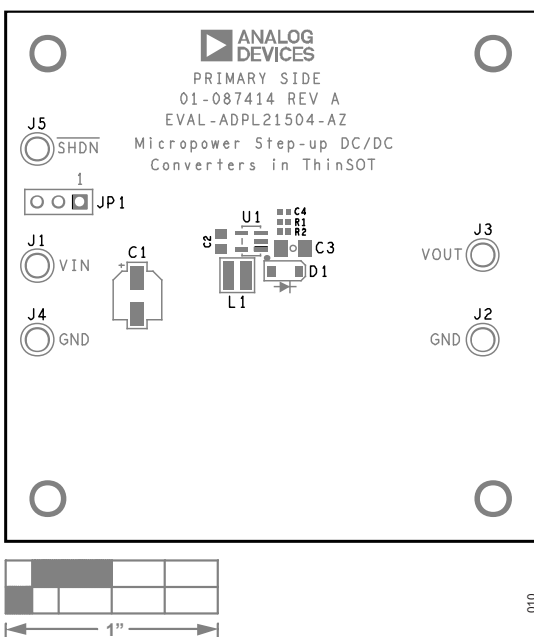


Figure 10. EVAL-ADPL21504-AZ Evaluation Board Component Placement Guide—Top Silkscreen

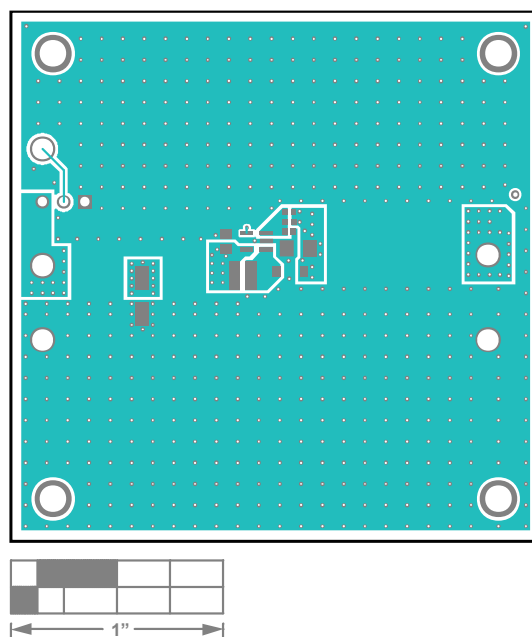


Figure 11. EVAL-ADPL21504-AZ Evaluation Board PCB Layout—Layer 1

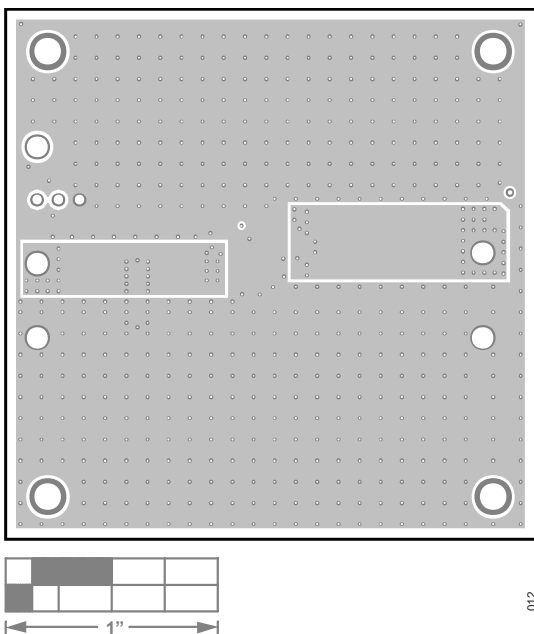


Figure 12. EVAL-ADPL21504-AZ Evaluation Board PCB Layout—Layer 2

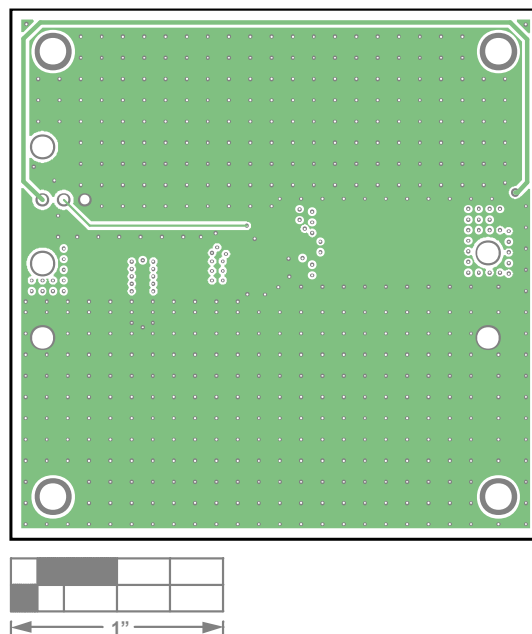


Figure 13. EVAL-ADPL21504-AZ Evaluation Board PCB Layout—Layer 3

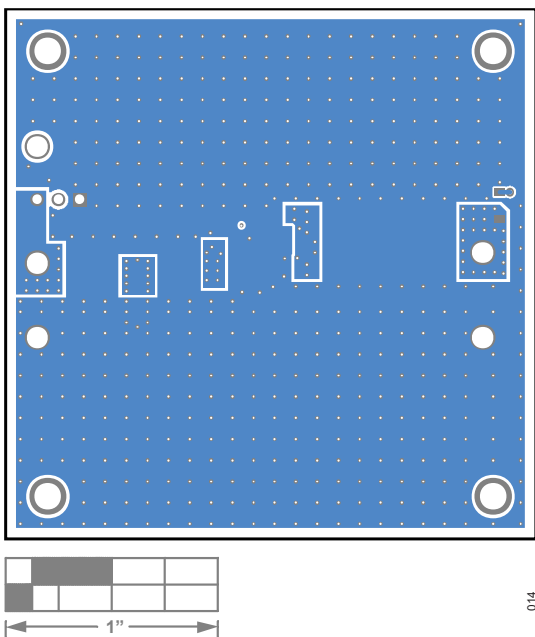


Figure 14. EVAL-ADPL21504-AZ Evaluation Board
PCB Layout—Layer 4

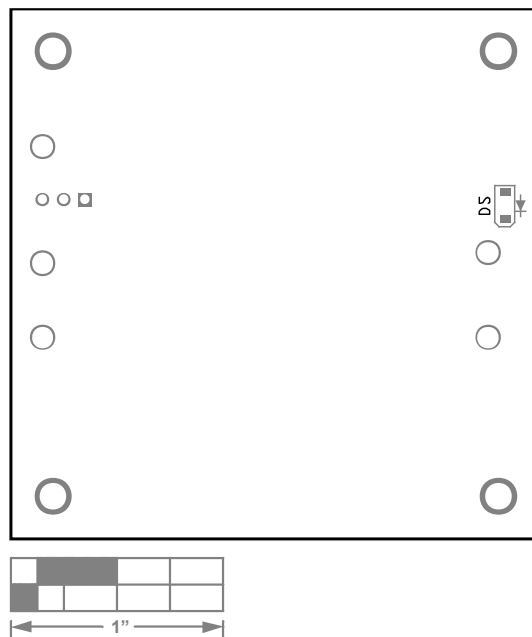


Figure 15. EVAL-ADPL21504-AZ Evaluation Board
Component Placement Guide—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	06/25	Initial release	—

Notes

ALL INFORMATION CONTAINED HEREIN IS PROVIDED “AS IS” WITHOUT REPRESENTATION OR WARRANTY. NO RESPONSIBILITY IS ASSUMED BY ANALOG DEVICES FOR ITS USE, NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THIRD PARTIES THAT MAY RESULT FROM ITS USE. SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. NO LICENSE, EITHER EXPRESSED OR IMPLIED, IS GRANTED UNDER ANY ADI PATENT RIGHT, COPYRIGHT, MASK WORK RIGHT, OR ANY OTHER ADI INTELLECTUAL PROPERTY RIGHT RELATING TO ANY COMBINATION, MACHINE, OR PROCESS, IN WHICH ADI PRODUCTS OR SERVICES ARE USED. TRADEMARKS AND REGISTERED TRADEMARKS ARE THE PROPERTY OF THEIR RESPECTIVE OWNERS. ALL ANALOG DEVICES PRODUCTS CONTAINED HEREIN ARE SUBJECT TO RELEASE AND AVAILABILITY.