Evaluating the ADPA1120 4.5W (36.5dBm), 8GHz to 12GHz, GaN Power Amplifier

FEATURES

- 2-layer Rogers 4350B evaluation board with heat spreader
- End launch 2.92mm jack RF connectors
- Through calibration path (depopulated)
- Drain or gate pulsing capability

EVALUATION KIT CONTENTS

- ADPA1120-EVALZ evaluation board
- 30V drain pulser board

EQUIPMENT NEEDED

- Pulse generator
- Oscilloscope, Keysight DSOX3034T or equivalent
- 32V, 1A power supply, Keysight E3634A or equivalent
- −4V power supply
- Keysight 1147B current probe or equivalent
- Keysight N2820A current probe or equivalent
- RF signal generator
- Directional coupler
- RF power sensor
- RF power meter
- RF attenuator
- Spectrum analyzer

DOCUMENTS NEEDED

- ADPA1120 data sheet

GENERAL DESCRIPTION

The ADPA1120-EVALZ consists of a 2-layer printed circuit board (PCB) fabricated from a 10mil thick, Rogers 4350B copper clad mounted to an aluminum heat spreader. The heat spreader assists in providing thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat spreader allow the spreader to be attached to a heatsink. Alternatively, the spreader can be clamped to a hot and cold plate. The RFIN and RFOUT ports on the ADPA1120-EVALZ are populated by 2.92mm (K) female coaxial connectors. The ADPA1120-EVALZ is populated with components suitable for use over the entire operating temperature range of the device. To calibrate board trace losses, a through calibration path is provided between the J5 and J6 connectors. J5 and J6 must be populated with 2.92mm (K) coaxial connectors to use the through calibration path.

Ground, power, and gate control are provided by two 24-pin headers (P3 and P4) on the ADPA1120-EVALZ. The pinouts for these two headers are shown in Table 1.

RF traces on the ADPA1120-EVALZ are 50Ω, grounded, coplanar waveguide. The package ground leads and the exposed paddle connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground paddle to provide adequate electrical conduction and thermal conduction to the heat spreader.

The ADPA1120-EVALZ ships with a drain pulser board that assists with control and application of a pulsed drain bias. The ADPA1120-EVALZ also ships with an extender board that can interconnect the pulser board and evaluation board, providing a cutout to allow drain-current monitoring with a current probe. The extender board also allows the ADPA1120-EVALZ to be inserted into an oven without having to insert the pulser board.

For full details on the ADPA1120, see the ADPA1120 data sheet, which must be consulted in conjunction with this user guide when using the ADPA1120-EVALZ.

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REVISION HISTORY

10/2025—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

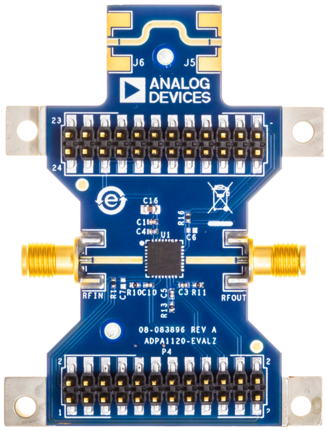

Figure 1. ADPA1120-EVALZ Evaluation Board, Primary Side

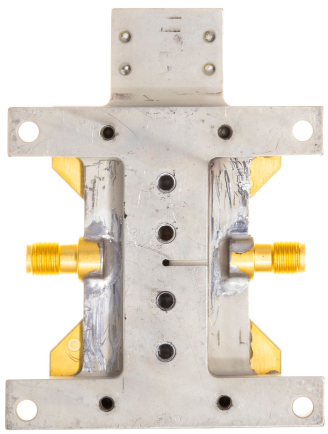

Figure 2. ADPA1120-EVALZ Evaluation Board, Secondary Side

Figure 3. Pulser Board, Primary Side

Figure 4. Pulser Board, Secondary Side

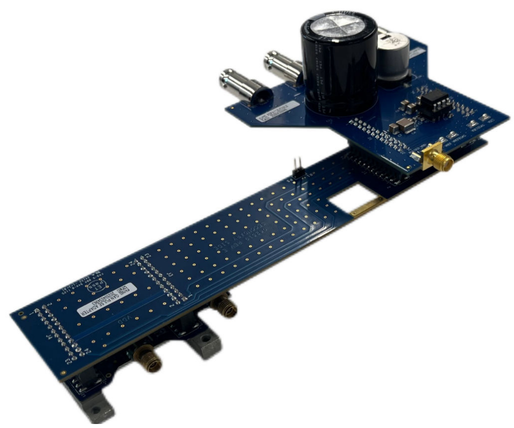

Figure 5. ADPA1120-EVALZ Evaluation Board with Extender Board and Pulser Board

HEADER PINOUT

The schematic for the ADPA1120-EVALZ is shown in Figure 10, and the ADPA1120-EVALZ contains two headers, P3 and P4, and Table 1 describes the pinout of these headers.

Table 1. P3 and P4 Header Connections on the ADPA1120-EVALZ

Header	Header Pin Number	Header Pin Name
P3	3, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 21, 22, 23, 24	GND
	16, 18, 20	VGG
	4, 6, 8	Not connected
	2	VDET_BIAS
	1	VDET
P4	1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 14, 15, 16, 17, 19, 21	GND
	6, 8, 10	Not connected
	18	VDD1_2
	20	VDD3
	22	VDD4
	23	VREF
	24	VREF_BIAS

INSERTION LOSS OF THE THROUGH CALIBRATION PATH

To calibrate board trace losses, a through calibration path is provided between the J5 and J6 connectors. J5 and J6 must be populated with 2.92mm, (K) RF connectors to use the through calibration path. Figure 6 shows the insertion loss, input return loss, and output return loss of the through calibration path. Table 2 lists the insertion loss of the through path vs. frequency.

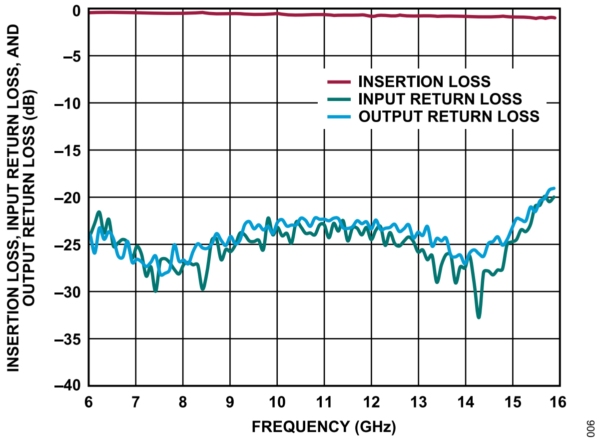

Figure 6. Insertion Loss, Input Return Loss, and Output Return Loss vs. Frequency of the Through Calibration Path

Table 2. Insertion Loss of Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
6	−0.4
7	−0.41
8	−0.49
9	−0.50
10	−0.55
11	−0.66
12	−0.71
13	−0.75
14	−0.84
15	−0.89
16	−0.97

OPERATING THE ADPA1120-EVALZ WITH THE DRAIN BIAS PULSER BOARD

The ADPA1120-EVALZ ships with a drain bias pulser board. A schematic of the pulser board is shown in Figure 7. The pulser board has two primary components. The IRFZ48NSTRLPBF is a 55V, 64A, metal-oxide semiconductor field effect transistor (MOSFET) that switches the drain voltage to the ADPA1120 on and off, and the MIC5021YN is a high-side, negative channel metal-oxide semiconductor (NMOS), static switch driver that controls the MOSFET.

The pulser board plugs into the P3 and P4 headers of ADPA1120-EVALZand can be configured to provide a pulsed drain voltage and a negative gate control voltage to control the biasing of the ADPA1120.

Table 3. Pulser Board Connections to the ADPA1120

Header	Header Pin Number	Header Pin Name
J1	Not applicable (BNC connector)	VDD
J2	Not applicable (BNC connector)	SENSE
J3	Not applicable (BNC connector)	VG1
J4	Not applicable (BNC connector)	PULSE
J5	Not applicable (Subminiature A (SMA) connector)	PULSED_VDD

Table 3. Pulser Board Connections to the ADPA1120 (Continued)

Header	Header Pin Number	Header Pin Name
VREFBIAS	Not applicable (surface-mount test point)	VREF_BIAS
VREF	Not applicable (surface-mount test point)	VREF
VDET	Not applicable (surface-mount test point)	VDET
VDETBIAS	Not applicable (surface-mount test point)	VDET_BIAS
P1	1	VDET
	2	VDETBIAS
	3, 5, 7, 9, 10, 11, 12, 13, 14, 15, 17, 19, 21, 22, 23, 24	GND
	4, 6, 8	PULSED_VDD
	16, 18, 20	VG1
P2	1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 14, 15, 16, 17, 19, 21	GND
	6, 8, 10	VG1
	18, 20, 22	PULSED_VDD
	23	VREF
	24	VREF_BIAS

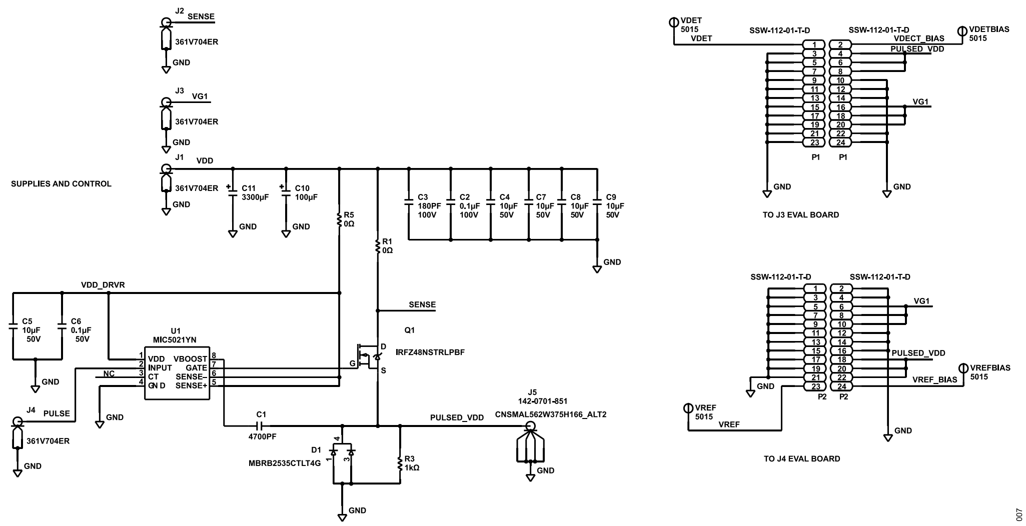

Figure 7. Analog Devices, Inc., Pulser Board Schematic

OPERATING THE ADPA1120-EVALZ WITH THE DRAIN BIAS PULSER BOARD

SETUP

The connections required to use the ADPA1120-EVALZ with the drain bias pulser board are shown in Figure 8. Before applying any bias or signals, plug the pulser board into the extender board and plug the extender board into the ADPA1120-EVALZ as shown in Figure 5. The P1 and P2 headers of the pulser board plug into the J2 and J1 headers of the extender board, and the J3 and J4 headers of the extender board plug into the P3 and P4 headers of the ADPA1120-EVALZ. The extender board is not strictly necessary but does serve the two following benefits:

- Contains a notched out section (the gold strip as shown in Figure 5) where a current clamp can be attached.
- Allows the ADPA1120-EVALZ to be inserted into a temperature chamber while the pulser board remains outside.

All external supply voltages and control signals are applied to the pulser board through the J1 through J4 connectors, which are listed in Table 3.

The gate control voltage applied to the J3 connector passes directly through the pulser board and drives the VGG1-2, VGG3 and VGG4 pins of the ADPA1120. Because the VDD and GND lines carry currents up to 1A, the use of heavy gauge, twisted pair wires is recommended to minimize voltage drops. To observe the pulsed drain voltage (PULSED_VDD) that drives the VDDx pins of the ADPA1120, connect an oscilloscope to the J5 coaxial connector on the pulser board.

Connect a pulse generator that can generate 0V to 5V pulses with a pulse width of 100μs and a duty cycle of 10% to the J4 connector.

To observe and measure the drain current and the RF output power of the ADPA1120, use a current probe and a pulsed RF power meter. If these methods are not available, make approximations as described in the Making Average to Pulsed Approximations section.

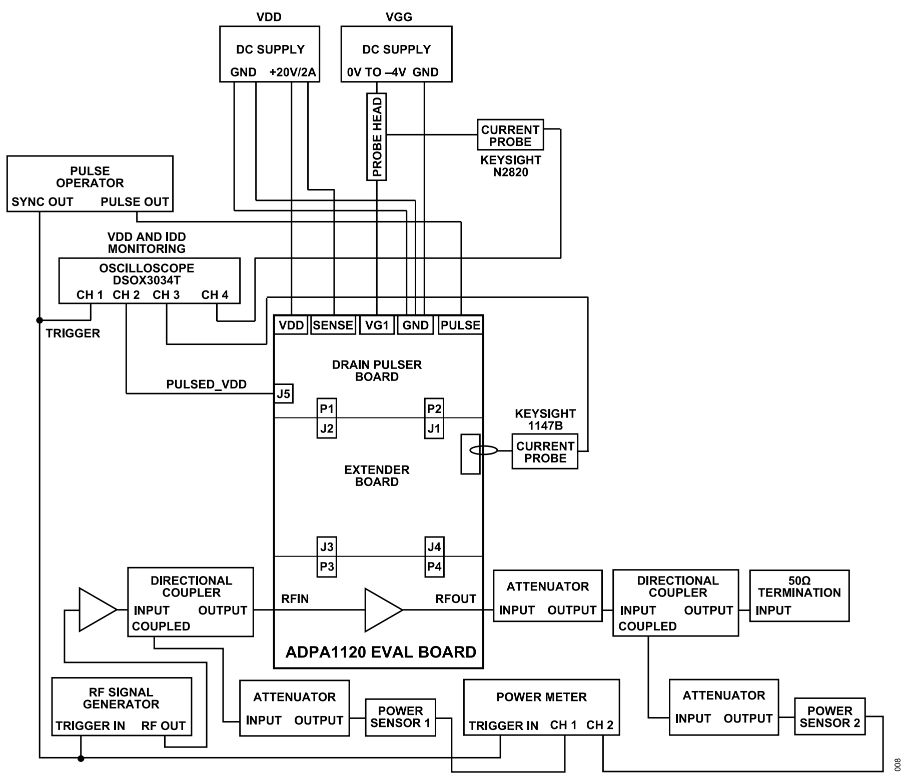

Figure 8. Drain Pulsing Setup

OPERATING THE ADPA1120-EVALZ WITH THE DRAIN BIAS PULSER BOARD

OPERATION

Take the following steps to power up (unless otherwise stated, all signals are applied to the pulser board):

1. Set the voltage on the J4 connector, PULSE, to 0V.
2. Set the voltage on the J3 connector, VG1, to −4V.
3. Set the voltage on the J1 connector, VDD, to 20V.
4. Turn on the J4 connector, PULSE (0V/5V, 100μs, 10% duty cycle).
5. Increase the voltage on the J3 connector, VG1, between −3V and −1V until the target pulsed quiescent current (I_{DQ}) is reached (nominally 50mA).
6. Apply the RF input signal to the RFIN connector of the ADPA1120-EVALZ. Trigger the RF source so that the RF is applied only during the time the drain pulse is high.

Take the following steps to power down:

1. Turn off the RF input signal.
2. Set the voltage on the J3 connector, VG1, to −4V.
3. Turn off the J4 connector, PULSE (set to 0V).
4. Set the voltage on the J1 connector, VDD, to 0V.
5. Set the voltage on the J3 connector, VG1, to 0V.

OPERATING THE ADPA1120-EVALZ WITH A PULSED GATE VOLTAGE

SETUP

The connections required to use the ADPA1120-EVALZ with the drain bias pulser board are shown in Figure 9. Before applying any bias or signals, plug the pulser board into the extender board and plug the extender board into the ADPA1120-EVALZ as shown in Figure 5. The P1 and P2 headers of the pulser board plug into the J2 and J1 headers of the extender board, and the J3 and J4 headers of the extender board plug into the P3 and P4 headers of the ADPA1120-EVALZ. The extender board is not strictly necessary but does serve the two following benefits:

- Contains a notched out section (the gold strip as shown in Figure 5) where a current clamp can be attached.
- Contains a header on the gate path for inserting a high-sensitivity current probe to measure gate current. Remove the 0 Ω resistor connected in parallel with the header to enable accurate measurement.
- Allows the ADPA1120-EVALZ to be inserted into a temperature chamber while the pulser board remains outside.

All external supply voltages and control signals are applied to the pulser board through the J1 through J4 connectors, which are listed in Table 3.

The gate control voltage applied to the J3 connector passes directly through the pulser board and drives the VGG1-2, VGG3 and VGG4 pins of the ADPA1120. Because the VDD and GND lines carry currents up to 1A, the use of heavy gauge, twisted pair wires is recommended to minimize voltage drops. To observe the pulsed drain voltage (PULSED_VDD) that drives the VDDx pins of the ADPA1120, connect an oscilloscope to the J5 coaxial connector on the pulser board.

Connect a pulse generator that can generate −4V to −1V pulses with a pulse width of 100µs and a duty cycle of 10% to the J4 connector. If the pulse generator has a 50Ω output impedance, C16 on the ADPA1120-EVALZ evaluation board must be removed. However, if the output impedance of the pulse generator is low impedance, C16 may remain installed.

To observe and measure the drain current and the RF output power of the ADPA1120, use a current probe and a pulsed RF power meter. If these methods are not available, make approximations as described in the Making Average to Pulsed Approximations section.

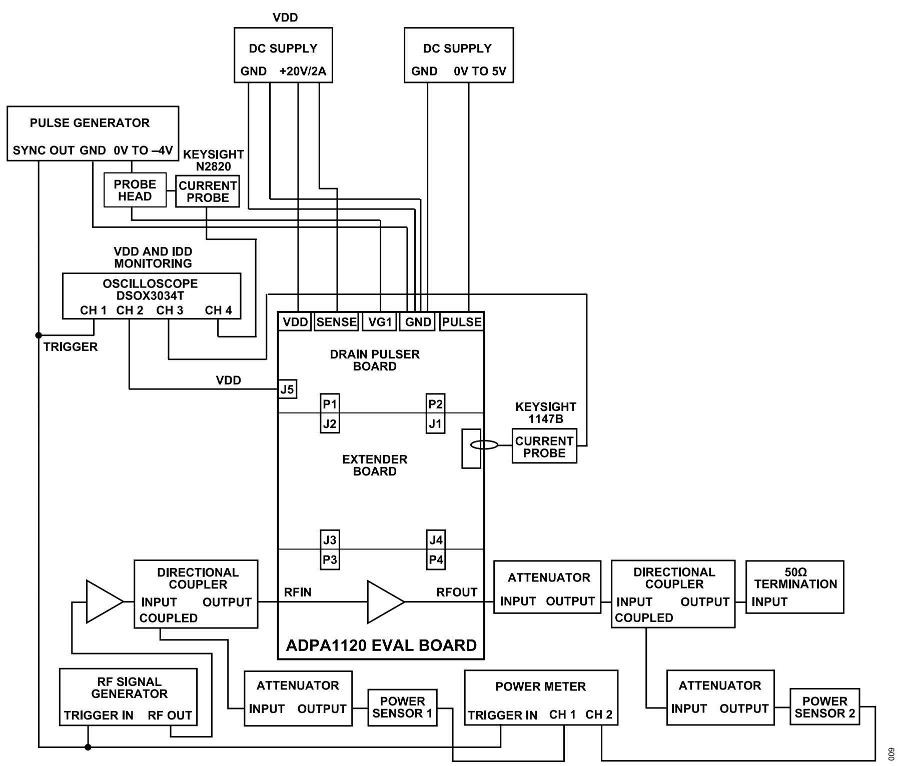

Figure 9. Gate Pulsing Setup

OPERATING THE ADPA1120-EVALZ WITH A PULSED GATE VOLTAGE

OPERATION

Take the following steps to power up:

1. Set the voltage on the J1 connector, VDD, to 0V.
2. Set the voltage on the J3 connector, VG1, to −4V.
3. Set VDD to 20V.
4. Turn on the gate voltage pulse (VG1 pulsing between −4V and approximately -3V, 100µs , 10% duty cycle).
5. Set the voltage on the J4 connector, PULSE, to 5V.
6. Fine tune the gate voltage pulse high voltage between −3V and −1V to achieve the desired pulsed I_{DQ} (nominally 50mA) while maintaining the pulse off voltage level at −4V.
7. Apply the RF input signal to the RFIN connector of the AD-PA1120-EVALZ. Trigger the RF source so that the RF is applied only during the time the gate pulse is high.

Take the following steps to power down:

1. Turn off the RF signal.
2. Turn off the pulse to VGG (VGG = −4V).
3. Set VDD to 0 V.
4. Increase the pulse to VGG to 0V.

MAKING AVERAGE TO PULSED APPROXIMATIONS

Instruments that can be triggered are required to measure the RF power, drain current, and power added efficiency (PAE) accurately under pulsed operation. When such instrumentation is not available, use averaging and approximations. The most common approximations involve measuring the average values and then adjusting those values to account for the duty cycle. These approximations can result in errors because of limited measurement bandwidths of instruments and/or the inclusion of on and off transients and/or partial periods in the measurement.

To ensure that partial periods do not contribute significant errors to the measurements, perform averaging over a large number of pulse periods. The results of such approximations can vary with the instruments and settings used. Therefore, experimentation can be necessary to achieve credible and repeatable results. When it is not possible to make pulse triggered measurements, the only pulse connection required is the connection from the pulse generator to the J4 connector of the pulser (see Figure 8).

EVALUATION BOARD SCHEMATIC AND ARTWORK

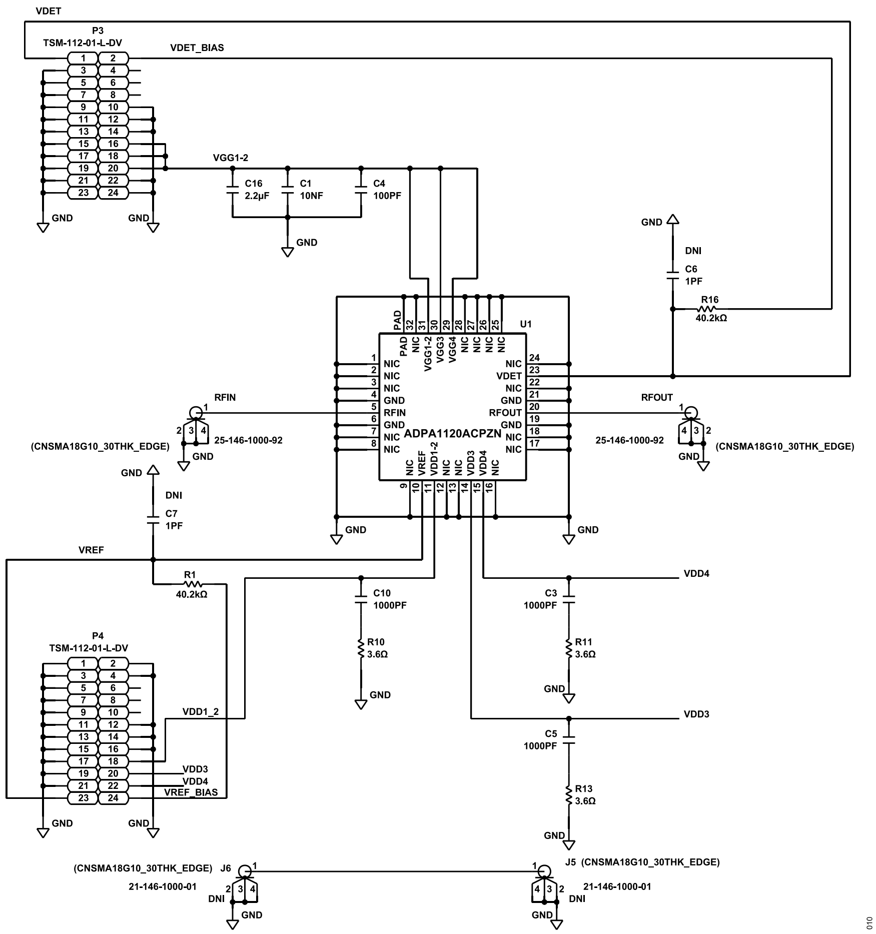

Figure 10. ADPA1120-EVALZ Schematic

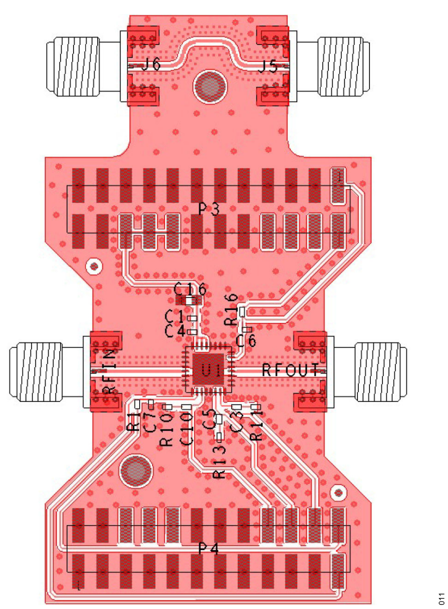

Figure 11. ADPA1120-EVALZ Assembly Drawing (J5 and J6 Not Installed)

ORDERING INFORMATION

EVALUATION BOARDS

Table 4. Evaluation Boards

Models[1]	Description
ADPA1120-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

BILL OF MATERIALS

Table 5. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C1	10nF ceramic capacitors, 16V, 5%, X7R, 0402	AVX Corporation	0402YC103JAT2A
C3, C5, C10	1000pF ceramic capacitors, 50V, 5%, X7R, 0402	KEMET Corporation	C0402C102J5RACAUTO
C16	2.2µF ceramic capacitors, 16V, 10%, X7S, 0603, low ESR	TDK	GA3E1X7S1C225K080AC
C4	100pF ceramic capacitor, 50V, 5%, C0G, 0402	TDK	C1005NP01H101J050BA
C6, C7	1pF ceramic capacitors, 25V, ±0.1pF, C0G, 0402 (not installed)	AVX Corporation	04023A1R0BAT2A
J5, J6	2.92mm (K) RF connectors, jack, EDGE_LAUNCH (not installed)	Winchester Interconnect	25-146-1000-92
P3, P4	Printed circuit board (PCB) connector, surface-mount, 24-position, male header, unshrouded double row ST, 2.54mm pitch	Samtec, Inc.	TSM-112-01-L-DV
RFIN, RFOUT	K connectors, jack, EDGE_LAUNCH	Winchester Interconnect	25-146-1000-92
R1, R16	40.2kΩ, surface-mounted device (SMD) resistors, 1%, 1/16W, 0402	Panasonic	ERJ-2RKF4022X
R10, R11, R13	3.6Ω SMD resistors, 5%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-U02J3R6X
U1	4.5W (36.5dBm), 8GHz to 12GHz, gallium nitride (GaN) power amplifier	Analog Devices	ADPA1120AEHZ
Not Applicable	Aluminum heatsink, 2.51in × 1.91in	Not applicable	Not applicable

ORDERING INFORMATION

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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