General Description

This user guide describes the various controls and indicators of the ADP1055 Evaluation Software. It gives the details of what each button on the GUI does in terms of the register that is being updated, along with a brief description.
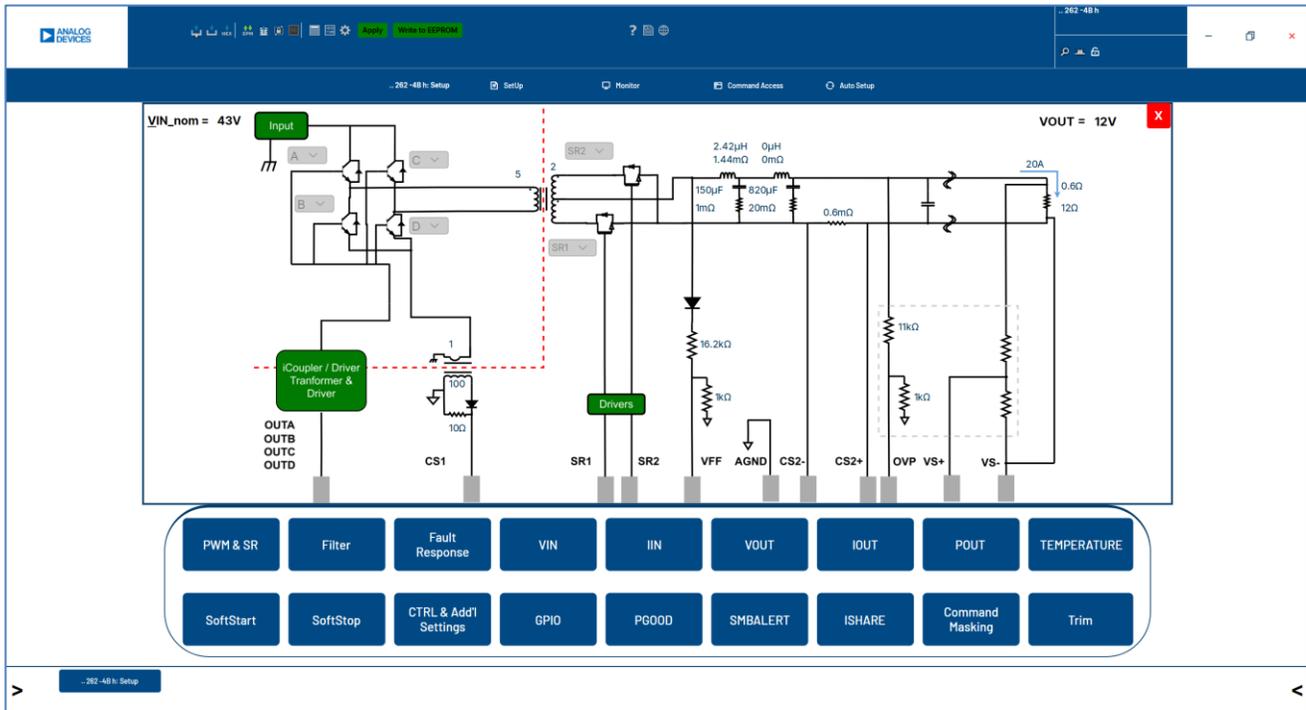

Figure 1. Main GUI Interface Window

TECHNICAL SUPPORT

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GUI Controls

Link

Figure 2. Link and Quick Action Tools

Table 1.   Figure 2 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	"USB to I2C interface" Number				This number shows the last three digits of the "USB to I2C interface" connected to ADP1055. This number is also physically printed on the "USB to I2C Interface".
2	ADP ADP1055 Address				This number shows the address of ADP1055 the GUI is connected to.
3	Scan				The GUI scans for all the ADP1055 connected to the computer. This helps in connecting and disconnecting devices once the GUI is already running.
4	Spy				This control opens the Spy window, which shows the I2C communication.
5	Lock/Unlock Commands				This control locks or unlocks trim registers.

Structural Navigation

Figure 3. Structural Navigation Bar

Table 2.   Figure 3 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Device – Window Info				This indicator shows the device address and the window name of the window that is currently open.
2	Structural Navigation				If you have only one device connected to the GUI, then clicking on the buttons opens the respective windows. If you have multiple devices connected, then clicking on the buttons opens the window for the device currently selected in the "Link" section shown above in *Figure 2*.

Windows Navigation

Figure 4. Window Navigation Bar

Table 3.   Figure 4 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Arrows				The arrows move the tabs in the respective directions.
2	Tabs				The windows open show up in the tab, and clicking it opens the respective window.

Tools

Figure 5. Tools, Load and Save

Table 4.   Figure 5 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Load register and board settings				This control loads the contents of the register map and external components to the device selected in the "Link" section shown above in *Figure 2*, from ".55s" file.
2	Save register and board settings				This control saves the contents of the register map and external components to the device selected in the "Link" section shown above in *Figure 2*, from ".55s" file.
3	Save a Hex file containing register settings				This control generates and saves the contents of the register map to a Hex file.
4	EEPROM Access				This control opens EEPROM Access window that can be used to read and write to EEPROM pages.
5	Restore register and board settings from EEPROM				This control loads the contents of the register map and external components to the device selected in the "Link" section show above in *Figure 2*, from EEPROM.
6	Change Keycode				This control opens window to change the current keycode.
7	Blackbox Access				This control opens Blackbox Access Window that can used to access backbox data.
8	PMBus Calculator				This control opens PMBus calculator for PMBus conversions.

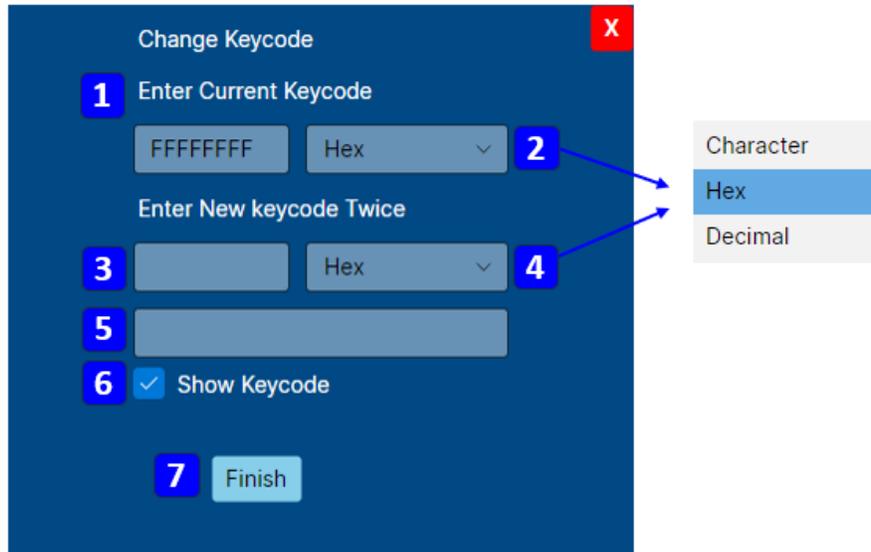| 9	CheckSum				Read back CheckSum from connected device, form indicated Register find and allows comparison.
10	GUI Settings				Enable/disable additional notification for actions that can change the entire configuration, e.g. loading new settings file, restoring default settings from EEPROM.
11	Apply				This control writes the settings of the GUI into the registers of the ADP1055. If the button is green then the GUI and ADP1055 register values are identical, if red then the current GUI values and ADP1055 register values do not match.
12	Update EEPROM				This control writes the contents of the registers to the EEPROM of ADP1055. If the button is green then the GUI and ADP1055 EEPROM values are identical, if red then the current GUI values and ADP1055 EEPROM values do not match, This button only operates when both the GUI and Register values match i.e. Apply is green.
13	GUI Reference Guide				Opens the GUI Reference Guide document
14	Datasheet				Opens the latest ADP1055 datasheet from Analog Devices website
15	ADP1055 Webpage				Opens the ADP1055 product page from Analog Devices website

Change Keycode

Figure 6. Keycode Change Form

Table 5. Figure 6 Callouts

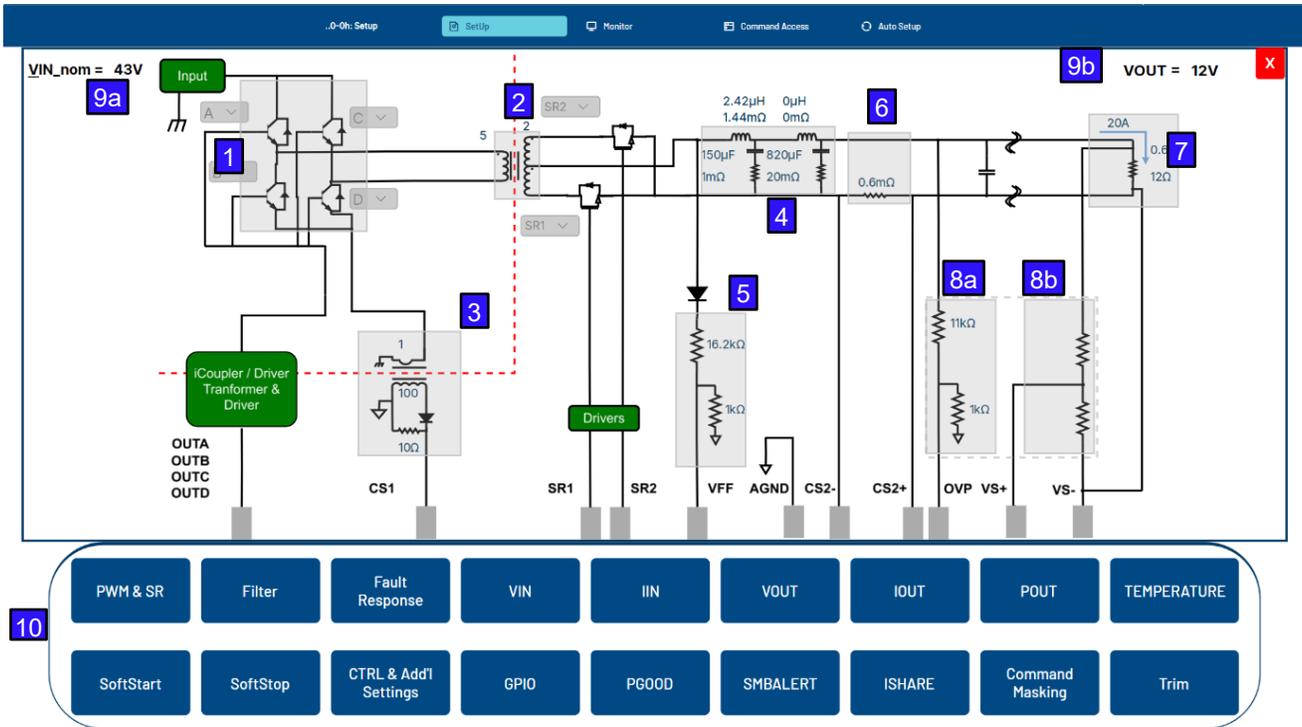| NO.	NAME	REG	BYTES	R/W	DESCRIPTION
1	Current key-code Field				Text field to enter the current user key-code.
2	Current key-code format				This is used to select the current key-code format. The options are character, hex, and decimal.
3	New key-code Fields				Text fields to enter new key-code twice.
4	New key-code format				This is used to select the new key-code format. The options are character, hex, and decimal.
5	Re-enter Key-code field				Text field for enter the user key-code.
6	Show key-code				If the checkbox is check, the key-code will be showed instead of asterisk.
7	Apply Settings	0xD7	4	BLKR/ BLKW	This sets the new key-code. To make the new key-code permanent registers contents must be saved to EEPROM.

Setup

Main

Figure 7. Board Settings

Table 6.   Figure 7 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Select Topology				PWM presets will be loaded based on the topology selected. Currently supported topologies are Full-Bridge, Half-Bridge and Phase-Shift Full-Bridge. Custom option can be selected to access to all the configurations. See PWM & SR Settings for more information.
2	Main Transformer				This sets the turns ratio of the power transformer.
3	CS Transformer				This sets the turns ratio of the primary Current Sense transformer and the termination resistance. Nominal input level is 1V. See IIN Settings for more information.
4	Output Filter				User enters output Capacitor and Inductor component related parameters for compensation calculation. See Filter Settings for more information.
5	VIN Divider				User enters VIN Sense resistor divider parameters. Nominal input level is 1V. See VIN Settings for more information.

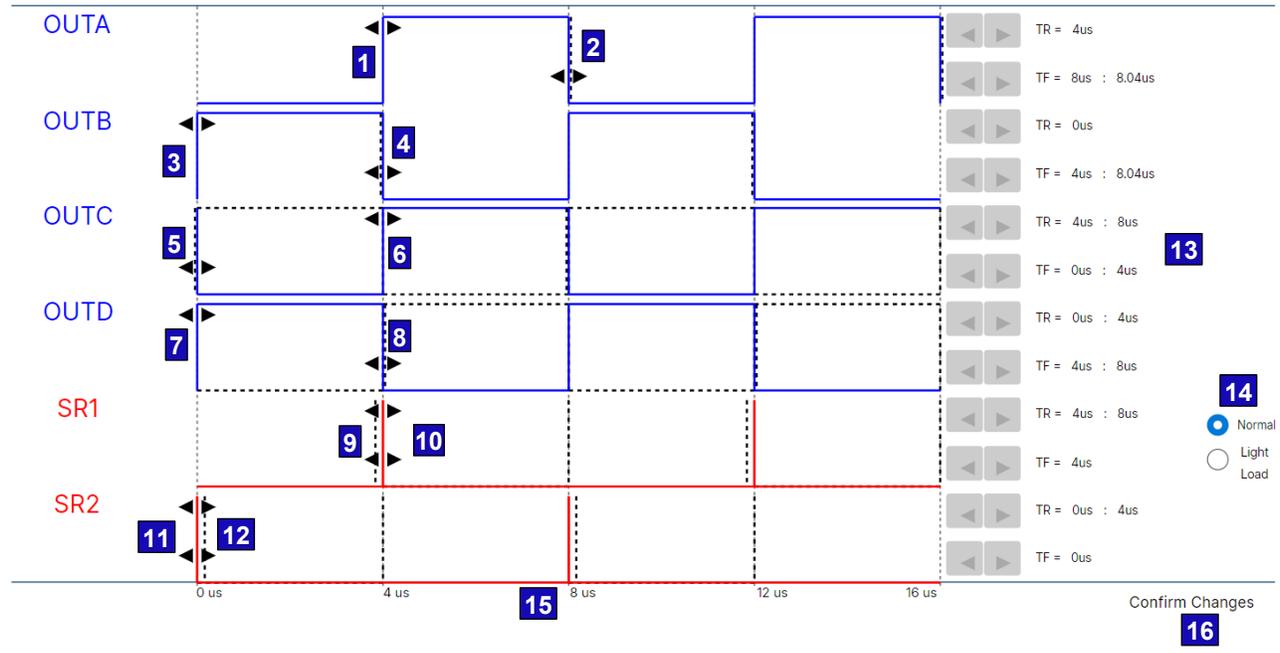| 6	Sense Location and Value	0xFE4F	[2]	R/W	This sets the location either high-side current sensing or low-side current sensing, and the sense resistor value for CS2. Low side sensing supports 30mV and 60mV ADC range while high side sensing supports 480mV. See IOUT Settings for more information.
7	Output Load				User enters output load current parameters. See IOUT/POUT Settings for more information.
8a	VOUT & OVP sensing				User enters resistor divider parameters which is applied to both VOUT and OVP pins. Nominal input level is 1V. See VOUT Settings for more information.
8b	VOUT sensing additional filters				User enters additional RC filters on VOUT sensing, if used in the circuit, for more accurate control loop modeling.

9a	Nominal Input Voltage info				This value represents the nominal input voltage of circuit design. This is equal to 1V on VFF pin reflected to primary side.
					$VIN\_nom = 1V*(1+R6/R7)*N1/N2*k,$
					    where R6,R7 are the resistor dividers,
					    N1/N2 is the transformer turns ratio, and
					    k is the scaling constant: k = 1 for Full-Bridge, Phase-Shift Full-Bridge, and Custom, and k = 2 for Half-Bridge.
					For example, in the default configuration of Full-Bridge topology with 5:2 transformer turns ratio and resistor dividers of 16.2kΩ & 1kΩ, $VIN\_nom = 1V*(1+16.2kΩ/1kΩ)*5/2*1 = 43V$

9b	VOUT info				This is the VOUT command value which represents the target output voltage. For optimum design, this should be close to the nominal output voltage equivalent to 1V on VS± pins. $Vout\_nom = 1V*(1+R1/R2),$ where R1,R2 are the resistor dividers on VS± and OVP pins. For example, $Vout\_nom = 1V*(1+11/1) = 12V$
10	ADP1055 Setup Blocks				The entire block represents ADP1055 and the blue tiles represent its various setup blocks. These blue tiles can be clicked to open the corresponding windows for settings.

PWM & SR Settings – Custom

Figure 8. PWM Window: Custom Topology

Table 7. Figure 8 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	OUTA Rising Edge Timing	0xFE0D	[15:4]	R/W	This sets OUTA Rising Edge timing.
2	OUTA Falling Edge Timing	0xFE0E	[15:4]	R/W	This sets OUTA Falling Edge timing.
3	OUTB Rising Edge Timing	0xFE0F	[15:4]	R/W	This sets OUTB Rising Edge timing.
4	OUTB Falling Edge Timing	0xFE10	[15:4]	R/W	This sets OUTB Falling Edge timing.
5	OUTC Rising Edge Timing	0xFE11	[15:4]	R/W	This sets OUTC Rising Edge timing.
6	OUTC Falling Edge Timing	0xFE12	[15:4]	R/W	This sets OUTC Falling Edge timing.
7	OUTD Rising Edge Timing	0xFE13	[15:4]	R/W	This sets OUTD Rising Edge timing.
8	OUTD Falling Edge Timing	0xFE14	[15:4]	R/W	This sets OUTD Falling Edge timing.
9	SR1/SR1 LLM Rising Edge Timing	0xFE15 0xFE19	[15:4] [15:4]	R/W R/W	This sets SR1 Rising Edge timing. This sets SR1 LLM Rising Edge timing.
10	SR1/SR1 LLM Falling Edge Timing	0xFE16 0xFE1A	[15:4] [15:4]	R/W R/W	This sets SR1 Falling Edge timing. This sets SR1 LLM Falling Edge timing.
11	SR2/SR2 LLM Rising Edge Timing	0xFE17 0xFE1B	[15:4] [15:4]	R/W R/W	This sets SR2 Rising Edge timing. This sets SR2 LLM Rising Edge timing.
12	SR2/SR2 LLM Falling Edge Timing	0xFE18 0xFE1C	[15:4] [15:4]	R/W R/W	This sets SR2 Falling Edge timing. This sets SR2 LLM Falling Edge timing.
13	Step Increment of Rising or Falling Edges				The arrows increment or decrement respective rising or falling edge by 5ns.

14	Normal or Light Load Mode for SR1 and SR2				The buttons toggles between Normal and Light Load Mode Settings for SR1 & SR2.
15	Timing Guides				Vertical lines every half switching period (Tsw/2) are provided to help user align PWM appropriately.
16	Confirm Changes				Save the changes of PWM settings to ADP1055. This button will turn red if any of the settings are changed. To update the PWM outputs after saving the settings, press the "Apply" button.

Note: Take special care in configuring the PWM edges to avoid shoot-through and cross-conduction on the target applications board.
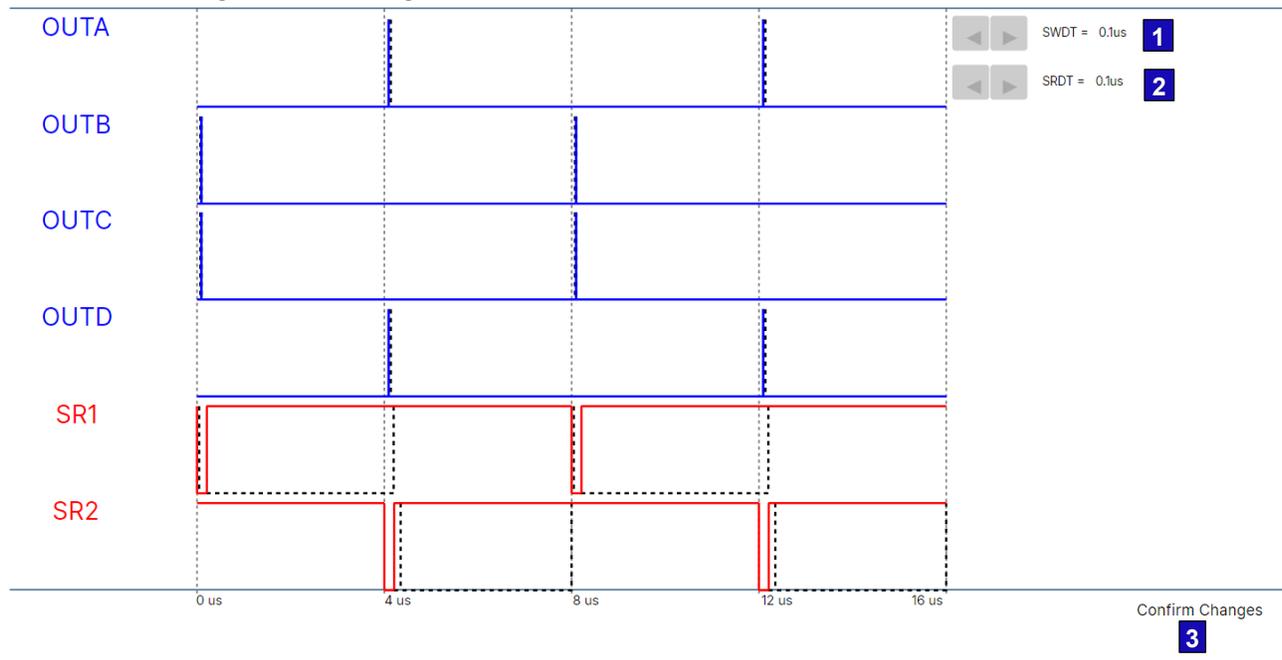
PWM & SR Settings – Full-Bridge

Figure 9. PWM Window: Full-Bridge Topology

Table 8. Figure 9 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	SWDT	0xFE0D to 0xFE1C	[15:4]	R/W	Switch Deadtime – delay applied to both rising and falling edges of the primary PWMs. The arrows increment or decrement the delay by 5ns. Click & hold the arrow key for continuous increment or decrement in value. Delay range is from 25ns to 1µs.
2	SRDT	0xFE0D to 0xFE1C	[15:4]	R/W	Sync Rect Deadtime – additional delay applied to rising edges of SR PWMs. The arrows increment or decrement the delay by 5ns. Click & hold the arrow key for continuous increment or decrement in value. Delay range is from 25ns to 1µs.
3	Confirm Changes				Save the changes of PWM settings to ADP1055. This button will turn red if any of the settings are changed. To update the PWM outputs after saving the settings, press the "Apply" button.

Note: Rising and Falling edges of PWMs are automatically calculated using SWDT and SRDT values. SR Light Load Mode is also automatically configured for forward conduction only.
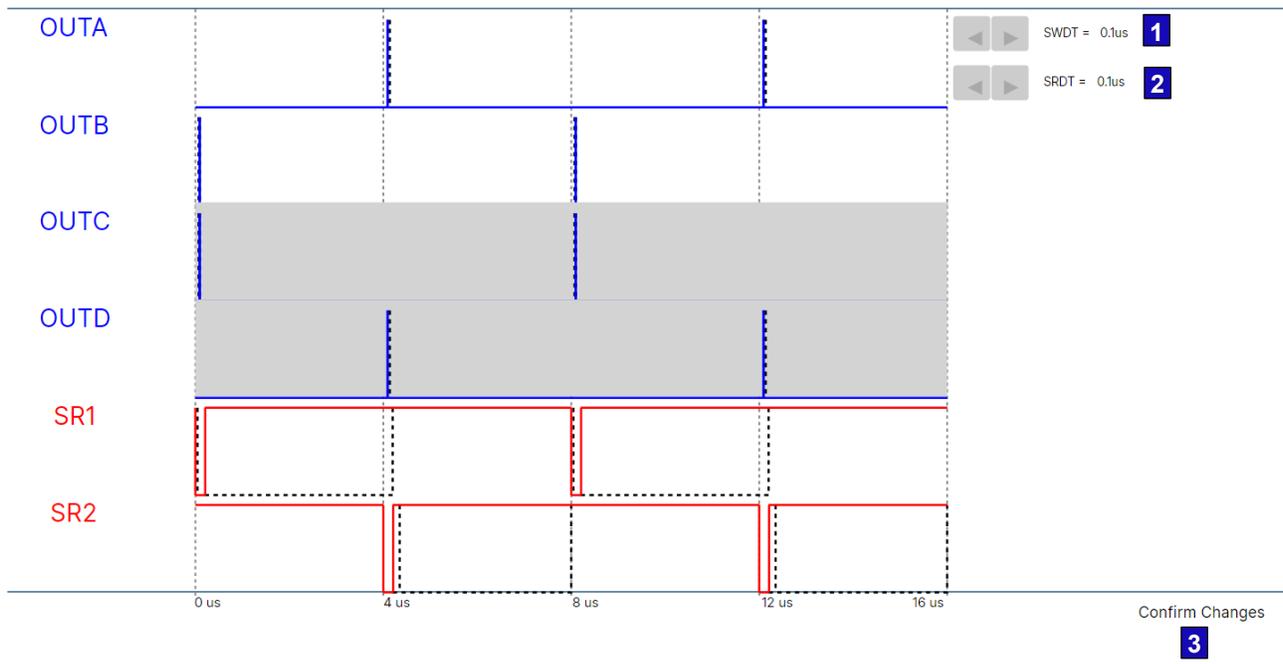
PWM & SR Settings – Half-Bridge

Figure 10. PWM Window: Half-Bridge Topology

Table 9.   Figure 10 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	SWDT	0xFE0D to 0xFE1C	[15:4]	R/W	Switch Deadtime – delay applied to both rising and falling edges of the primary PWMs. The arrows increment or decrement the delay by 5ns. Click & hold the arrow key for continuous increment or decrement in value. Delay range is from 25ns to 1µs.
2	SRDT	0xFE0D to 0xFE1C	[15:4]	R/W	Sync Rect Deadtime – additional delay applied to rising edges of SR PWMs. The arrows increment or decrement the delay by 5ns. Click & hold the arrow key for continuous increment or decrement in value. Delay range is from 25ns to 1µs.
3	Confirm Changes				Save the changes of PWM settings to ADP1055. This button will turn red if any of the settings are changed. To update the PWM outputs after saving the settings, press the "Apply" button.

Note: Rising and Falling edges of PWMs are automatically calculated using SWDT and SRDT values. SR Light Load Mode is also automatically configured for forward conduction only.

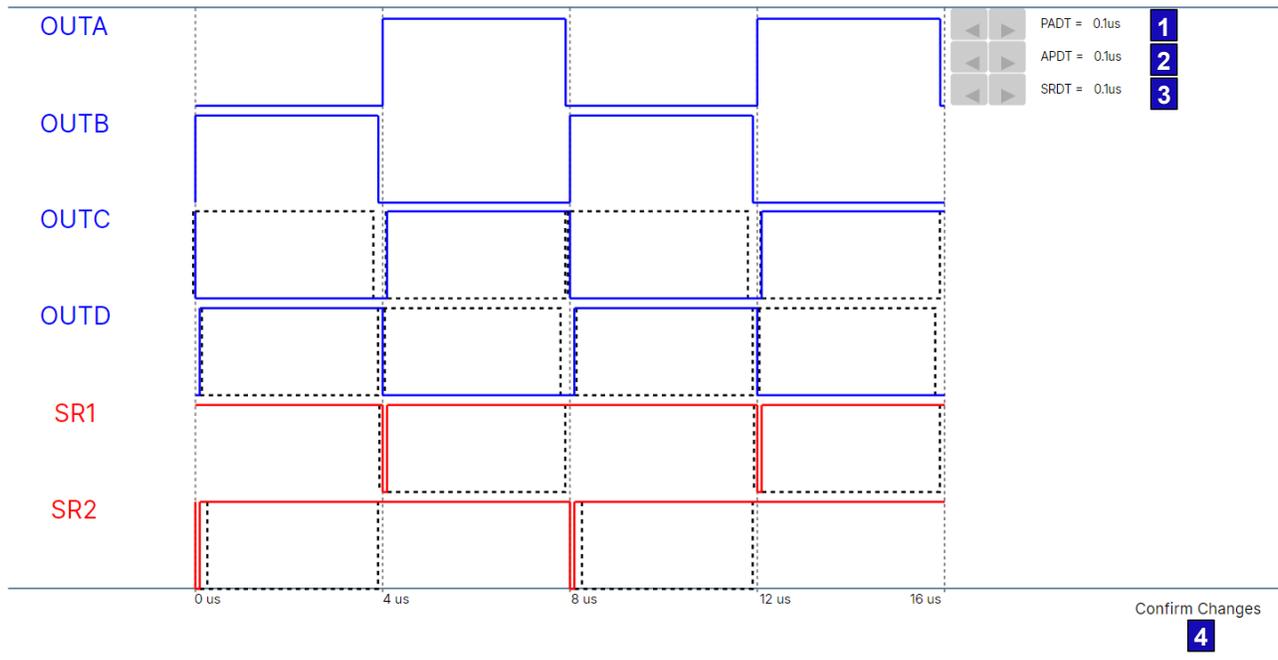## PWM & SR Settings – Phase-Shift Full-Bridge

Figure 11. PWM Window: Phase-Shift Full-Bridge

Table 10. Figure 11 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	PADT	0xFE0D to 0xFE1C	[15:4]	R/W	Passive to Active Deadtime – delay applied to falling edges of OUTA and OUTB PWMs. The arrows increment or decrement the delay by 5ns. Click & hold the arrow key for continuous increment or decrement in value. Delay range is from 25ns to 1µs.
2	APDT	0xFE0D to 0xFE1C	[15:4]	R/W	Active to Passive Deadtime – delay applied to rising edges of OUTC and OUTD PWMs. The arrows increment or decrement the delay by 5ns. Click & hold the arrow key for continuous increment or decrement in value. Delay range is from 25ns to 1µs.
3	SRDT	0xFE0D to 0xFE1C	[15:4]	R/W	Sync Rect Deadtime – additional delay applied to rising edges of SR PWMs. The arrows increment or decrement the delay by 5ns. Click & hold the arrow key for continuous increment or decrement in value. Delay range is from 25ns to 1µs.
4	Confirm Changes				Save the changes of PWM settings to ADP1055. This button will turn red if any of the settings are changed. To update the PWM outputs after saving the settings, press the "Apply" button.

Note: Rising and Falling edges of PWMs are automatically calculated using PADT, APDT and SRDT values. SR Light Load Mode is also automatically configured for forward conduction only.
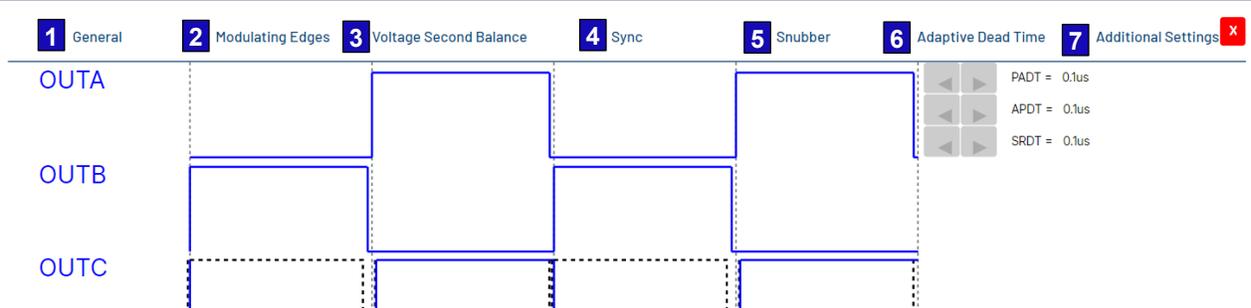
PWM and SR Settings – Other Settings

Figure 12. PWM Window – Other Settings

Table 11. Figure 12 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	General				User can change the switching frequency, modulation limit, pulse skipping and sync rect transitions.
2	Modulating Edges				User can define which edge is the PWM modulation is applied.
3	Voltage Second Balance				User can define volt-second balance to prevent flux walking in bridge topologies or ensure current balancing for interleaved topologies.
4	Sync				Synchronization settings
5	Snubber				User can configure GPIO3 and GPIO4 snubber PWM output for driving active clamp circuits.
6	Adaptive Dead Time				User can configure adaptive dead time for quasi-resonant topologies to optimize zero voltage switching (ZVS).
7	Additional Settings				User can copy PWM edges to make configuration faster.

Note: To open a sub-setting, click on the tab. Then click again to close it. To execute the changes, press Confirm Changes, then Apply. The Adaptive Dead Time sub-setting has its own dedicated close button at the upper right corner of the screen.
For pre-configured topology like Full-Bridge, Half-Bridge and Phase-Shift Full-Bridge, some of the settings are automatically configured and no longer editable by the user.
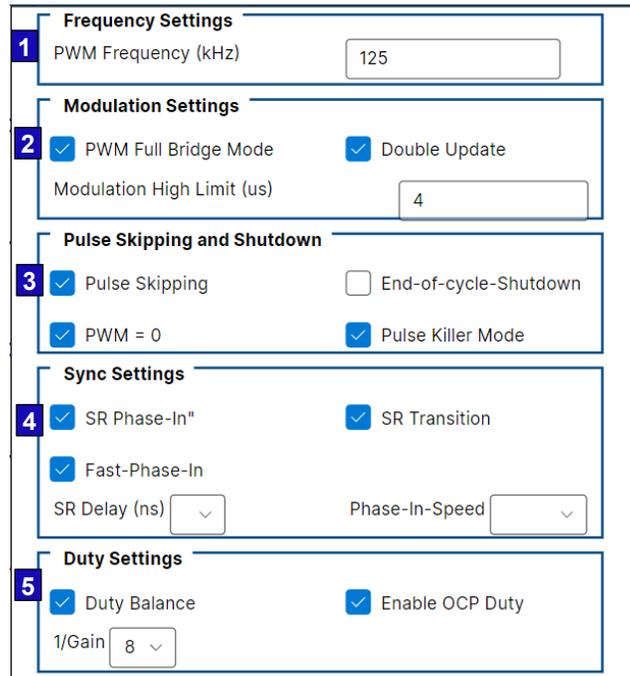
Figure 13. PWM General Settings

Table 12. Figure 13 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Frequency Settings: Exponent-N	0x33	[15:11]	R/W	This sets the PWM frequency. The user can type in the target frequency and list narrows down as digit is typed. The user can then select the closest value.
	Mantissa-Y	0x33	[10:0]	R/W	Register value is in linear data format $X = Y*2^N$
2	Modulation Settings: PWM Full Bridge Mode	0xFE53	[7:7]	R/W	This enables PWM Full Bridge Mode and affects the modulation limit.
	Modulation Limits	0xFE53	[6:0]	R/W	This sets the maximum modulation limits.
	Double Update	0XFE57	[0:0]	R/W	This enables a double update rate.
3	Pulse Skipping and Shutdown: Pulse Skipping	0xFE50	[1:1]	R/W	If set, pulse skipping will be enabled.
	End-of-cycle Shutdown	0xFE50	[3:3]	R/W	If set, all PWMs are disabled at end of switching cycle on a shutdown condition.
	PWM = 0	0xFE50	[0:0]	R/W	If set, all modulated edges are set to t = 0
	Pulse Killer Mode	0xFE50	[4:4]	R/W	If set, kills all PWM during pulse skip

4	Sync Settings: SR Phase-In	0xFE4C	[7:7]	R/W	This sets SR phase-in.
	SR Transition	0xFE50	[5:5]	R/W	If set enables SRs move from LLM to normal mode instantly. If unset, SR transitions from one mode to another at phase-in speed (recommended).
	Fast Phase In	0xFE4B	[0:0]	R/W	This sets fast phase in.
	SR Delay	0xFE52	[5:0]	R/W	This sets the SR driver delay in step of 5ns.
	Phase-In Speed	0xFE5F	[7:4]	R/W	This sets the phase-in speed.
5	Duty Settings: Duty Balance	0xFE57	[7:7]	R/W	This sets duty balance.
	Enable OCP Duty	0xFE57	[6:6]	R/W	This sets OCP duty equalization.
	1/Gain	0xFE57	[5:4]	R/W	This sets duty balance averaging time.

Note: For Full-Bridge, Half-Bridge and Phase-Shift Full-Bridge, only the PWM Frequency setting is available to edit, other settings are automatically configured.

Figure 14. PWM Modulation Settings

Table 13. Figure 14 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	OUTx and SRx Modulation Enable	0xFE0D to 0xFE18	[3]	R/W	Tick the box to enable the modulation on the rising and/or falling edges of each PWM signal.
2	OUTx and SRx Modulation Sign	0xFE0D to 0xFE18	[2]	R/W	Tick the appropriate box to define the polarity of the modulation either positive or negative for each PWM signal.

Note: For Full-Bridge, Half-Bridge and Phase-Shift Full-Bridge these settings are automatically configured.
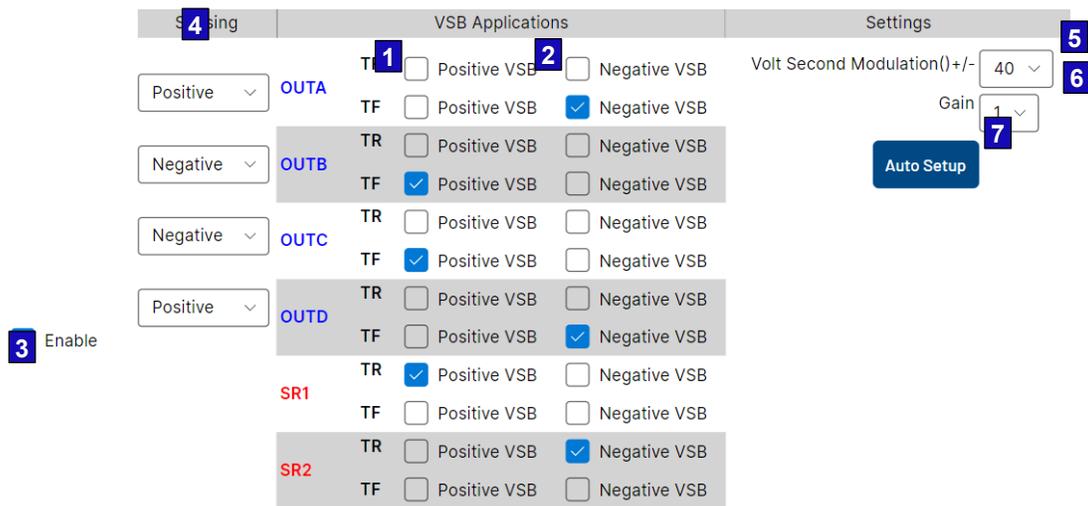

Figure 15. Voltage Second Balance Settings

Table 14. Figure 15 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	OUTx and SRx VSB Enable	0xFE26 to 0xFE28	[7,5,3,1]	R/W	Tick the box to enable voltage second balance on the rising and/or falling edges of each PWM signal.
2	OUTx and SRx VSB Polarity	0xFE26 to 0xFE28	[6,4,2,0]	R/W	Tick the appropriate box to define the polarity of the voltage second balance either positive or negative for each PWM signal.
3	VSB Enable/Disable	0xFE25	[6]	R/W	This enables or disables VSB settings.
4	Current Sensing Direction	0xFE56	[7:0]	R/W	This sets the current sensing direction for OUTA, OUTB, OUTC and OUTD.
5	VSB Modulation Limit	0xFE57	[2:1]	R/W	This sets the VSB modulation limit.
6	VSB Gain Setting	0xFE25	[1:0]	R/W	This sets the gain of the volt-second balance circuit.
7	VSB Auto-Setup				This automatically setup the VSB settings.

Note: For Full-Bridge, Half-Bridge and Phase-Shift Full-Bridge these settings are automatically configured.
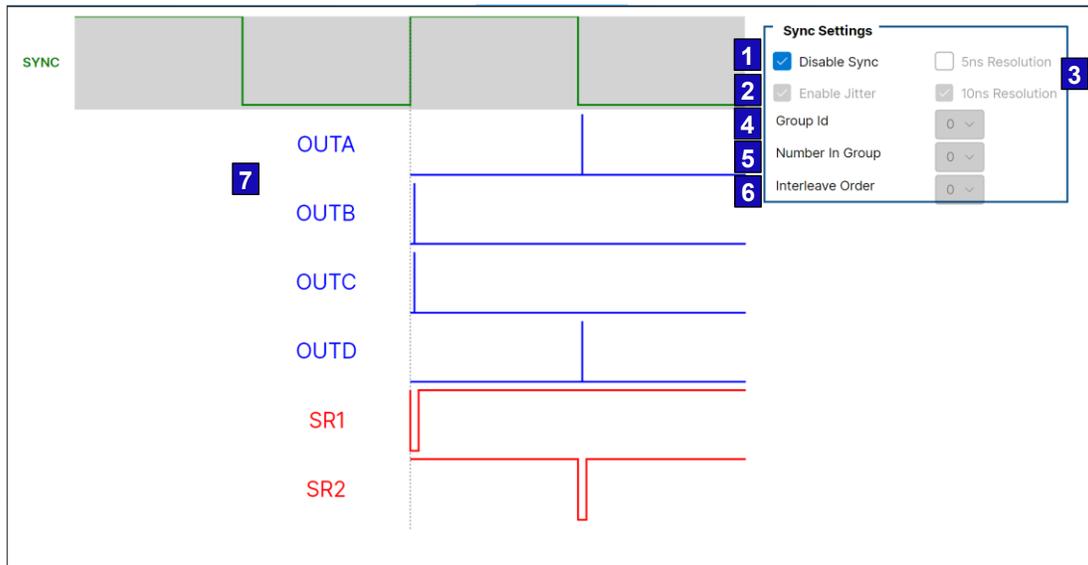
Figure 16. Sync Settings

Table 15. Figure 16 Callouts

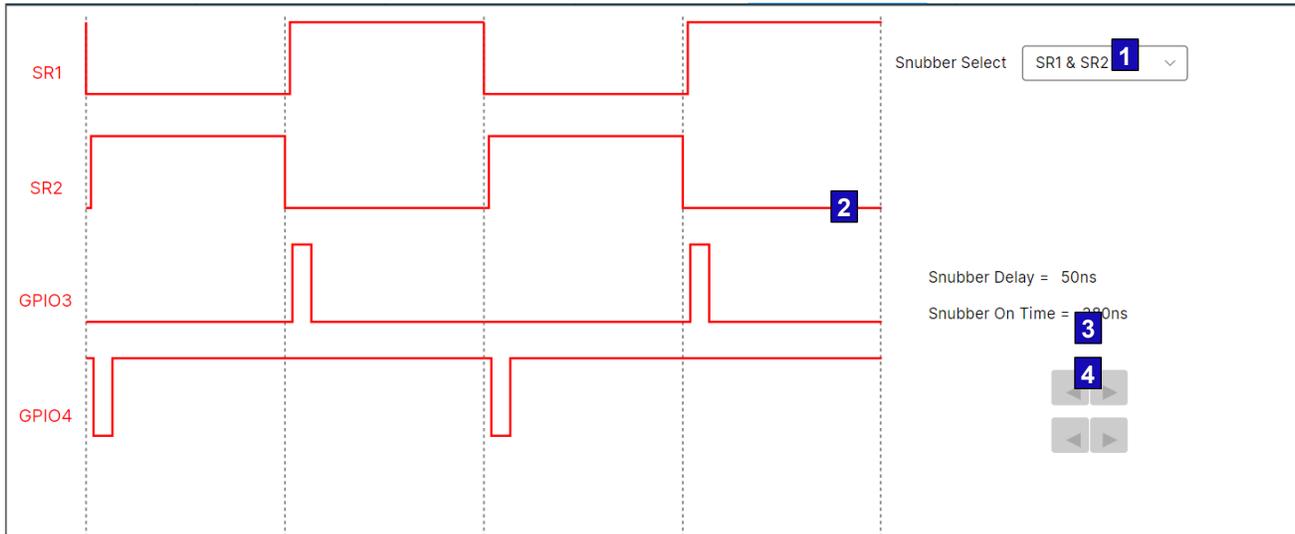| NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Sync Disable	0xFE55	[6:6]	R/W	This disables/enables SYNC function. If SYNC is disabled, other settings are greyed out.
2	Jitter Enable	0xFE55	[1:1]	R/W	This enables/disables jitter on clock to randomize frequency components.
3	Resolution Select	0xFE55	[0:0]	R/W	This toggles between the resolutions of Tsw.
4	Group ID	0x37	[11:8]	R/W	This sets the group ID number for interleave.
5	Number in Group	0x37	[7:4]	R/W	This sets the number of units in the group.
6	Interleave order	0x37	[3:0]	R/W	This sets the phase shift for the unit in 22.5° steps, e.g. 0 to 337.5°.
7	PWM Capture				This is a snapshot of the PWMs from the main window and the phase relationship to SYNC signal

Figure 17. Snubber Settings

Table 16. Figure 17 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Snubber Select	0xFE65	[7:7]	R/W	This selects the reference for snubber signal(s): either based on the falling edges of SR1 & SR2 or #OUTC & #OUTD
2	Snapshots of PWM				This is a snapshot of PWMs from the main PWM window. Note that OUTC & OUTD signals are inverted in this view. GPIO3 and GPIO4 can be configured for the snubber signals in the GPIO section.
3	Snubber Delay	0xFE64	[5:0]	R/W	This adds dead-time delay, in 5ns steps, between the fall of SR or OUTC/D and the rise of GPIO3/4. Click and hold buttons to increment/decrement faster.
4	Snubber On-Time	0xFE63	[7:0]	R/W	This sets the maximum on time, in 20ns steps, the GPIO3/4 until SRx goes high or OUTC/D goes low.

Figure 18. Additional Settings Edge Copy

Table 17. Figure 18 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Copy Edge				This selects the reference and the target PWM signal for the edge copy.
2	Copy Type				This defines the copy type: direct, inverter, 180° phase-shifted or inverted 180° phase-shifted.

Note: This setting is not available in Full-Bridge, Half-Bridge or Phase-Shift Full-Bridge topologies.

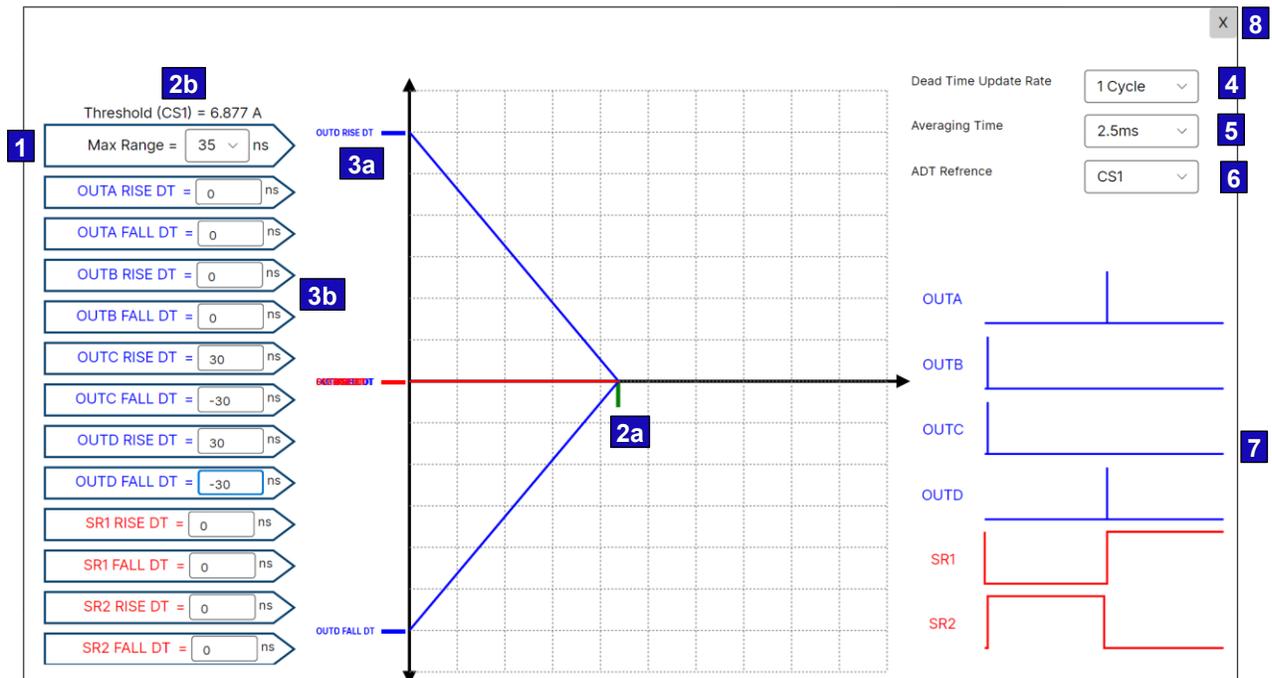### PWM & SR Settings – Adaptive Dead Time

Figure 19. Additive Dead Time

Table 18. Figure 19 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range	0xFE1D	[2:0]	R/W	This sets the maximum value for dead time adjustment: 35ns to 280ns.
2a 2b	Adaptive Dead Time Threshold	0xFE1E	[7:0]	R/W	This sets the Adaptive Deadtime current threshold. The vertical green bar [2a] can be dragged across x-axis to set the current level. Threshold value and source is displayed in [2b].
3a 3b	Individual PWM Edge Adaptive Dead Time Adjustment Settings	0xFE1F to 0xFE24	[7:0]	R/W	User can set adaptive dead time value to individual PWM edge in either positive or negative polarity up to the max range value. Input can be done by dragging the horizontal red or blue bars across y-axis [3a] or via direct value input [3a].
4	Dead Time Update Rate	0xFE1D	[5:3]	R/W	This sets the number of switching cycles before the ADT algorithm adjusts the deadtime in 5ns steps.
5	Averaging Time	0xFE1D	[7:7]	R/W	This sets the averaging period of the current measurement.
6	ADT Reference	0xFE1D	[6:6]	R/W	This sets the source either CS1 or CS2 for the current threshold.
7	PWM Snapshot				This shows the snapshot of PWM configuration.
8	Close Button				Close the Adaptive Dead Time window.

Filter Settings

Figure 20. Filter Window

Table 19. Figure 20 Callouts

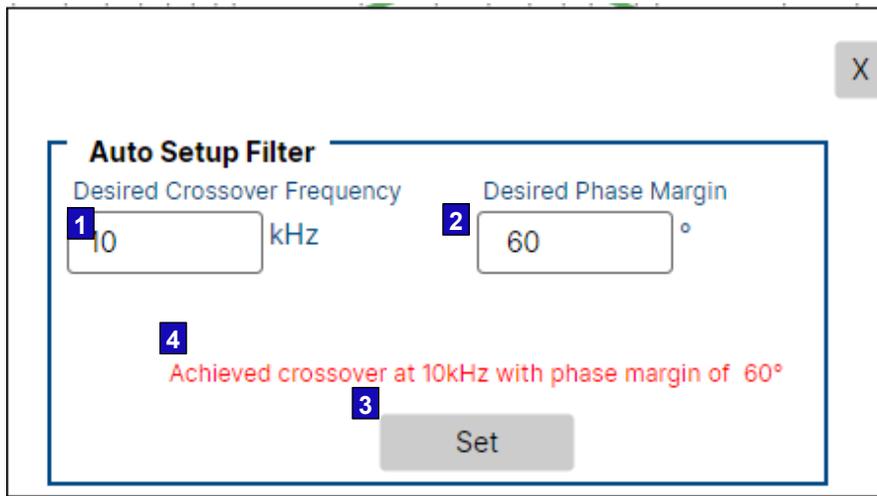| NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Mode				This selects the mode for which the filter is to be configured, Normal, Light-load, Soft-Start.
2	Enable Controls				This enables and disables the sliders.
3	Plot select				This is used to select plots that are to be shown.
4	LF Gain: Normal Mode Light Load Mode Soft-Start Mode	0xFE01 0xFE05 0xFE09	[7:0]	R/W	This sets the LF Gain for the mode selected in 1.
5	Zero Placement: Normal Mode Light Load Mode Soft-Start Mode	0xFE02 0xFE06 0xFE0A	[7:0]	R/W	Allows user adjust zero placement.
6	Pole Placement & HF Gain: Normal Mode Light Load Mode Soft-Start Mode	0xFE03/4 0xFE07/8 0xFE0B/C	[7:0]	R/W	Allows user adjust pole placement and HF Gain.
7	Full Loop Calculation				Shows the loop gain values using the current digital filter settings.
8	Command Values				Shows the equivalent register values of the current digital filter settings.
9	Auto Setup				Allows user to automatically configure filter values using desired crossover frequency and phase margin. Refer to succeeding section for details.
10	Additional Settings				Opens additional settings menu. Refer to succeeding section for details.
11	Apply Changes				Writes the changes made to the registers.

Figure 21. Auto Setup Filter Dialog Box

Table 20. Figure 21 Callouts

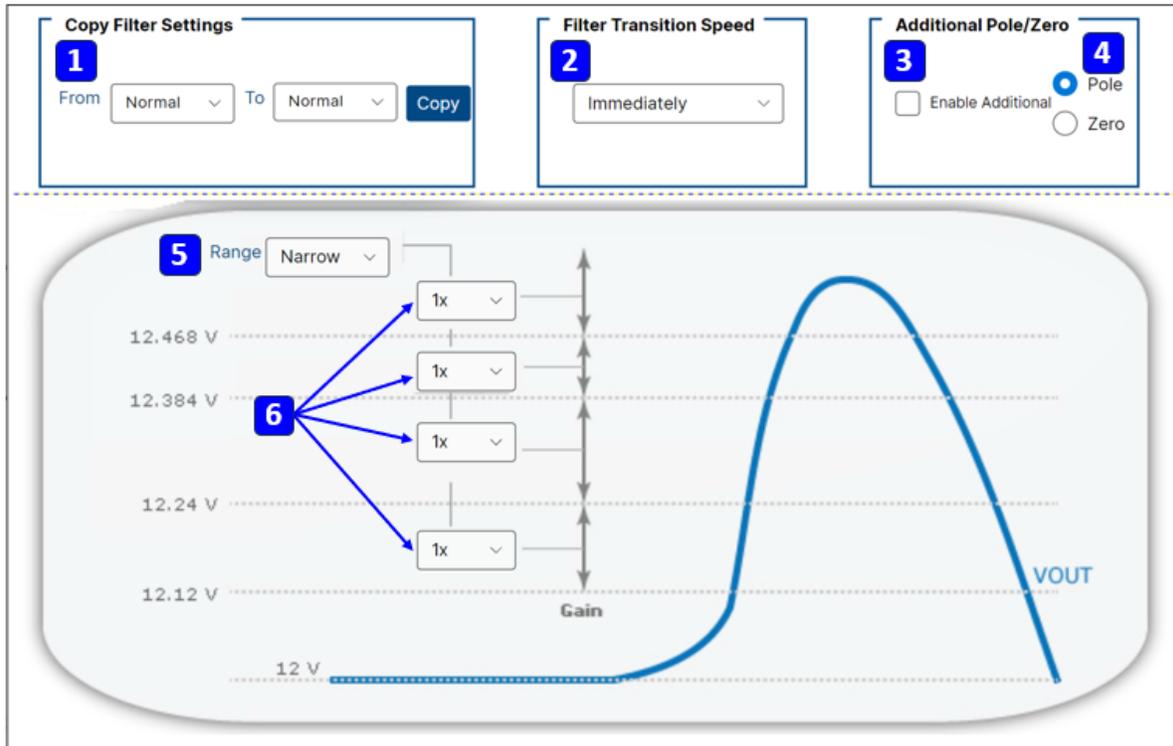| NO.	NAME	DESCRIPTION
1	Desired Crossover Frequency	Set the desired crossover frequency between 6.5kHz and 20kHz.
2	Desired Phase Margin	Set the desired phase margin between 0° to 70°.
3	Set	Run Calculation to determine the Digital Filter values that will closely match the desired parameters.
4	Achieved Value	A note will appear with achieved result. The achieved cross over frequency and/or phase margin may not exactly matched the original inputs.

Figure 22. Filter - Additional Settings Window

Table 21. Figure 22 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Copy Filter Configuration				This copies the filter configuration between different modes.
2	Filter Transition Speed	0xFE4A	[1:0] [2:2]	R/W	This sets the filter transition speed.
3	Enable Additional Pole or Additional Zero	0xFE60 0xFE61	[7:0] [7:0]	R/W	This configures additional digital pole or zero setting ADD_PZ.
4	Additional Pole or Zero configuration	0xFE62	[7:7]	R/W	This configures additional ADD_PZ as either digital pole or zero.
5	Global Non-Linear Gain	0xFE29	[0:0]	R/W	This sets universal nonlinear gain.
6	Non-Linear Gains	0xFE5E	[7:0]	R/W	These set the nonlinear gain for different ranges.

Fault Response Settings

Figure 23. Fault Response Window

Table 22. Figure 23 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Fault Response Configuration				This section lists all the fault response configuration, more details in Table 23.
2	Disable PWM on Fault	0xFE3D	[5:0]	R/W	This sets which PWM to disable when a fault occurs.
3	Watchdog Timer	0xFE3F	[1:0]	R/W	This sets the time for shutting down the system during a "Disable Output" fault response.
4	Reset				This discards all the changes that are not applied yet.

Note: Click "Apply" to write the modified settings to the registers.

Figure 24. Fault Response Configuration

Table 23. Figure 24 Callouts

NO.	NAME		REG	BITS	R/W	DESCRIPTION
1	IOUT_OC:	Debounce	0xFE31	[3:0]	R/W	This sets the debounce time for IOUT_OC fault.
		Fault Response	0x47	[7:6]		This sets the response after the fault has occurred.
		Delay	0x47	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0x47	[5:3]		This sets the number of retires following a fault condition.
2	IOUT_OC_FAST:	Debounce	0xFE2D	[1:0]	R/W	This sets the debounce time for IOUT_OC_FAST fault.
		Fault Response	0xFE35	[7:6]		This sets the response after the fault has occurred.
		Delay	0xFE35	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0xFE35	[5:3]		This sets the number of retires following a fault condition.
3	IOUT_UC	Debounce	0xFE31	[7:4]	R/W	This sets the debounce time for IOUT_OC fault.
		Fault Response	0x4C	[7:6]		This sets the response after the fault has occurred.
		Delay	0x4C	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0x4C	[5:3]		This sets the number of retires following a fault condition.

4	IOUT_UC_FAST	Debounce	0xFE2D	[1:0]	R/W	This sets the debounce time for IOUT_OC_FAST fault.
		Fault Response	0xFE36	[7:6]		This sets the response after the fault has occurred.
		Delay	0xFE36	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0xFE36	[5:3]		This sets the number of retires following a fault condition.
5	IIN_OC	Debounce	0xFE31	[11:8]	R/W	This sets the debounce time for IIN_OC fault.
		Fault Response	0x5C	[7:6]		This sets the response after the fault has occurred.
		Delay	0x5C	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0x5C	[5:3]		This sets the number of retires following a fault condition.
6	IIN_OC_FAST	Debounce	0xFE2C	[1:0]	R/W	This sets the debounce time for IIN_OC_FAST fault.
		Fault Response	0xFE37	[7:6]		This sets the response after the fault has occurred.
		Delay	0xFE37	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0xFE37	[5:3]		This sets the number of retires following a fault condition.
7	ISHARE	Debounce	0xFE31	[15:12]	R/W	This sets the debounce time for ISHARE fault.
		Fault Response	0xFE38	[7:6]		This sets the response after the fault has occurred.
		Delay	0xFE38	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0xFE38	[5:3]		This sets the number of retires following a fault condition.
8	VOUT_OV	Debounce	0xFE30	[3:0]	R/W	This sets the debounce time for VOUT_OV fault.
		Fault Response	0x41	[7:6]		This sets the response after the fault has occurred.
		Delay	0x41	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0x41	[5:3]		This sets the number of retires following a fault condition.
9	VOUT_OV_FAST	Debounce	0xFE2F	[1:0]	R/W	This sets the debounce time for VOUT_OV_FAST fault.
		Fault Response	0xFE34	[7:6]		This sets the response after the fault has occurred.
		Delay	0xFE34	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0xFE34	[5:3]		This sets the number of retires following a fault condition.
10	VOUT_UV	Debounce	0xFE30	[10:8]	R/W	This sets the debounce time for VOUT_UV fault.
		Fault Response	0x45	[7:6]		This sets the response after the fault has occurred.
		Delay	0x45	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0x45	[5:3]		This sets the number of retires following a fault condition.
11	IOUT_OC_LV	Debounce	0xFE30	[15:14]	R/W	This sets the debounce time for IOUT_OC_LV fault.
		Fault Response	0x49	[7:6]		This sets the response after the fault has occurred.
		Delay	0x49	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0x49	[5:3]		This sets the number of retires following a fault condition.
12	VIN_OV	Debounce	0xFE30	[7:4]	R/W	This sets the debounce time for VIN_OV fault.
		Fault Response	0x56	[7:6]		This sets the response after the fault has occurred.
		Delay	0x56	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0x56	[5:3]		This sets the number of retires following a fault condition.
13	VIN_UV	Debounce	0xFE30	[13:11]	R/W	This sets the debounce time for VIN_UV fault.
		Fault Response	0x5A	[7:6]		This sets the response after the fault has occurred.
		Delay	0x5A	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0x5A	[5:3]		This sets the number of retires following a fault condition.
14	OT	Debounce	0xFE32	[3:0]	R/W	This sets the debounce time for OT fault.
		Fault Response	0x50	[7:6]		This sets the response after the fault has occurred.
		Delay	0x50	[2:0]		This sets the delay time for retries.
		Shutdown Settings	0x50	[5:3]		This sets the number of retires following a fault condition.

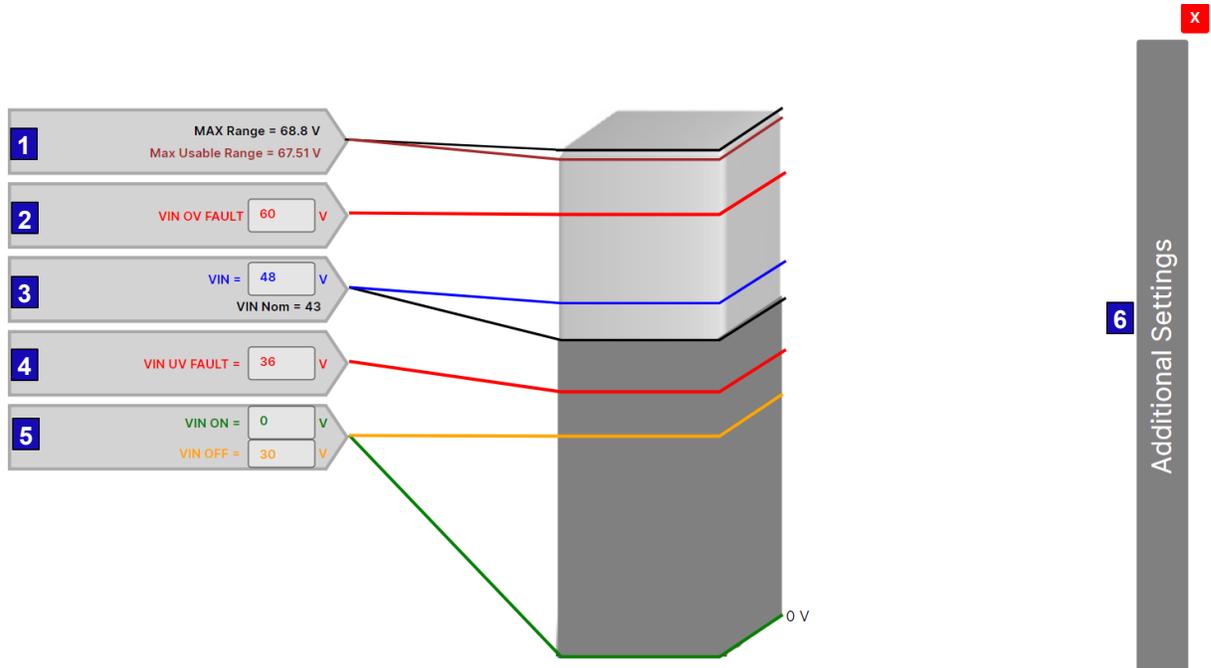| 15	TON_MAX	Debounce Fault Response Delay Shutdown Settings	0xFE32 0x63 0x63 0x63	[7:4] [7:6] [2:0] [5:3]	R/W	This sets the debounce time for TON_MAX fault. This sets the response after the fault has occurred. This sets the delay time for retries. This sets the number of retires following a fault condition.
16	POUT_OP	Debounce Fault Response Delay Shutdown Settings	0xFE32 0x69 0x69 0x69	[11:8] [7:6] [2:0] [5:3]	R/W	This sets the debounce time for POUT_OP fault. This sets the response after the fault has occurred. This sets the delay time for retries. This sets the number of retires following a fault condition.
17	GPIO1	Debounce Fault Response Delay Shutdown Settings	0xFE33 0xFE39 0xFE39 0xFE39	[3:0] [7:6] [2:0] [5:3]	R/W	This sets the debounce time for GPIO1 fault. This sets the response after the fault has occurred. This sets the delay time for retries. This sets the number of retires following a fault condition.
18	GPIO2	Debounce Fault Response Delay Shutdown Settings	0xFE33 0xFE3A 0xFE3A 0xFE3A	[7:4] [7:6] [2:0] [5:3]	R/W	This sets the debounce time for GPIO2 fault. This sets the response after the fault has occurred. This sets the delay time for retries. This sets the number of retires following a fault condition.
19	GPIO3	Debounce Fault Response Delay Shutdown Settings	0xFE33 0xFE3B 0xFE3B 0xFE3B	[11:8] [7:6] [2:0] [5:3]	R/W	This sets the debounce time for GPIO3 fault. This sets the response after the fault has occurred. This sets the delay time for retries. This sets the number of retires following a fault condition.
20	GPIO4	Debounce Fault Response Delay Shutdown Settings	0xFE33 0xFE3C 0xFE3C 0xFE3C	[15:12] [7:6] [2:0] [5:3]	R/W	This sets the debounce time for GPIO4 fault. This sets the response after the fault has occurred. This sets the delay time for retries. This sets the number of retires following a fault condition.
21	VDD/VCORE OV:	Debounce Fault Response Shutdown Settings	0xFE4D	[5:5] [6:6] [7:7]	R/W	This sets the debounce time for VDD/VCORE OV fault. This sets the response after the fault has occurred. This sets the number of retires following a fault condition.
22	VDD UV	Debounce	0xFE4D	[4:4]	R/W	This sets the debounce time for VDD UV fault.

VIN Settings

Figure 25. VIN Window

Table 24. Figure 25 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range Max Usable Range				Max Range is the equivalent maximum input voltage based on VFF ADC input voltage, VFF resistor dividers, transformer turns ratio and the topology selected. Max usable range represents ADC usable range. Value of parameters with text boxes can be changed by using slider or direct input method. Press "Apply" to confirm changes.
2	VIN OV Fault	0x55	[15:0]	R/W	Sets the upper voltage threshold in volts that will cause an Over-Voltage FAULT condition.
3	VIN Vin Nom				User can input voltage for loop calculation in Filter Settings. Represents the nominal input voltage equivalent to 1V on VFF pin.
4	VIN UV Fault	0x59	[15:0]	R/W	Sets the lower voltage threshold in volts that will cause an Under-Voltage FAULT condition.
5	VIN ON VIN OFF	0X35 0x36	[15:0] [15:0]	R/W	Sets the value of the input voltage (Vrms) to start power conversion. Sets the value of the input voltage (Vrms) to stop power conversion. Note: For isolated topologies, set VIN ON =0V since input voltage is not available before IC switching begins. VIN OFF is not checked until regulation voltage is reached or TON_MAX has expired.
6	Additional Settings				Opens the voltage feedforward settings, see succeeding section.

Figure 26. VIN - Additional Settings

Table 25. Figure 26 Callout

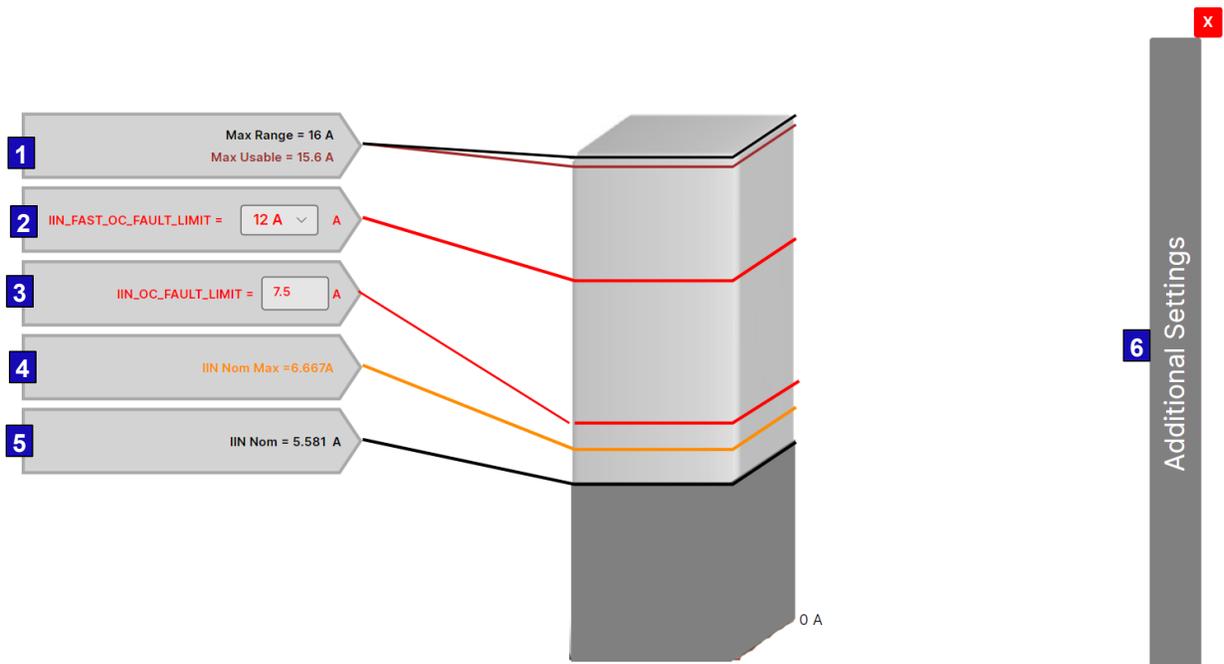| NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Voltage Feed Forward Setting	0xFE29	[2:2]	R/W	This enables/disable the voltage line feed forward loop. Press Apply to confirm changes.

IIN Settings

Figure 27. IIN Window

Table 26. Figure 27 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range Max Usable Range				Max Range is the equivalent maximum input current based on CS1 ADC input voltage, current transformer turns ratio and termination resistance. Max usable range represents the ADC usable range. Value of parameters with text boxes can be changed by using slider or direct input method. Press Apply to confirm changes.
2	IIN FAST OC FAULT LIMIT	0xFE2C	[7:2]	R/W	Using a dropdown, set the Input Fast Overcurrent Limit range between 1.2V and 250mV CS1 ADC equivalent pin voltage.
3	IIN FAST OC FAULT	0x5B	[15:0]	R/W	Sets the Input Fast Overcurrent limit threshold. Maximum value allowed is 90% of range selected in [2].
4	IIN Nom Max				Expected Input Current at lowest operating voltage before Input UV fault is triggered. Value is approximately equal to POUT/VIN UV Fault.
5	IIN Nom				Expected Input Current at Nominal Input voltage. Value is approximately equal to output power POUT/VIN nominal.
6	Additional Settings				Opens Input Current Additional Settings, see succeeding section.

Figure 28. IIN - Additional Settings Window

Table 27. Figure 28 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Input Fast OCP Bypass	0xFE4E	[3:3]	R/W	This selects GPIO1 pin or CS1 pin for CS1 Fast OCP.
2	Input Fast OCP Blanking	0xFE4E	[6:4]	R/W	This selects blanking value of 0/40/80/120/200/400/600/800 ns.
3	Input Fast OCP Debounce				This opens the fault window where IIN_OC_FAST debounce can be set.
4	Input Fast OCP Timeout	0xFE4E	[2:0]	R/W	This sets the number of consecutive switching cycles with a CS1 OCP condition before the IIN_OC_FAST_FAULT flag is set.

VOUT Settings

Figure 29. VOUT Window

Table 28. Figure 29 Callouts

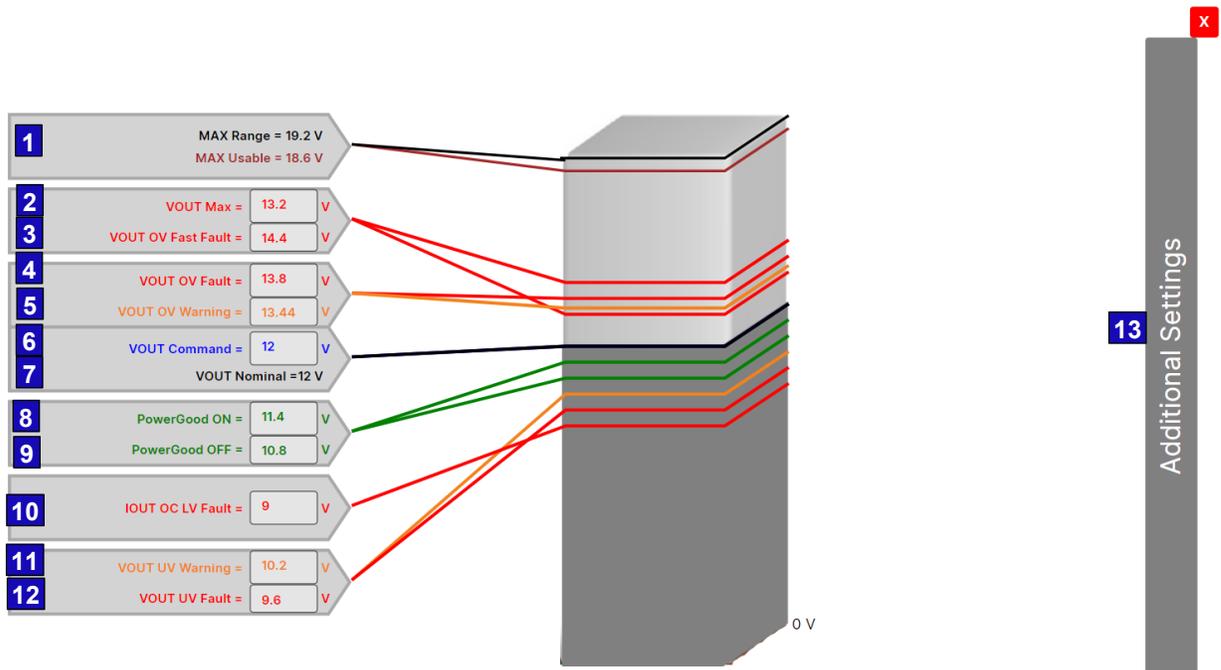| NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	MAX Range MAX Usable				Max Range is the equivalent maximum output voltage based on VS± & OVP ADC input voltage and resistor dividers. Max usable range represents the ADC usable range. Value of parameters with text boxes can be changed using the slider or direct input method. Press "Apply" to confirm changes.
2	VOUT Max	0x24	[15:0]	R/W	Sets the upper limit on VOUT.
3	VOUT OV Fast Fault Threshold	0xFE2F	[7:2]	R/W	Sets the VOUT OV Fast Fault Threshold.
4	VOUT OV Fault Limit	0x40	[15:0]	R/W	Sets the upper voltage that will cause an Over-Voltage FAULT condition.
5	VOUT OV Warn Limit	0x42	[15:0]	R/W	Sets the upper voltage that will cause an Over-Voltage WARN condition.
6	VOUT Command	0x21	[15:0]	R/W	Sets VOUT to the commanded value.
7	VOUT Nominal				Represents the nominal output voltage equivalent to 1V on VS± pins.
8	Power Good ON Limit	0x5E	[15:0]	R/W	Sets the limit of the output volt when POWER_GOOD signal is asserted.
9	Power Good OFF Limit	0x5F	[15:0]	R/W	Sets the limit of the output volt when POWER_GOOD signal is de-asserted.

10	IOUT OC LV Fault Limit	0x48	[15:0]	R/W	Sets lower volage threshold that will cause an Under-Voltage-in-current limiting mode FAULT condition.
11	VOUT UV Warn Limit	0x43	[15:0]	R/W	Sets the lower volt that will cause Under-Voltage WARN condition.
12	VOUT UV Fault Limit	0x44	[15:0]	R/W	Sets the Under-voltage threshold that causes an under voltage fault condition.
13	Additional Settings				Opens the Output Voltage Additional Settings menu, refer to succeeding section.

Figure 30. VOUT - Additional Settings Window

Table 29. Figure 30 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	VOUT Droop	0x28	[15:0]	R/W	Sets the rate, in mV/A, at which output voltage decreases (increases) with increasing (decreasing) output current.
2	Droop Sample Rate	0xFE65	[1:0]	R/W	Select the rate from the drop down at which IOUT is sampled.
3	VOUT Transition Rate	0x27	[15:0]	R/W	Sets the output transition rate, in mV/us, on a VOUT_COMMAND or OPERATION commands.
4	Disable VOUT Transition	0xFE65	[2:2]	R/W	Disables or Enables Vout transition from one value to another set by Transition Rate.
5	VOUT_OV Sampling	0xFE4D	[3:2]	R/W	Select from drop down menu the VOUT_OV Sampling rate.

Note: Press ENTER to confirm the value. Press Apply to write changes to the registers.

IOUT Settings

Figure 31. IOUT Window

Table 30. Figure 31 Callouts

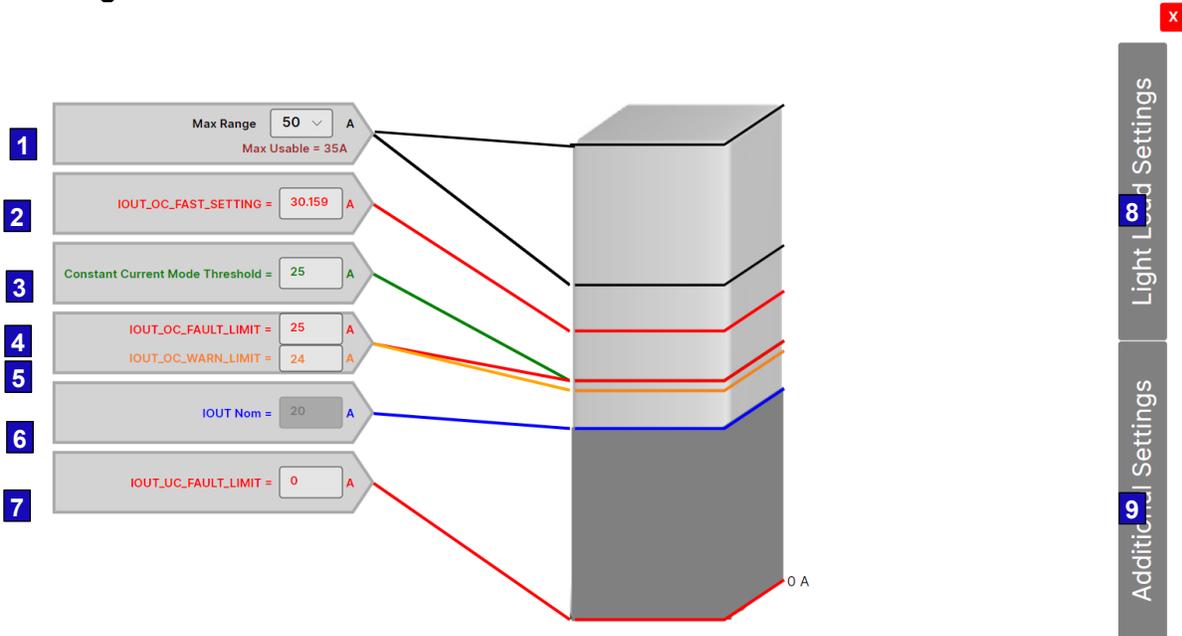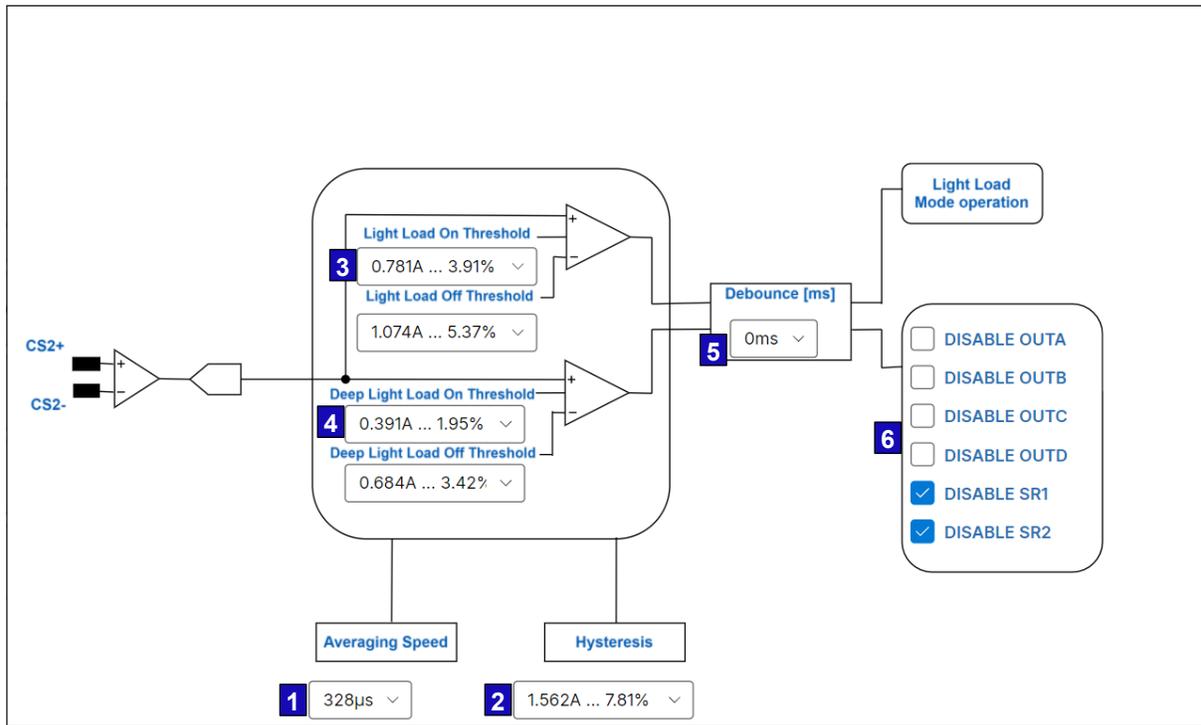| NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range Max Usable	0xFE4F	[1:0]	R/W	Max Range is the equivalent maximum output current based on CS2± ADC input voltage and sense resistor value & location. For low side sensing, 30mV and 60mV ranges are available, while 480mV is available for high side sensing. Max usable range represents the ADC usable range. Value of parameters with text boxes can be changed using the slider or direct input method. Press "Apply" to confirm changes.
2	IOUT OC FAST Threshold	0xFE2D	[7:2]	R/W	Sets IOUT OC FAST threshold.
3	CC Mode Threshold	0xFE5D	[3:3] [2:0]	R/W	CC mode polarity if above or below the OCP limit. Sets the threshold based percentage above or below OCP limit.
4	IOUT OC Fault Limit	0x46	[15:0]	R/W	Sets the current threshold that will cause an Over-Current Fault condition.
5	IOUT OC Warn Limit	0x4A	[15:0]	R/W	Sets the current threshold that will cause an Over-Current WARN condition.
6	IOUT Nom				This is the Load Current value set on the Main page which represent the nominal full load current of the converter.
7	IOUT UC FAULT LIMIT	0x4B	[15:0]	R/W	Sets the current threshold that will cause an output Under-Current FAULT.
8	Light Load Settings				Opens the Light Load Settings menu, refer to succeeding section.
9	Additional Settings				Opens the Light Load Settings menu, refer to succeeding section.

Figure 32. IOUT - Light Load Settings Window

Table 31. Figure 32 Callouts

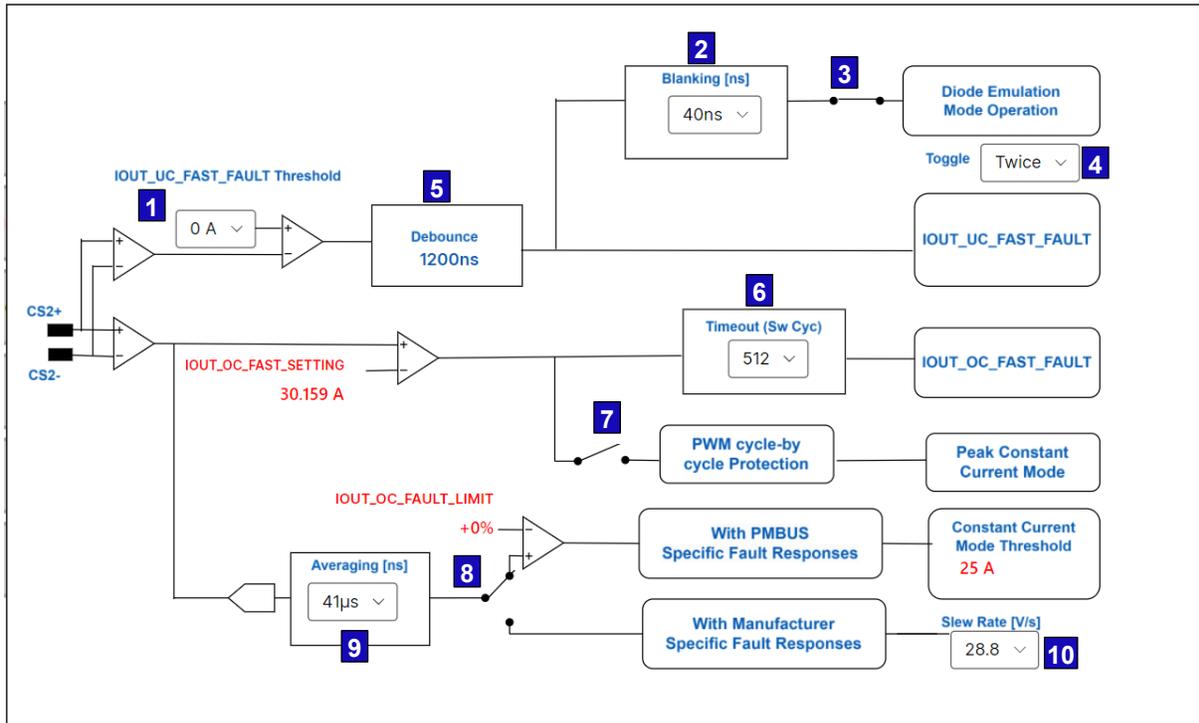| NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Deep Light Load Mode and Light Load Mode Averaging Speed	0xFE4B	[4:3]	R/W	Sets the averaging speed and resolution used for the light load mode and deep light load mode thresholds.
2	Deep Light Load Mode and Light Load Mode Hysteresis	0xFE4B	[2:1]	R/W	Sets the amount of hysteresis applied to the light load mode and deep light load mode thresholds.
3	SR LLM Threshold	0xFE5F	[3:1]	R/W	Sets the load current limit on the CS2 ADC below which SR1 and SR2 enter the light load mode.
4	Deep LLM Threshold	0xFE4B	[7:5]	R/W	Sets the load current limit on the CS2 ADC below which SR1 and SR2 enter the deep light load mode.
5	SR Debounce	0xFE5C	[7:5]	R/W	Sets the time for which any further transition of the thresholds will be ignored after the SR have been turned on and off.
6	Deep LLM OUTx and SRx disable	0xFE4C	[6:1]	R/W	Disables selected OUTx and SRx if the load current drops below the deep light load SR disable threshold.

Figure 33. IOUT - Additional Settings Window

Table 32. Figure 33 Callouts

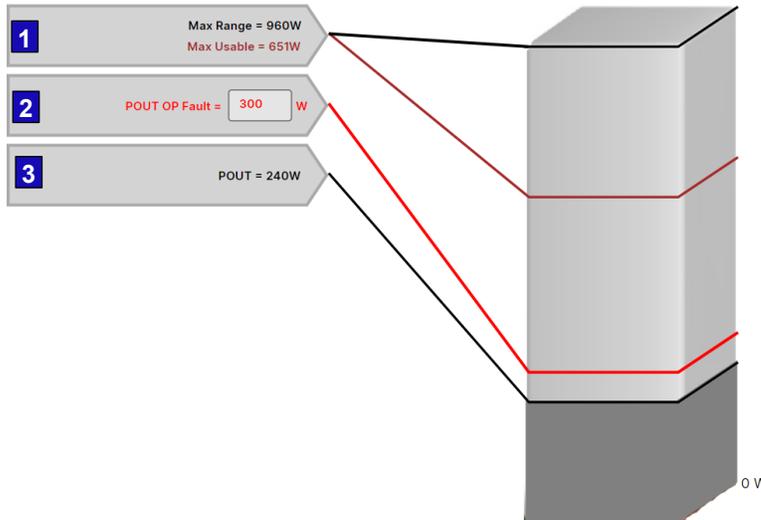| NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	IOUT_UC_FAST_FAULT Threshold	0xFE2E	[1:1] [7:2]	R/W	Sets the IOUT_UC_FAST_FAULT Threshold Level and polarity. Current setting range is ±30mV/Rsense.
2	SR Blanking	0xFE52	[7:6]	R/W	Sets SR Blanking time
3	Diode Emulation Mode	0xFE5C	[1: 1]	R/W	Sets diode emulation mode
4	SR toggle rate in Diode Emulation Mode	0xFE5C	[0:0]	R/W	Sets number of toggles in one Tsw.
5	IOUT_UC_FAST_FAULT Debounce	0xFE2E	[0:0]	R/W	Thie debounce time is automatically set based on 0xFE2D [1:0] setting in the Fault Response Window
6	CS2 Fast OCEP Timeout	0xFE4F	[6:4]	R/W	Sets number of consecutive switching cycles with a CS2 OCP condition before the IOUT_OC_FAST_FAULT flag is set.
7	Peak Constant Current Mode	0xFE4F	[3:3]	R/W	Sets CS2 Fast OCP cycle-by-cycle protection on OUTA to OUTD.
8	Average Constant Current Settings	0xFE4F	[2:2]	R/W	Selects between PMBUS and Manufacture Specific Fault Response.
9	Constant Current Turbo Mode	0xFE4F	[7:7]	R/W	Sets CS2 Averaging time.
10	Slew rate during CC mode(turbo mode only)	0xFE5D	[5:4]	R/W	Sets slew rate during CC mode.

POUT settings

Figure 34. POUT Settings Window

Table 33. Figure 34 Callouts

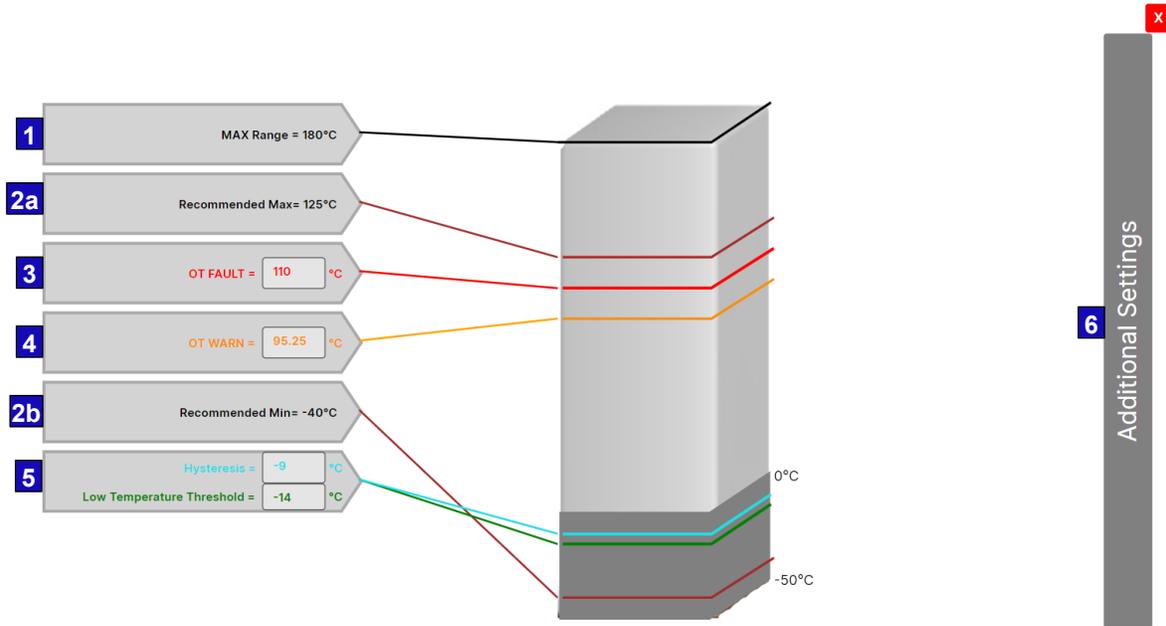| NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range Max Usable				Max Range = Vout Max * Iout Max. Max Usable = Vout Max Usable * Iout Max Usable. These represent the maximum power that can be achieved by this configuration. Value of parameters with text boxes can be changed by using the slider or direct input method. Press "Apply" to confirm changes.
2	POUT OP Fault	0x68	[15:0]	R/W	Sets the upper power limit that will cause an Over-Power FAULT condition.
3	POUT				The nominal output power which is equal to VOUT * IOUT Nom.

Temperature settings

Figure 35. Temperature Settings Window

Table 34. Figure 35 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Max Range				The maximum temperature that can be read.
2a 2b	Recommended Max Temp Recommended Min Temp				This represents the operating range of ADP1055. Temperature settings must be within this range for proper operation.
3	OT Fault	0x4F	[15:0]	R/W	Sets the upper temperature limit that will cause an Over-Temp FAULT condition.
4	OT Warn	0x51	[15:0]	R/W	Sets the upper temperature limit that will cause an Over-Temp WARN condition.
5	Low Temperature Hysteresis and Threshold	0xFE62	[6:4] [3:2]	R/W	Low temperature settings can be enabled/disabled in the Additional Settings menu. Low Temperature Threshold can be set in ±4°C steps from -14°C to +10°C. The hysteresis added to the threshold is in 5°C steps from 5°C to 20°C.
6	Additional Settings				Opens the Additional Settings menu, refer to succeeding section.

Figure 36. Temperature - Additional Settings Window

Table 35. Figure 36 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Temperature sense Current Select	0xFE5A	[2:0]	R/W	Sets the bias current for external Tj sense. Recommended value is 10uA.
2	Temperature sense ADC Resolution	0xFE5A	[6:5]	R/W	Sets Temperature sensing ADC resolution.
3	Temperature sense Level-Shift Disable	0xFE5A	[3:3]	R/W	Enables/disables internal diode level shifter during external Tj sense.
4	Temperature sense point	0xFE62	[1:0]	R/W	Sets sensing point for low temperature.

Soft-Start settings

Figure 37. Soft-Start Settings Window

Table 36. Figure 37 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	TON Delay	0x60	[15:0]	R/W	Sets the time from start (ON_OFF_CONFIG) until output starts to rise.
2	TON Max	0x62	[15:0]	R/W	Sets the maximum time before which the output voltage must exceed VOUT_UV_FAULT limit.
3	TON Rise	0x61	[15:0]	R/W	Sets the time from output rises until voltage enters regulation band.
4	Additional Settings				Opens Soft-Start Settings and Blanking menu, refer to succeeding section.

Figure 38. Soft-Start - Additional Settings Window

Table 37. Figure 38 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Soft-Start Settings: SStart from Pre-Charge Disable LL Filter during SStart Force SStart Filter Blank SRs during SStart	0xFE51 0xFE51 0xFE51 0xFE5F	[0:0] [1:1] [2:2] [0:0]	R/W	Enables soft-start from pre-charge value. Disables switching to DCM filter during soft-start. When set, soft-start filter is used regardless of low temp filter Blank SRs during soft-start
2	Soft-Start Blanking	0xFE46	[15:0]	R/W	Set the flags to be ignored during soft-start

Soft-Stop settings

Figure 39. Soft-Stop Settings Window

Table 38. Figure 39 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	TOFF Delay	0x64	[15:0]	R/W	Sets the time from stop (ON_OFF_CONFIG) until stops transferring energy to output.
2	TOFF Max	0x66	[15:0]	R/W	Sets the maximum time that will cause an TOFF-Max WARN condition, that is the time its takes to power down the output voltage from VOUT to 12.5% of VOUT.
3	TOFF Fall	0x65	[15:0]	R/W	Sets the time from end of turn-off delay time to voltage = 0.
4	Additional Settings				Opens the Soft-Stop Settings and Blanking menu, refer to succeeding section.

Figure 40. Soft-Stop - Additional Settings

Table 39. Figure 40 Callouts

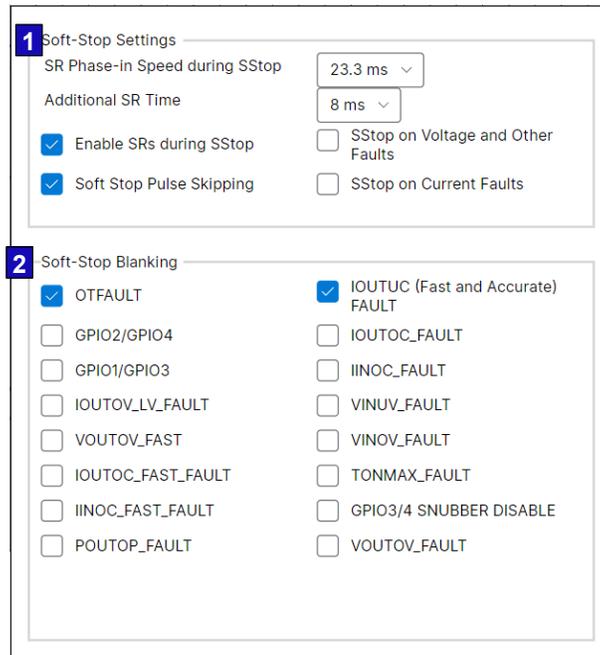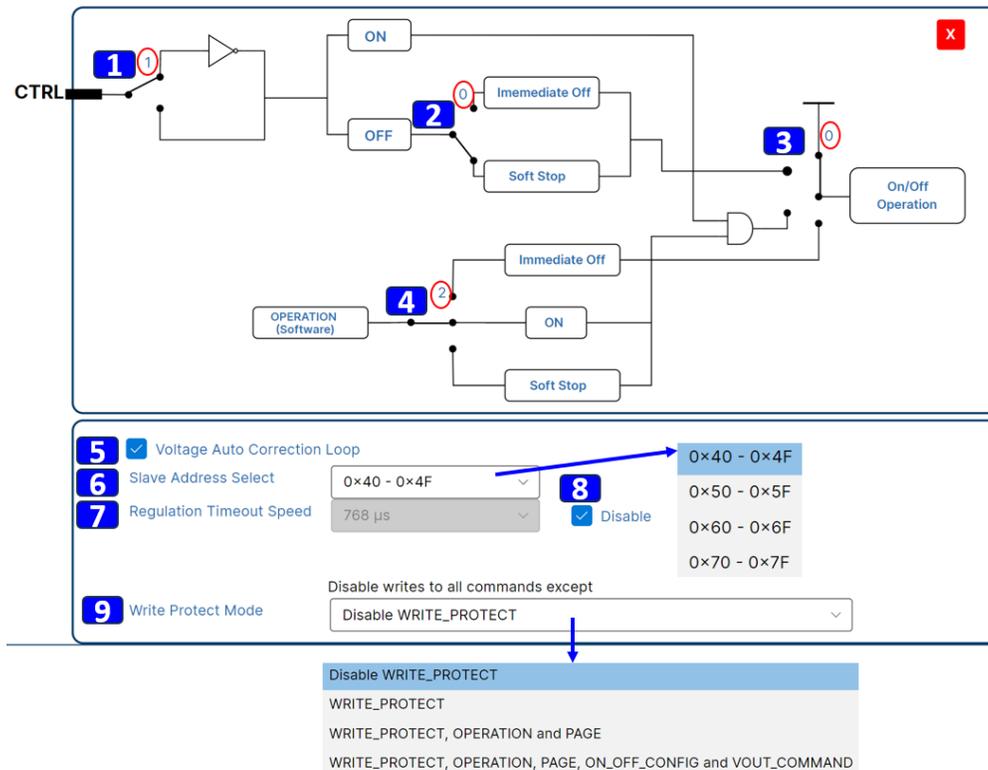| NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Soft-Stop Settings: SR Phase-in Speed during SStop Additional SR Time Enable SRs during SStop Soft-Stop Pulse Skipping SStop on Voltage & Other Faults SStop on Current Faults	0xFE51 0xFE50 0xFE4C 0xFE50 0xFE51 0xFE51	[5:3] [7:6] [0:0] [2:2] [6:6] [7:7]	R/W	Sets the SR edge phase-in/transitioning speed during soft-stop. Sets the time SRs are kept active after the soft-stop ramp down. Re-enables SRs during soft-stop, recommended setting is enabled. Allow pulse skipping during soft stop, SRs are not affected. Enable soft-stop on voltage and other fault. Enable soft-stop on current fault.
2	Soft-Stop Blanking	0xFE47	[15:0]		Set the flags to be ignored during Soft Stop.

Control and Additional Settings

Figure 41. Control and Additional Settings Window

Table 40. Figure 41 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	CONTROL pin polarity	0x02	[1:1]	R/W	This sets the polarity of the CONTROL pin. 0 = Active Low 1 = Active High
2	CONTROL pin power-down action	0x02	[0:0]	R/W	This sets the CTRL pin power-down action. 0 = uses TOFF_DELAY and TOFF_FALL values 1 = turns off the output as quickly as possible
3	ON/OFF Operation	0x02	[4:2]	R/W	Device's response to On/Off Operation. 0 = device powers up when power is present 1 = CTRL pin must be asserted to enable device 2 = OPERATION must be 1 to enable device 3 = CTRL and OPERATION required to enable device
4	OPERATION Command	0x01	[7:6]	R/W	Device's response to OPERATION command. 0 = immediate off 1 = soft off 2 = device on
5	Voltage Auto Correction Loop Enable	0xFE4A	[4:4]	R/W	This Enables/disables the Auto Correction Loop.
6	Slave address select	0xD0	[5:4]	R/W	This sets the slave address for the part.

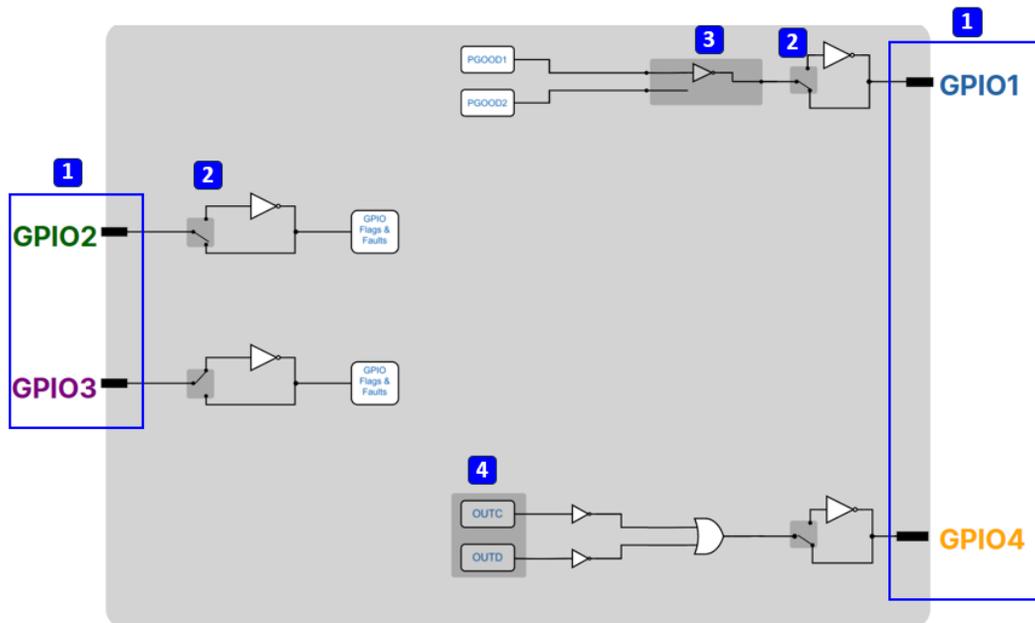| 7 | Regulation Timeout Speed | 0xFE4A | [6:6] | R/W | Selects the speed of regulation correction between 48 or 96 switching cycles.
Double update rate affects this register. |
| 8 | Overshoot protection disable | 0xFE4A | [7:7] | R/W | Disables or enables setpoint reference tracking. |
| 9 | Write Protect Mode | 0x10 | [7:5] | R/W | This selects between different combinations for Write Protect command. |

GPIO Settings

Figure 42. GPIO Settings

Table 41. Figure 42 Callouts

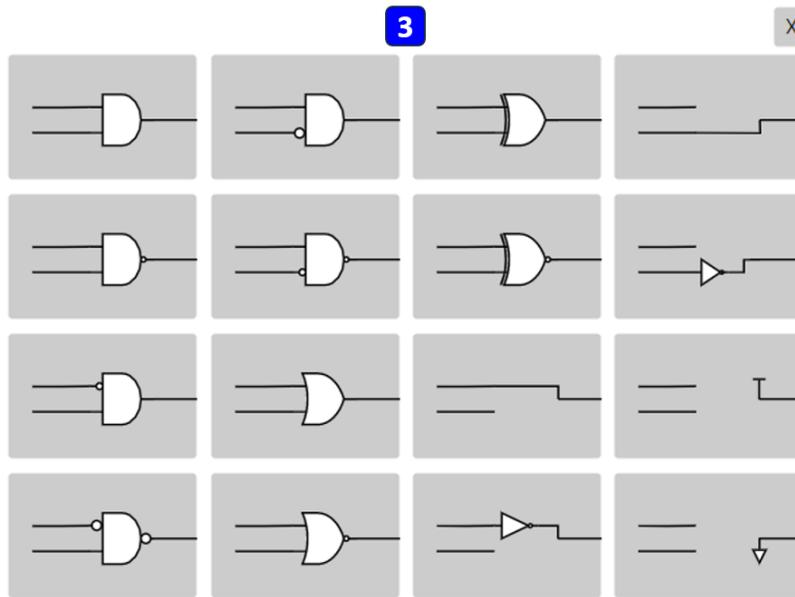| No.	Name	REG	Bits	R/W	Description
1	Change direction of GPIOx Click on relevant GPIO text to have GUI change pin direction	0xFE40	[0:0] [2:2] [4:4] [6:6]	R/W	This changes the direction of GPIO1. This changes the direction of GPIO2. This changes the direction of GPIO3. This changes the direction of GPIO4
2	Change polarity of GPIOx	0xFE40	[1:1] [3:3] [5:5] [7:7]	R/W	This changes the polarity of GPIO1. This changes the polarity of GPIO2. This changes the polarity of GPIO3. This changes the polarity of GPIO4.
3	Select the logic function. Refer to Figure 43 below.	0xFE41 0xFE41 0xFE42 0xFE42	[3:0] [7:4] [3:0] [7:4]	R/W	This selects GPIO1 logic function. This selects GPIO2 logic function. This selects GPIO3 logic function. This selects GPIO4 logic function.
4	GPIO 3 & 4 snubber enable. Refer to Figure 44 below.	0xFE64	[7:6]	R/W	This selects GPIO3/GPIO to be either PGOOD or active snubber. (Only applies to GPIO3 & GPIO4)

Figure 43. Logic Selection Table

Figure 44. GPIO3 & GPIO4 PGOOD / Snubber selection options

PGOOD Settings

Figure 45. PGOOD Settings

Table 42. Figure 45 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	PGOOD2 Fault Select	0xFE45	[15:0]	R/W	This selects the flags, if any of the selected flags is asserted it will set the PGOOD2 flag.
2	PGOOD1 Fault Select	0xFE44	[15:0]	R/W	This selects the flags, if any of the selected flags is asserted it will set the PGOOD1 flag.
3	PGOOD1 Debounce	0xFE43	[3:2] [1:0]	R/W	Sets the PGOOD1 OFF debounce time. Sets the PGOOD1 ON debounce time.
4	PGOOD2 Debounce	0xFE43	[7:6] [5:4]	R/W	Sets the PGOOD2 OFF debounce time. Sets the PGOOD2 ON debounce time.

SMBALERT Settings

Figure 46. SMB_ALERT Mask settings

Table 43. Figure 46 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	SMBALERT_MASK	0x1B	[15:8] [7:0]	W	Command code of the STATUS_x mask register to update Update mask register with this value

Current Share (Ishare) Settings

Figure 47. Current Share Settings

Table 44. Figure 47 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Current Share Select	0xFE2B	[3:3]	R/W	Selects between CS1 and CS2 reading used for current share.
2	Select Bitstream	0xFE2B	[4:4]	R/W	Selects between analog and digital current sharing.
3	Share Bus Bandwidth	0xFE2B	[2:0]	R/W	Sets the amount of bandwidth dedicated to the share bus.
4	Bit difference between Master and Slave	0xFE2A	[3:0]	R/W	Sets how closely a slave tries to match the current of master device.
5	Number of Bits Dropped by Master	0xFE2A	[7:4]	R/W	Sets how much a master device reduces its output voltage to main current sharing.

Monitor

Main

Figure 48. Monitor Window

Table 45. Figure 48 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Circuit Diagram				Displays the simplified circuit diagram of the system with the circuit values and the read values of input voltage, input current, output voltage and output current.
2	Flags and Readings				Opens the Flags and Readings Window

Flags and Readings

Figure 49. Flags and Readings Window

Table 46. Figure 49 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Output Voltage	0x8B	[15:0]	R	Displays the output voltage.
2	Output Current	0x8C	[15:0]	R	Displays the output current.
3	Output Power	0x96	[15:0]	R	Displays the output power.
4	Input Voltage	0x88	[15:0]	R	Displays the input voltage.
5	Input Current	0x89	[15:0]	R	Displays the input current.
6	Input Power				Displays the input power that is calcualted using the input voltage and current.
7	External Temperature 1	0x8E	[15:0]	R	Displays the external temperature 1.
8	External Temperature 2	0x8F	[15:0]	R	Displays the external temperature 2.
9	Duty Cycle	0x94	[15:0]	R	Displays the duty cycle.
10	Frequency	0x95	[15:0]	R	Displays the frequency.

11	**Status_Word:** None CML Temperature VIN UV IOUT OC VOUT OV OFF BUSY Unknown Other Fans Power Good # MFR Input IOUT/POUT VOUT	0x79	[0] [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11] [12] [13] [14] [15]	R	Red means the corresponding fault has occurred. A fault or warning not listed in bits [7:1] Communication, memory, or logic fault. Temperature fault or warning. Input under-voltage fault. Output over-current fault. Output over-voltage fault. Asserted if unit is not proving power to output. Device was busy and unable to respond. A fault or warning not listed in bits STATUS_WORD[15:1] A bit in STATUS_OTHER is set. Fan or airflow fault or warning (not supported). POWER_GOOD is negated. Manufacturer-specific fault or warning. Input voltage, input current, or input power fault or warning. Output current or output power fault or warning. Output voltage fault or warning.
12	**Fault Flags:** IOUT_OC IOUT_OC_FAST IOUT_UC IOUT_UC_FAST IIN_OC IIN_OC_FAST ISHARE VOUT_OV VOUT_OV_FAST VOUT_UV IOUT_OC_LV VIN_OV VIN_UV OT TON_MAX POUT_OP GPIO1 GPIO2 GPIO3 GPIO4	0x7B 0x80 0x7B 0x80 0x7C 0x80 0x7B 0x7A 0x80 0x7A 0x7B 0x7C 0x7C 0x7D 0x7A 0x7B 0x80 0x80 0x80 0x80	[7] [1] [4] [2] [2] [3] [3] [7] [0] [4] [6] [7] [4] [7] [2] [1] [4] [5] [6] [7]	R	Red means the corresponding fault has occurred. Output Over-Current fault. Fast output Over-Current fault. Output Under-Current fault. Fast output reverse current fault. Input Over-Current fault. Fast input Over-Current fault. Current sharing fault. Output Over-Voltage fault. Fast output Over-Voltage fault. Output Under-Voltage fault. Output Over-Current fault and Low-Voltage fault. Input Over-Voltage fault. Input Under-Voltage fault. Over temperature fault. The device did not reach VOUT_MAX within the given time. Output Over-Power fault. GPIO1 fault. GPIO2 fault. GPIO3 fault. GPIO4 fault.

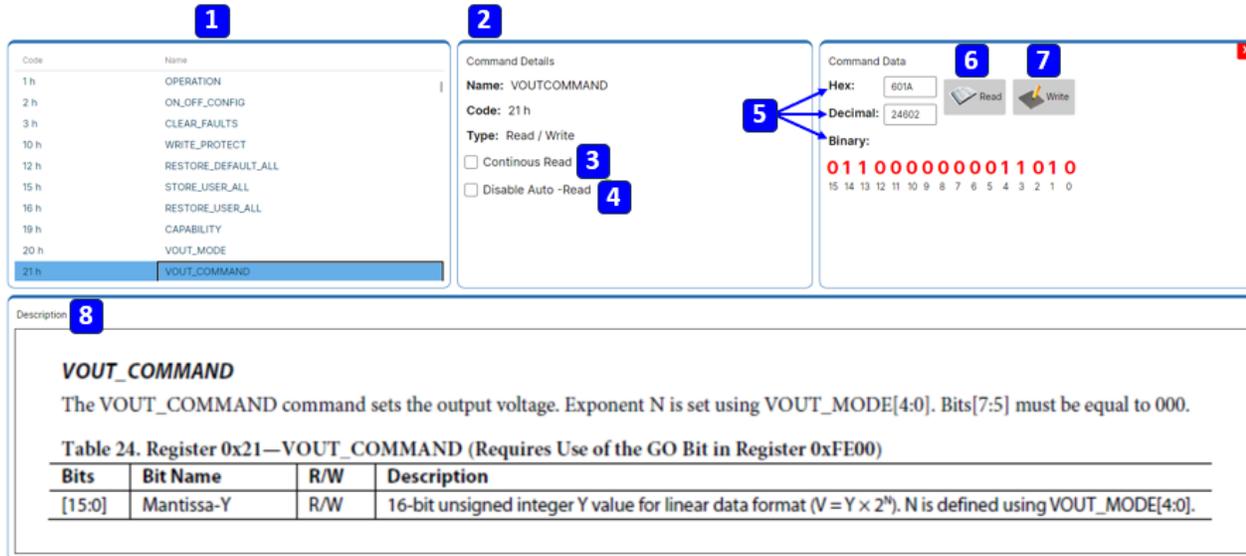|					
13	**Status Flags:** TOFF_MAX_WARN VOUT_MAX_WARN VOUT_UV_WARN VOUT_OV_WARN IOUT_OC_WARN VIN_LOW OT_WARN COMM_ERR CRC_ERR PEC_ERR DATA_ERR CMD_ERR VDD UV VDD OV VCORE OV Address Warning SR Off Sync Unlock PGOOD1 Fault PGOOD2 Fault Constant Current	0x7A 0X7A 0X7A 0X7A 0X7B 0X7C 0X7D 0X7E 0X7E 0X7E 0X7E 0X7E 0XFE94 0XFE94 0XFE94 0XFE94 0XFE94 0XFE94 0XFE94 0XFE94 0XFE94	[1] [3] [5] [6] [5] [3] [6] [1] [4] [5] [6] [7] [0] [1] [2] [3] [4] [5] [6] [7] [8]	R	Red means the corresponding fault has occurred. Device took too long to power down to 12.5% of its output voltage. Output voltage was great than VOUT_MAX command. Output under voltage warning has occurred. Output over voltage warning has occurred. Output over current warning has occurred. The device is off due to insufficient input voltage. Over temperature warning has occurred. Other communication fault has occurred. Memory fault detected. Packet error check failed. Invalid or unsupported data received. Invalid or unsupported command received. VDD is below limit. VDD is above limit. 2.5V VCORE is above limit. I2C address warning. Address resistor is out-of-range. Synchronous rectifiers SR1 and SR2 are disabled. Sync mode is enabled but unit not locked to sync input frequency. PGOOD1 Fault. PGOOD2 Fault. Power supply is operating in constant current mode.
14	Regular/Latched Flags				This selects between regular flags and latched flags.
15	First Flag	0xFE95	[7:0]	R	This shows the name of the first fault.
16	Clear Faults	0x03	[7:0]	Send	This clears all bits in PMBUS status register (latched flags).

Register Access

Main

Figure 50. Register Access Window

Table 47. Figure 50 Callouts

NO.	NAME	REG	BITS	R/W	DESCRIPTION
1	Register Map	0x01 to 0xFEA3			This control displays the complete ADP1055 register map, Selecting any particular register will display the data contained in that register, and will allow this register to be read and written to.
2	Register Details				These set of indicators display the selected register's (selected in 1) Command Name, Code and its value in hexadecimal and decimal formats.
3	Continuous Read				If this checkbox is enabled then the GUI will continuously read the value of the register selected in control 1.
4	Disable Automatic Read-Back				The GUI automatically does a read operation after a write operation to verify if the write operation was successful. Enabling this checkbox disables this automatic read-back feature.
5	Bit Display				This control / indicator displays the current value of the selected register, in Hex, Decimal and Binary. Each field can be entered with Binary bits modified by clicking on the individual bits.
6	Read				This control reads the value of the register selected by control 1.
7	Write				This control writes the value to the register selected by control 1.
8	Description				This indicator displays the description of the selected register.

Revision History

REVISION HISTORY	REVISION DATE	DESCRIPTION	PAGES CHANGED
A	01/07	—	—
B	05/25	Updated description section, figures and tables to match the latest version.	1–57

Notes