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Evaluating the ADMV8052 30 MHz to 520 MHz, Digitally Tunable Band-Pass Filter

FEATURES

Fully featured evaluation board for the ADMV8052
On-board SDP-S connector for the SPI
Evaluation using on-board LDO regulators powered by the USB
ACE software interface for SPI control

EQUIPMENT NEEDED

Network analyzer
Windows® PC
USB cable
EVAL-SDP-CS1Z (SDP-S) controller board

DOCUMENTS NEEDED

ADMV8052 data sheet

SOFTWARE NEEDED

ACE software

GENERAL DESCRIPTION

The ADMV8052-EVALZ is available for evaluating the ADMV8052 digitally tunable, band-pass filter (BPF). The ADMV8052-EVALZ incorporates the ADMV8052 chip, as well as a negative voltage generator, low dropout (LDO) regulators, and an interface to the EVAL-SDP-CS1Z (SDP-S) system demonstration platform (SDP) to allow simple and efficient evaluation. The negative voltage generator and LDO regulators allow the ADMV8052 to be powered by either the 5 V USB supply voltage from the PC via the SDP-S or by using two external power supplies.

The ADMV8052 is an IC that features a digitally selectable frequency of operation. The chip features three BPFs that span from 30 MHz to 520 MHz. The chip can be programmed using a 4-wire serial port interface (SPI), and the SDP-S controller allows the user to interface with the SPI of the ADMV8052 through the Analog Devices, Inc., Analysis | Control | Evaluation (ACE) software.

For full details on the ADMV8052, see the ADMV8052 data sheet, which must be consulted in conjunction with this user guide when using the ADMV8052-EVALZ.

EVALUATION BOARD PHOTOGRAPH

Figure 1.

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REVISION HISTORY

/202—R evision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADMV8052-EVALZ has the ADMV8052 chip on board. The ADMV8052-EVALZ also includes a negative voltage generator and three LDO regulators to provide the necessary supply voltages for the chip. The regulators can be entirely powered by the 5 V USB supply voltage from the PC via the SDP-S.

To power the ADMV8052-EVALZ using the 5 V USB supply, slide the S1 switch down (as shown in Figure 2) to power the on-board negative voltage generator and LDO regulators. Alternatively, the ADMV8052-EVALZ can be powered externally by sliding the S1 switch up and then connecting the power supplies to the VPOS and VNEG Subminiature Version A (SMA) ports or test points. The applicable voltage range for the positive input VPOS is between 3.5 V and 5.5 V, and the applicable voltage range for the negative input VNEG is between −5.5 V and −2.7 V.

Figure 2 shows an example lab bench setup for the ADMV8052-EVALZ. To observe the filter response from the ADMV8052-EVALZ, connect the RF1 and RF2 ports to a network analyzer (or similar instrument). Typically, RF1 and RF2 are connected to Port 1 and Port 2 on the network analyzer, as shown in Figure 2.

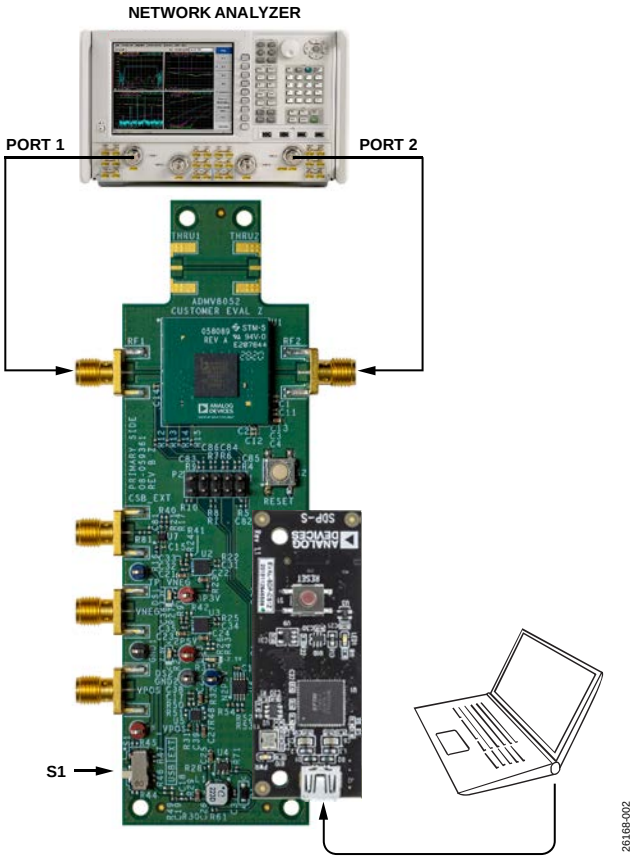


Figure 2. Lab Bench Setup

EVALUATION BOARD SOFTWARE

INSTALLING THE ACE SOFTWARE, ADMV8052 PLUG-INS, AND DRIVERS

The ADMV8052-EVALZ uses the Analog Devices ACE software. For instructions on how to install and use the ACE software, go to the ACE software page.

If the ACE software is already installed on the PC, ensure that the installed ACE software is the latest version, as listed on the ACE software page. If the installed software is not the latest version, take the following steps to install the updated ACE software:

1. Uninstall the current version of the ACE software on the PC.
2. Delete the ACE folder found in **C:\ProgramData\Analog Devices** and **C:\Program Files (x86)\Analog Devices**.
3. Install the latest version of the ACE software. During the installation, ensure that the **.NET 40 Client**, **SDP Drivers**, and **LRF Drivers** components are selected (see Figure 3).

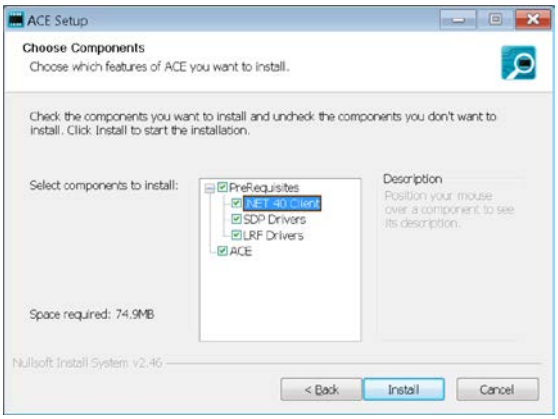


Figure 3. Required Driver Installations with the ACE Software

Once the installation finishes, the **ADMV8052 Board** plug-in appears in the **Attached Hardware** section of the **Start** tab when the ACE software is running. (see Figure 4).

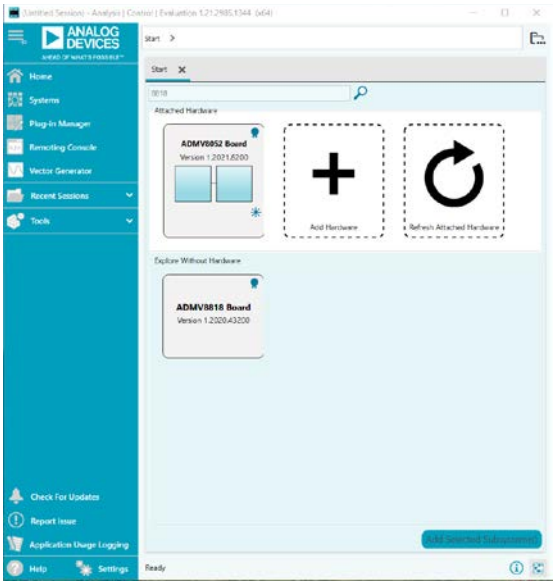


*Figure 4. **ADMV8052 Board** Plug-In Window after Opening the ACE Software*

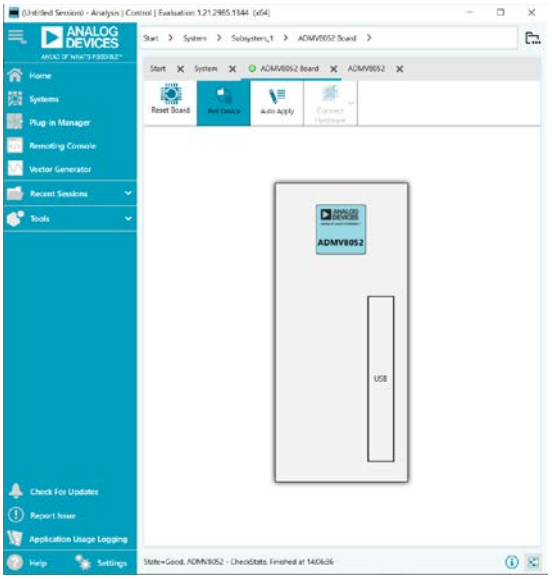
PLUG-IN OVERVIEW

When the ADMV8052-EVALZ is connected to the PC, the **ADMV8052 Board** appears in the **Attached Hardware** section of the **Start** tab. Double-click the **ADMV8052 Board** plug-in to open two tabs, which are the **ADMV8052 Board** plug-in view (see Figure 5) and the **ADMV8052** chip plug-in view (see Figure 6), respectively.

The **ADMV8052** chip plug-in view includes the following feature sections (see Table 1 for additional information on these sections):

- The **CONFIGURATION** section (load from .csv)
- The **Logic Pins** section
- The **SFL Settings** section
- The chip **Status** section
- The **Display** controls section
- The **Filter Settings** section

The ACE software provides a simple tutorial for testing the ADMV8052. For a more customized and detailed implementation, refer to ADMV8052 data sheet for a full description of the functionality, registers, and corresponding settings.



26168-005

Figure 5. ADMV8052 Board Plug-In View

26168-006

Figure 6. ADMV8052 Chip Plug-In View

PLUG-IN DETAILS

The full screen ADMV8052 chip plug-in with labels is shown in Figure 7. The labels correspond to items listed in Table 1, which describes the functionality of each section. For additional detailed programming, refer to the ADMV8052 data sheet.

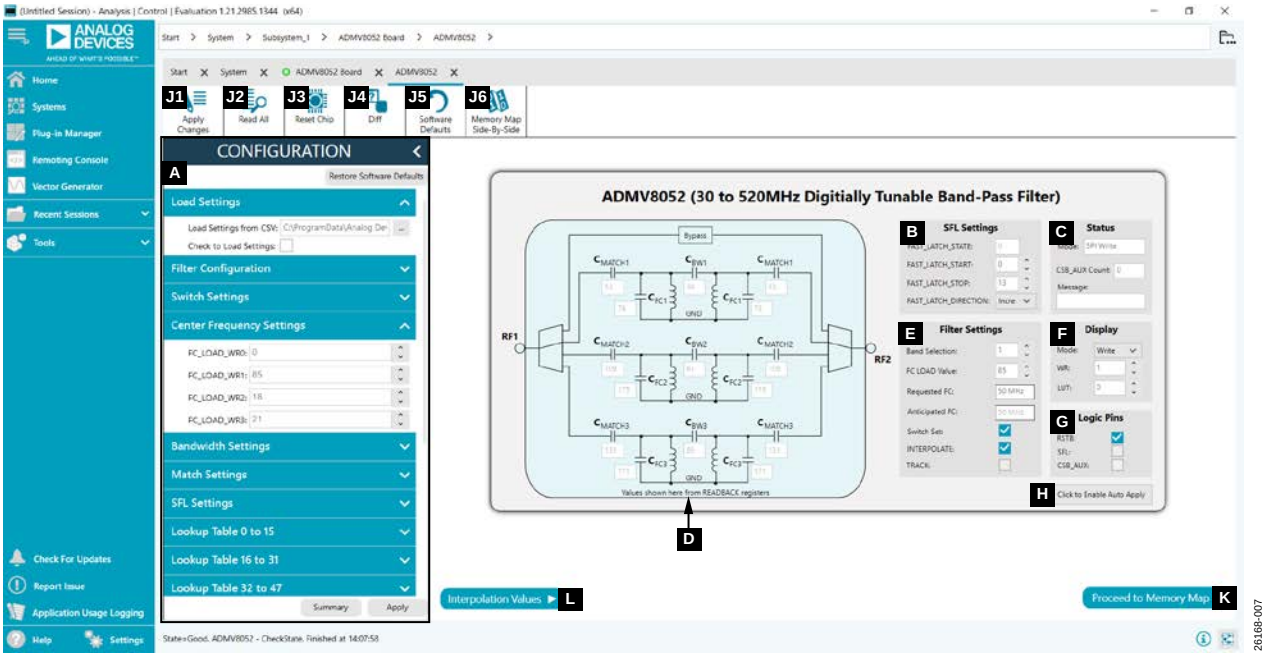


*Figure 7. **ADMV8052** Chip Plug-In with Labels*

Table 1. ADMV8052 Block Diagram Label Functions (See Figure 7)

Label	Function
A	Use the **CONFIGURATION** section to initialize the ADMV8052-EVALZ. **Load Settings from CSV**: click the **…** button to select which .csv file to load into the **CONFIGURATION** section. **Check to Load Settings**: once a file is selected, select this check box to load the .csv file contents into the **CONFIGURATION** section. Note that a check mark does not appear when the check box is selected. **Filter Configuration:** select the configuration settings for interpolation, tracking, or debug. **Switch Settings:** select the switch position settings for SPI write mode. **Center Frequency Settings:** select the center frequency settings for SPI write mode. **Bandwidth Settings:** select the bandwidth settings for SPI write mode. **Match Settings:** select the match settings for SPI write mode. **SFL Settings**: select the SPI fast latch (SFL) settings that are used when the chip is placed into the SPI fast latch mode. **Lookup Table 0 to 15**: define the configuration for lookup table (LUT)0 to LUT15. **Lookup Table 16 to 31**: define the configuration for LUT16 to LUT31. **Lookup Table 32 to 47**: define the configuration for LUT32 to LUT47. Note that following functions are not shown in Figure 7. Scroll down in the **CONFIGURATION** section to view these functions. **Lookup Table 48 to 63**: define the configuration for LUT48 to LUT63. **Lookup Table 64 to 79**: define the configuration for LUT64 to LUT79. **Lookup Table 80 to 95**: define the configuration for LUT80 to LUT95. **Lookup Table 96 to 111**: define the configuration for LUT96 to LUT111. **Lookup Table 112 to 127**: define the configuration for LUT112 to LUT 127.

Label	Function
	Band 1 Coefficients: define the interpolation coefficients for Band 1. **Band 2 Coefficients:** define the interpolation coefficients for Band 2. **Band 3 Coefficients:** define the interpolation coefficients for Band 3. **Summary**: click this button to review the settings for the initial setup. **Apply**: click this button to apply the settings to the chip. Note that clicking **Apply Changes** (J1) does not update the changes in this section. In addition, at startup, the main diagram user controls cannot be updated until the **Apply** button is clicked at least once. **Restore Software Defaults**: click this button to zero out the **CONFIGURATION** section prior to loading a different .csv file.
B	Use the **SFL Settings** section to configure the SPI fast latch settings on the chip when in the SFL mode. Refer to the ADMV8052 data sheet for more information regarding the internal state machine and SFL mode functionality. This section includes the following: **FAST_LATCH_STATE**: this value is the next state of the internal state machine pointer (read only). **FAST_LATCH_START**: this value determines the start location within the internal state machine. **FAST_LATCH_STOP**: this value determines the stop location within the internal state machine. **FAST_LATCH_DIRECTION**: this bit determines the direction that the internal state machine advances for each rising edge of the $\overline{CS}$ pin when in SFL mode.
C	The **Status** section includes the following: **Mode**: when the SFL pin is low, the mode is **SPI Write**. When the SFL pin is high, the mode is **SPI Fast Latch**, and the chip uses the LUT. **CSB_AUX Count**: when in SFL mode, this field displays the number of times the SDP-S logic pin, CSB_AUX, was toggled. **Message**: upon entering SFL mode, the **Message** field displays **Waiting for CSB**. Once the CSB_AUX pin is toggled, the **Message** field displays the current LUT number followed by the next LUT number.
D	The displayed block diagram section shows the position of the switch and capacitor codes for each filter band within the chip. While in **SPI Write** mode, any changes to the WRx registers automatically trigger a read operation of the **READBACK** registers, so that this section always reflects the actual hardware.
E	The **Filter Settings** section shows several controls for configuring each filter band in the chip. Depending upon if **INTERPOLATE** is enabled, various controls can be visible. When **INTERPOLATE** is enabled (as shown in Figure 7), the following controls are visible: **Band Selection:** this numeric up and down box (0 to 3) is used to set the desired filter band. A value of 0 corresponds to the bypass configuration, and all other values correspond to the filter band number. **FC_LOAD Value:** this numeric up and down box (0 to 255) is used to set the desired center frequency value. Note that this is a unitless quantity, where a 0 corresponds to the lowest center frequency within a particular band, and 255 corresponds to the highest center frequency within a particular band. **Requested FC:** enter in a requested center frequency in this text box. The value entered is used to select the desired band of operation and compute the closest **FC_LOAD Value** for that frequency of operation. **Anticipated FC:** this text box is an estimation of the operating center frequency based upon the **FC_LOAD Value**. **Switch Set:** this check box determines if the input and output switches change. **INTERPOLATE:** this check box enables the interpolation functionality on the chip. **TRACK:** this check box enables filter tracking, whereby when the capacitor codes of one filter are changed, the other two non-selected filter capacitor codes are also set to the same values. When **INTERPOLATE** is disable (not shown in Figure 7), the following controls are visible: **Band Selection:** this numeric up and down box (0 to 3) is used to set the desired filter band. A value of 0 corresponds to the bypass configuration, and all other values correspond to the filter band number. **FC_LOAD Value:** this numeric up and down box (0 to 255) is used to set the desired center frequency capacitor code. **BW_LOAD Value:** this numeric up and down box (0 to 255) is used to set the desired bandwidth capacitor code. **MATCH_LOAD Value:** this numeric up and down box (0 to 255) is used to set the desired input and output match capacitor code. **Switch Set:** this check box determines if the input and output switches change. **INTERPOLATE:** this check box enables the interpolation functionality on the chip. **TRACK:** this check box enables filter tracking, whereby when the capacitor codes of one filter are changed, the other two non-selected filter capacitor codes are also set to the same values. **READBACK Values --> Filter Settings:** this button is available when interpolation is disabled. Click this button to populate the read back values from the hardware into the **FC_LOAD**, **BW_LOAD**, and **MATCH_LOAD** values.

Label	Function
F	The **Display** section determines the actively selected WR or LUT number. This section includes the following: **Mode**: use the drop-down menu to select either **Write** or **LUT** display mode. **WR**: when the **Mode** is set to **Write**, scroll up and down to set the WR number (0 to 3) that is currently being configured and displayed in the **Filter Settings** section. Changing the WR number automatically changes the **Mode** to **Write**. **LUT**: when the **Mode** is set to **LUT**, scroll up and down to set the LUT number (0 to 127) that is currently being configured and displayed in the **Filter Settings** section. Changing to the LUT number automatically changes the **Mode** to **LUT**.
G	Use the **Logic Pins** section to toggle the SDP-S logic pins, which are connected to the logic pins on the ADMV8052 chip. This section includes the following: **RSTB**: clear the check box to bring the ADMV8052 $\overline{\text{RST}}$ pin low, which holds the chip in reset. Select the check box again to bring the chip out of reset. **SFL**: select the check box to bring the ADMV8052 SFL pin high, which places the chip in SFL mode. This action also toggles the on-board ADG749BKSZ switch connected to the ADMV8052 $\overline{\text{CS}}$ pin (see Figure 11). While in SFL mode, the ADMV8052 $\overline{\text{CS}}$ pin is connected to the SDP-S logic pin, CSB_AUX, and normal SPI transactions are disallowed. **CSB_AUX**: this pin is only available in SFL mode. Selecting the check box brings the CSB_AUX pin high, which advances the internal state machine pointer to the next LUT. If an external waveform generator is connected to the CSB_EXT port on the ADMV8052-EVALZ, the CSB_AUX pin has no effect, and the CSB_EXT port takes precedence.
H	Use the **Click to Enable Auto Apply** button to toggle the **ADMV8052 Board** plug-in **Auto Apply** feature. This feature is useful for quickly enabling auto apply so that any change made to the chip settings are automatically sent to the ADMV8052-EVALZ. Once the button is clicked, the **Click to Disable Auto Apply** button appears.
K	Click **Proceed to Memory Map** to open the **ADMV8052 Memory Map** (see Figure 8).
J1	All changes, except those made within the **CONFIGURATION** section, do not take effect until clicking **Apply Changes**. If **Auto Apply** is highlighted in the ADMV8052 Board tab (see Figure 5), the **Apply Changes** feature continuously runs every few seconds, and users do not have to click **Apply Changes** to apply or read back the block diagram settings.
J2	To read back all of the SPI registers of the chip, click **Read All**.
J3	Click **Reset Chip** to reset the chip.
J4	Click **Diff** to show registers that are different on the chip.
J5	Click **Software Defaults** to restore the software defaults to the chip, and then click **Apply Changes**. The software defaults for the ADMV8052 are for all registers to be zero, except for Register 0x011, which is set to 0x7F, and the interpolation coefficients in Register 0x300 to Register 0x32F.
J6	Click **Memory Map Side-By-Side** to enable the side by side memory map view.
L	Click **Interpolation Values** to open the subdiagram for displaying and editing the interpolation coefficients (see Figure 9). The interpolation coefficients can be changed to calibrate the center frequency and/or change the desired operating bandwidth for each filter band. Refer to the ADMV8052 data sheet for guidance on editing the interpolation coefficients.

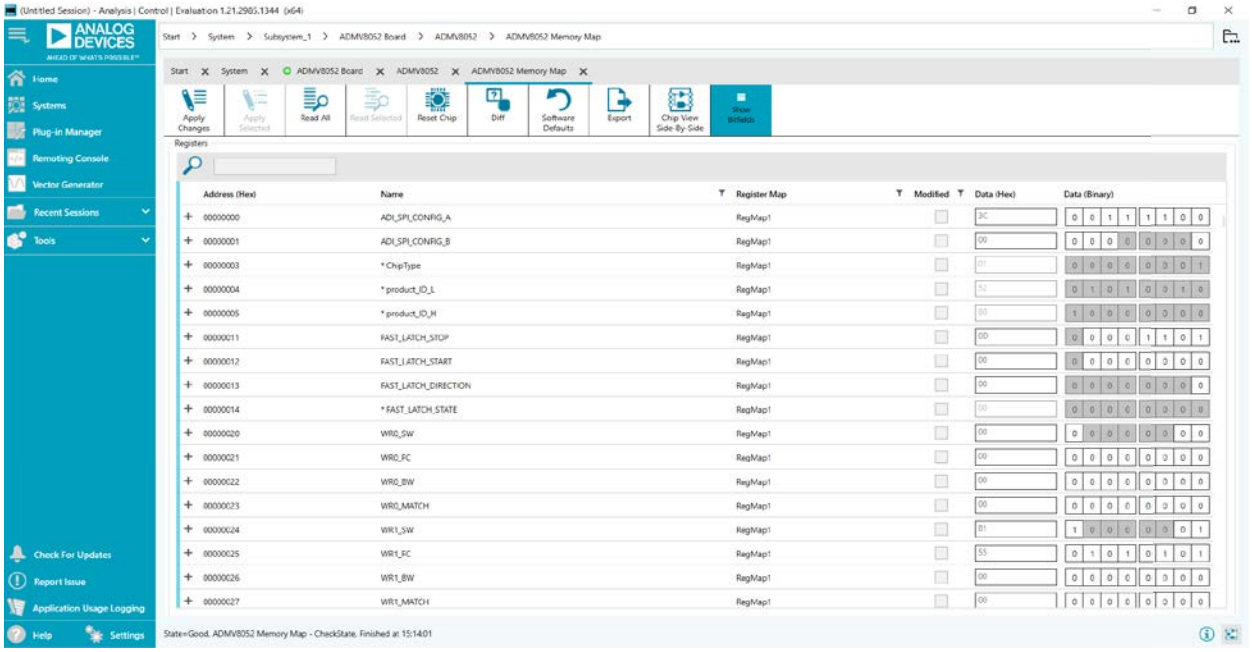


*Figure 8. **ADMV8052 Memory Map** in the ACE Software*

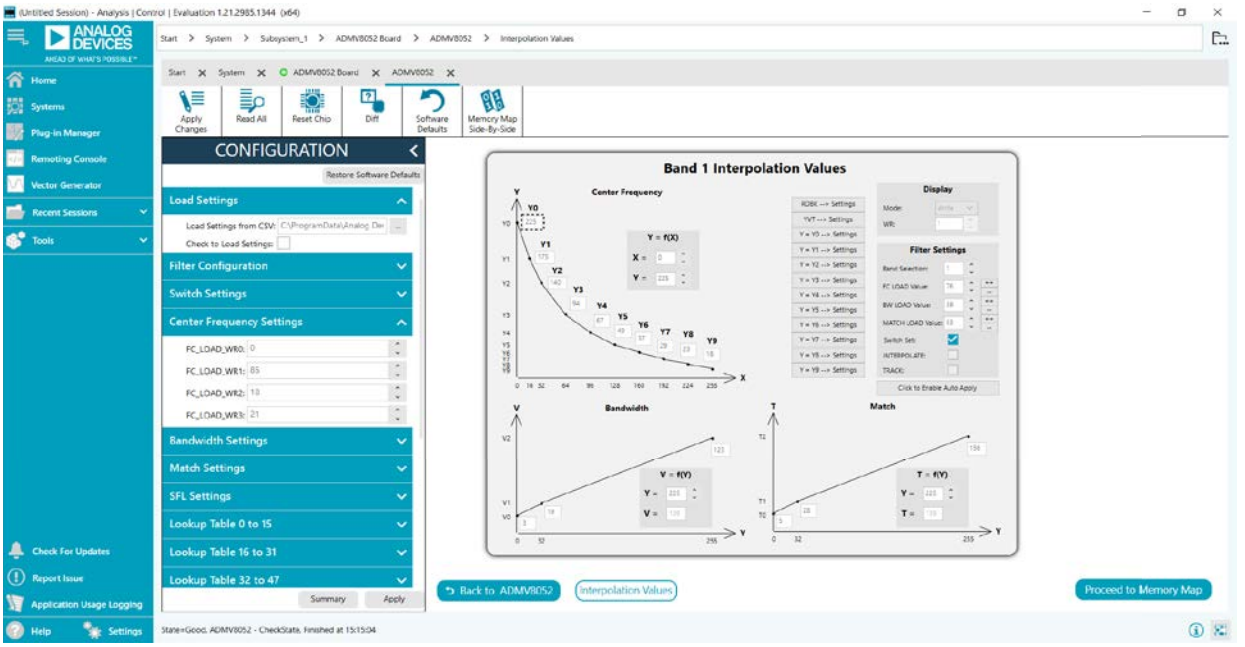


*Figure 9. **Interpolation Values** Subdiagram in the ACE Software*

PERFORMING EVALUATION

ADMV8052-EVALZ QUICK START

To set up the ADMV8052-EVALZ, take the following steps:

1. Connect the RF1 and RF2 ports to a network analyzer (or a similar instrument). Typically, RF1 and RF2 are connected to Port 1 and Port 2 on the network analyzer, as shown in Figure 2.
2. Connect the SDP-S to the 120-pin connector on the ADMV8052-EVALZ. Do not connect the SDP-S to the PC until after completing Step 3 or Step 4.
3. On the ADMV8052-EVALZ, slide the S1 switch down (as shown in Figure 2) to power the ADMV8052-EVALZ from the 5 V USB supply voltage from the PC via the SDP-S.
4. Alternatively to Step 3, slide the S1 switch up and connect the power supplies to the VPOS and VNEG ports. The applicable voltage range for VPOS is between +3.5 V and +5.5 V and for VNEG is between −5.5 V and −2.7 V. The external supply current limits must be set to 20 mA. Expected supply current drawn for VPOS is 12 mA to 14 mA and for VNEG is 2 mA to 3 mA. The ADMV8052 chip current drawn per supply pin is typically 10s of microamps or less. Most of the current drawn from the ADMV8052-EVALZ comes from the LDO regulators and the status indicator light emitting diodes (LEDs), DS1 to DS3.
5. Connect a USB cable between the PC and the SDP-S.
6. Open the ACE software. The **ADMV8052 Board** appears in the **Attached Hardware** section of the **Start** tab. Double-click the **ADMV8052 Board** plug-in to open two tabs, one is the **ADMV8052 Board** plug-in view and one is the ADMV8052 chip plug-in.
7. Use the **CONFIGURATION** section (see Figure 10) in the ACE software to initialize the chip. By default, the **ADMV8052_Register_Load_BW9.csv** file is loaded into this section. Click **Apply** to send the default settings to the chip and to allow the main diagram user controls to become editable.

NETWORK ANALYZER SETTINGS

When evaluating the ADMV8052-EVALZ, a good starting point for configuring the network analyzer is as follows:

- Start frequency = 0.01 GHz
- Start frequency = 1.01 GHz
- Number of points = 1001
- Step size = 1 MHz
- Power level = −10 dBm
- Measure types = S-parameters (S21, S11, and S22)
- Format = log magnitude (S21), smith charts (S11 and S22)
- Calibration = full 2-port

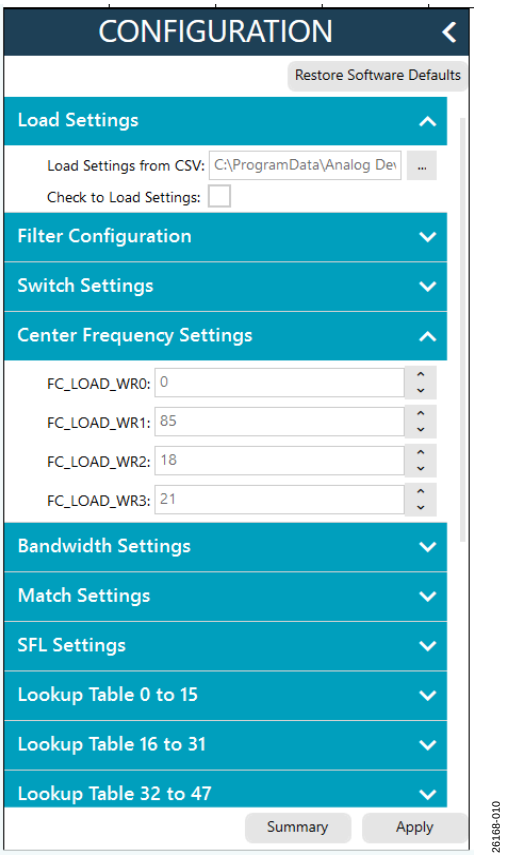


*Figure 10. ADMV8052 **CONFIGURATION** Section*

CSV FILES

By default, the **ADMV8052_Register_Load_BW9.csv** file is loaded into the **CONFIGURATION** section. This file contains interpolation coefficients that correspond to approximately 9% bandwidth. There are two additional .csv files provided that contain interpolation coefficients for 7% and 11% bandwidth, respectively. To load a different .csv file in the **CONFIGURATION** section, take the following steps:

1. If the **Modify** button is visible, click to allow changes.
2. Click **Restore Software Defaults** to zero out the **CONFIGURATION** section.
3. Click the **…** button next to **Load Settings from CSV** to select which .csv file to load (see Figure 10).
4. Select the **Check to Load Settings** check box to load the .csv file contents into the **CONFIGURATION** section. Note that a check mark does not appear when the check box is selected.
5. Click **Apply** to send out the settings to the hardware.

AUTOMATIC CHIP RESET

If a reset of the ADMV8052 chip is required on the ADMV8052-EVALZ, click **Reset Chip** (see Figure 7 and Label J3 in Table 1 for additional information). This automated sequence performs the following actions:

- Toggles all SDP-S general-purpose input/output (GPIO) logic pins to a low state, which brings the RST pin of the ADMV8052 low to initiate a hard reset of the ADMV8052.
- Toggles the RST pin high to bring the ADMV8052 chip back to the normal operating state.
- Programs Register 0x000 to 0x81, which also resets the ADMV8052. This step covers legacy boards that did not have the RST pin connected.
- Programs Register 0x000 to 0x3C to enable the SDO pin on the ADMV8052 and to allow SPI streaming with Endian register ascending order.
- Reads back the register settings of the ADMV8052.

MANUAL CHIP RESET

For manual reset operations, the following outlines various ways to perform a reset:

- There is a reset button (S2) on the ADMV8052-EVALZ evaluation board. Pressing this button pulls the RST pin low to initiate a reset to the factory power-up state.
- The RST pin can also be pulled low from within the ACE software by unchecking the **RSTB** check box in the lower right corner of Figure 7 (see Label G). When using this option, be sure to click the check box again to return the RST pin high.
- Register 0x000 can be programmed to 0x81 to initiate a reset of the ADMV8052.

Regardless of the manual reset option used, it is recommended to perform the following after the device resets:

- Programs Register 0x000 to 0x3C to enable the SDO pin on the ADMV8052 and to allow SPI streaming with Endian register ascending order.
- Read back all registers on the ADMV8052.

LOSS OF BOARD COMMUNICATION

When the ADMV8052 is turned off and then on, or if the USB cable is disconnected and connected while the ACE software is running, communication with the ADMV8052 may be lost. To regain communication, take the following steps:

1. Click the **System** tab.
2. Click the USB symbol in the **SDP-S Controller** subsystem.
3. Click **Acquire**.

If this action does not work, restart the ACE software to reinitiate communication with the ADMV8052-EVALZ.

REGULATOR BYPASS

The ADMV8052-EVALZ has a negative voltage generator and three LDO regulators on board that allow the user to operate the device using the 5 V USB supply voltage from the PC via the SDP-S. By default, the provisional 2.5 V LDO regulator U3 is not installed because the ADMV8052 has a built-in LDO regulator for that supply voltage. The other two on-board LDO regulators, U2 and U5, provide the necessary supply voltages of +3.3 V and −2.5 V, respectively. If desired, these two LDO regulators can be bypassed by removing the 0 Ω resistors (R23 and R32) from the ADMV8052-EVALZ and then by applying each voltage independently by using the corresponding test points. Bypassing the on-board regulators is useful for measuring the ADMV8052 supply current, but it must be noted that each supply pin is also connected to status indicator LEDs, DS1 to DS3, and each LED draws approximately 2 mA of current. Remove the R2, R3, and R91 resistors to disable these status indicators. See Figure 11 and Figure 12 for more details.

PLUG-IN SPI REGISTER CONTROLLER

The ADMV8052 plug-in utilizes an SPI register controller to communicate with the ADMV8052. When using the ADMV8052 in a system, it is recommended to follow a similar methodology for implementing SPI communication. The following is a summary of the SPI register controller:

1. Determine if Register 0x000 is not set to 0x3C.
2. If Step 1 is true, set Register 0x000 to 0x3C to enable the SDO pin on the ADMV8052 and to allow SPI streaming with Endian register ascending order.
3. Determine if the values have changed for any of the WRx registers (Register 0x020 to Register 0x02F).
4. If Step 3 is true, write Register 0x020 to Register 0x02F by pointing to Register 0x020 and streaming out 16 bytes of data. The transaction is 144 bits in total (R/W bit + 15 address bits + 128 data bits). Streaming out the data in this order ensures that the switch position priority is WR0 to WR3.
5. If Step 4 has occurred, write dummy data to Address 0x0A. Note that Address 0x0A does not exist in the ADMV8052, and the written dummy data is ignored. This step is microcontroller architecture dependent and can be ignored in most cases. It is necessary for the SDP-S to clear the SPI bus and reconfigure for a standard 24-bit SPI transaction.
6. Determine if the values have changed for any of the LUT registers (Register 0x100 to Register 0x2FF).
7. If Step 6 is true, write to Register 0x100 to Register 0x2FF by performing the following:
    - Pointing to Register 0x100 and streaming out 64 bytes of data.
    - Pointing to Register 0x140 and streaming out 64 bytes of data.
    - Pointing to Register 0x180 and streaming out 64 bytes of data.
    - Pointing to Register 0x1C0 and streaming out 64 bytes of data.
    - Pointing to Register 0x200 and streaming out 64 bytes of data.
    - Pointing to Register 0x240 and streaming out 64 bytes of data.
    - Pointing to Register 0x280 and streaming out 64 bytes of data.
    - Pointing to Register 0x2C0 and streaming out 64 bytes of data.
8. If Step 7 has occurred, repeat Step 5.
9. Write out any remaining registers that may have changed.

EVALUATION BOARD SCHEMATICS AND ARTWORK

ADMV8052-EVALZ

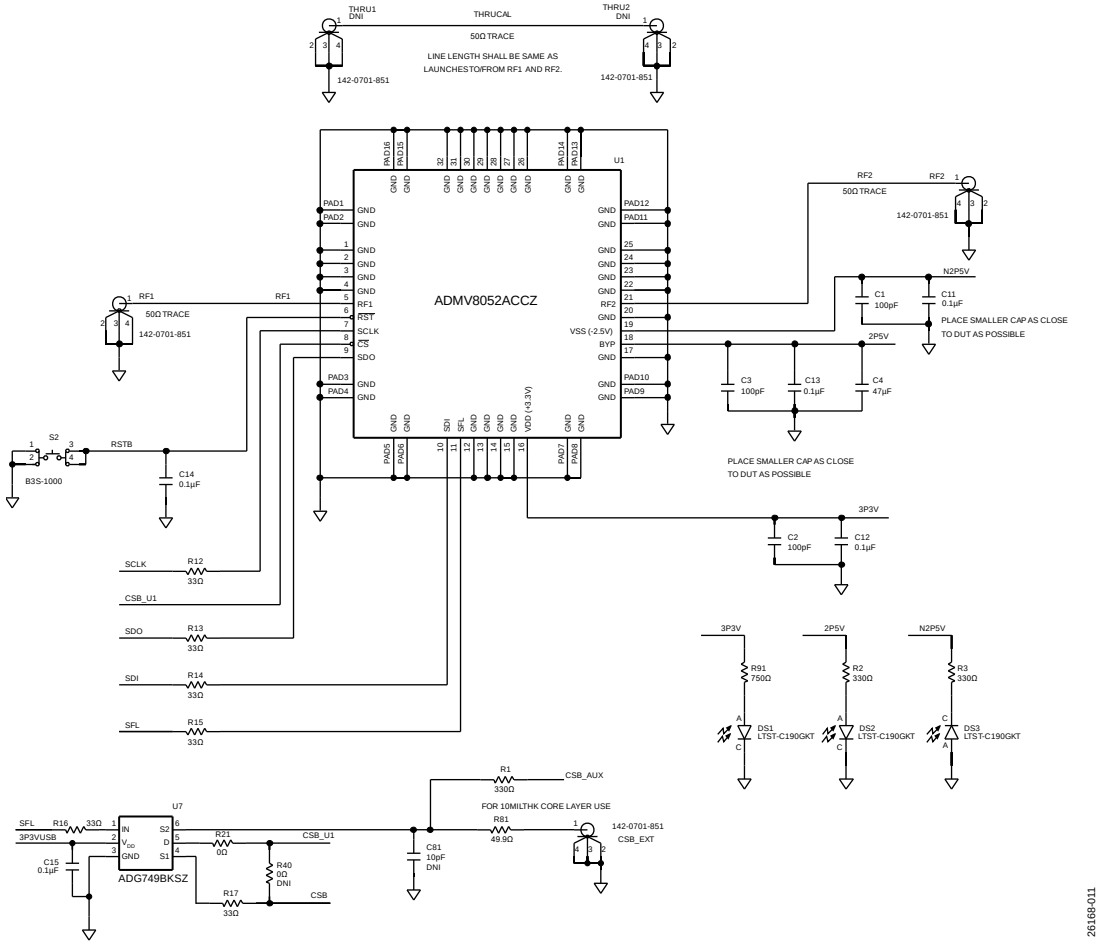


Figure 11. ADMV8052-EVALZ Schematic, Page 1

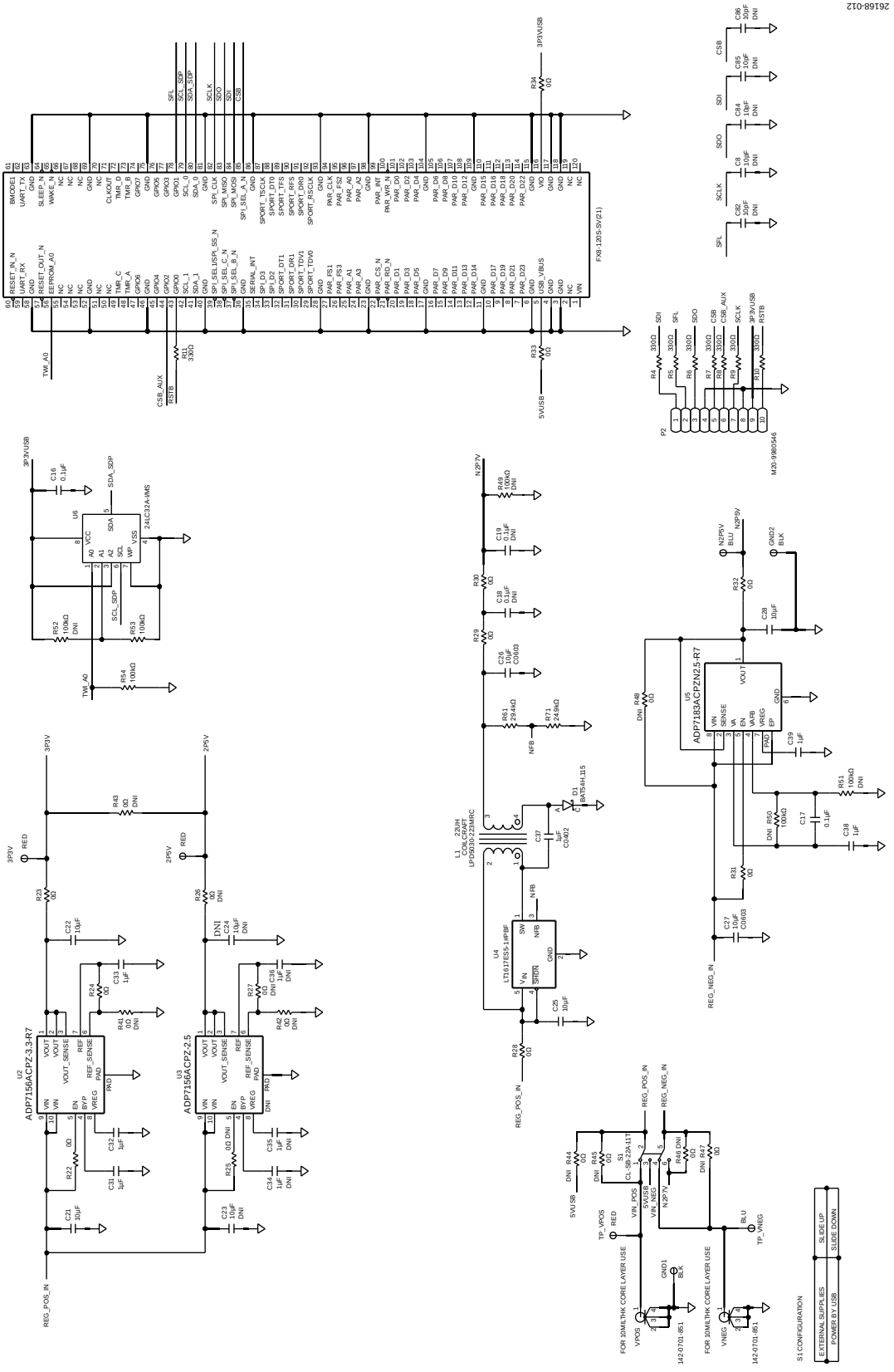


Figure 12. ADMV8052-EVALZ Schematic, Page 2

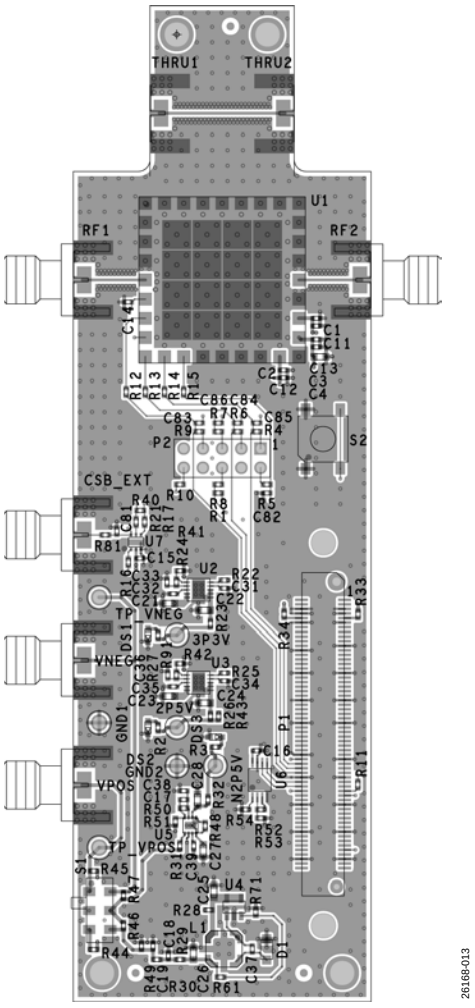


Figure 13. ADMV8052-EVALZ Layer 1

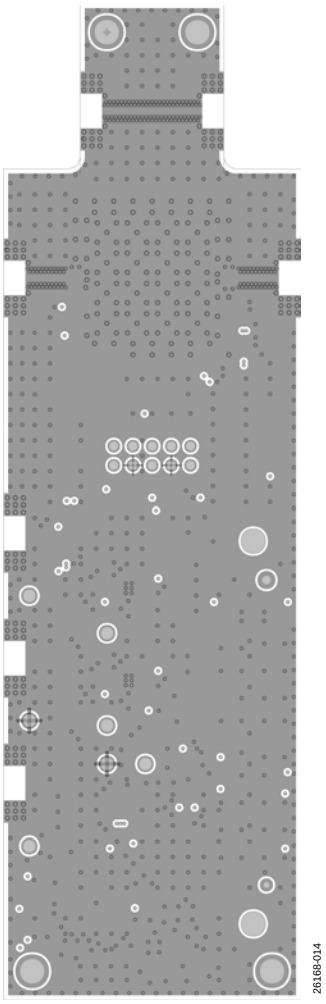


Figure 14. ADMV8052-EVALZ Layer 2

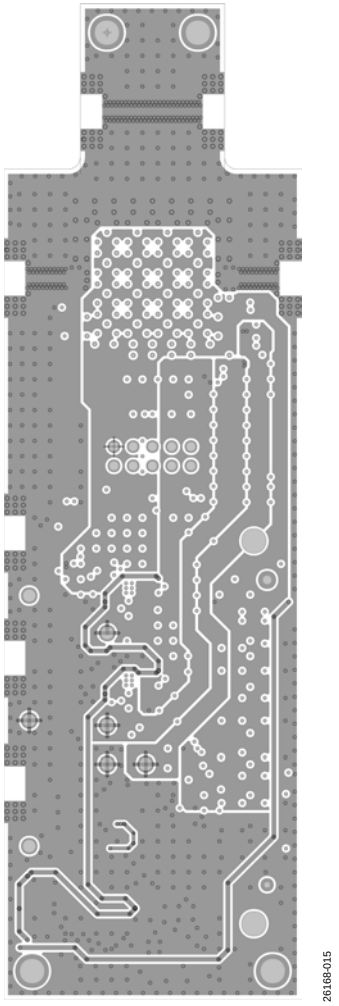


Figure 15. ADMV8052-EVALZ Layer 3

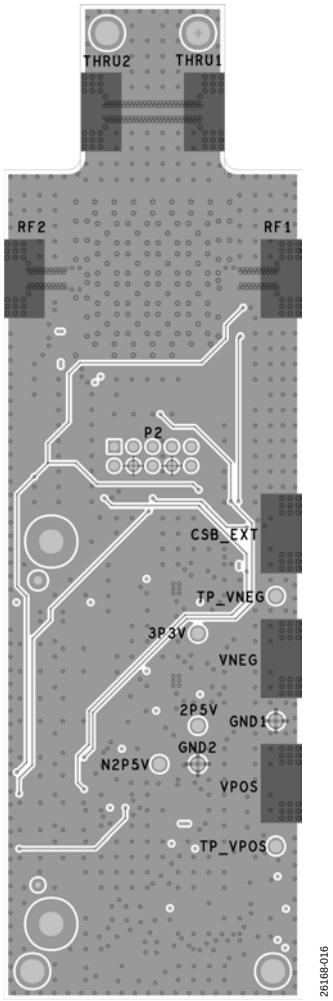


Figure 16. ADMV8052-EVALZ Layer 4

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. ADMV8052-EVALZ

Qty.	Reference Designator	Description	Manufacturer	Part Number
3	2P5V, 3P3V, TP_VPOS	Test points, red	Components Corporation	TP-104-01-02
2	GND1, GND2	Test points, black	Components Corporation	TP-104-01-00
2	N2P5V, TP_VNEG	Test points, blue	Components Corporation	TP-104-01-06
5	CSB_EXT, RF1, RF2, VNEG, VPOS	Connectors, edge launch, SMA	Cinch Connectivity	142-0701-851
3	C1 to C3	Capacitors, 100 pF, 50 V, 5%, 0402	Johanson Dielectrics	500R07N101JV4T
7	C11 to C17	Capacitors, 0.1 µF, 16 V, 5%, 0402	Kemet	C0402C104J4RACTU
6	C21, C22, C25 to C28	Capacitors, 10 µF, 16 V, 10%, 0603	Murata	GRM188R61C106KAALD
6	C31 to C33, C37 to C39	Capacitors, 1 µF, 16 V, 20%, 0402	Murata	GRM155R61C105MA12D
1	C4	Capacitor, 47 µF, 6.3 V, 20%, 0603	Murata	GRM188R60J476ME15D
1	D1	Diode, BAT54H, 30 V, SOD123F	NXP Semiconductor	BAT54H,115
3	DS1 to DS3	LED, LTST-C190GKT, green, 0603	Lite-On Technology	LTST-C190GKT
1	L1	Coupled inductor, 22 µH, 20%	Coilcraft	LPD5030-223MRC
1	P1	Connector, vertical, surface-mount technology (SMT), 120-pin	Hirose Electric Co.	FX8-120S-SV(21)
1	P2	Connector, vertical, header, 10-pin	Harwin, Inc.	M20-9980546
11	R1 to R11	Resistors, 330 Ω, 1/10 W, 5%, 0402	Panasonic	ERJ-2GEJ331X
6	R12 to R17	Resistors, 33 Ω, 1/10 W, 1/%, 0402	Panasonic	ERJ-2RKF33R0X
11	R21 to R24, R28 to R34	Resistors, 0 Ω, 1/16 W, 0402	Stackpole	RMCF0402ZT0R00
2	R53, R54	Resistors, 100 kΩ, 1/16 W, 5%, 0402	Yageo	RC0402JR-07100KL
1	R61	Resistor, 29.4 kΩ, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF2942X
1	R71	Resistor, 24.9 kΩ, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF2492X
1	R81	Resistor, 49.9 Ω, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF49R9X
1	R91	Resistor, 750 Ω, 1/10 W, 5%, 0402	Panasonic	ERJ-2GEJ751X
1	S1	Switch, mechanical, slide, DPDT, 0.2 A	Nidec Copal Electronics	CL-SB-22A-11T
1	S2	Switch, mechanical, push button	Omron Electronics Inc.	B3S1000
1	U1	30 MHz to 520 MHz, digitally tunable BPF	Analog Devices	ADMV8052ACCZ
1	U2	1.2 A, ultralow noise, high power supply rejection ratio (PSRR), fixed output, RF linear regulator, 3.3 V	Analog Devices	ADP7156ACPZ-3.3-R7
1	U4	Micropower inverting dc-to-dc converter	Analog Devices	LT1617ES5-1#PBF
1	U5	−300 mA, ultralow noise, high PSRR, low dropout linear regulator, −2.5 V	Analog Devices	ADP7183ACPZN2.5-R7
1	U6	IC, 24LC32A, EEPROM, I^2C	Microchip Technology	24LC32A-I/MS
1	U7	CMOS, 1.8 V to 5.5 V, 2.5 Ω, 2:1 mux/SPDT switch in SC70 package	Analog Devices	ADG749BKSZ
2	C18, C19	Capacitors, 0.1 µF, 16 V, 5%, 0402, do not install (DNI)	Kemet	C0402C104J4RACTU
2	C23, C24	Capacitors, 10 µF, 16 V, 10%, 0603, DNI	Murata	GRM188R61C106KAALD
3	C34 to C36	Capacitors, 1 µF, 16 V, 20%, 0402, DNI	Murata	GRM155R61C105MA12D
6	C81 to C86	Capacitor, 10 pF, 50 V, 5%, 0402, DNI	Yageo	CC0402JRNPO9BN100
12	R25 to R27, R40 to R48	Resistors, 0 Ω, 1/16 W, 0402, DNI	Stackpole	RMCF0402ZT0R00
4	R49 to R52	Resistors, 100 kΩ, 1/16 W, 5%, 0402, DNI	Yageo	RC0402JR-07100KL
1	U3	1.2 A, ultralow noise, high PSRR, fixed output, RF linear regulator, 2.5 V, DNI	Analog Devices	ADP7156ACPZ-2.5-R7
2	THRU1, THRU2	Connectors, edge launch, SMA, DNI	Cinch Connectivity	142-0701-851

NOTES

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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