Evaluating the ADMV1355 17.7GHz to 55GHz, Wideband, Microwave Upconverter

FEATURES

- Fully featured evaluation board for the ADMV1355
- On-board EVAL-SDP-CS1Z (SDP-S) connector for the SPI
- Evaluation using on-board power regulators powered by the USB
- Analog Devices, Inc., **Analysis | Control | Evaluation (ACE) Software** interface for SPI control

EQUIPMENT NEEDED

- Network analyzer
- 50Ω coax cables
- Windows® PC
- USB cable
- SDP-S controller board
- 5V USB-C adapter or power supply

DOCUMENTS NEEDED

- ADMV1355 data sheet

SOFTWARE NEEDED

- **ACE Software**

GENERAL DESCRIPTION

The ADMV1355-EVALZ is available for evaluating the ADMV1355 wideband microwave upconverter. The ADMV1355-EVALZ incorporates the ADMV1355 chip, as well as a power regulator and an interface to the EVAL-SDP-CS1Z (SDP-S) system demonstration platform (SDP) controller board to allow simple and efficient evaluation. The power regulator allows the ADMV1355 to be powered by a 5V USB-C adapter or by using a 5V external power supply.

The ADMV1355 is a highly integrated wideband, microwave upconverter for wideband radio designs operating in the 17.7GHz to 55GHz frequency range. The chip can be programmed using a 4-wire serial peripheral interface (SPI). The SDP-S controller board allows the user to interface with the ADMV1355 SPI through the **ACE Software**.

For full details on the ADMV1355, see the ADMV1355 data sheet, which must be consulted in conjunction with this user guide when using the ADMV1355-EVALZ.

EVALUATION BOARD PHOTOGRAPH

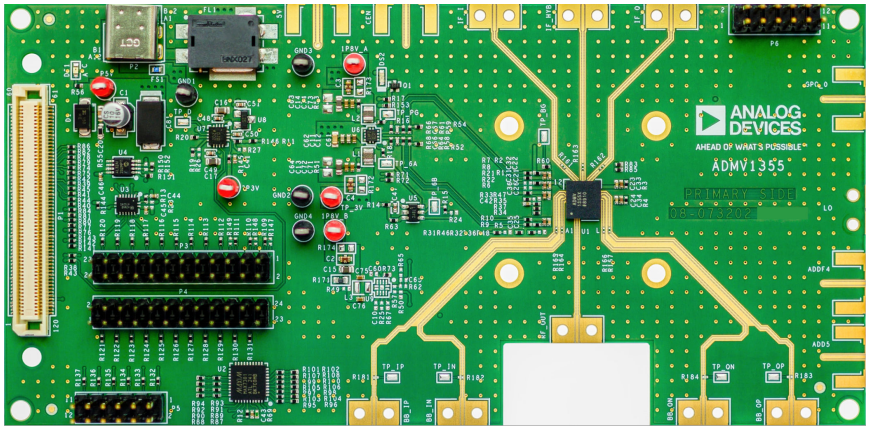

Figure 1. ADMV1355-EVALZ Evaluation Board Photograph

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REVISION HISTORY

4/2026—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADMV1355-EVALZ has the ADMV1355 chip on board and a power regulator to provide the necessary supply voltages for the chip. The power regulator can be entirely powered using a 5V USB-C adapter.

To power the ADMV1355-EVALZ, connect a 5V USB-C adapter to the P2 connector. Alternatively, the ADMV1355-EVALZ can be powered by connecting a 5V power supply to the P5V test point. The applicable input voltage range is between 3.5V and 5.5V.

Figure 2 shows an example lab bench setup for the ADMV1355-EVALZ. To observe the upconverter response from the ADMV1355-EVALZ, connect the IF_HYB, RF_OUT, and LO ports to a network analyzer (or similar instrument) using 50Ω coax cables. Typically, IF_HYB is connected to Port 1, RF_OUT is connected to Port 2, and LO is connected to Port 3 on the network analyzer, as shown in Figure 2.

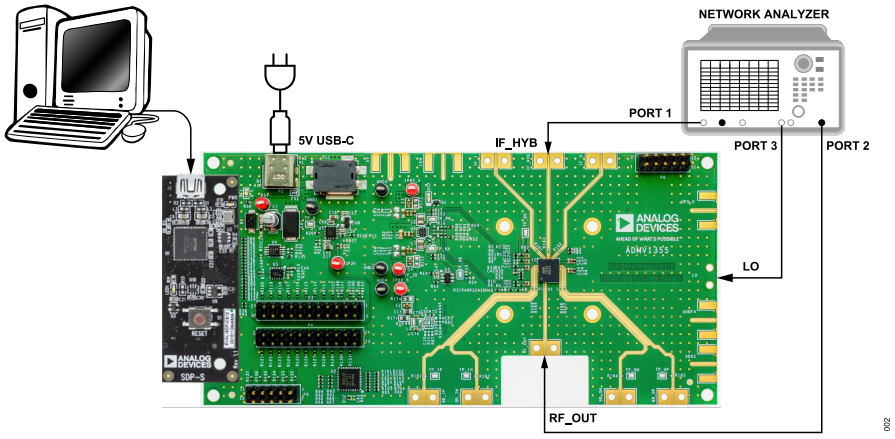

Figure 2. Lab Bench Setup for the ADMV1355-EVALZ

EVALUATION BOARD SOFTWARE

ACE SOFTWARE OVERVIEW

The **ACE Software** provides a simple tutorial for testing the ADMV1355. For more customized and detailed implementations, refer to the ADMV1355 data sheet for a full description of the functionality, registers, and corresponding settings.

INSTALLING THE ACE SOFTWARE AND DRIVERS

The ADMV1355-EVALZ uses the **ACE Software**. For instructions on how to install and use the **ACE Software**, go to the **ACE Software** page.

If the **ACE Software** is already installed on the PC, ensure that the installed software is the latest version, as shown on the **ACE Software** page. If the installed software is not the latest version, take the following steps to install the updated **ACE Software**:

1. Uninstall the current version of the **ACE Software** on the PC.
2. Delete the ACE folder found in **C:\ProgramData\Analog Devices** and **C:\Program Files (x86)\Analog Devices**.
3. Install the latest version of the **ACE Software** from the **ACE Software** page. During installation, ensure that the **SDP Drivers**, **LRF Drivers**, and **.NET 4.8** components are selected (see Figure 3).

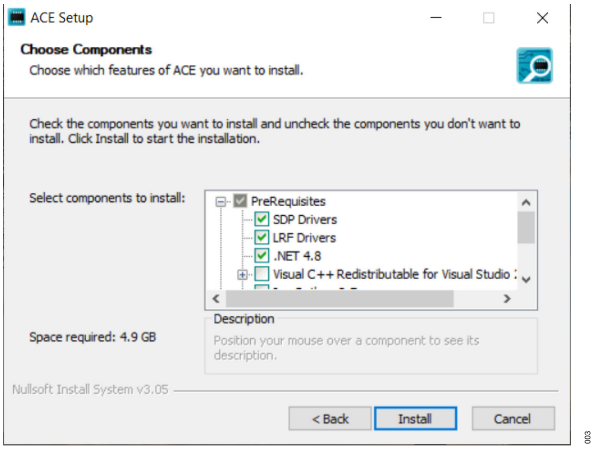

Figure 3. Required Driver Installations with the ACE Software

INSTALLING THE PLUG-INS

Install the ADMV1355 plug-in by doing one of the following:

- Open the **ACE Software** and then use the **Plug in Manager** within to install the ADMV1355 plug-in.
- Download the **ACEZIP** file from https://www.analog.com/ace. Double-click the ADMV1355 file, which then automatically opens the **ACE Software** and installs the plug-in.

Once the ADMV1355 plug-in is installed and the ADMV1355-EVALZ is connected to the PC, the **ADMV1355 Board** plug-in appears in the **Attached Hardware** section of the **Start** tab when the **ACE Software** is running (see Figure 4). Double click the **ADMV1355 Board** to open the plug-in.

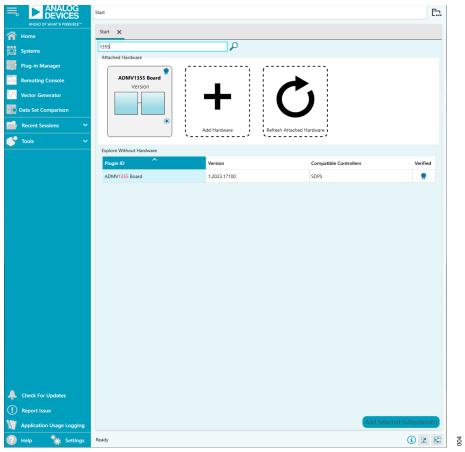

Figure 4. ADMV1355 Board Plug-In Window After Opening the ACE Software

EVALUATION BOARD SOFTWARE

BOARD PLUG-IN OVERVIEW

The **ADMV1355 Board** plug-in view (see Figure 5) includes the following features (see Figure 7 and Table 1 for additional information on these items):

- The **SDP-S** configuration block for setting the SDP-S logic general-purpose inputs and outputs (GPIOs).
- The **Supply Adjust** section for setting the supply voltages by using the **AD5686R** digital-to-analog converter (DAC).
- The **MAX7301** GPO expander for setting the logic state of the ADD_F and ADD_G balls of the ADMV1355 .
- The **ADMV1355** chip for opening the chip plug-in.

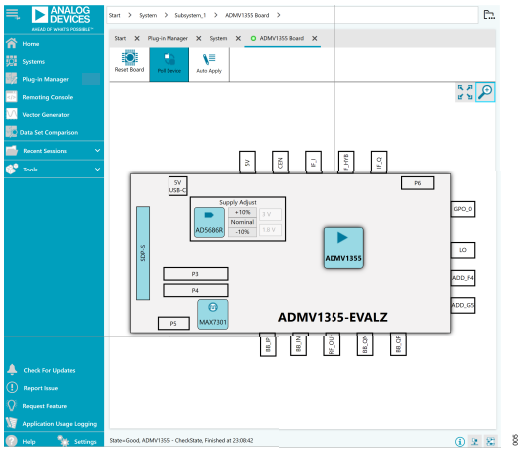

Figure 5. ADMV1355 Board Plug-In View

CHIP PLUG-IN OVERVIEW

The **ADMV1355** chip plug-in view (see Figure 6) includes the following features (see Figure 11 and Table 2 for additional information on these items):

- **Sequences** for configuring the chip to a predefined state
- A signal chain block diagram
- User controls for adjusting chip parameters
- Subdiagram navigation for opening various subdiagrams that allow additional chip configuration

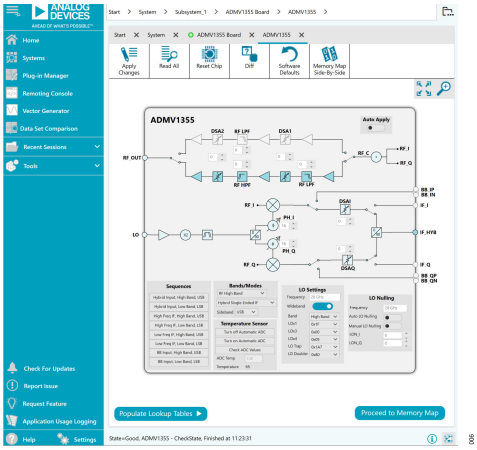

Figure 6. ADMV1355 Chip Plug-In

EVALUATION BOARD SOFTWARE

BOARD PLUG-IN DETAILS

The full screen **ADMV1355 Board** plug-in with labels is shown in Figure 7, and the labels correspond to the items listed in Table 1 that describes the functionality of each section.

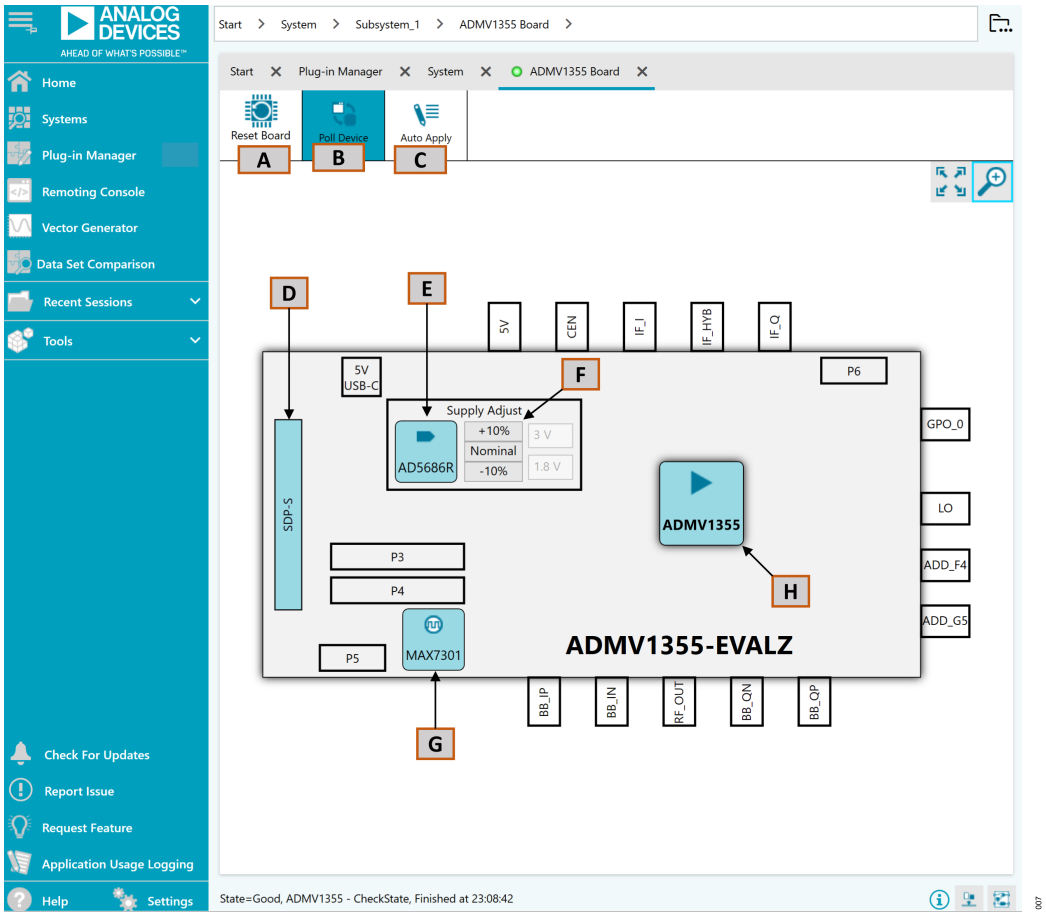

Figure 7. ADMV1355 Board Plug-In with Labels

Table 1. ADMV1355 Board Block Diagram Label Functions (See Figure 7)

Label	Function
A	Click **Reset Board** to reset the board. **Reset Board** performs the sequence detailed in the Reset Board Sequence section.
B	The **Poll Device** feature is enabled by default and queries the ADMV1355-EVALZ every one second to verify it is still connected to the PC. Click this button to disable this feature.
C	When the **Auto Apply** feature is enabled, the **ADMV1355** chip apply changes sequence runs every few seconds, and the **Apply Changes** button does not need to be clicked to apply the block diagram settings (see Figure 6).
D	Click the **SDP-S** block for a window to open that allows configuring of the logic GPIOs on the SDP-S. The GPIOs enable the power solution and set the state of various logic signals on the ADMV1355-EVALZ. Figure 8 shows the logic signals that can be controlled on the ADMV1355-EVALZ.
E	Double-click to open the **AD5686R** chip plug-in that can be used to configure the AD5686R DAC on the ADMV1355-EVALZ. This DAC allows for trimming of the on-board power solution up to ±10%. Figure 9 shows the **AD5686R** chip plug-in.
F	Use the buttons in the **Supply Adjust** section to quickly configure the AD5686R for **+10%**, **Nominal**, or **−10%** voltages.
G	Double-click to open the **MAX7301** chip plug-in that can be used to configure the MAX7301 I/O expander on the ADMV1355-EVALZ. The I/O expander allows for setting the logic state of the ADMV1355 ADD_F balls and ADD_G balls. Figure 10 shows the **MAX7301** chip plug-in.
H	Double-click to open the **ADMV1355** chip diagram.

EVALUATION BOARD SOFTWARE

Reset Board Sequence

The **ACE Software** reset board sequence for the **ADMV1355 Board** plug-in follows:

1. Bring all SDP-S controller board GPIO pins low (also see Figure 8).
2. Pause for 100ms.
3. Set PS_EN high on the SDP-S to enable the power solution.
4. Pause for 100ms.
5. Set DAC_RSTB high on the SDP-S to bring the AD5686R out of reset.
6. Pause for 100ms.
7. Run the AD5686R reset sequence.
8. Pause for 100ms.
9. Run the MAX7301 reset sequence.
10. Pause for 100ms.
11. Set DUT_RSTB high on the SDP-S to bring the ADMV1355 out of reset.
12. Pause for 100ms.
13. Set DUT_CEN high on the SDP-S to enable and fully power the ADMV1355.
14. Pause for 100ms.
15. Run the ADMV1355 reset sequence.
16. Pause for 100ms.
17. Run the ADMV1355 sequence for IF mode, RF high band, and upper sideband.
18. Set the board level initialization flag high.

During testing of the ADMV1355-EVALZ, it was found that the voltage from some bench supplies can drop when the power solution requires an inrush current. Some types of supplies, such as source and measure units (SMUs), can experience a drop in voltage by up to 50ms before the supplies recover.

The 100ms pauses in the previous sequence are used as a conservative approach to allow any bench supply time for the voltage to settle. In a practical system with good supply regulation, these pauses are not required.

SDP-S, AD5686R, and MAX7301 Subviews

See Table 1 for additional details on the Figure 8, Figure 9, and Figure 10 windows.

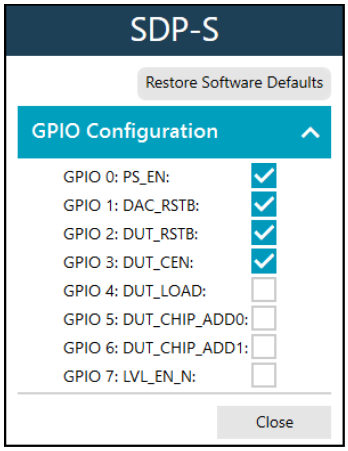

Figure 8. SDP-S Block

EVALUATION BOARD SOFTWARE

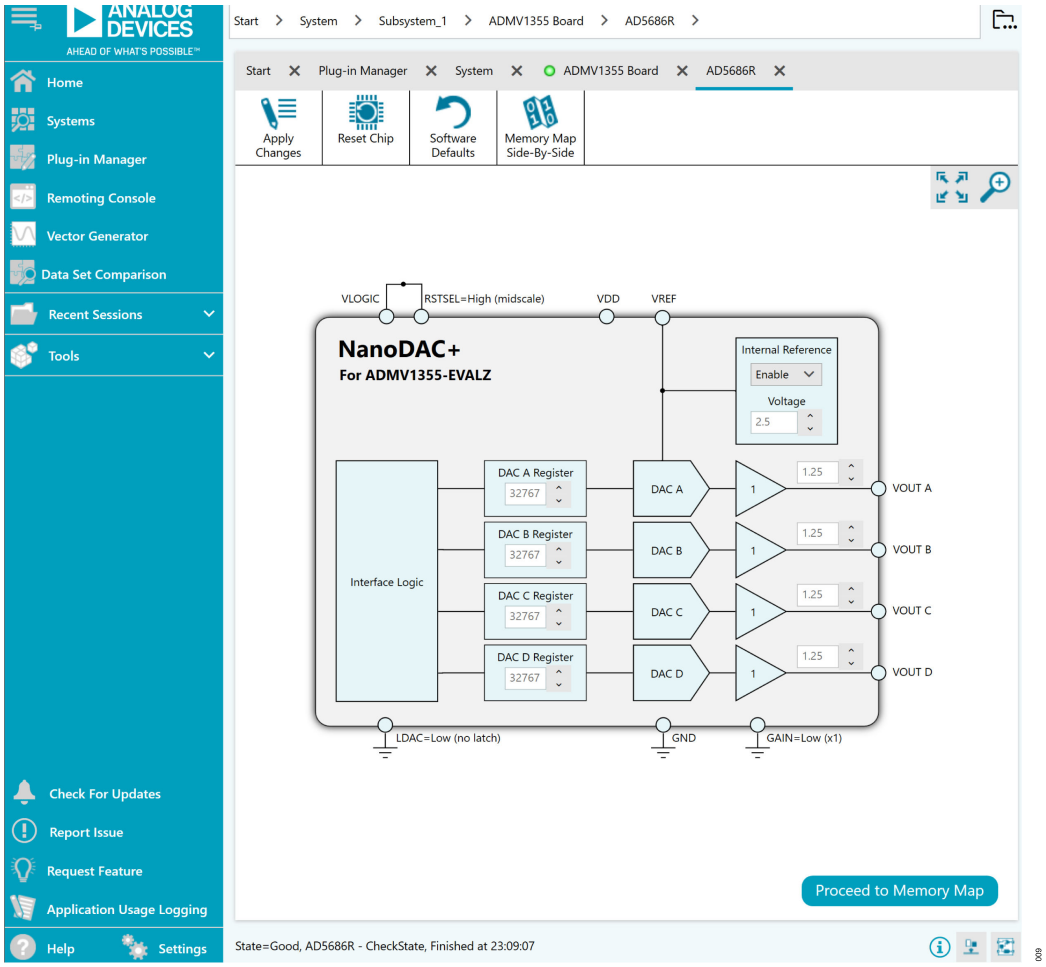

Figure 9. AD5686R Chip Plug-in

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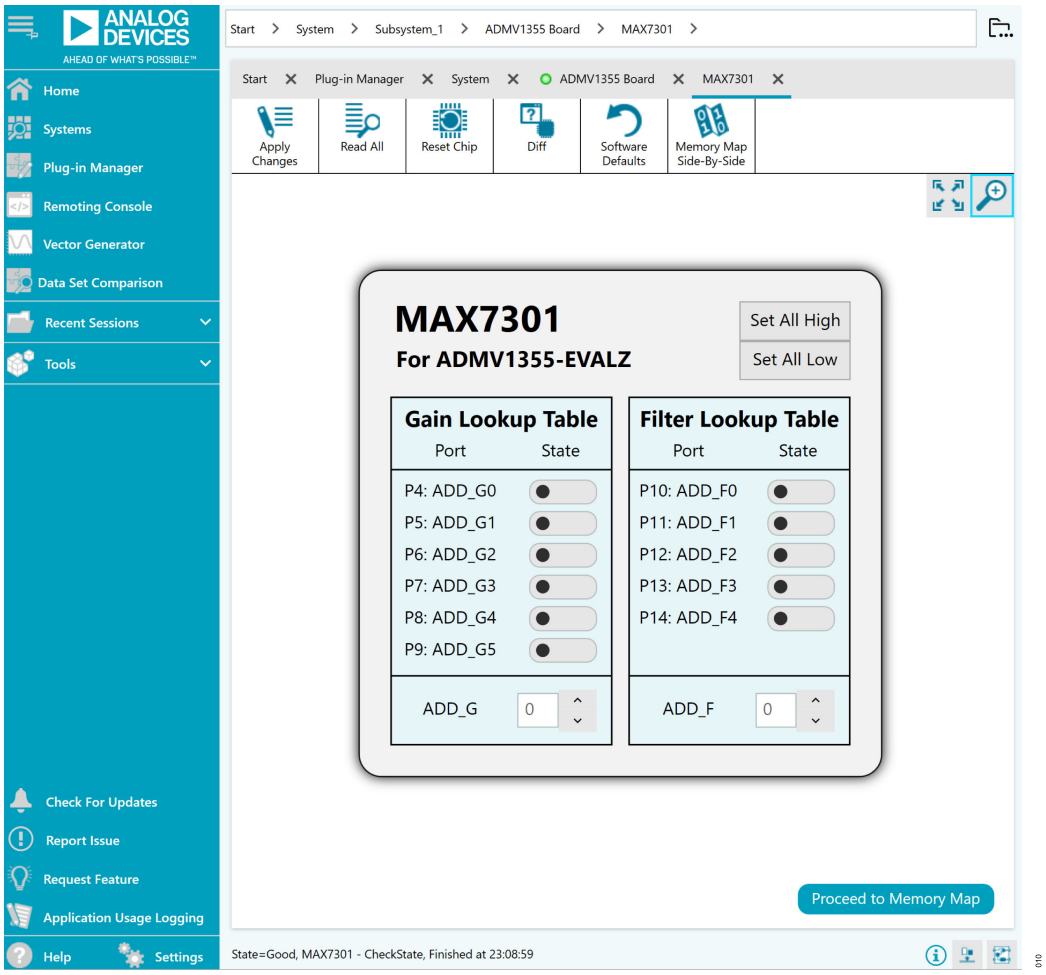

Figure 10. MAX7301 Chip Plug-in

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CHIP PLUG-IN DETAILS

The full screen **ADMV1355** chip plug-in with labels is shown in Figure 11, and the labels correspond to the items listed in Table 2, which describe the functionality of each section.

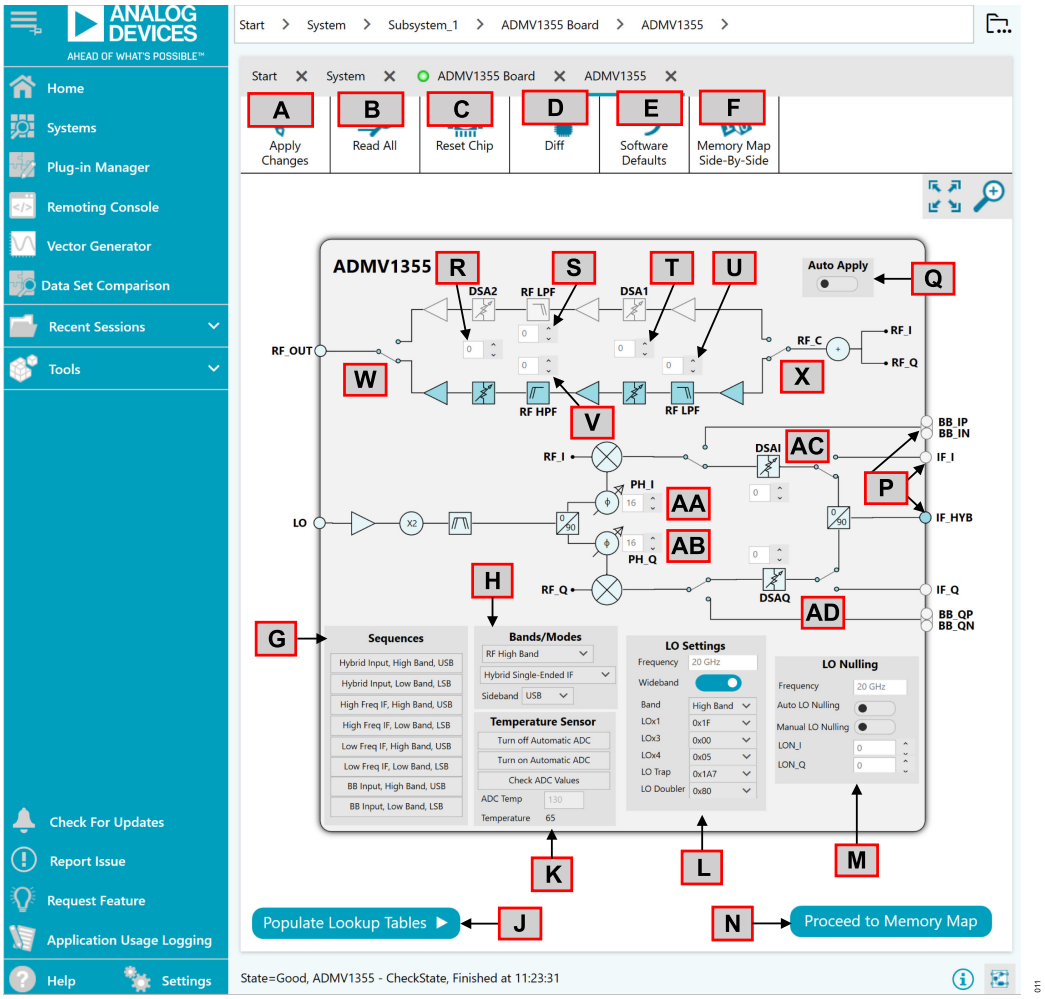

Figure 11. ADMV1355 Chip Plug-In with Labels

Table 2. ADMV1355 Block Diagram Label Functions (See Figure 11)

Label	Function
A	All block diagram and register map changes do not take effect until **Apply Changes** is clicked. If **Auto Apply** is highlighted in the **ADMV1355 Board** tab (see Figure 5) or the **Auto Apply** slider (Label Q) is enabled, the **Apply Changes** feature runs every few seconds, and the**Apply Changes** button does not need to be clicked to apply the block diagram settings.
B	Click **Read All** to read back all the SPI registers of the chip.
C	Click **Reset Chip** to reset the chip. **Reset Chip** writes Register 0x000 to value 0x81 to perform a soft reset, then Register 0x000 is set to value 0x18 to enable the SDO ball. After the SDO ball is enabled, the **Reset Chip** programs the NVM load instructions and performs a NVM health check, followed by a read back of the SPI registers of the chip. If the NVM health check does not return expected values, a caution message appears on ADMV1355 chip plug-in diagram.
D	Click **Diff** to show registers that are different on the chip. In Figure 15, the registers that are bold indicate hardware values that are different than the software values.
E	Click **Software Defaults** to restore the register map to the software defaults for the chip.
F	Click **Memory Map Side-By-Side** to enable the side-by-side memory map view.

EVALUATION BOARD SOFTWARE

Table 2. ADMV1355 Block Diagram Label Functions (See Figure 11) (Continued)

Label	Function
G	Select one of the **Sequences** to configure the chip to a predefined state. The sequences configure the ADMV1355 for wideband LO filter settings and an 8GHz IF_HYB or high and low frequency complex IF inputs or baseband inputs. The Chip Plug-In Sequences section contains the list of register settings that are programmed by each sequence.
H	Use the dropdown menus in the **Bands/Modes** section to select the desired RF band, the desired input configuration, and the desired sideband selection.
J	Click **Populate Lookup Tables** to navigate through the subviews, starting with the **Populate Lockup Tables** subview (see Figure 12). Additional subviews include the **Lookup Table Settings** (see Figure 13) and the **General Purpose Outputs** (see Figure 14).
K	Use the **Temperature Sensor** section to **Turn On Automatic ADC** or **Turn Off the Automatic ADC** and read back the ADC values. The estimated chip temperature is shown when the **ADC Temp** value is read back.
L	Use the **LO Settings** to configure the LO band and the LO tunable filters. The two primary inputs are the **Frequency** textbox and the **Wideband** slider button. Type in the desired LO frequency into the **Frequency** textbox, and slide the **Wideband** slider button to the left for narrow-band filter settings and slide the **Wideband** slider button to the right for wideband filter settings. The other LO settings are determined automatically based upon these inputs and the ADMV1355 data sheet recommended values.
M	Use the **LO Nulling** section to null the LO feedthrough. The primary input is the **Frequency** textbox. Type in the desired LO frequency into the **Frequency** textbox and enable the **Auto LO Nulling** or **Manual LO Nulling** feature. In the **Manual LO Nulling** setting, use the **LON_I** and **LON_Q** textboxes to set the I and Q offsets manually.
N	Click **Proceed to Memory Map** to open the **ADMV1355 Memory Map** (see Figure 15).
P	To change the input mode, click any of the input balls on the diagram. The input balls are highlighted in blue when they are enabled.
Q	Use the **Auto Apply** slider to enable or disable the **Auto Apply** feature. When enabled, the **Apply Changes** feature runs every few seconds, and the **Apply Changes** button does not need to be clicked to apply the block diagram settings.
R	Use the **DSA2** arrows to scroll up or down to adjust the gain (0dB to 15dB) of the DSA. A value of 0 corresponds to maximum gain, and a value of 15 corresponds to minimum gain.
S	Use the **RF LPF** arrows to scroll up or down to adjust the low band RF tunable low-pass filter (LPF). The cutoff frequency is inversely proportional to the value programmed.
T	Use the **DSA1** arrows to scroll up or down to adjust the gain (0dB to 15dB) of the DSA. A value of 0 corresponds to maximum gain, and a value of 15 corresponds to minimum gain.
U	Use the **RF LPF** arrows to scroll up or down to adjust the high band RF tunable low-pass filter (LPF). The cutoff frequency is inversely proportional to the value programmed.
V	Use the **RF HPF** arrows to scroll up or down to adjust the high band RF tunable high-pass filter (HPF). The cutoff frequency is inversely proportional to the value programmed.
W and X	Toggle the switches to select either the RF high band or RF low band signal chain.
AA	Use the **PH_I** arrows to scroll up or down to adjust the phase of 2×LO_I (0 to 31). Use this feature to achieve good quadrature for sideband rejection optimization.
AB	Use the **PH_Q** arrows to scroll up or down to adjust the of 2×LO_Q (0 to 31). Use this feature to achieve good quadrature for sideband rejection optimization.
AC	Use the **DSAI** arrows to scroll up or down to adjust the amplitude of IF_I (0 to 15). Use this feature to achieve good amplitude imbalance for sideband rejection optimization.
AD	Use the **DSAQ** arrows to scroll up or down to adjust the amplitude of IF_Q (0 to 15). Use this feature to achieve good amplitude imbalance for sideband rejection optimization.

For additional detailed programming, refer to the ADMV1355 data sheet.

EVALUATION BOARD SOFTWARE

Chip Plug-In Sequences

The ADMV1355 chip plug-in contains eight sequences (see Table 3 and Table 4) that configure the chip for wideband LO filter settings. The configurations include four different input modes (IF hybrid, complex IF low frequency, complex IF high frequency and I/Q baseband) and both RF bands.. The RF low-band sequences configure the chip for lower sideband, and the RF high-band sequences configure the chip for upper sideband. These recommended settings can be considered the minimum requirements for configuring the ADMV1355. Additional features can be configured, and all settings can be tailored for a particular end application. Refer to the Theory of Operation section of the ADMV1355 data sheet for additional information.

Table 3. Recommended Settings for IF Hybrid Mode and I/Q Baseband Mode

	IF Hybrid Mode		I/Q Baseband Mode		
Register	RF Low Band	RF High Band	RF Low Band	RF High Band	Notes
0x000	0x18	0x18	0x18	0x18	Enables the SDO output.
0x13E	0x02	0x02	0x02	0x02	Configures the power downs.
0x202	0x00	0x00	0x00	0x00	Disables the lookup table (LUT) of the filter.
0x208	0x00	0x00	0x00	0x00	Disables the load enable bit of the filter.
0x2A0	0x10	0x10	0x10	0x10	Sets the RF chain LPF to the highest cutoff frequency.
0x2A1	0xBF	0xBF	0xBF	0xBF	Sets the RF chain HPF to the lowest cutoff frequency.
0x600	0x00	0x00	0x00	0x00	Configures the maximum gain.
0x602	0x08	0x08	0x01	0x01	Sets the single-ended IF hybrid or baseband signal chain.
0x800	0x05	0x05	0x05	0x05	Configures the filters.
0x801	0x00	0x00	0x00	0x00	Configures the filters.
0x802	0x1F	0x1F	0x1F	0x1F	Configures the filters.
0x804	0xA7	0xA7	0xA7	0xA7	Configures the filters.
0x805	0x41	0xC1	0x41	0xC1	Configures the bands, LO phase, and filters.
0x806	0x90	0xF0	0x90	0xF0	Configures the LO phase and LO band.
0x80A	0x00	0x00	0x00	0x00	Configures the IF gain adjust for sideband rejection.
0x80C	0x80	0x80	0x80	0x80	Configures the filters.

Table 4. Recommended Settings for Complex IF Low Frequency Mode and Complex IF High Frequency Mode

	Complex IF Low Frequency Mode		Complex IF High Frequency Mode		
Register	RF Low Band	RF High Band	RF Low Band	RF High Band	Notes
0x000	0x18	0x18	0x18	0x18	Enables the SDO output.
0x13E	0x02	0x02	0x02	0x02	Configures the power downs.
0x202	0x00	0x00	0x00	0x00	Disable the LUT of the filter.
0x208	0x00	0x00	0x00	0x00	Disables the load enable bit of the filter.
0x2A0	0x10	0x10	0x10	0x10	Sets the RF chain LPF to the highest cutoff frequency.
0x2A1	0xBF	0xBF	0xBF	0xBF	Sets the RF chain HPF to the lowest cutoff frequency.
0x600	0x00	0x00	0x00	0x00	Configures the maximum gain.
0x602	0x02	0x02	0x04	0x04	Enables the complex IF low frequency or high frequency signal chain.
0x800	0x05	0x05	0x05	0x05	Configures the filters.
0x801	0x00	0x00	0x00	0x00	Configures the filters.
0x802	0x1F	0x1F	0x1F	0x1F	Configures the filters.
0x804	0xA7	0xA7	0xA7	0xA7	Configures the filters.
0x805	0x41	0xC1	0x41	0xC1	Configures the bands, LO phase, and filters.
0x806	0x90	0xF0	0x90	0xF0	Configures the LO phase and LO band.
0x80A	0x00	0x00	0x00	0x00	Configures the IF gain adjust for sideband rejection.
0x80C	0x80	0x80	0x80	0x80	Configures the filters.

EVALUATION BOARD SOFTWARE

ADMV1355 Chip Plug-In Subviews

See Table 2 for additional details on Figure 12, Figure 13, Figure 14, and Figure 15.

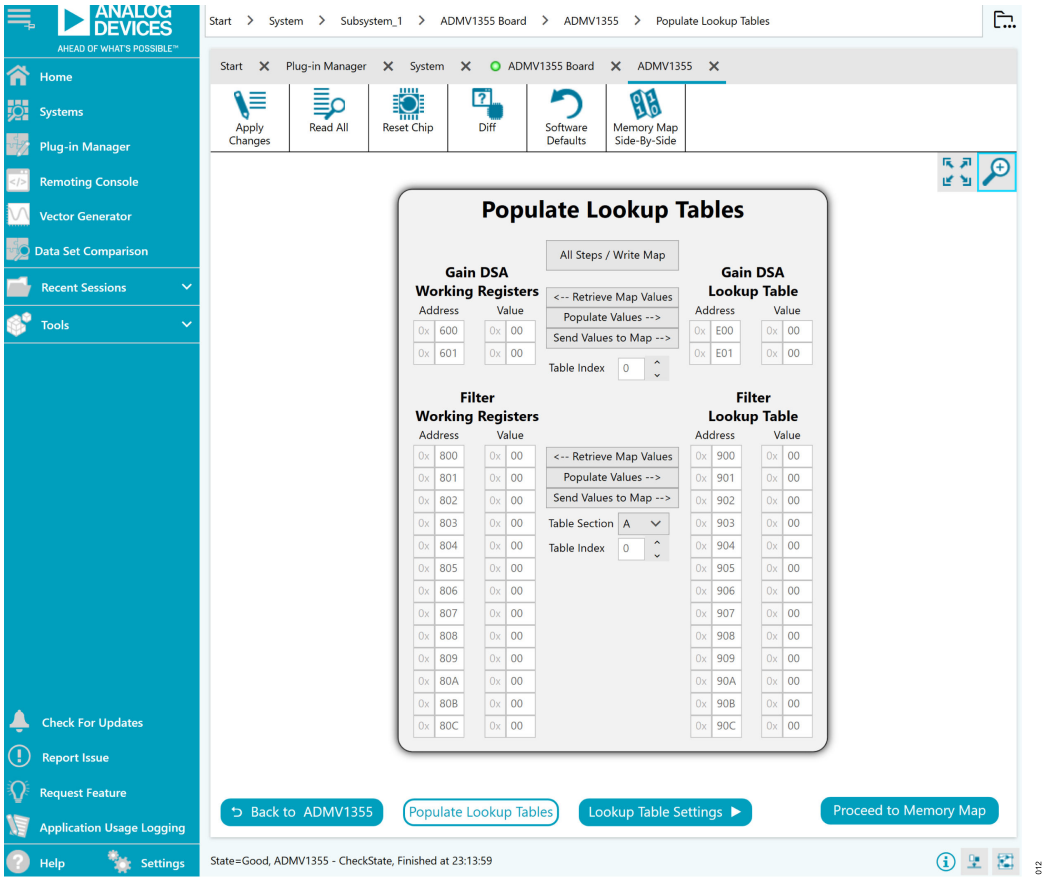

Figure 12. ADMV1355 Populate Lookup Tables Subview in the ACE Software

EVALUATION BOARD SOFTWARE

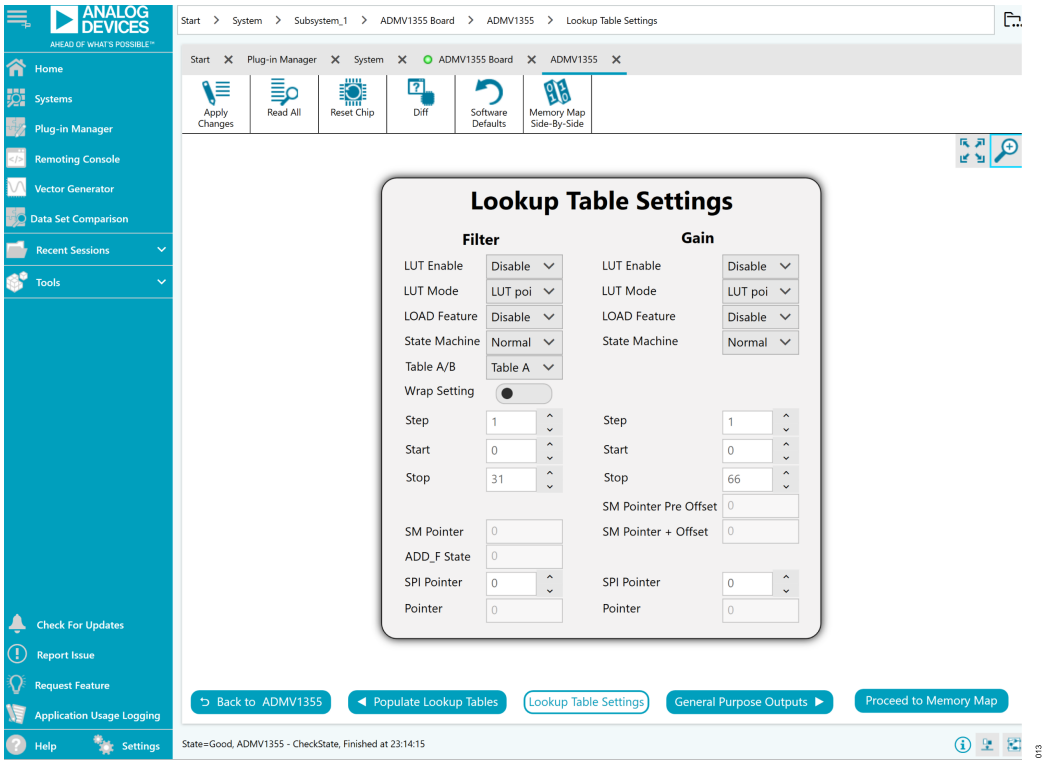

Figure 13. ADMV1355 Lookup Table Settings Subview in the ACE Software

EVALUATION BOARD SOFTWARE

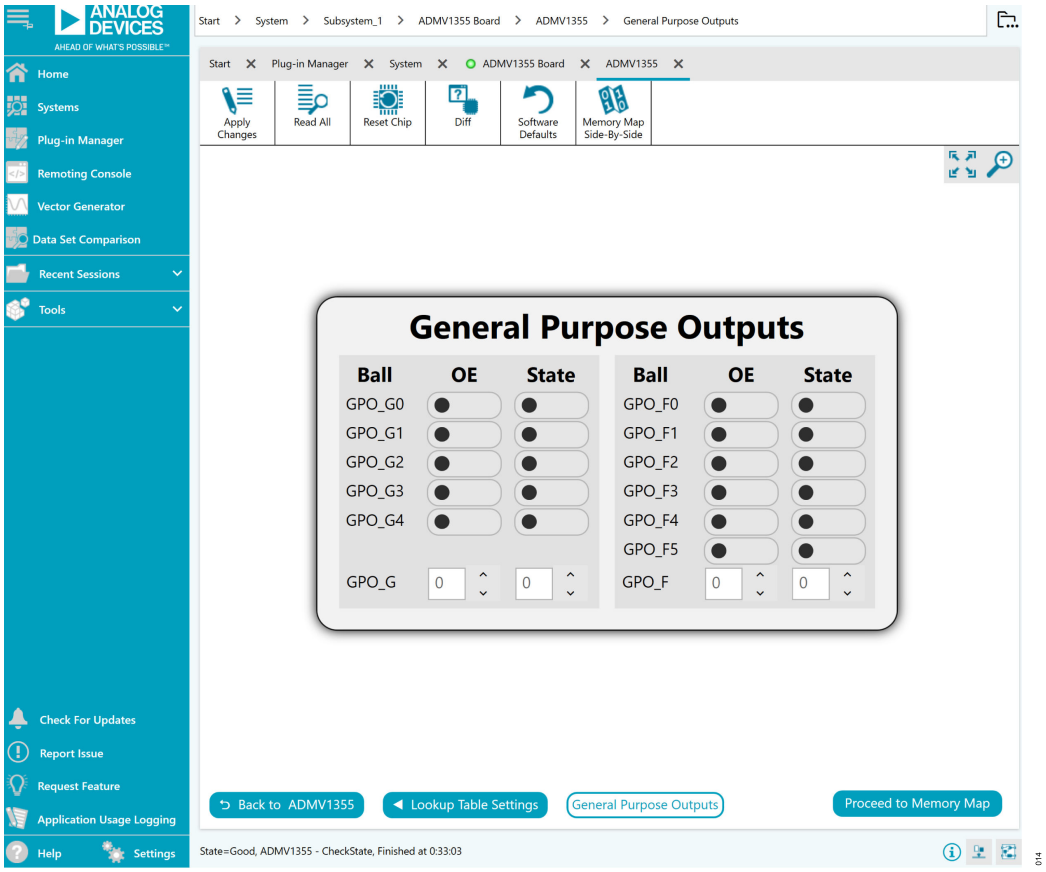

Figure 14. ADMV1355 General Purpose Outputs Subview in the ACE Software

EVALUATION BOARD SOFTWARE

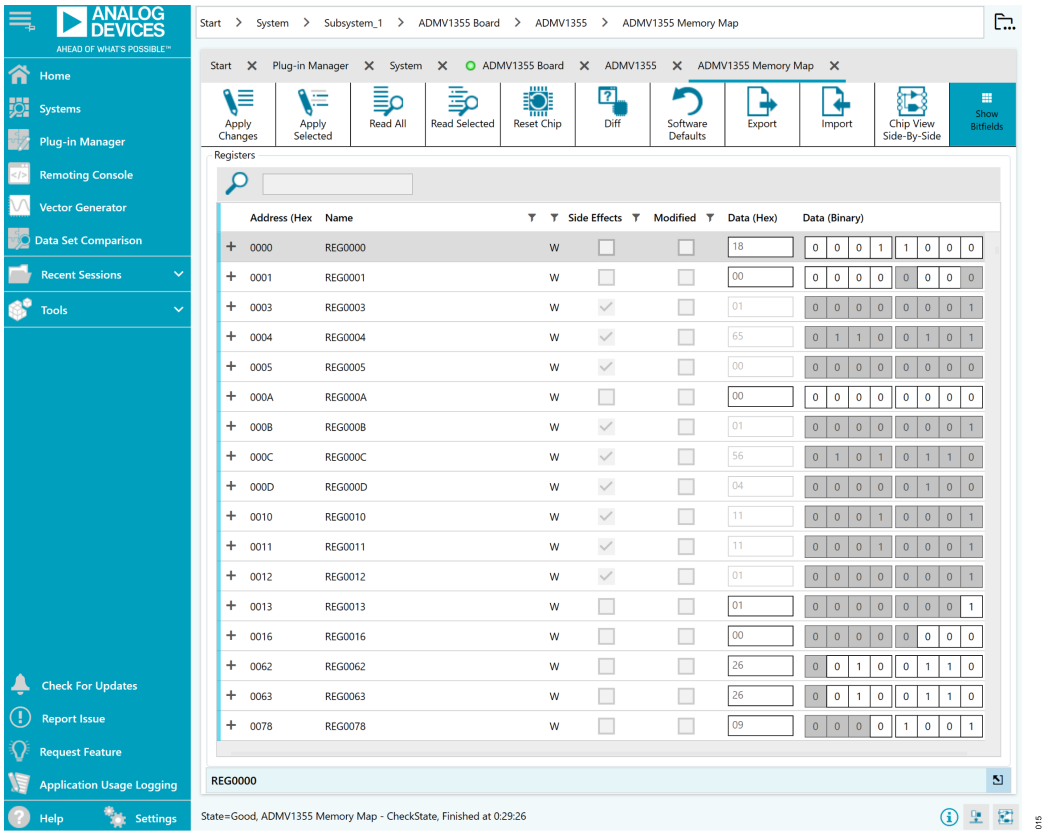

Figure 15. ADMV1355 Memory Map in the ACE Software

PERFORMING EVALUATION

QUICK START

To set up the ADMV1355-EVALZ with a network analyzer, take the following steps (in addition, see Figure 2):

1. Connect the IF_HYB port to Port 1 of the network analyzer using a 50Ω coax cable.
2. Connect the RF_OUT port to Port 2 of the network analyzer using a 50Ω coax cable.
3. Connect the LO port to Port 3 of the network analyzer using a 50Ω coax cable.
4. Connect the SDP-S to the P1 connector.
5. Connect a 5V USB-C adapter to the P2 connector.
6. Alternatively to Step 5, connect the P5V test point to a power supply. The power supply current limit must be set to 500mA and the voltage must be set to 5V. Prior to controlling the ADMV1355-EVALZ with the **ACE Software**, the current draw is approximately 8mA. After the **ADMV1355 Board** plug-in is opened, the current draw is approximately 365mA.
7. Open the **ACE Software**. The **ADMV1355 Board** appears in the **Attached Hardware** section of the **Start** tab (see Figure 4).
8. Double-click the **ADMV1355 Board** to open the **ADMV1355 Board** plug-in (see Figure 5). If the **ADMV1355 Board** plug-in is opened before power is applied (Step 5 or Step 6 was missed), then follow the instructions in the Loss of Power section before applying power.
9. Double-click the **ADMV1355** chip to open the ADMV1355 chip plug-in (see Figure 6).
10. Select one of the **Sequences** to configure the chip to the desired predefined state.

NETWORK ANALYZER SETTINGS

When evaluating the ADMV1355-EVALZ for a high-band input signal chain with an IF_HYB input and an upper sideband configuration, a good starting point for configuring the network analyzer is as follows:

- Define the frequencies as follows:
  - F1 = 8GHz (IF_HYB)
  - F2 = 4GHz to 29GHz (LO)
  - F3 = 2× F2 = 8GHz to 58GHz (2×LO)
  - F4 = F3 + F1 = 16GHz to 66GHz (upper sideband)
  - F5 = F3 − F1 = 0GHz to 50GHz (lower sideband)
- For Port 1, set to the following:
  - Input power level = −20dBm
  - Input frequency = F1 (IF_HYB)
- For Port 2, set and measure the following:
  - Observation frequencies = F1, F2, F3, F4, and F5
  - Number of swept points = 501
  - Measure the power at F1 (IF_HYB feedthrough)
  - Measure the power at F2 (LO feedthrough)
  - Measure the power at F3 (2×LO feedthrough)
  - Measure the power at F4 (upper sideband)
  - Measure the power at F5 (lower sideband)
  - Measure the conversion gain (Upper Sideband – IF_HYB)
  - Mesaure sideband suppression (Upper Sideband − Lower Sideband)
- For Port 3, set to the following:
  - Input power level = −5dBm
  - Input frequency = F2 (LO)
  - Number of points = 501
  - Step size = 50MHz
- For calibration, do the following:
  - Perform a RF power calibration by using a power sensor.
  - Perform a full 3-port calibration with an electronic calibration (E-Cal) module or SOLT standards.
  - Apply board loss de-embedding files and enable power compensation.

Note, the frequencies previously listed are for testing purposes only. For exact frequency specifications of the ADMV1355, refer to the ADMV1355 data sheet.

TYPICAL PERFORMANCE

Given the network analyzer settings detailed in the Network Analyzer Settings section, see Figure 16 for the typical conversion gain performance.

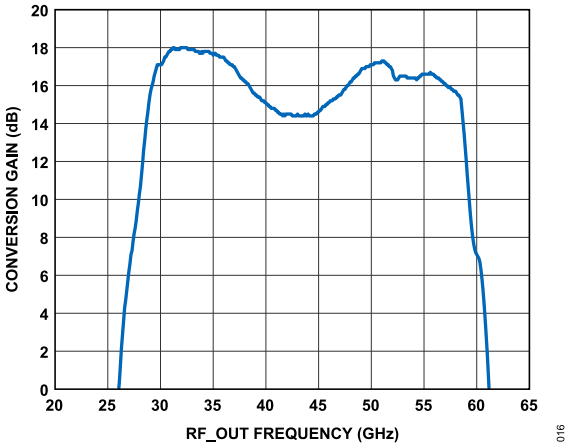

Figure 16. ADMV1355-EVALZ Conversion Gain vs. RF_OUT Frequency, 8 GHz IF_HYB, Upper Sideband

PERFORMING EVALUATION

POWER REGULATOR OVERVIEW

The ADMV1355-EVALZ on board power regulator utilizes two silent switcher chips and a precision DAC for voltage adjustment.

The LTC3315B is the primary regulator used to generate the 3V and the 1.8V power supply voltages for the ADMV1355. The LTC3315B uses a 6MHz clock from the LTC6908, which allows for high-efficiency and fast transient response in a small application footprint.

The LTC3307B is a provisional regulator used for generating an additional 1.8V for the VDD_MIX and VDD_LO supply inputs on the ADMV1355. In sensitive spurious applications, it may be desirable to use the provisional regulator. By default, the provisional regulator is bypassed, and these pins are powered by the main regulator.

The ADMV1355-EVALZ normal bill of materials (BOM) uses the AD5684R 12-bit DAC for power regulator voltage adjustments. The AD5684R 12-bit DAC provides sufficient resolution; however, the ADMV1355-EVALZ can also be populated with the AD5685R 14-bit DAC or the AD5686R 16-bit DAC.

The AD5684R is used to adjust the power regulator voltages by ±10%. The AD5684R uses its 2.5V internal reference voltage, resulting in adjustment voltages from 0V to 2.5V. By default, the outputs are set to midscale for 1.25V on all outputs. The AD5684R outputs are then connected to the feedback networks of the LTC3315B and LTC3307B. The resistors in the feedback networks have been configured to support the following equations:

- 3V_SUPPLY = 3.3 – 0.24 × VADJ_3V = 3.3 – 0.0.24 × $V_{OUT}A$
- 1P8V_A = 2 – 0.16 × VADJ_1V8_A = 2 – 0.16 × $V_{OUT}B$
- 1P8V_B = 2 – 0.16 × VADJ_1V8_B = 2 – 0.16 × $V_{OUT}C$

The AD5684R $V_{OUT}D$ output is not connected to anything on the ADMV1355-EVALZ and can be accessed using the TP_D test point for evaluation prototyping purposes.

POWER REGULATOR ADJUSTMENT

The **ADMV1355 Board** plug-in implements the AD5686R. When either the AD5684R or AD5685R are installed on the ADMV1355-EVALZ, the extra bits sent in the SPI transaction are ignored.

When the **ADMV1355 Board** plug-in is initialized, it configures the AD5686R for an internal voltage reference with midscale output voltages.

In the **ADMV1355 Board** plug-in view diagram (see Figure 5), users can click one of three buttons to set the DAC voltage, which include **+10%**, **Nominal**, or **−10%**. If additional power-supply voltage adjustment is required, double-click the **AD5686R** chip to manually adjust the voltages.

POWER REGULATOR BYPASS

The ADMV1355-EVALZ on board power regulator can be bypassed by removing the C2, C3, and C4 three terminal capacitors. To power the ADMV1355 with these capacitors removed, an external 3V supply can be connected to TP_3V test point, and an external 1.8V supply can be connected to both the 1P8V_A and 1P8V_B test points.

LOSS OF COMMUNICATION

If the USB cable is disconnected from the SDP-S or the PC while the **ACE Software** is running, communication with the ADMV1355 will be lost, and the light emitting diode (LED) in the **ADMV1355 Board** plug-in tab will be red (see Figure 5). Upon reconnecting the USB cable, the **ACE Software** should reacquire communication, and the LED will then be green. If the LED remains red, take the following steps to regain communications:

1. Click the **System** tab.
2. Click the USB symbol in the **SDP-S Controller** subsystem.
3. Click **Acquire**.

Once communication has been re-established, and the LED is green, it is necessary to click **Reset Board** in the **ADMV1355 Board** plug-in to reset the board to its default state.

If this action does not work, restart the **ACE Software** to re-established communication with the ADMV1355-EVALZ and then reopen the **ADMV1355 Board** plug-in to reset the board to its default state.

PERFORMING EVALUATION

LOSS OF POWER

If the power supplied to the ADMV1355-EVALZ is turned off while the SDP-S remains connected to the PC and the ADMV1355-EVALZ, it is necessary to follow Option 1 or Option 2 before reapplying power. The ADMV1355 CEN input is set high when the **ADMV1355 Board** plug-in is opened or when the **Reset Board** button is clicked; however, this input must be low during power up, which can be accomplished with either option.

For Option 1, do the following:

1. Disable all SDP-S GPIO pins by using the SDP-S block in the **ADMV1355 Board** plug-in. Disabling the GPIO pins on the SDP-S ensures that the power solution on the board will be disabled, and the ADMV1355 CEN input will be low when power is reapplied to the ADMV1355-EVALZ.
2. Apply 5V power to the ADMV1355-EVALZ. The current draw is approximately 8mA.
3. Click the **Reset Board** button in the **ADMV1355 Board** plug-in to reset the board to its default state.

For Option 2, do the following:

1. Disconnect and then re-connect the USB cable from the SDP-S. Disconnecting and reconnecting this cable causes the SDP-S GPIO pins to reset to a high impedance state, ensuring that when power is reapplied to the ADMV1355-EVALZ, the power solution on the board will be disabled, and the ADMV1355 CEN input will be low.
2. Apply 5V power to the ADMV1355-EVALZ. The current draw is approximately 8mA.
3. Follow the instructions in the Loss of Communication section.

SCHEMATICS AND ARTWORK

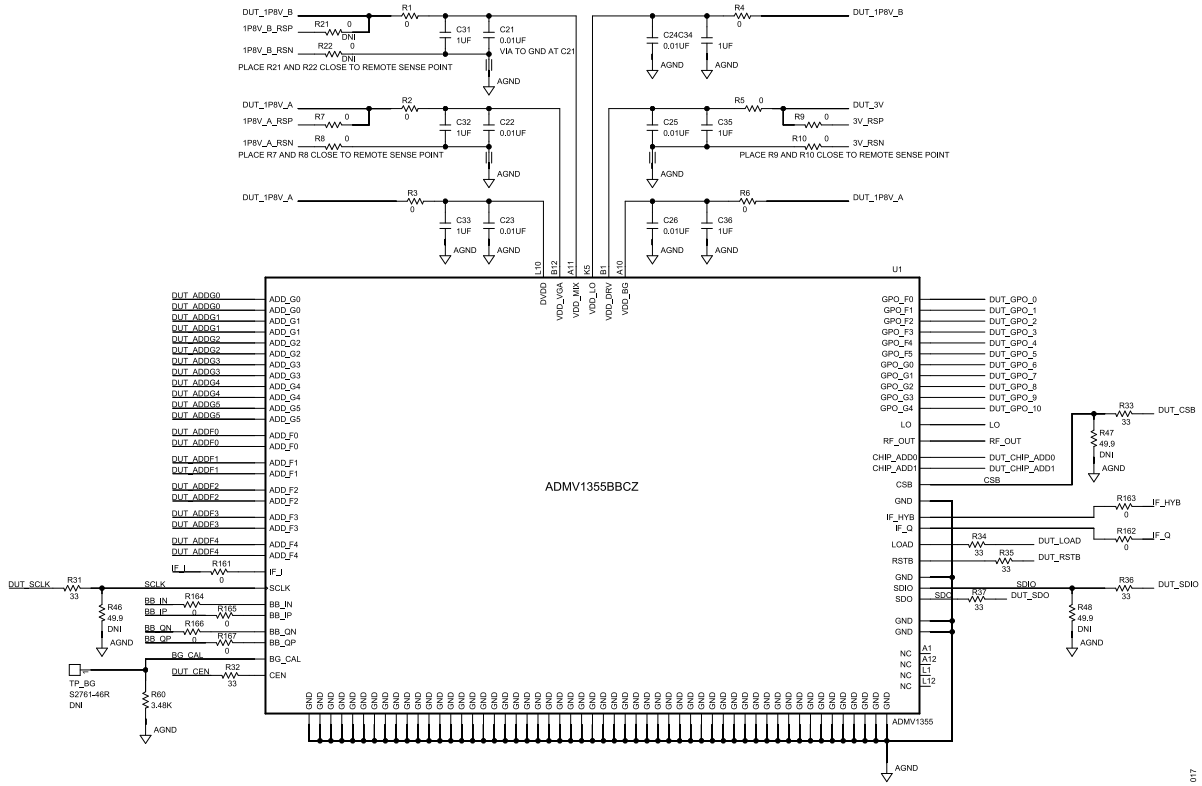

Figure 17. ADMV1355-EVALZ Schematic, U1, ADMV1355

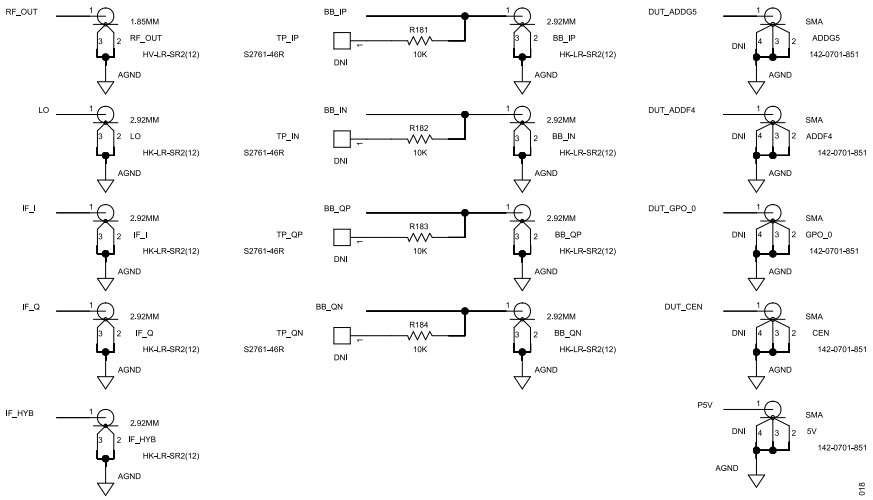

Figure 18. ADMV1355-EVALZ Schematic, RF Connectors

SCHEMATICS AND ARTWORK

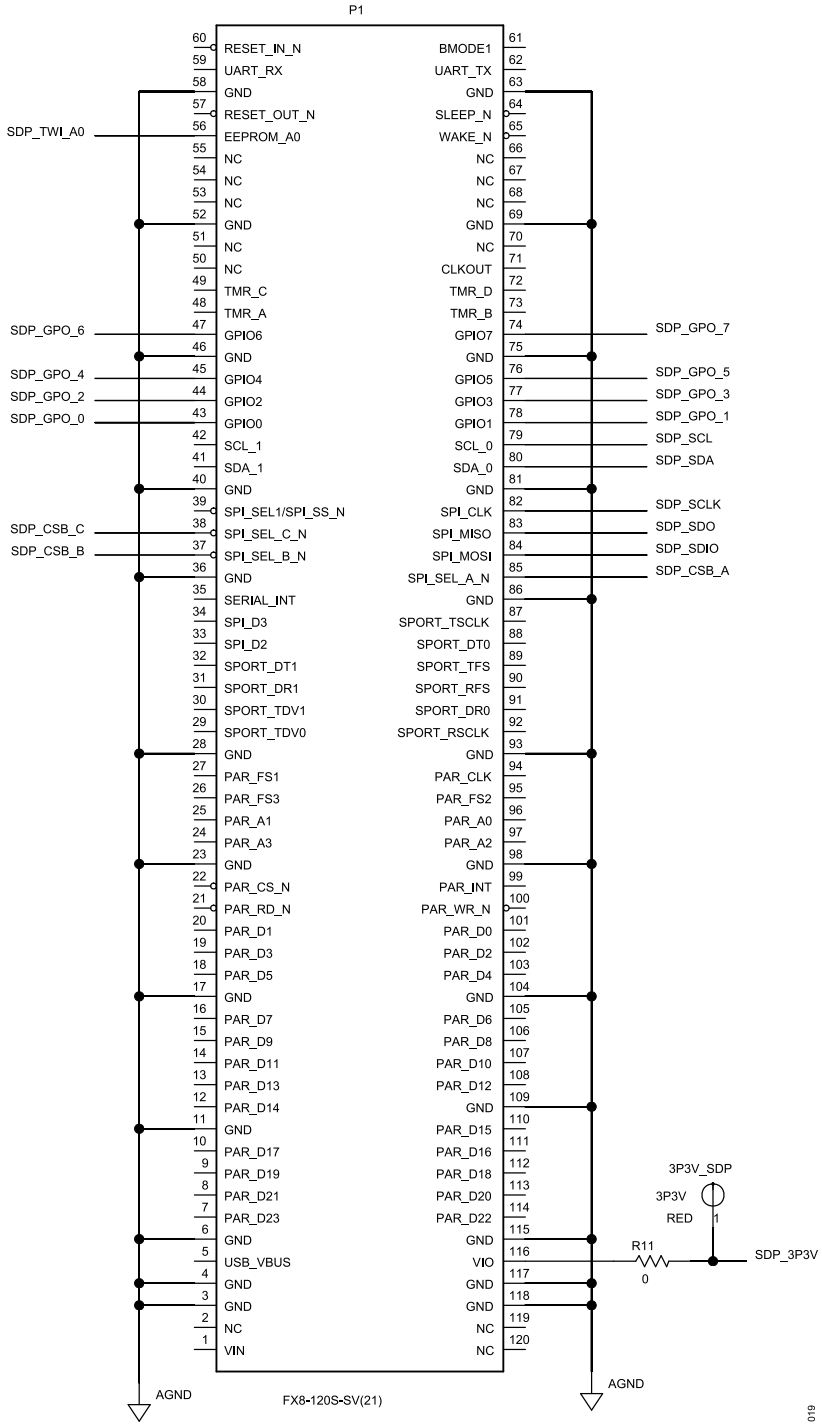

Figure 19. ADMV1355-EVALZ Schematic, P1, SDP-S Connector

SCHEMATICS AND ARTWORK

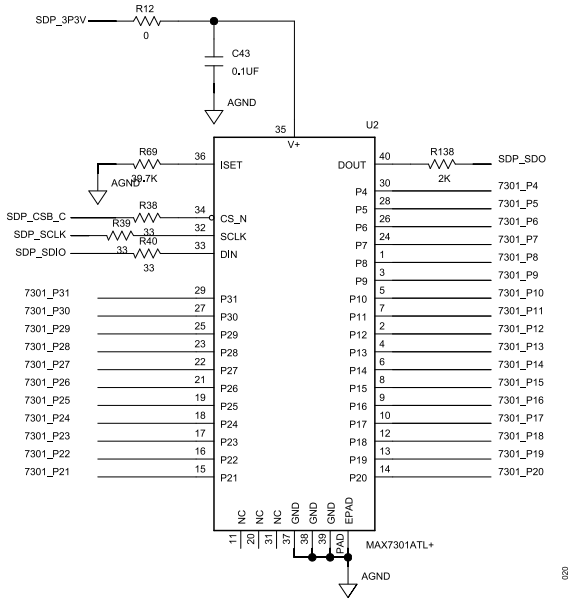

Figure 20. ADMV1355-EVALZ Schematic, U2, MAX7301

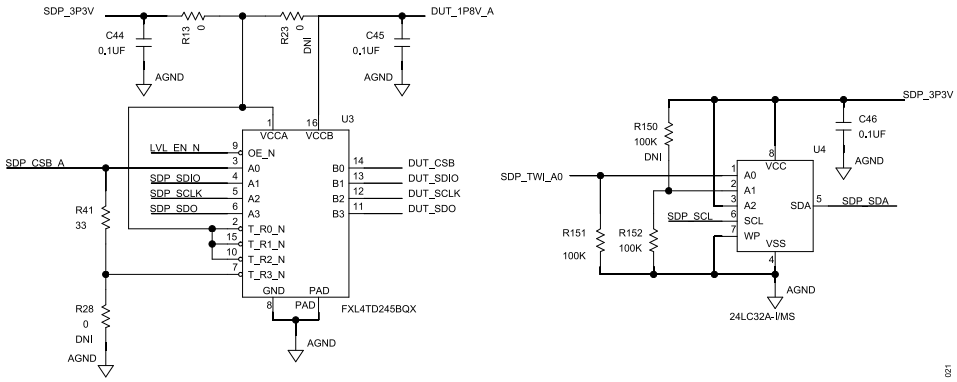

Figure 21. ADMV1355-EVALZ Schematic, U3 and U4, SPI Level Shifter and Board ID Electrically Erasable Programmable Read-Only Memory (EEPROM)

SCHEMATICS AND ARTWORK

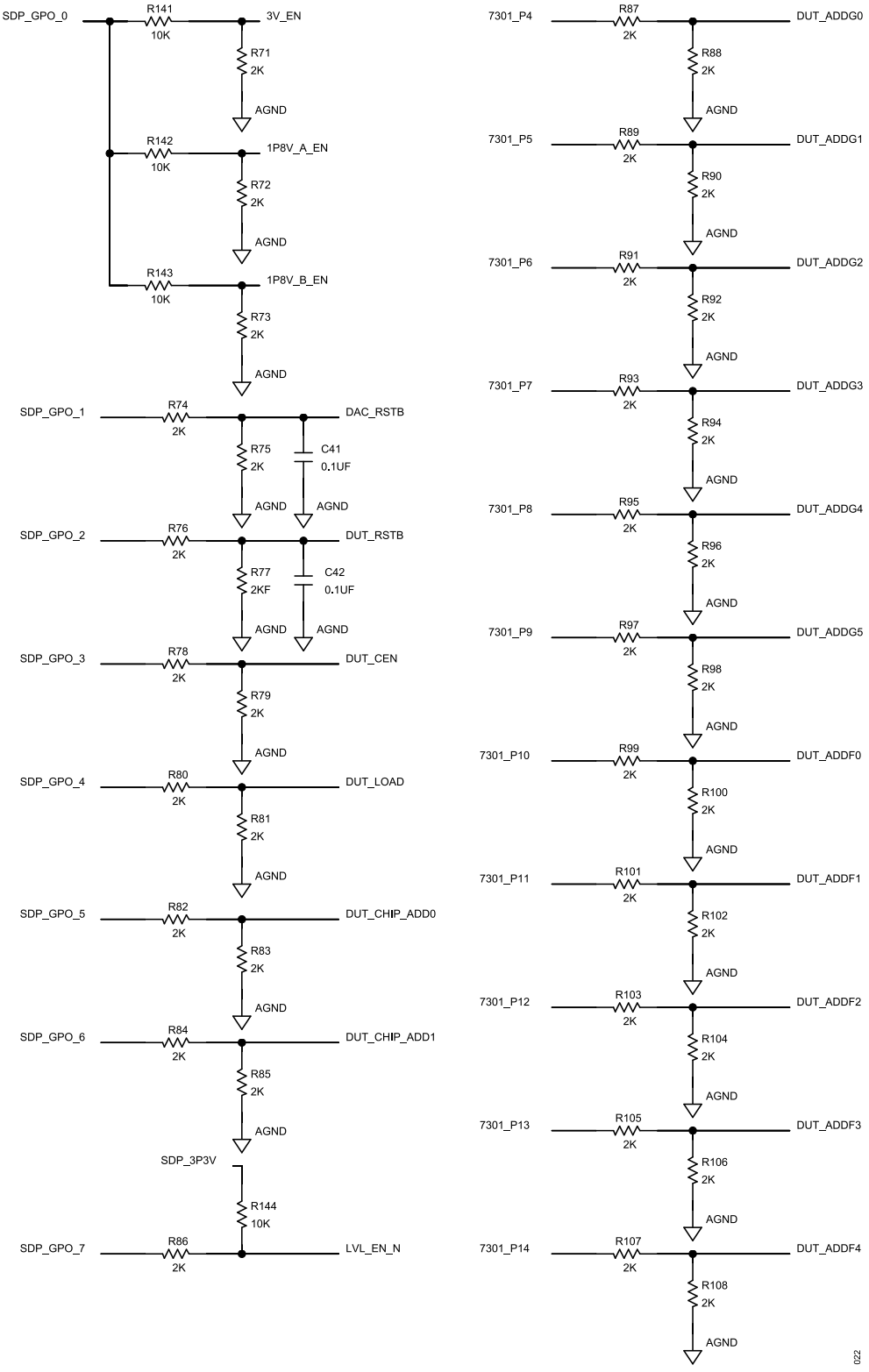

Figure 22. ADMV1355-EVALZ Schematic, Logic Signal Resistor Dividers

SCHEMATICS AND ARTWORK

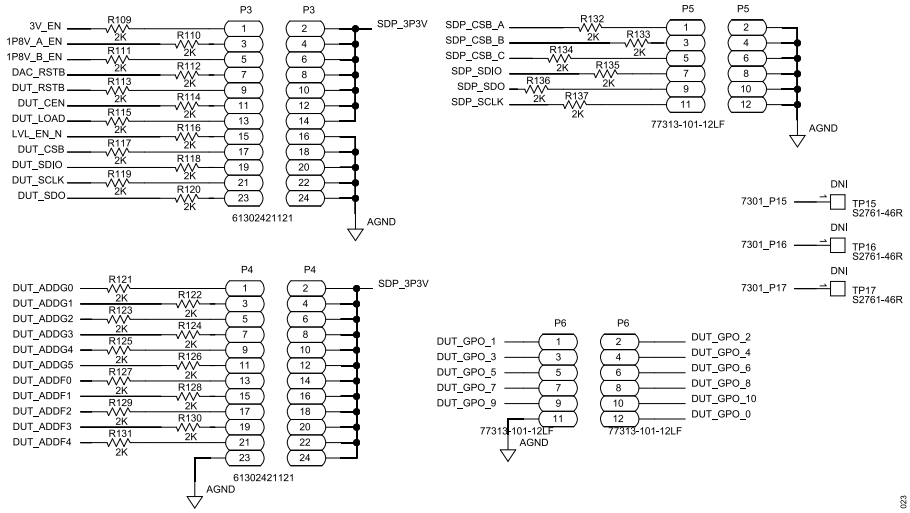

Figure 23. ADMV1355-EVALZ Schematic, P3 to P6 Headers and TP15 to TP17 Test Points

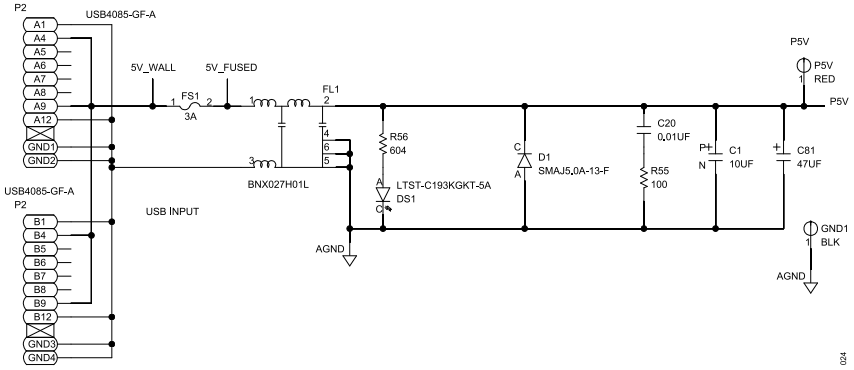

Figure 24. ADMV1355-EVALZ Schematic, P2, USB-C

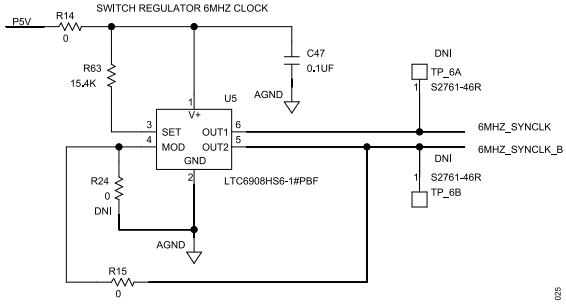

Figure 25. ADMV1355-EVALZ Schematic, U5, 6MHz Clock

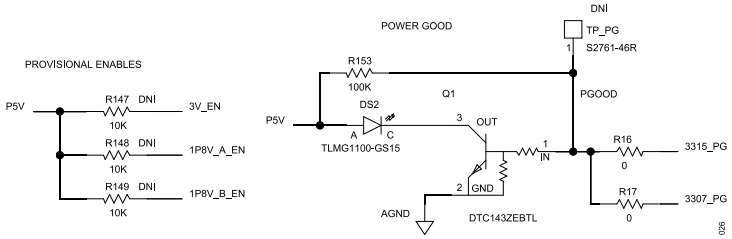

Figure 26. ADMV1355-EVALZ Schematic, Provisional Enables and Power Good

SCHEMATICS AND ARTWORK

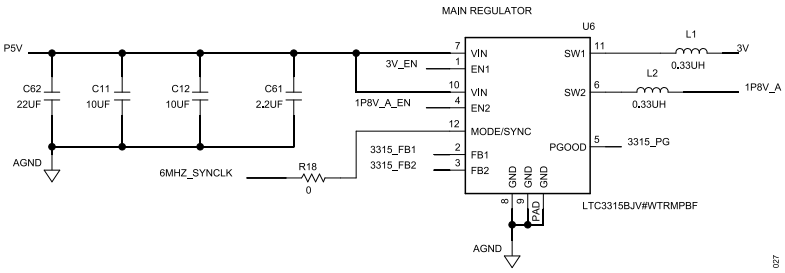

Figure 27. ADMV1355-EVALZ Schematic, U6, Main Regulator

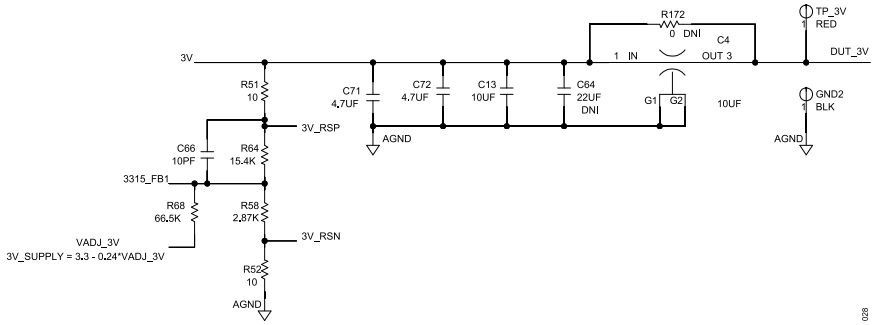

Figure 28. ADMV1355-EVALZ Schematic, 3V Feedback Network

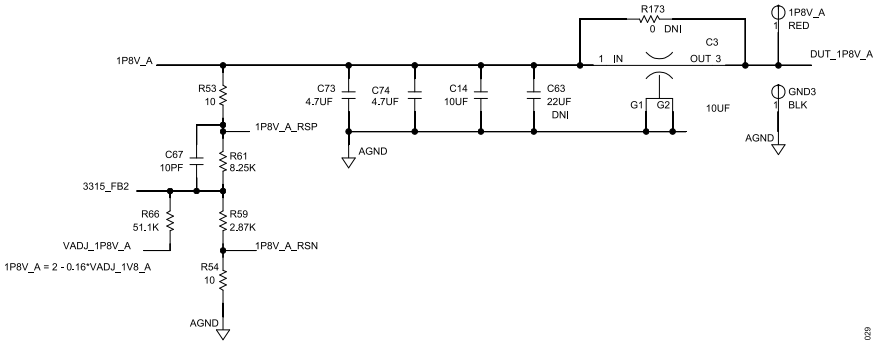

Figure 29. ADMV1355-EVALZ Schematic, 1.8V Feedback Network

SCHEMATICS AND ARTWORK

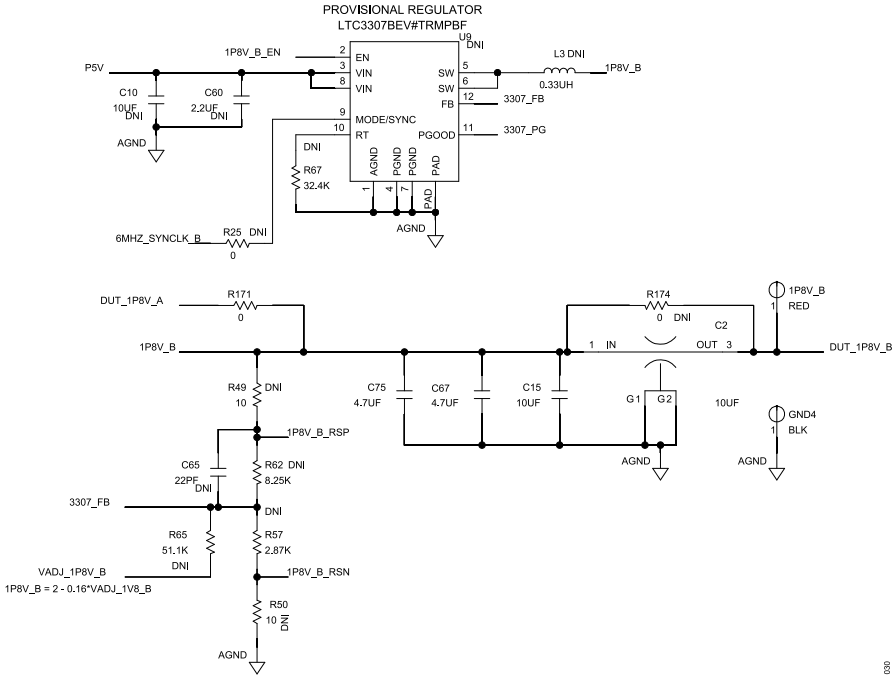

Figure 30. ADMV1355-EVALZ Schematic, Provisional Regulator and 1.8V Feedback Network

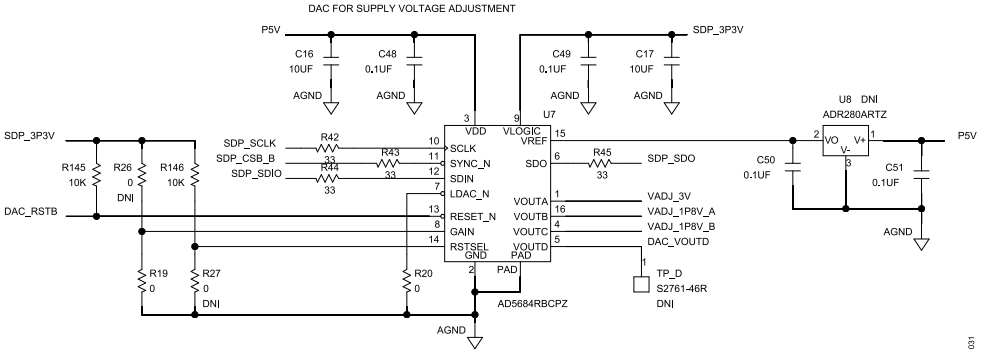

Figure 31. ADMV1355-EVALZ Schematic, U7, AD5684R DAC

SCHEMATICS AND ARTWORK

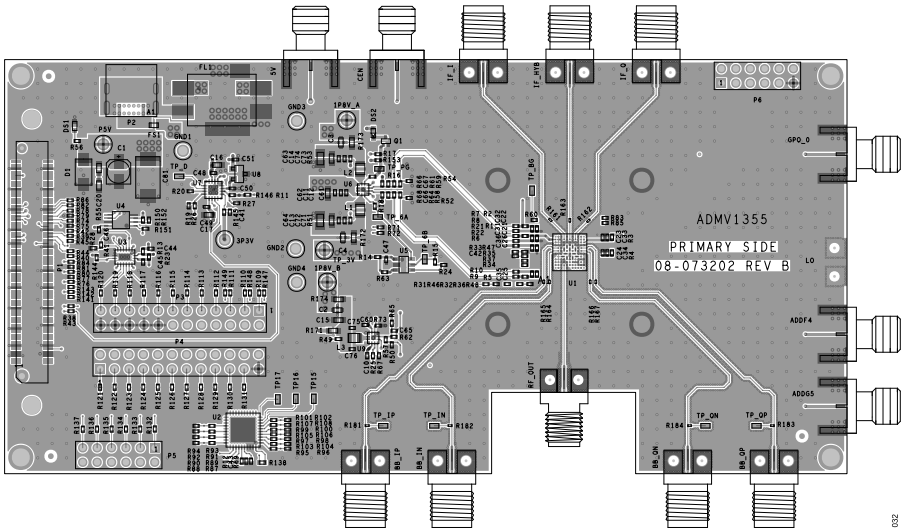

Figure 32. ADMV1355-EVALZ Layer 1

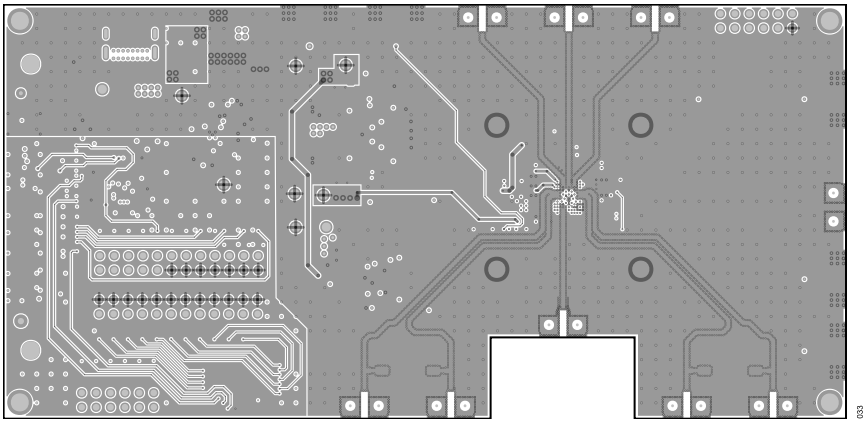

Figure 33. ADMV1355-EVALZ Layer 2

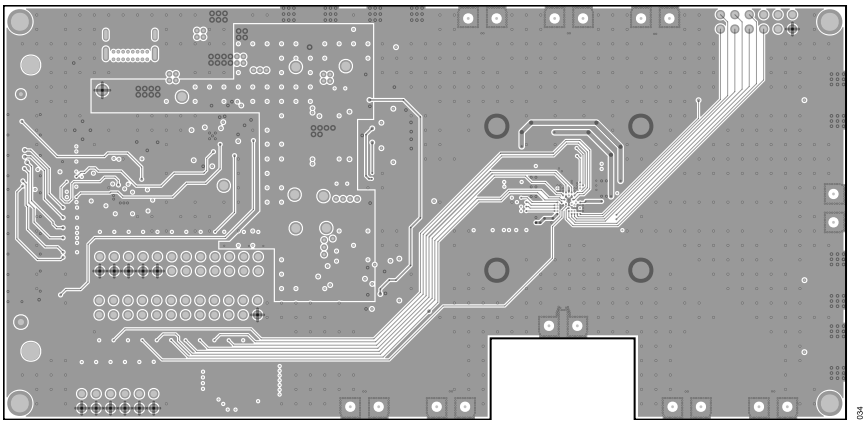

Figure 34. ADMV1355-EVALZ Layer 3

SCHEMATICS AND ARTWORK

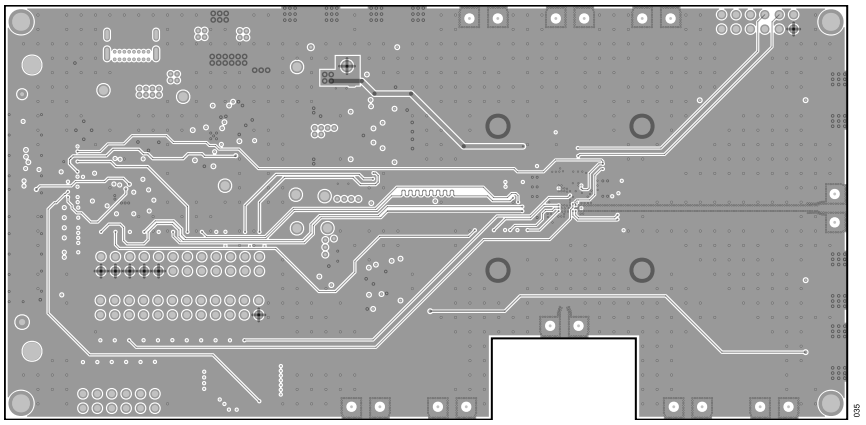

Figure 35. ADMV1355-EVALZ Layer 4

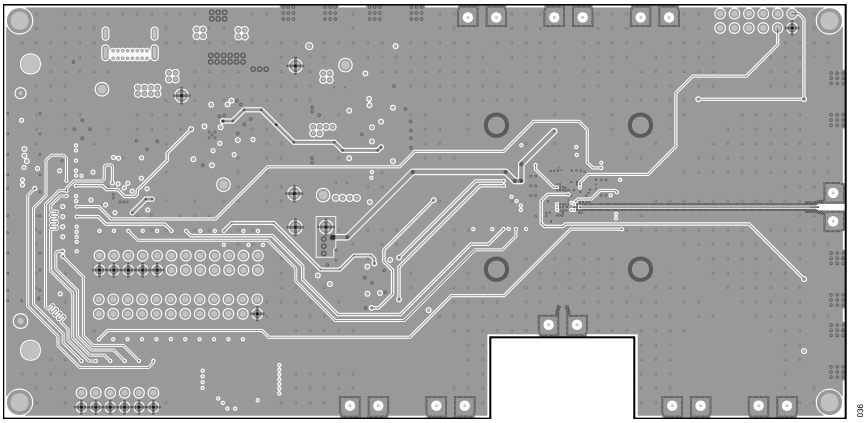

Figure 36. ADMV1355-EVALZ Layer 5

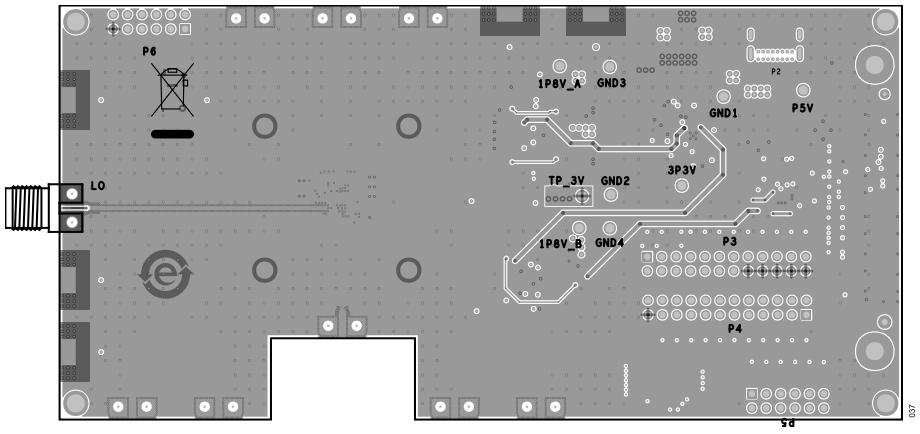

Figure 37. ADMV1355-EVALZ Layer 6

ORDERING INFORMATION

ORDERING GUIDE

Table 5. Evaluation Boards

Model[1]	Description
ADMV1355-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

BILL OF MATERIALS

Quantity	Reference Designator	Description	Manufacturer	Part Number
5	1P8V_A, 1P8V_B, 3P3V, P5V, TP_3V	Test points, red	Components Corporation	TP-104-01-02
4	GND1 to GND4	Test points, black	Components Corporation	TP-104-01-00
8	BB_IN, BB_IP, BB_QN, BB_QP, IF_HYB, IF_I, IF_Q, LO	Connectors, 2.92mm, 40GHz	Hirose Electric Co.	HK-LR-SR2(12)
1	RF_OUT	Connector, 1.85mm, 67GHz	Hirose Electric Co.	HV-LR-SR2(12)
1	P1	Connector, vertical, surface-mount technology (SMT), 120-pin	Hirose Electric Co.	FX8-120S-SV(21)
1	P2	Connector, USB-C	Global Connector Technology	USB4085-GF-A
2	P3, P4	Connectors, headers, vertical, unshrouded, 2×12 pins, 2.54mm	Wurth Elektronik	61302421121
2	P5, P6	Connectors, headers, vertical, unshrouded, 2×6 pins, 2.54mm	Amphenol	77313-101-12LF
1	C1	Capacitor, 10µF, 16V, 20%, radial can	Multicomp Pro	MCESL16V106M4X5.2
3	C2 to C4	Capacitors, 10µF, 4V, 20%, 3-terminal, feed through, 0603	Murata	NFM18PC106D0G3
2	C11, C12	Capacitors, 10µF, 10V, 20%, X5R, 0402	Samsung	CL05A106MP8NUB8
5	C13 to C17	Capacitors, 10µF, 6.3V, 20%, X7S, 0603	TDK Corporation	C1608X7S0J106M080AC
1	C20	Capacitor, 0.01µF, 100V, 10%, X7R, 0603	TDK Corporation	C1608X7R2A103K080AA
6	C21 to C26	Capacitors, 0.01µF, 50V, 10%, X7R, 0402	Samsung	CL05B103KB5NNNC
6	C31 to C36	Capacitors, 1µF, 10V, 10%, X7R, 0402	Murata	GRM155Z71A105KE01D
6	C41 to C46	Capacitors, 0.1µF, 16V, 10%, X7R, 0402	Kyocera AVX	530L104KT16T
5	C47 to C51	Capacitors, 0.1µF, 50V, 10%, X7R, 0402	TDK Corporation	CGA2B3X7R1H104K050BB
1	C61	Capacitor, 2.2µF, 6.3V, 10%, X7S, 0402	Murata	GRM155C70J225KE11D
1	C62	Capacitor, 22µF, 10V, 20%, X5R, 0603	Murata	GRM188R61A226ME15D
2	C66, C67	Capacitors, 10pF, 50V, 5%, C0G, 0402	Yageo	CC0402JRNPO9BN100
6	C71 to C76	Capacitors, 4.7µF, 6.3V, 20%, X6S, 0402	Murata	GRT155C80J475ME13D
1	C81	Capacitor, 47µF, 16 V, 20%, polymer SMD, 7343	Murata	ECASD31C476M040KA0
1	D1	Diode, TVS, 9.2V, DO-214AC, SMA	Diodes Incorporated	SMAJ5.0A-13-F
1	DS1	LED, green, 2V, 75mW, 16.25mcd, 0603	Lite-On Technology	LTST-C193KGKT-5A
1	DS2	LED, green, 2.1V, 0603	Vishay	TLMG1100-GS15
1	FB5	Ferrite bead, 1kΩ at 100MHz, 25%, 0603	Murata	BLM18HK102SN1D
1	FL1	Filter, EMI, 22µF, 16V, 20A, 4-SMD, no lead	Murata	BNX027H01L
1	FS1	Fuse, fast acting, 32V, 3A, 0603	Eaton	0603FA3-R
2	L1, L2	Inductors, 0.33µH, 4.3A, 31mΩ, 1MHz, 20%, 0806	TDK Corporation	TFM201610AL-MAR33MTAA
20	R1 to R20	Resistors, 0Ω jumper, 1/10W, 0402	Panasonic	ERJ-2GE0R00X

ORDERING INFORMATION

Quantity	Reference Designator	Description	Manufacturer	Part Number
15	R31 to R45	Resistors, 33Ω, 1/10W, 5%, 0402	Panasonic	ERJ-2GEJ330X
4	R51 to R54	Resistors, 10Ω, 1/10W, 1%, 0402	Panasonic	ERJ-2RKF10R0X
1	R55	Resistor, 100Ω, 1/10W, 1%, 0603	Panasonic	ERJ-3EKF1000V
1	R56	Resistor, 604Ω, 1/10W, 1%, 0402	Panasonic	ERJ-2RKF6040X
2	R58, R59	Resistors, 2.87kΩ, 1/16W, 1%, 0402	Vishay	CRCW04022K87FKED
1	R60	Resistor, 3.48kΩ, 1/16W, 0.1%, 0402	Panasonic	ERA-2ARB3481X
1	R61	Resistor, 8.25kΩ, 1/10W, 1%, 0402	Panasonic	ERJ-2RKF8251X
2	R63, R64	Resistor, 15.4kΩ, 1/10W, 1%, 0402	Panasonic	ERJ-2RKF1542X
1	R66	Resistor, 51.1kΩ, 1/16W, 1%, 0402	Yageo	RC0402FR-0751K1L
1	R68	Resistor, 66.5kΩ, 1/16W, 1%, 0402	Vishay	CRCW040266K5FKED
1	R69	Resistor, 39.7kΩ, 1/10W, 0.1%, 0402	Vishay	TNPW040239K7BEED
68	R71 to R138	Resistors, 2kΩ, 1/10W, 1%, 0402	Panasonic	ERJ-2RKF2001X
6	R141 to R146	Resistors, 10kΩ, 1/10W, 1%, 0402	Panasonic	ERJ-2RKF1002X
3	R151 to R153	Resistors, 100kΩ, 1/10W, 1%, 0402	Panasonic	ERJ-2RKF1003X
7	R161 to R167	Resistors, 0Ω jumper, 1/20W, 1%, 0201	KOA Speer Electronics, Inc.	RK73Z1HTTC
1	R171	Resistor, 0Ω, 45A, 0603 copper strip	Vishay	WSL060300000ZEA9
4	R181 to R184	Resistors, 10kΩ, 1/20W, 0.1%, 0201	Panasonic	ERA-1AEB103C
1	Q1	Transistor, BJT, NPN, prebiased, 50V, 100mA, 150mW, SOT-416FL	Rohm Semiconductor	DTC143ZEBTL
1	U1	IC, 17.7GHz to 55GHz, wideband, microwave up-converter	Analog Devices Inc.	ADMV1355BBCZ
1	U2	IC, 4-wire interfaced, 2.5V to 5.5V, 20-port and 28-port input and output (I/O) expander	Analog Devices Inc.	MAX7301ATL+
1	U3	IC, level translator, dual-supply, 4-bit	Onsemi	FXL4TD245BQX
1	U4	IC, 24LC32A, EEPROM, I^2C, MSOP8	Microchip Technology	24LC32A-I/MS
1	U5	IC, resistor set SOT-23 oscillator with spread spectrum modulation	Analog Devices Inc.	LTC6908HS6-1#TRPBF
1	U6	IC, dual 5V, 2A synchronous step-down DC/DC converter in 2mm × 2mm LQFN	Analog Devices Inc.	LTC3315BJV#TRMPBF
1	U7	IC, quad, 12-Bit *nano*DAC+ with 2ppm/°C on-chip reference and SPI	Analog Devices Inc.	AD5684RBCPZ-RL7
12	TP15. TP16, TP17, TP_6A, TP_6B, TP_BG, TP_D, TP_IN, TP_IP, TP_PG, TP_QN, TP_QP	Test points, SMT, do not install (DNI)	Harwin, Inc.	S2761-46R
5	5V, ADD_F4, ADD_G5, CEN, GPO_0	Connectors, edge launch, SMA, DNI	Cinch Connectivity Solutions	142-0701-851
1	C10	Capacitor, 10µF, 10V, 20%, X5R, 0402, DNI	Samsung	CL05A106MP8NUB8
1	C60	Capacitor, 2.2µF, 6.3V, 10%, X7S, 0402, DNI	Murata	GRM155C70J225KE11D
2	C63, C64	Capacitors, 22µF, 6.3V, 20%, X7S, 0805, DNI	TDK Corporation	C2012X7S0J226M125AC
1	C65	Capacitor, 22pF, 50V, 5%, C0G, 0402, DNI	Yageo	0402CG220J9B200
1	L3	Inductor, 0.33µH, 4.3A, 31mΩ, 1MHz, 20%, 0806, DNI	TDK Corporation	TFM201610AL-MAR33MTAA
8	R21 to R28	Resistors, 0Ω jumper, 1/10W, 0402, DNI	Panasonic	ERJ-2GE0R00X
3	R46, R47, R48	Resistors, 49.9Ω, 1/10W, 1%, 0402, DNI	Panasonic	ERJ-2RKF49R9X
2	R49, R50	Resistors, 10Ω, 1/10W, 1%, 0402, DNI	Panasonic	ERJ-2RKF10R0X
1	R57	Resistor, 2.87kΩ, 1/16W, 1%, 0402. DNI	Vishay	CRCW04022K87FKED

ORDERING INFORMATION

Quantity	Reference Designator	Description	Manufacturer	Part Number
1	R62	Resistor, 8.25kΩ, 1/10W, 1%, 0402, DNI	Panasonic	ERJ-2RKF8251X
1	R65	Resistor, 51.1kΩ, 1/16W, 1%, 0402, DNI	Yageo	RC0402FR-0751K1L
1	R67	Resistor, 32.4kΩ, 1/10W, 1%, 0402, DNI	Panasonic	ERJ-2RKF3242X
3	R147, R148, R149	Resistors, 10kΩ, 1/10W, 1%, 0402, DNI	Panasonic	ERJ-2RKF1002X
1	R150	Resistor, 100kΩ, 1/10W, 1%, 0402, DNI	Panasonic	ERJ-2RKF1003X
3	R172, R173, R174	Resistors, 0Ω, 45A, 0603 copper strip, DNI	Vishay	WSL060300000ZEA9
1	U8	IC, 1.2V ultralow power, high PSRR, voltage reference, DNI	Analog Devices Inc.	ADR280ARTZ-REEL7
1	U9	IC, 5V, 3A, 10MHz synchronous step-down silent switcher in 2mm × 2mm LQFN, DNI	Analog Devices Inc.	LTC3307BEV#TRMPBF

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.