Evaluating the ADL8112 Low Noise Amplifier with Bypass Switches, 10 MHz to 26.5 GHz

FEATURES

- 4-layer, Rogers 4350B and Isola 370HR evaluation board
- End launch, 2.92 mm RF connectors
- Through calibration path (depopulated)

EVALUATION KIT CONTENTS

- ADL8112-EVALZ evaluation board

EQUIPMENT NEEDED

- RF signal generator
- RF spectrum analyzer
- RF network analyzer
- 8.5 V, 300 mA power supply
- +3.3 V and −3.3 V, 100 mA power supplies

GENERAL DESCRIPTION

The ADL8112-EVALZ is a 4-layer printed circuit board (PCB) fabricated from 10 mil thick, Rogers 4350B and Isola 370HR, copper clad, forming a nominal thickness of 62 mils. The RFIN and RFOUT ports on the ADL8112-EVALZ are populated with 2.92 mm, female coaxial connectors, and the corresponding RF traces have a 50 Ω characteristic impedance. The ADL8112-EVALZ is populated with components suitable for use over the entire −40°C to +85°C operating temperature range of the ADL8112. To calibrate board trace losses, two through calibration paths are provided. Install RF connectors in the J5, J6, J11, and J12 positions to use the through calibration paths. Refer to Table 1 and Figure 3 for the through calibration RF path performance.

Access the ADL8112-EVALZ power supply and digital control pins through the surface-mount technology (SMT) test point connectors, VDD_PA, GND, VDD_SW, VSS_SW, VA, and VB.

The RF traces on the ADL8112-EVALZ are 50 Ω, grounded, coplanar waveguides. The package ground leads and the exposed pad connect directly to the ground plane. Multiple vias connect the top and bottom ground planes with particular focus on the area directly beneath the ground paddle to provide adequate electrical conduction and thermal conduction to the ADL8112-EVALZ.

Figure 4 shows the ADL8112-EVALZ schematic and configuration used to characterize and qualify the device.

For full details on the ADL8112, see the ADL8112 data sheet, which must be consulted in conjunction with this user guide when using the ADL8112-EVALZ.

EVALUATION BOARD PHOTOGRAPHS

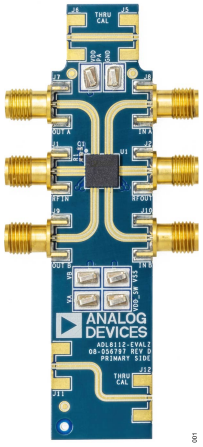

Figure 1. ADL8112-EVALZ Primary Side

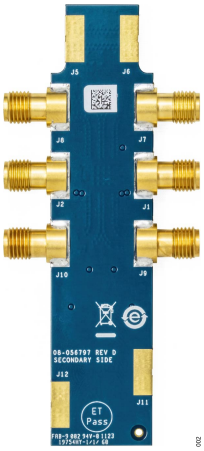

Figure 2. ADL8112-EVALZ Secondary Side

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REVISION HISTORY

8/2024—Rev. 0 to Rev. A

Changes to Operating the ADL8112-EVALZ Section 3
Changes to Figure 4 4
Changes to Table 2 5

4/2023—Revision 0: Initial Version

OPERATING THE ADL8112-EVALZ

Connect an 8.5 V, 300 mA power supply to the VDD_PA SMT test point. Connect the power supply ground to the GND test point. Connect a +3.3 V, 100 mA, and a −3.3 V, 100 mA power supply to the VDD_SW and VSS_SW test points of the ADL8112-EVALZ to provide biasing to the VDD2 and VSS2 pins. To enable the two digital control input pins, VA and VB, connect either 0 V or 3.3 V.

Refer to the ADL8112 data sheet for the recommended resistor values to achieve different supply currents. The default value of the external resistor, R1, connected on the ADL8112-EVALZ is 750 Ω, which is the same value used to characterize the ADL8112.

The following bias conditions are recommended to achieve the performance specified in the ADL8112 data sheet:

- V_{DD1} = 8.5 V
- Total supply current (I_{DQ}) = 90 mA
- Bias resistance (R_{BIAS}) = 750 Ω

RECOMMENDED BIAS SEQUENCING

During Power-Up

To power up the ADL8112-EVALZ, take the following bias sequencing steps:

1. Set the VDD2 supply to 3.3 V.
2. Set the VSS2 supply to −3.3 V.
3. Set the VDD1 supply to 8.5 V.
4. Apply the RF input signal.

During Power-Down

To power down the ADL8112-EVALZ, take the following bias sequencing steps:

1. Turn off the RF input signal.
2. Set the VDD1 supply to 0 V.
3. Set the VSS2 supply to 0 V.
4. Set the VDD2 supply to 0 V.

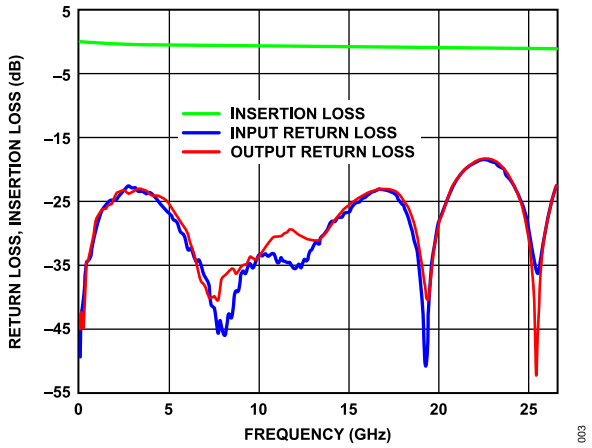

Figure 3. Insertion Loss and Return Loss of the J6 to J5 Through Calibration Path

Table 1. Insertion Loss and Return Loss of the J6 to J5 Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)	Input Return Loss (dB)	Output Return Loss (dB)
0.01	–0.03	–49.26	–45.91
1.01	–0.26	–28.62	–27.44
3.01	–0.43	–22.85	–23.46
5.01	–0.51	–26.98	–25.54
9.01	–0.65	–36.49	–35.16
11.01	–0.70	–34.57	–30.45
13.01	–0.74	–32.15	–31.11
15.01	–0.78	–26.54	–25.49
17.01	–0.83	–23.18	–23.02
19.01	–0.84	–38.76	–33.37
21.01	–0.91	–21.22	–21.04
23.01	–0.99	–18.97	–18.67
25.01	–0.77	–23.12	–22.13
26.5	–1.02	–22.43	–22.52

EVALUATION BOARD SCHEMATIC AND ARTWORK

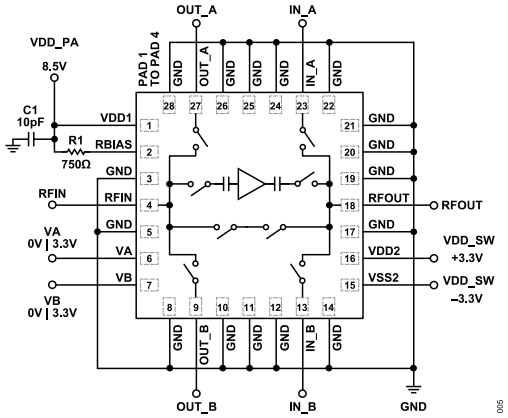

Figure 4. ADL8112-EVALZ Schematic

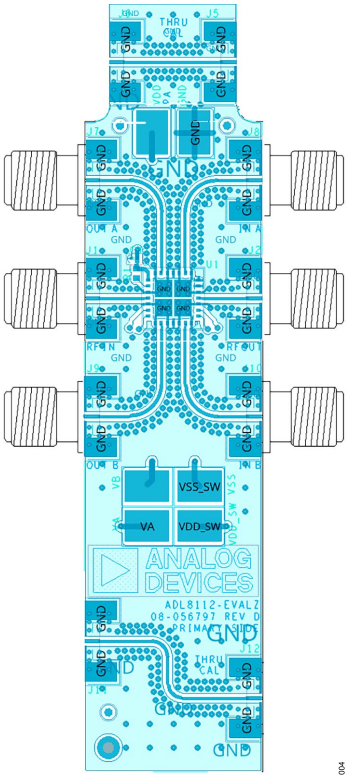

Figure 5. ADL8112-EVALZ Assembly Drawing (J5, J6, J11, and J12 Are Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C1	Capacitor, ceramic, 10 pF, 25 V, 5%, C0G, 0201	Murata	GRM0335C1E100JA01D
VDD_PA, GND, VDD_SW, VSS_SW	Connectors, SMT test points	Keystone Electronics	5016
J1 RFIN, J2 RFOUT, J7 OUT_A, J8 IN_A, J9 OUT_B, J10 IN_B	Connectors, 2.92 mm, jack edge	SRI Connector Gage Co.	25-146-1000-92
J6, J5, J11, J12	Connectors, 2.92 mm, jack edge (not installed)	SRI Connector Gage Co.	25-146-1000-92
R1	Resistor SMD, 750 Ω, 1%, 1/16 W, 0402	Vishay	CRCW0402750RFKED

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.