

Evaluating the ADIN1320 Robust, Industrial Low Latency Gigabit Ethernet PHY with Copper and Fiber Interface

FEATURES

- ▶ Dual ADIN1320 PHY with configurable port connectivity
 - ▶ Flexible PHY interface configuration
 - ▶ Port 0 ADIN1320 supports connection to both RJ45 and SFP connectors
 - ▶ Port 1 ADIN1320 supports connection to RJ45 and SMA connectors for SGMII signal access
- ▶ Standalone operation via hardware configuration
- ▶ FMC connector for FPGA/SoC integration
- ▶ GBPHY-FMC-B2B expansion board included
 - ▶ MAC signal probing
 - ▶ Loopback testing
 - ▶ Back-to-back PHY operation
- ▶ Flexible power supplies options
 - ▶ Selectable VDDIO voltage
 - ▶ Power rail measurement points
- ▶ Software and GUI support
 - ▶ On-board Arm® Cortex®-M4 processor [MAX32670](#) microcontroller
 - ▶ Supports execution of [NO-OS driver and firmware examples](#)
 - ▶ Enables communication with an [ACE software GUI](#)

EVALUATION KIT CONTENTS

- ▶ EV-ADIN1320FMCZ evaluation board
- ▶ GBPHY-FMC-B2B FMC expansion board
- ▶ 2× Ethernet cable with RJ45 connectors
- ▶ USB-A to USB-C cable

EQUIPMENT NEEDED

- ▶ RJ45 cable or fiber optic cable
- ▶ SFP module
- ▶ USB-C cable

SOFTWARE NEEDED

- ▶ ACE software
- ▶ ADIN1320 ACE plug-in
- ▶ Serial port terminal software (optional)

GENERAL DESCRIPTION

The EV-ADIN1320FMCZ (see [Figure 1](#)) evaluation board is designed to simplify the testing and integration of the ADIN1320, a low-power, single-port Gigabit Ethernet physical layer (PHY) optimized for industrial applications. The platform enables comprehensive evaluation of the ADIN1320 functionality, including Ethernet

and serializer/deserializer (SerDes) interfaces. By supporting the ADIN1320 copper and fiber Ethernet capabilities, the platform allows evaluation of the following:

- ▶ Copper Ethernet: 10BASE-Te, 10BASE-T, 100BASE-TX, 1000BASE-T
- ▶ Fiber and SerDes protocols: 1000BASE-X, 100BASE-FX, 1000BASE-KX

The evaluation board integrates two ADIN1320 PHYs, each connected to an RJ45 connector with integrated magnetics for copper connectivity and configured to support different SGMII interface options as follows:

- ▶ Port 0 ADIN1320 with an SFP cage for fiber or copper SGMII modules
- ▶ Port 1 ADIN1320 with SMA connectors for SGMII signal access

Both PHYs have their media access control (MAC) I/O pins routed to a field-programmable gate array (FPGA) mezzanine card (FMC) connector, which allow seamless integration with FMC-compatible FPGA or system on a chip (SoC) platforms. An included GBPHY-FMC-B2B expansion board enables MAC signal probing, MAC loopback, and back-to-back PHY connection for advanced evaluation scenarios.

Power can be supplied by USB-C, terminal block (P23), or barrel connector (P4). On-board DC-DC converters and buck regulators generate all required rails, with easy VDDIO level switching by a rotary switch and current measurement points for AVDD_3P3, DVDD_0P9, and VDDIO.

An on-board Arm Cortex-M4 processor (MAX32670) provides additional control and diagnostics, which supports NO-OS examples and ACE software (GUI) communication. The board supports two primary modes of operation as follows:

- ▶ PC-connected mode: full register access, status monitoring, and diagnostics by USB using a GUI or terminal interface.
- ▶ Standalone mode: controlled through on-board hardware switches, with LEDs for link status indication.

While the ACE software offers extended control, it is recommended to configure the EV-ADIN1320FMCZ using hardware switches first to ensure proper initialization. The ACE software reflects the current hardware configuration and allows further customization once a stable setup is established.

Full specifications on the ADIN1320 are available in the [ADIN1320](#) data sheet available from Analog Devices, Inc., and must be consulted with this user guide when using the EV-ADIN1320FMCZ evaluation board.

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REVISION HISTORY**7/2026—Rev. 0 to Rev. A**

Reorganized Layout (Universal).....	1
Changes to Features Section.....	1
Changes to Evaluation Kit Contents Section.....	1
Changes to Software Needed Section.....	1
Changes to General Description Section.....	1
Changes to Figure 1.....	4
Added Figure 2; Renumbered Sequentially.....	4
Changes to Figure 3.....	5
Changes to Table 1 to Table 3.....	6
Changes to Modes of Operation Section.....	8
Change to Copper PHY Core Section.....	8
Change to SERDES Subsystem Section.....	8
Changes to MAC Interface Section.....	9
Changes to FMC Connector Section.....	9
Changes to Status LED Pin Section.....	9
Change to Clock Options Section.....	9
Changes to MAX32670 Section.....	10
Changes to MDIO Header Section.....	10
Deleted Software Overview Section, Installing the ADIN1320 Software Section, and Figure 3 to Figure 7; Renumbered Sequentially.....	10
Deleted Initial Setup Section.....	10
Deleted Evaluation Software Section, Table 4, and Figure 8; Renumbered Sequentially	10
Added Software Quick Start Procedures Section.....	11
Added Accessing ACE Software for ADIN1320 Evaluation Section and Figure 4.....	11
Added Using the Software for Evaluation Section.....	11
Added ADIN1320 Board View Section and Figure 5.....	11
Deleted Local Devices Section and Figure 9.....	11
Deleted User Buttons Section, Figure 10, and Figure 11.....	11
Added Device Status and Control Tab Section and Figure 6.....	11
Replaced Link Properties Tab Section.....	11
Deleted Figure 12.....	11
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3/2026—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

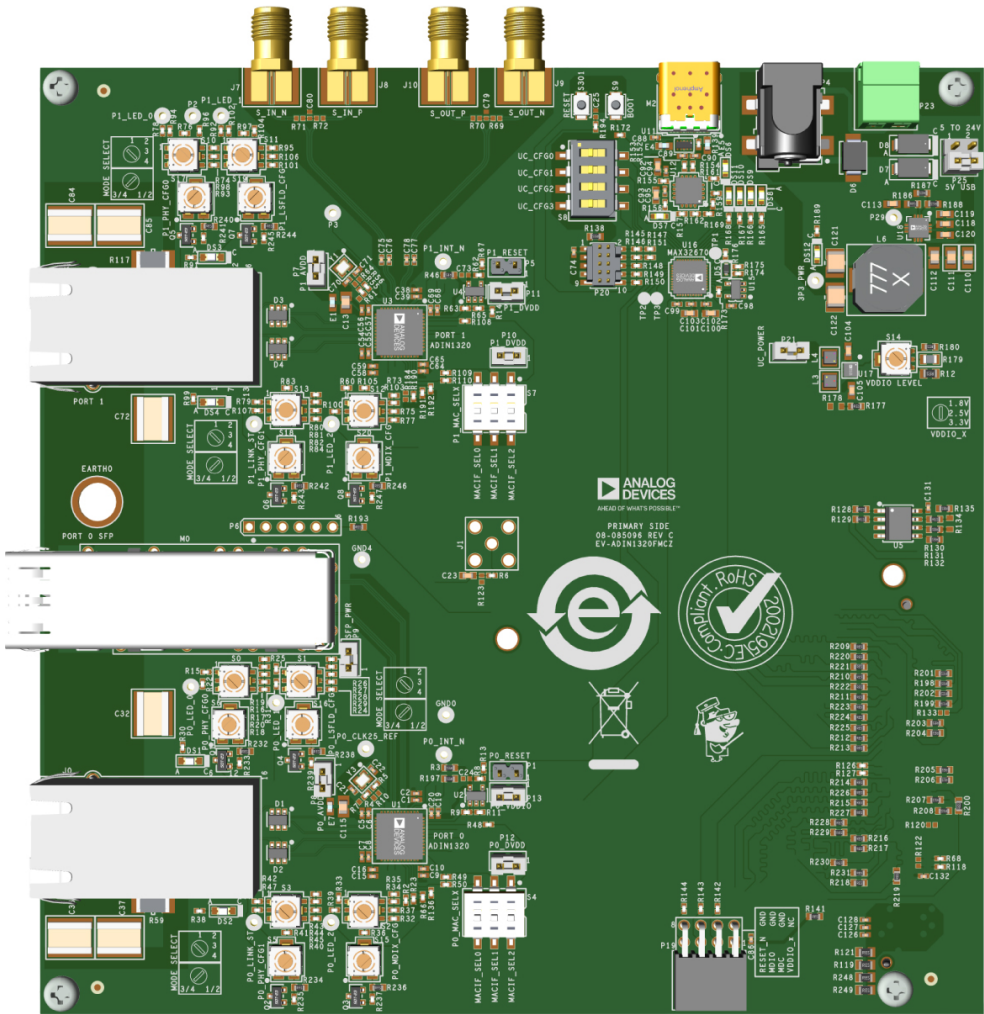


Figure 1. EV-ADIN1320FMCZ Evaluation Board

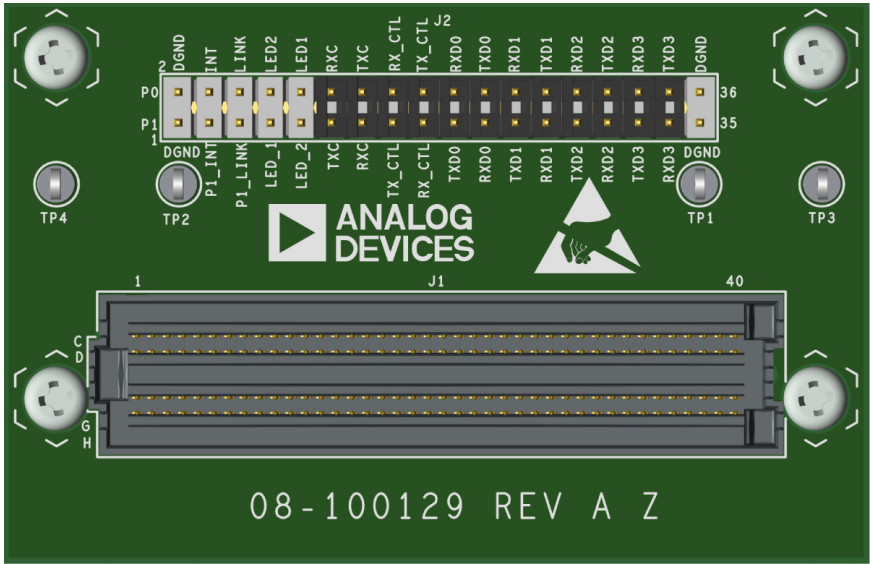


Figure 2. GBPHY-FMC-B2B FMC Expansion Board

HARDWARE OVERVIEW

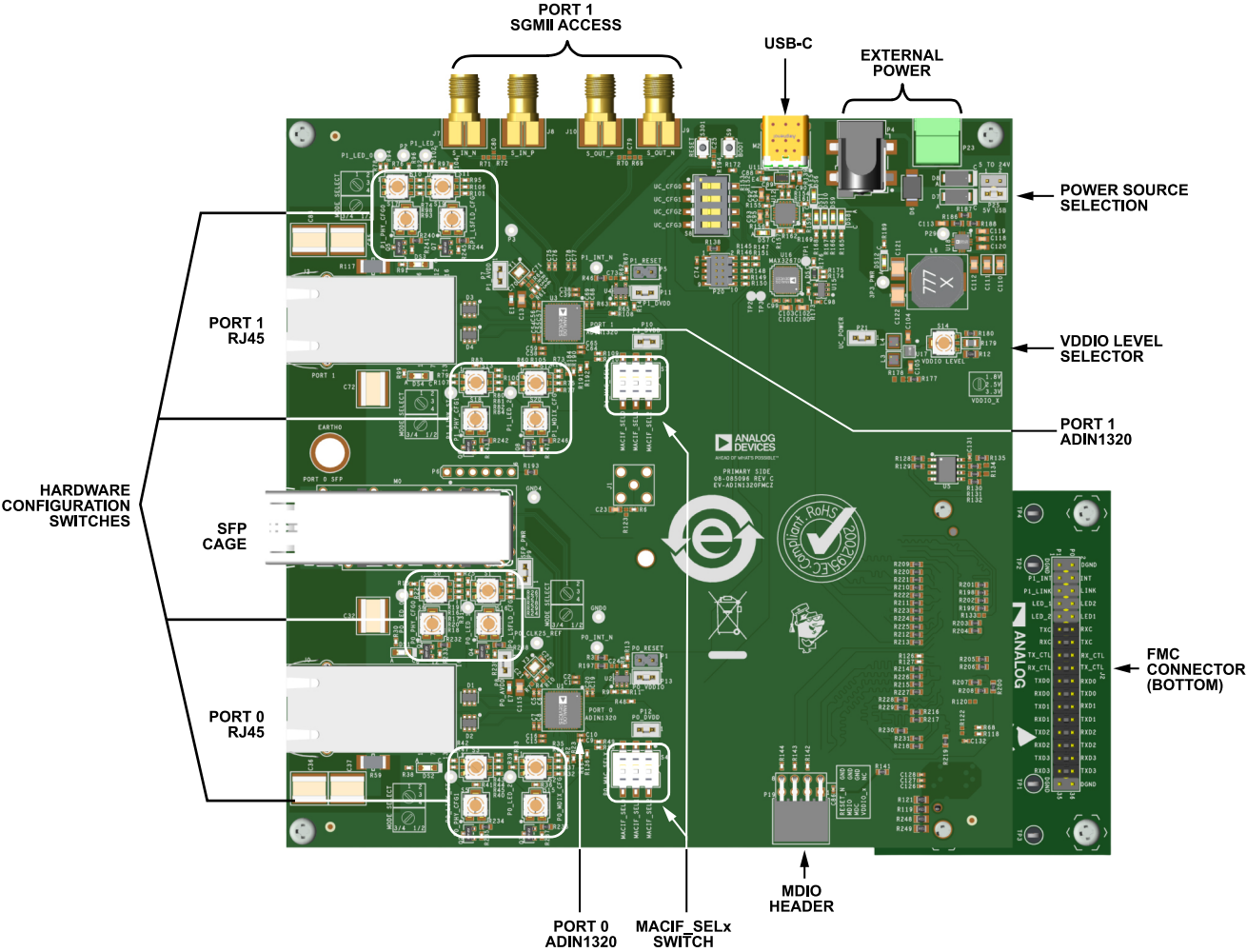


Figure 3. Board Connectors and Controls

EVALUATION BOARD CONTROL COMPONENTS

Table 1. Board Control Components

Reference	Name	Description
S301	Board Reset Button	Push button used to reset the entire evaluation board, which includes the microcontroller and both the ADIN1320 PHYs.
S9	µC Bootload Button	Push button used to place the MAX32670 microcontroller into bootloader mode for firmware updates by USB.
S8	µC CFG	The switch for microcontroller firmware mode of operation. The switch must be set to required combination before power-up or reset. The switch is sampled by firmware only once, short time after the microcontroller reset. All switches must be set to OFF when using the evaluation board with ACE GUI.
R6, R123	EXT_CLK Source Selection	Resistors used to configure the external clock source for the ADIN1320. The clock can be sourced either from the FMC connector or from an on-board SMB connector, which depends on the resistor population. This allows flexible integration with system-level clocking architectures or external test equipment.
P21	µC Power Enable Header	Header that allows enabling or disabling power to the microcontroller section. It can be used to isolate the microcontroller for low-level testing or power measurements.
P25	Board Power Selection	Jumper used to select the power input source for the board: Position 1 to Position 2: Power from screw terminal or barrel (wall wart) jack, Position 3 to Position 4: Power from USB.
S14	VDDIO Level Selector	A 3-position switch used to select the VDDIO voltage level supplied to the ADIN1320 MAC interface and related I/O. Available options are 1.8V, 2.5V, or 3.3V, which allow compatibility with a range of logic level requirements.

Table 2. Board Control Components for Port 0

Reference	Name	Description
R4, R5, R7	XTAL_I Options	Resistors used to configure the external crystal input for Port 0, which select between a crystal oscillator or an external clock.
P1	P0 Force Reset	A jumper used to connect the ADIN1320 to GND for resetting Port 0, which forces the device into a reset state.
P8	3P3 Power	Jumper to supply 3.3V power to the ADIN1320 for Port 0 components.
P12	0P9 Power	Jumper to supply 0.9V power to the ADIN1320 for Port 0 components.
P13	VDDIO Power	Jumper to supply VDDIO Power to the ADIN1320 for Port 0 components.
S4	MAC Interface Configuration	Switch used to select the MAC interface mode for Port 0 (for example, MII, RMII, RGMII, or SGMII). For more details, refer to MAC Interface and Functional Mode Selection table of the ADIN1320 data sheet.
S0, S3	Configuration Switches	Used to set specific configuration options for Port 0. The switches must be set before power-up or reset, as they are sampled when the ADIN1320 comes out of reset. For more details, refer to the Hardware Configuration Pins section of the ADIN1320 data sheet.
S1	LSFLD Mode Selector	Depending on the ADIN1320 mode, this switch is used to configure various link-related settings, which include: ▶ LINK_ST polarity ▶ Enable/Disable fast link down ▶ Enable/Disable Clause 37 auto-negotiation The switch allows customization of the ADIN1320's link behavior for specific operational needs. For detailed mode-specific settings, refer to LED_1 Hardware Configuration Pin table of the ADIN1320 data sheet.
S2	MDIX Mode Selector	This switch configures the MDI/MDIX mode or determines the behavior of the SGMII/RGMII bridge mode, which depends on the set ADIN1320 mode. For more details, refer to LED_2/MDIX_MODE Hardware Configuration table of the ADIN1320 data sheet.
S5, S6, S15, S16	LED Drive Switch	These switches determine how the LEDs should be driven: in MODE_4 and MODE_3, the LEDs should be driven directly from the ADIN1320 LEDx pins, while in MODE_2 and MODE_1, they should be driven through a transistor.
R51, R52, R53, R54	PHY Address	Resistors used to set the PHY address for Port 0. The default address for Port 0 is 0x0. Adjusting these resistors allows for the selection of a unique PHY address for communication between the MAC and the physical layer.
P9	SFP 3.3V Power	Supplies 3.3V power to the SFP module for Port 0 when using fiber or copper SFP.

EVALUATION BOARD CONTROL COMPONENTS

Table 3. Board Control Components for Port 1

Reference	Name	Description
R55, R56, R61	XTAL_I Options	Resistors used to configure the external crystal input for Port 1, which select between a crystal oscillator or an external clock.
P5	P1 Force Reset	A jumper used to connect the ADIN1320 to GND for resetting Port 1, which forces the device into a reset state.
P7	3P3 Power	Jumper to supply 3.3V power to the ADIN1320 for Port 1 components.
P10	0P9 Power	Jumper to supply 0.9V power to the ADIN1320 for Port 1 components.
P11	VDDIO Power	Jumper to supply VDDIO Power to the ADIN1320 for Port 1 components.
S7	MAC Interface Configuration	Switch used to select the MAC interface mode for Port 1 (for example, MII, RMII, RGMII, or SGMII). For more details, refer to MAC Interface and Functional Mode Selection table of the ADIN1320 data sheet.
S10, S13	Configuration Switches	Used to set specific configuration options for Port 1. The switches must be set before power-up or reset, as they are sampled when the ADIN1320 comes out of reset. For more details, refer to the Hardware Configuration Pins section of the ADIN1320 data sheet.
S11	LSFLD Mode Selector	Depending on the ADIN1320 mode, this switch is used to configure various link-related settings, which include: ▶ LINK_ST polarity ▶ Enable/Disable fast link down ▶ Enable/Disable Clause 37 auto-negotiation The switch allows customization of the ADIN1320's link behavior for specific operational needs. For detailed mode-specific settings, refer to LED_1 Hardware Configuration Pin table of the ADIN1320 data sheet.
S12	MDIX Mode Selector	This switch configures the MDI/MDIX mode or determines the behavior of the SGMII/RGMII bridge mode, which depends on the set ADIN1320 mode. For more details, refer to LED_2/MDIX_MODE Hardware Configuration table of the ADIN1320 data sheet.
S17, S18, S19, S20	LED Drive Switch	These switches determine how the LEDs should be driven: in MODE_4 and MODE_3, the LEDs should be driven directly from the ADIN1320 LEDx pins, while in MODE_2 and MODE_1, they should be driven through a transistor.
R111, R112, R113, R114	PHY Address	Resistors used to set the PHY address for Port 1. The default address for Port 0 is 0x8. Adjusting these resistors allows for the selection of a unique PHY address for communication between the MAC and the physical layer.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The evaluation board can be powered from an external 5V to 24V supply by the 4-position terminal block (P23) or the barrel connector (P3). Alternatively, setting the P25 jumper to the appropriate position allows the board to be powered through the USB-C connector. For the power source selection options, see [Table 1](#).

All required power rails are generated on-board using an [ADP2441](#) DC-DC converter and an [ADP5133](#) dual buck regulator. The ADP2441 steps down the external input voltage to 3.3V, which supplies the 3P3_PWR rail. This 3.3V output is then fed to the ADP5133, which generates two additional supply rails:

- ▶ 0P9_PWR (0.9V)
- ▶ VDDIO (selectable 1.8V, 2.5V, or 3.3V)

The VDDIO rail voltage can be configured to either 1.8V, 2.5V, or 3.3V by adjusting S14. For more details on configuring this rail, see [Table 1](#).

POWER SEQUENCING

There are no special power sequencing requirements for the devices. The evaluation board is configured to bring up the power rails together.

MODES OF OPERATION

The EV-ADIN1320FMCZ evaluation board supports multiple modes of operation to show the full flexibility of the [ADIN1320](#) Ethernet PHYs. It features two independent ports, each equipped with its own ADIN1320 device, separate hardware configuration switches, and power domains, which allow both ports to be used simultaneously:

- ▶ Port 0 provides copper Ethernet and includes an SGMII interface by an SFP cage, which supports both fiber and copper SFP and enables flexible media evaluation and interoperability testing.
- ▶ Port 1 provides copper Ethernet and includes an SGMII interface by SMA connectors, suitable for high-speed differential signaling over coaxial cabling or custom setups.

Both ports support MAC interface access through the FMC connector, which exposes RGMII/RMII/MII signals for easy connection to FPGAs or other MAC devices.

Each port's mode is determined by the settings of its switches and resistors:

- ▶ For Port 0, the combination of S4, S0, and S3 sets the operational mode, while S1, S2, and the PHY address resistors provide additional configuration for link behavior and address assignment.
- ▶ Similarly, for Port 1, S7, S10, S13, S11, S12, and the PHY address resistors configure the operational mode and link settings.

Proper configuration of the switches and PHY address resistors are essential for ensuring the correct operation of the board in the

required mode. Configuration must be completed before power-up or reset.

Supported modes of operation include:

- ▶ RGMII/RMII/MII/SGMII to copper PHY
- ▶ RGMII/RMII/MII to fiber PHY
- ▶ RGMII/RMII/MII to copper/fiber (auto media detect)
- ▶ Media converter mode copper PHY and fiber PHY
- ▶ Bridge mode between RGMII and SGMII

This wide range of operating modes enable the evaluation board to function in diverse scenarios, such as MAC Interface bridging, MAC-to-PHY interfacing, and copper-to-fiber media conversion. The on-board SGMII interfaces (by SFP or SMA) further enhance compatibility with a range of test setups and system architectures.

For more details on hardware configuration and mode selection for each operating mode, refer to the Hardware Configuration Pins section of the ADIN1320 data sheet.

COPPER PHY CORE

The EV-ADIN1320FMCZ evaluation board is equipped with two ADIN1320 PHYs, each supporting copper Ethernet connectivity. Each port features a dedicated RJ45 Ethernet connector with integrated magnetic for network access. The integrated magnetic provides electrical isolation and maintain signal integrity in compliance with Ethernet standards, while the TVS diode offers protection against transient voltage spikes, which improves the interface's resilience in electrically noisy environments. This setup supports 10Mbps/100Mbps/1000Mbps speeds based on the capabilities of the PHY, which ensures reliable and flexible copper Ethernet performance across both ports.

SERDES SUBSYSTEM

The evaluation board provides multiple options for evaluating the SERDES subsystem, which leverages both SFP and SMA connectors.

Port 0 supports SGMII connectivity by an SFP cage, which enables the use of both fiber and copper SFPs for versatile media evaluation. To power the SFP module, the 3P3_PWR supply rail is used, and a jumper must be inserted at P9 to ensure proper power delivery to the SFP module.

Port 1 offers SGMII connectivity through an SMA connector, which enables high-speed differential signaling for custom setups or external testing.

EVALUATION BOARD HARDWARE

MAC INTERFACE

The EV-ADIN1320FMCZ evaluation board provides several options for evaluating the MII, RMII, RGMII, and SGMII interfaces of the ADIN1320 PHY.

Both ports on the board are equipped with ADIN1320 PHYs and support RGMII, RMII, and MII interfaces through the FMC connector, which allow connection to external systems such as FPGAs or other MAC devices.

For SGMII connectivity, SMA connectors are available, which enable the direct communication with external SGMII devices.

This setup provides flexible evaluation capabilities for a wide range of Ethernet configurations, suitable for various testing and development scenarios.

FMC CONNECTOR

The EV-ADIN1320FMCZ evaluation board includes an FMC connector that provides access to the MAC interface signals of both ADIN1320 PHYs. This connector enables seamless integration with FMC-compatible FPGA or SoC platforms, which allow system-level evaluation and development of Ethernet-based applications.

The FMC interface routes relevant MAC-side signals, which include RGMII, RMII, and MII, which makes it suitable for a wide range of configurations. For enhanced flexibility, the included GBPHY-FMC-B2B expansion board breaks out these signals to male header pins, which enable signal probing for debugging and analysis, and back-to-back PHY connection between the two ADIN1320.

This design simplifies evaluation and accelerates prototyping by providing both direct FMC connectivity and accessible breakout points for advanced testing scenarios. By default, the jumpers in the GBPHY-FMC-B2B connects the two ADIN1320 in RGMII back-to-back connection.

STATUS LED PIN

The EV-ADIN1320FMCZ evaluation board features configurable status LEDs that provide visual indicators for operational states. These LEDs can also serve as indicators for link status, activity, or speed of operation, with their behavior adjustable in software to suit different modes of operation.

The following LEDs are available on the evaluation board:

- ▶ LED_0: connected to the PHY_CFG0 pin, this LED indicates the PHY configuration status. By default, LED_0 illuminates when a link is established and blinks during activity.
- ▶ LED_1: provides status for a 1Gbps link. It illuminates when a 1Gbps connection is active.
- ▶ LED_2: indicates a 100Mbps link status. LED_2 lights up when a 100Mbps connection is established.
- ▶ LINK_ST: integrated with the RJ45 connector, the LINK_ST pin shows the link status by the on-board LED in the RJ45 jack. The LINK_ST LED reflects whether a link is established.

These default behaviors, such as LED_0 illuminating for an active link and blinking during activity, LED_1 lighting up for a 1Gbps connection, and LED_2 showing a 100Mbps link can be modified in software and may vary depending on the mode of operation. This behavior can vary between modes and can be changed in software. The polarity of each LED can be configured by the management data input/output (MDIO) registers for the ADIN1320 PHY if needed.

CLOCK OPTIONS

The EV-ADIN1320FMCZ evaluation board provides flexible options for supplying the required clock to the ADIN1320 PHYs. Each port supports operation from either an on-board crystal oscillator or an external clock source, which allow users to tailor the setup for standalone evaluation or system-level integration.

On-Board Clocking

By default, both ADIN1320 ports are configured to use on-board crystal oscillators:

- ▶ Port 0:
 - ▶ A 25MHz crystal (Y3) is connected across the XTAL_I and XTAL_O pins.
 - ▶ The clock input path can be configured using resistors R4, R5, and R7, which allow selection between the crystal oscillator and an external clock.
- ▶ Port 1:
 - ▶ A 25MHz crystal (Y5) is connected across the XTAL_I and XTAL_O pins.
 - ▶ Clock source selection is configured by R55, R56, and R61.

These configurations support typical use cases without requiring any external signal sources.

External Clock Input

Each port also supports external clocking for advanced timing scenarios:

- ▶ External clocks can be applied through connector J1 (Port 0) or P4 (shared or Port 1), which depend on board routing.
- ▶ The source of the clock is selectable through population/depopulation of specific resistors (R6 and R123) to switch between on-board and off-board sources.

This flexibility allows integration into synchronized systems or precise timing environments.

EVALUATION BOARD HARDWARE

Clock Output Options

The [ADIN1320](#) can also be configured to output a 25MHz reference clock on the CLK25_REF pin. This output can be routed to another device (such as a second PHY) to act as a shared clock source. The default clock driving this output is the crystal connected to the ADIN1320 (Y3 or Y5, which depends on port).

Additionally, the GP_CLK pin, available on connector P4, can be configured via register settings to output a variety of clocks for diagnostic or system synchronization purposes.

MAX32670

The EV-ADIN1320FMCZ evaluation board features the [MAX32670](#) microcontroller, which plays a key role in managing and configuring the on-board ADIN1320 Ethernet PHYs. By default, the MAX32670 facilitates communication with the ACE software GUI, providing users with an intuitive interface for device setup, configuration, and monitoring. Through the MDIO interface, the MAX32670 enables communication with the PHYs, allowing developers to adjust essential parameters such as link speed, auto-negotiation, and operational modes. Additionally, it provides capability to issue a HW reset to the ADIN1320 PHYs, ensuring proper initialization.

In addition to GUI-based operation, users have the flexibility to download custom firmware onto the MAX32670 using Analog Devices NO-OS drivers and example projects. This enables the implementation of automated configuration routines or application-specific control without reliance on the GUI. By leveraging the MDIO interface, the microcontroller offers access to PHY registers, simplifying configuration, and debugging, while providing the flexibility to optimize overall system performance.

MDIO HEADER

The EV-ADIN1320FMCZ evaluation board includes an MDIO header (P19), which enables the connection of an external MDIO interface to the on-board ADIN1320 Ethernet PHYs. This header allows external devices to communicate with the PHYs, which provide the ability to configure, monitor, and control the PHYs remotely, thus enhancing the flexibility of the evaluation setup. Note that the MAX32670 must be powered down when using external MDIO driver.

SOFTWARE QUICK START PROCEDURES

ACCESSING ACE SOFTWARE FOR ADIN1320 EVALUATION

To evaluate the [ADIN1320](#), do the following steps:

1. Download and install the ACE software.
2. Run the ACE software.
3. The ADIN1320 plug-in must be automatically listed in **Plug-in Manager**. If a user does not find it, refresh the plug-ins and install the new ADIN1320 plug-ins listed under available packages.
4. Connect a USB cable from the PC to the EV-ADIN1320FMCZ evaluation board. The board can be powered via USB. Ensure jumper P25 is set to the 5V USB position to enable this.
5. The board appears as **Attached Hardware** (see [Figure 4](#)). To continue, double click the **ADIN1320 Board** window.

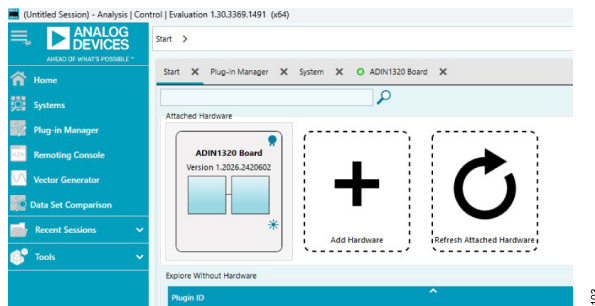


Figure 4. ACE Evaluation Software—Attached Hardware

USING THE SOFTWARE FOR EVALUATION

ADIN1320 Board View

The **Board** view in ACE (see [Figure 5](#)) provides a graphical representation of the EV-ADIN1320FMCZ evaluation board, showing the location and connectivity of key components. It displays the two ADIN1320 PHY devices (Port 0 and Port 1), each connected to RJ45 interfaces, with Port 0 also supporting an SFP cage and Port 1 providing SMA connectors for SGMII access. The USB interface, on-board [MAX32670](#) microcontroller, and power block are also shown.

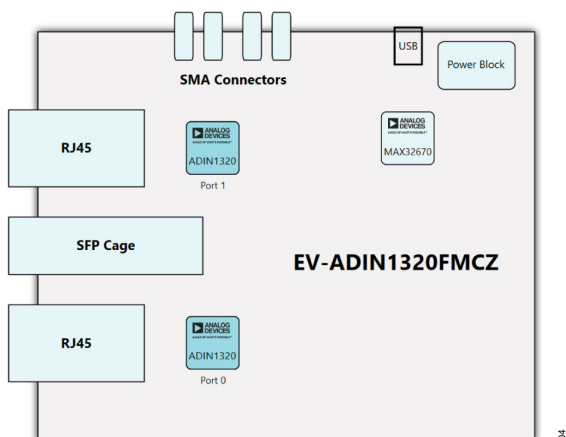


Figure 5. ADIN1320 Board View

In the **Board** view, active ADIN1320 device blocks are highlighted. Selecting a block opens the device view with control panels that reflect the device hardware strap configuration and operating mode.

Device Status and Control Tab

The **Device Status and Control** view provides a summary of the current PHY operating state along with access to commonly used control functions.

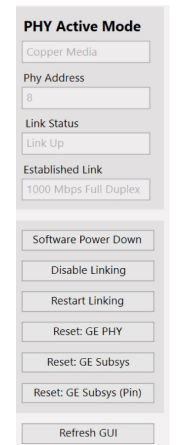


Figure 6. Device Status and Control

The status section displays key information for the selected ADIN1320 device, including the **PHY Active Mode** (**Copper Media**, **Fiber/Backplane Media**, **Media Converter**, or **Bridge Mode**), **PHY Address**, **Link Status**, and **Established Link** speed and duplex. This information provides a real-time indication of link activity and configuration.

The control section includes buttons for direct interaction with the device. These allow the user to place the PHY into **Software Power Down**, **Disable Linking** or **Restart Linking** operation, and perform reset actions. Available reset options include **Reset: GE PHY**, **Reset: GE Subsys**, and **Reset: GE Subsys (Pin)**, enabling reinitialization of the device.

A **Refresh GUI** option is also provided to update the displayed values and ensure the interface reflects the current hardware state.

Link Properties Tab

The **Link Properties** view provides configuration and real-time status monitoring for the selected ADIN1320 PHY port. The content of this view depends on the active operating mode of the ADIN1320 device.

SOFTWARE QUICK START PROCEDURES

Copper Media Mode

Figure 7 shows the **Link Properties** view in **Copper Media** mode, which provides configuration and real-time status monitoring for copper Ethernet operation of the ADIN1320.

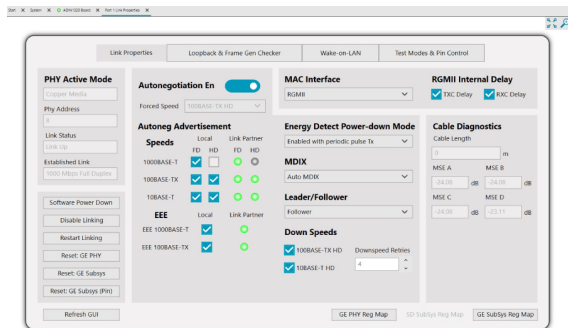


Figure 7. Link Properties—Copper Media Mode

The main configuration area allows control of autonegotiation, including enabling or disabling autonegotiation and selecting advertised speeds and duplex modes for 10BASE-T, 100BASE-TX, and 1000BASE-T. The interface also shows local and link partner capabilities, allowing users to verify negotiation results. Energy efficient Ethernet (EEE) settings are available for supported speeds, with status indication for both local and link partner.

Additional controls include **MAC Interface** selection and configuration of **RGMII Internal Delay** for transmit and receive clock alignment. The view also provides options for **MDIX** configuration, **Leader/Follower** selection, and **Down Speeds** control, as well as **Energy Detect Power-down Mode** for power savings.

The **Cable Diagnostics** section provides physical layer insight, including estimated **Cable Length** and mean square error (**MSE**) measurements for each cable pair, enabling link quality analysis.

This view consolidates all controls and diagnostics required for evaluating and configuring the ADIN1320 in copper Ethernet applications.

Fiber Media Mode

Figure 8 shows the **Link Properties** view in **BackPlane/Fiber Media** mode, which provides configuration and status monitoring for SerDes-based operation of the ADIN1320.

The main configuration area provides speed mode selection for supported SerDes standards, including **1000BASE-X** (full- and half-duplex), **1000BASE-KX**, and **100BASE-FX**. The selected mode defines the active link configuration. The interface also displays **Link Partner Speeds** status, allowing verification of the negotiated link parameters.

Additional configuration includes **MAC Interface** selection and **RGMII Internal Delay** settings (if selected) for transmit and receive clock alignment.

The layout is simplified to present only the controls and status relevant to SerDes-based links. This view provides the necessary controls and visibility for evaluating the ADIN1320 in fiber and backplane Ethernet applications.

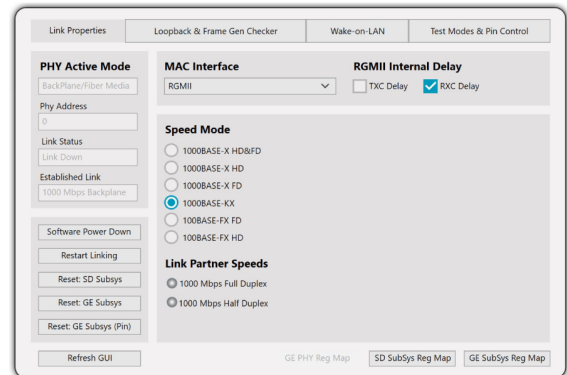


Figure 8. Link Properties—Fiber Media Mode

Media Converter

Figure 9 shows the **Link Properties** view in **Media Converter** mode, which enables the ADIN1320 to operate as a bridge between copper and fiber interfaces.

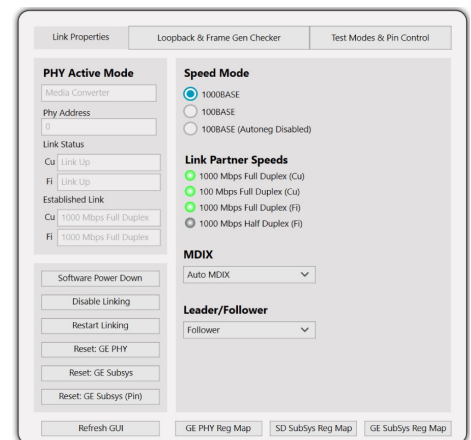


Figure 9. Link Properties—Media Converter Mode

The left panel displays PHY status information for both interfaces, including separate **Link Status** indicators for copper (**Cu**) and fiber (**Fi**), along with the **Established Link** speed and duplex for each side. This provides a clear view of the independent link conditions on both media types.

The main configuration area allows selection of the operating speed, such as **1000BASE** or **100BASE**, with an option to operate without autonegotiation. The interface also displays **Link Partner Speeds** information for both copper and fiber links, enabling verification of link establishment on each side of the converter.

Additional controls include **MDIX** configuration and **Leader/Follower** selection for the copper interface, which define device roles during link establishment. Standard control functions, such as **Soft-**

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ware Power Down, Restart Linking, and Reset options, are also available.

This view provides a consolidated interface for configuring and monitoring the ADIN1320 in media converter applications, allowing simultaneous visibility and control of both copper and fiber links.

Bridge Mode

Figure 10 shows the Link Properties/device view in Bridge Mode, where the ADIN1320 operates as a bridge between SGMII and RGMII MAC interfaces.

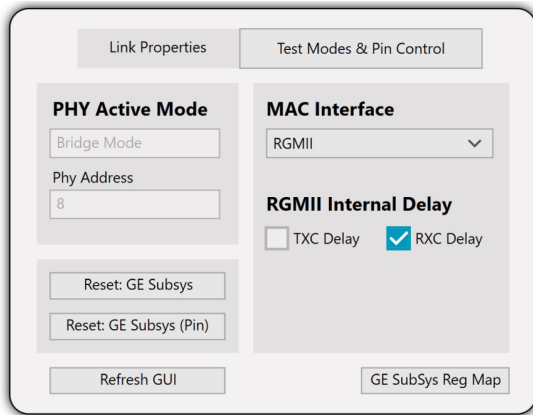


Figure 10. Link Properties—Bridge Mode

The left panel displays basic PHY information, including the **PHY Active Mode (Bridge Mode)** and **PHY Address**. Unlike other ADIN1320 modes, link-specific status is not the primary focus, as the device operates in a MAC interface bridging configuration rather than a media-dependent link mode.

The main configuration area provides control of the **MAC Interface** selection (**SGMII** or **RGMII**) used to connect to the host MAC. The selected interface defines the direction of MAC connectivity, while the opposite interface is expected to be connected to a PHY. This configuration ensures the ADIN1320 correctly routes data and handles in-band status signaling between interfaces. Additional configuration includes **RGMII Internal Delay** settings for transmit (**TXC Delay**) and receive (**RXC Delay**) clock alignment to ensure proper timing between the PHY and MAC.

Loopback and Frame Generator and Checker Tab

Figure 11 shows the Loopback & Frame Gen Checker view, which provides tools for validating data paths, performing loopback tests, and generating and analyzing Ethernet frames within the ADIN1320.

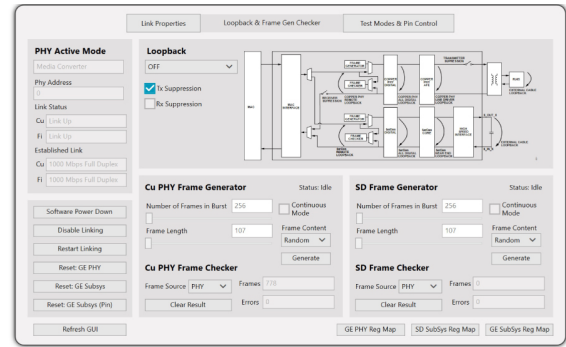


Figure 11. Loopback and Frame Generator/Checker

The top section includes a **Loopback** configuration panel and a block diagram, illustrating the available loopback paths through the device. The **Loopback** selector allows users to enable different internal and external loopback modes, while **TX Suppression** and **RX Suppression** options provide control over transmit and receive data paths during test scenarios.

The left panel continues to display PHY status information, including **PHY Active Mode**, **PHY Address**, **Link Status** for copper (**Cu**) and fiber (**Fi**), and **Established Link** parameters. Standard control buttons are also available for **Software Power Down**, **Disable/Restart Linking** control, **Reset** operations, and **Refresh GUI**.

The lower section provides frame generation and checking capabilities for both the copper PHY (**Cu**) and SerDes (**SD**) paths. The **Frame Generator** allows configuration of test traffic, including:

- **Number of Frames in Burst or Continuous Mode**
- **Frame Length**
- **Frame Content**

Generated frames can be injected into the selected data path for validation.

The **Frame Checker** monitors received frames and provides statistics such as total frames received and error counts. Options are provided to select the **Frame Source** and to **Clear Result** for repeated testing.

This view provides a comprehensive environment for link validation, data path testing, and diagnostic evaluation, enabling users to verify correct operation of the ADIN1320 across both copper and SerDes interfaces.

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Wake-On-Lan Tab

Figure 12 shows the **Wake-on-LAN (WoL)** view, which provides configuration options for enabling and customizing wake-up events based on network activity.

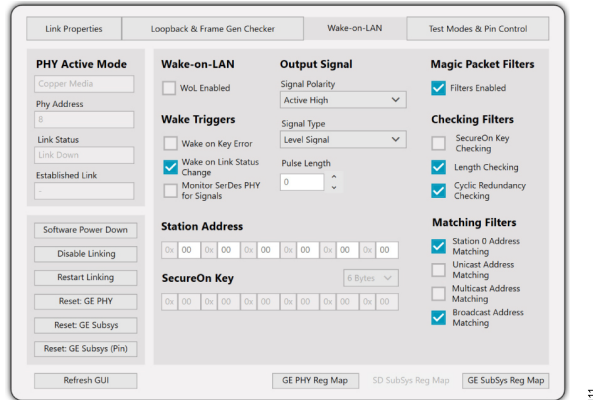


Figure 12. Wake-On-Lan Tab

The **Wake-on-LAN** section allows the feature to be enabled and configured. Users can select different **Wake Triggers**, such as **Wake on Key Error**, **Wake on Link Status Change**, or **Monitor SerDes PHY for Signals**. These options define the conditions under which the ADIN1320 asserts a wake event.

The **Output Signal** section controls how the wake event is signaled externally. This includes configuration of **Signal Polarity** (for example, **Active High**), **Signal Type** (level or pulse), and **Pulse Length**, allowing integration with system-level power management logic.

The **Magic Packet Filters** section enables filtering of incoming packets to identify valid wake events. Additional checking filters can be applied, including **SecureOn Key Checking**, packet **Length checking**, and **Cyclic Redundancy Checking (CRC)** verification to ensure only valid wake packets trigger an event.

The **Matching Filters** section defines which packet types can trigger a wake event, including **Station 0 Address Matching**, **Unicast Address Matching**, **Multicast Address Matching**, and **Broadcast Address Matching**. The **Station Address** and optional **SecureOn Key** fields allow configuration of the target MAC address and security key used for magic packet detection.

The left panel continues to display PHY status information and provides standard control options such as **Software Power Down**, **Disable/Restart Linking** control, **Reset** operations, and **Refresh GUI**. This view provides a complete interface for configuring and validating Wake-on-LAN functionality on the ADIN1320, allowing precise control over wake sources, filtering, and signaling behavior.

Test Modes and Pin Control Tab

Figure 13 shows the **Test Modes & Pin Control** view, which provides access to PHY test configurations, pin-level control, and register debugging features.

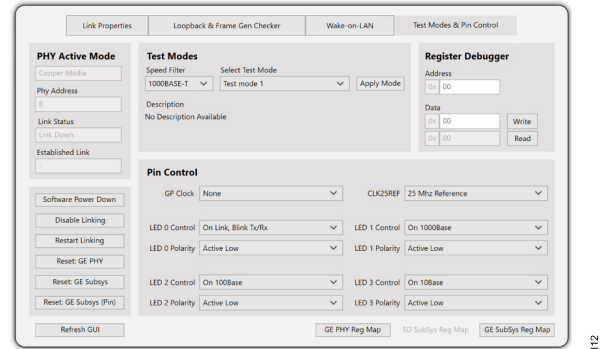


Figure 13. Test Modes and Pin Control Tab

The **Test Modes** section allows selection of standardized PHY test modes used for compliance and validation. The **Speed Filter** is used to limit the available test modes, and the **Select Test Mode** can be applied using the **Apply Mode** control. The associated waveform generation for these test modes is only available in copper (Cu) mode, as these tests are specific to copper Ethernet physical layer validation.

The **Pin Control** section provides configuration of various output pins and indicators. This includes general-purpose clock (**GP Clock**) and **CLK25REF** output selection, along with configuration of LED behavior (**LED0** to **LED3**). Each LED can be assigned specific functions (for example, link status or speed indication) and configured for active high or active low polarity, allowing flexible system-level integration.

The **Register Debugger** section allows direct access to device registers. Users can read from or write to specific register addresses by entering the address and data values, providing a low-level interface for debugging and advanced configuration.

The left panel continues to display PHY status information and provides standard device control options such as **Software Power Down**, **Disable/Restart Linking** control, **Reset** operations, and **Refresh GUI**.

This view provides a comprehensive interface for PHY compliance testing, pin configuration, and low-level debugging, with test mode waveform features specifically available when operating in copper mode.

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Register Access

The ACE plug-in provides direct access to the [ADIN1320](#) register maps for advanced configuration, debugging, and status monitoring. Register access is available from all device views through the buttons located in the lower-right corner of the interface (**GE PHY Reg Map**, **SD SubSys Reg Map**, and **GE SubSys Reg Map**).

Depending on the active operating mode, users can access the following register maps:

- ▶ **GE PHY Reg Map**—opens the Gigabit Ethernet PHY register map, providing access to standard and vendor-specific PHY registers.
- ▶ **SD SubSys Reg Map**—opens the SerDes subsystem register map, providing access to registers associated with the ADIN1320

SerDes functionality. This option is available only when the selected operating mode includes SerDes functionality.

- ▶ **GE SubSys Reg Map**—opens the Gigabit Ethernet subsystem register map, providing access to subsystem-level configuration and status registers.

Each register map view allows users to browse registers by address, view current register contents, and modify register fields where appropriate. Changes made through the register maps are applied directly to the selected ADIN1320 device, enabling detailed investigation and configuration beyond the controls exposed in the graphical interface.

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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