Evaluating the ADGM3144 0Hz/DC to 30GHz, SP4T, MEMS Switch

FEATURES

- Single-supply voltage: 3.3V
- Wide frequency range: DC to 30GHz
- 2.92mm connectors for RF signals
- Parallel interface and SPI
- On-board calibration through transmission line for analyzer calibration

EVALUATION KIT CONTENTS

- EVAL-ADGM3144SDZ evaluation board
- 2m USB 2.0 (male) to Mini-USB (male) cable

ADDITIONAL EQUIPMENT NEEDED

- 3.3V DC power supply or USB port
- Vector network analyzer (VNA)
- EVAL-SDP-CB1Z (SDP-B) controller board
- Analysis | Control | Evaluation (ACE) Software with EVAL-ADGM3144SDZ plugin

GENERAL DESCRIPTION

This user guide describes the EVAL-ADGM3144SDZ for the ADGM3144, a dual-chip, RF switching solution containing a single-pole, four-throw (SP4T), microelectromechanical systems (MEMS) switch, and a control chip co-packaged in a compact, 3.00mm × 3.00mm × 1.50mm, LGA package.

The SP4T switch uses Analog Devices, Inc., MEMS switch technology, providing optimum performance in terms of bandwidth, power handling capability, and linearity for RF applications. The control chip generates the high-voltage signals needed for the MEMS switch and allows the user to control its operation through a simple and flexible complementary metal-oxide semiconductor (CMOS)/low voltage transistor to transistor logic (LVTTL)-compliant parallel-interface as well as through a serial-peripheral interface (SPI). It is possible to daisy-chain multiple ADGM3144 devices together to enable the configuration of multiple devices with a minimal number of digital lines.

For SPI, the EVAL-ADGM3144SDZ connects to the USB port of a PC through the system demonstration platform (SDP) board. The EVAL-SDP-CB1Z board (SDP-B controller board) is available to order at the Analog Devices website.

The ADGM3144 comes fitted with connectors for RF and control signals as well as links to control the operation of the switch and evaluate its performance.

For full details on the ADGM3144, see the ADGM3144 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADGM3144SDZ.

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REVISION HISTORY

12/2025—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

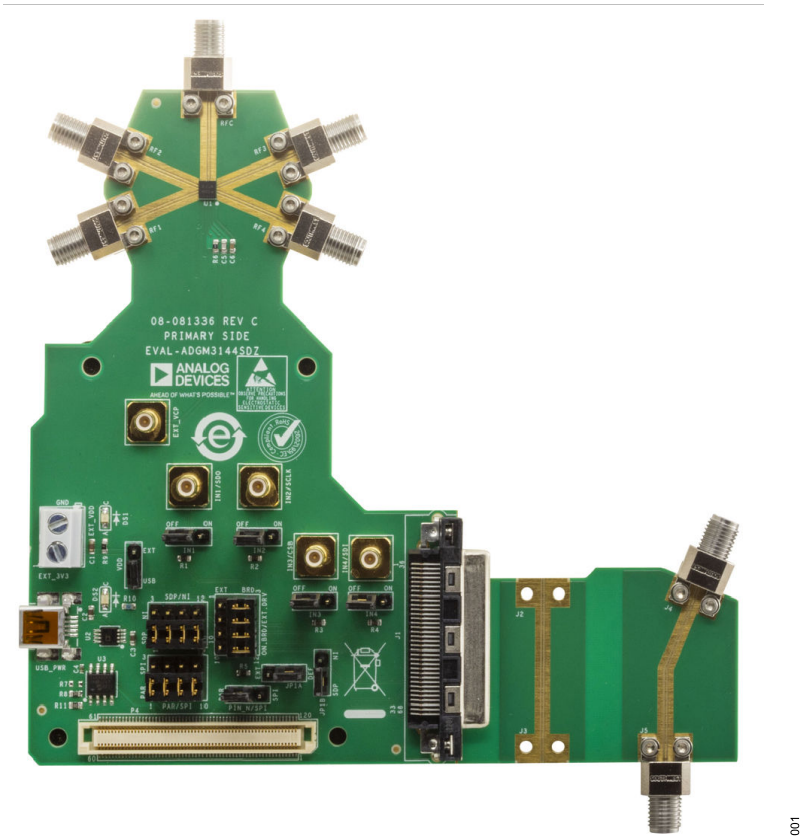

Figure 1. EVAL-ADGM3144SDZ Evaluation Board Photograph

EVALUATION BOARD HARDWARE

The EVAL-ADGM3144SDZ evaluation kit contains a fully fitted printed circuit board (PCB).

The EVAL-ADGM3144SDZ allows the user to connect RF signals to the MEMS switch. The user controls the switch operation using the on-board links or by applying the correct control signals to the appropriate connectors.

The EVAL-ADGM3144SDZ provides an additional transmission line to facilitate the calibration of the network analyzer to minimize the effects of the PCB tracks that connect the RF signals to the MEMS switch. See the Network Analyzer Calibration Procedure section for more information on the calibration process.

POWER SUPPLY

To operate the EVAL-ADGM3144SDZ, the user must provide an external power supply either through a Mini-USB connector (USB_PWR) or through the power block (EXT_3V3). When the VDD link is in the USB_PWR position, the EVAL-ADGM3144SDZ is powered by the Mini-USB connector, and when the VDD link is in the EXT_3V3 position, the EVAL-ADGM3144SDZ is powered by the external 3.3V power supply through the power block (see Table 1). The power-supply voltage required for the EVAL-ADGM3144SDZ is 3.3V, and it must be positive with respect to the ground of the EVAL-ADGM3144SDZ. The ground of the EVAL-ADGM3144SDZ is marked with GND on the silkscreen (see Figure 22).

Table 1. VDD Link Position

Position	Power Supply Selection
USB_PWR	EVAL-ADGM3144SDZ powered by the Mini-USB
EXT_3V3	EVAL-ADGM3144SDZ powered by the external 3.3V power supply

RF CONNECTORS

The 2.92mm end launch connectors on the EVAL-ADGM3144SDZ (RF1, RF2, RF3, RF4, and RFC) connect to each switch in the ADGM3144 for performance evaluation. The J2 and J3 or J4 and J5 connectors connect to a transmission line to estimate the loss associated with the PCB (see the Measuring Switch Performance section). Table 2 describes the RF connectors to the ADGM3144.

Table 2. Connecting the RF Connectors to the ADGM3144

Connector	Description
RF1	Port RF1 of the ADGM3144
RF2	Port RF2 of the ADGM3144
RF3	Port RF3 of the ADGM3144
RF4	Port RF4 of the ADGM3144
RFC	Common RFC port of the ADGM3144
J2, J3 or J4, J5	Calibration thru transmission lines used for calibration

SWITCH CONTROL CONNECTORS

The EVAL-ADGM3144SDZ can either be controlled through an on-board parallel interface and an off-board SPI or parallel-interface through the SDP connector (P4).

On-Board or Off-Board Digital Control

The EVAL-ADGM3144SDZ can be controlled via the on-board parallel interface or by connecting to a USB port of a PC through the SDP connector (P4). Links ON.BRD/EXT.DRV (Table 3), PAR/SPI (Table 4), and JP1A (Table 5) should be set accordingly to enable either on-board or off-board digital control.

Table 3. ON.BRD/EXT.DRV Link Position

Position	Digital Control Interface Setting
BRD (Default)	Digital control pins IN1 to IN4 are controlled on-board
EXT	Digital control pins IN1 to IN4 are controlled via SDP connector (P4)

Table 4. PAR/SPI Link Position (When link JP1A is in EXT position and ON.BRD/EXT.DRV is in EXT position)

Position	ADGM3144 Digital Control Interface Setting
PAR (Default)	Parallel-interface programming via SDP connector (P4)
SPI	SPI programming via SDP connector (P4)

The ADGM3144's PIN_N/SPI (Pin 19) can be controlled either on-board or via an SDP connector (P4). This is controlled by link JP1A (see Table 5).

When link JP1A is set to the DEF position, control of Pin 19 is done through link PIN_N/SPI. When link PIN_N/SPI is set to PAR position, the parallel-interface is enabled. When PIN_N/SPI is set to SPI position, SPI control is enabled. See Table 6.

When link JP1A is set to EXT position, control of Pin 19 is done through the SDP connector (P4). Refer to the Evaluation Board Software for the SPI section on how to program Pin 19 via Analog Devices ACE software.

Table 5. JP1A Link Position

Position	PIN/N/SPI Control Interface Setting
DEF (Default)	PIN_N/SPI controlled on-board
EXT	PIN_N/SPI controlled via SDP connector (P4)

Table 6. PIN_N/SPI Link Position (When link JP1A is in DEF position)

Position	ADGM3144 Control Interface Setting
PAR (Default)	Parallel-interface enabled
SPI	SPI enabled, parallel-interface disabled

EVALUATION BOARD HARDWARE

Parallel On-Board Control

The EVAL-ADGM3144SDZ comes with an on-board standard LVTTL parallel-interface consisting of four input pins (IN1, IN2, IN3, and IN4) controlled by the IN1, IN2, IN3, and IN4 links. See Table 7 for more details on the logic control when using the parallel-interface. Link JP1A should be moved to the default DEF position (see Table 5). Link PIN_N/SPI should be moved to PAR position (see Table 6).

Table 7. Link Settings (Per PCB Label) for Parallel-Interface Use

Link Name	Link Position	RF Switch Status
IN1	OFF (default)	RF1 to RFC = OFF
	ON	RF1 to RFC = ON
IN2	OFF (default)	RF2 to RFC = OFF
	ON	RF2 to RFC = ON
IN3	OFF (default)	RF3 to RFC = OFF
	ON	RF3 to RFC = ON
IN4	OFF (default)	RF4 to RFC = OFF
	ON	RF4 to RFC = ON

SPI Control via SDP Connector

The EVAL-ADGM3144SDZ also has SPI that can be controlled by connecting to the USB port of a PC through the SDP board connected to the SDP connector (P4).

Link JP1A can be either set to the default DEF or EXT position (see Table 5). If link JP1A is in the DEF position, link PIN_N/SPI should be moved to SPI position to enable SPI control (see Table 6). If link JP1A is in the EXT position, refer to the Evaluation Board Software for the SPI section on how to program PIN_N/SPI for SPI control.

Links ON.BRD/EXT.DRV (Table 3) should be moved to EXT.DRV position and PAR/SPI (Table 4) should be moved to SPI position to control EVAL-ADGM3144SDZ via the SDP connector.

Parallel Control via SDP Connector

The EVAL-ADGM3144SDZ can be programmed with parallel interface using the SDP connector (P4).

Link JP1A can be either set to the default DEF or EXT position (see Table 5). If link JP1A is in the DEF position, link PIN_N/SPI should be moved to PAR position to enable parallel-interface control (see Table 6). If link JP1A is in the EXT position, refer to the Evaluation Board Software for the SPI section on how to program PIN_N/SPI for parallel-interface control.

Links ON.BRD/EXT.DRV (Table 3) should be moved to EXT.DRV position and PAR/SPI should be moved to PAR (Table 4) position to control EVAL-ADGM3144SDZ via the SDP connector.

EVALUATION BOARD SOFTWARE FOR THE SPI

INSTALLING THE SOFTWARE

The ADGM3144 uses the Analog Devices ACE software, a desktop software application that allows the evaluation and control of multiple evaluation systems.

The ACE software installer installs the necessary SDP drivers and .NET Framework 4 by default. Install the ACE software before connecting the SDP driver. The Analog Devices website provides the ACE software and access to full instructions on how to install and use it.

After the installation completes, the ADGM3144 plugin appears when opening the ACE software.

INITIAL SETUP

Complete the following steps to set up the ADGM3144:

1. Set link JP1A (Table 5) to EXT position.
2. Set link ON.BRD/EXT.DRV (Table 3) to EXT position.
3. Set link PAR/SPI Table 4 to either PAR or SPI depending on the digital control interface used.
4. Connect the ADGM3144 to the SDP board and connect the SDP board to the computer through a USB cable.
5. Power the ADGM3144, as described in the Power Supply section.
6. Run the ACE software. The ADGM3144 plugins appear in the **Attached Hardware** window of the **Start** tab (see Figure 2).
7. Double-click the EVAL-ADGM3144SDZ plugins to open the evaluation board view in Figure 3.
8. The chip block diagram can be accessed by double-clicking the **ADGM3144** chip (see Figure 3). The view after clicking the **ADGM3144** chip provides a basic representation of the functionality of the **ADGM3144**. The main functions are labeled in Figure 4.

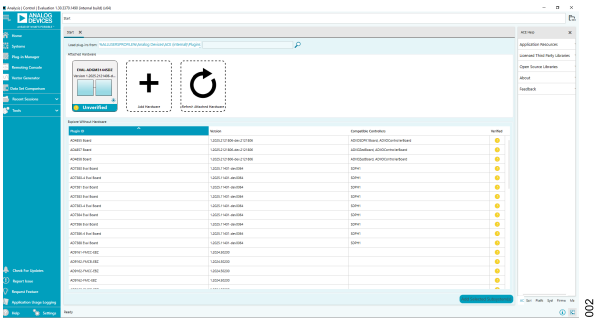

Figure 2. EVAL-ADGM3144SDZ Plugin Start-Up Window

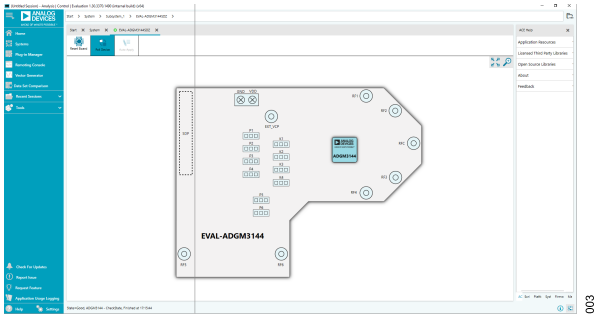

Figure 3. Evaluation Board View of the EVAL-ADGM3144SDZ

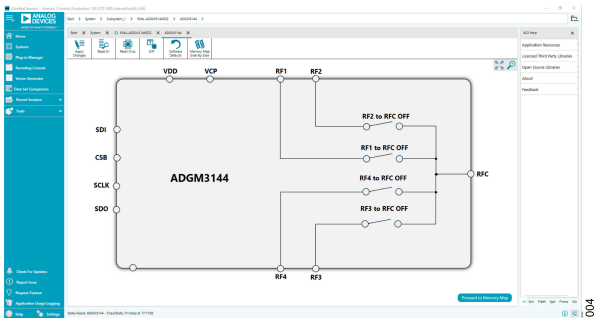

Figure 4. Chip Block Diagram View for the ADGM3144

EVAL-ADGM3144SDZ BLOCK DIAGRAM AND DESCRIPTIONS

The EVAL-ADGM3144SDZ software is organized so that it appears similar to the functional block diagram shown in the ADGM3144 data sheet. A full description of each block and register, as well as their respective settings, are given in the ADGM3144 data sheet.

Some of the blocks and their functions are described in Table 8 because these blocks pertain to the ADGM3144. The full screen block diagram, shown in Figure 5, describes the functionality of each block.

All changes to the blocks correspond to the block diagram in the software. For example, if the internal register bit is enabled, it displays as enabled on the block diagram. If any bits or registers have modified values not transferred to the ADGM3144, they appear in bold in Figure 5. After clicking **Apply Changes**, the data is transferred to the ADGM3144.

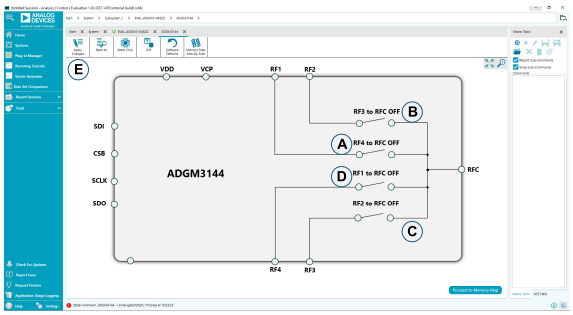

Figure 5. EVAL-ADGM3144SDZ Block Diagram with Labels

Table 8. EVAL-ADGM3144SDZ Block Diagram Function Descriptions (See Figure 5)

Label	Function Description
A	Click the switch symbol to open and close the RF1 to RFC switch.
B	Click the switch symbol to open and close the RF2 to RFC switch.
C	Click the switch symbol to open and close the RF3 to RFC switch.
D	Click the switch symbol to open and close the RF4 to RFC switch.
E	Click **Apply Changes** to apply all the modified values to the devices.

EVAL-ADGM3144SDZ BLOCK DIAGRAM AND DESCRIPTIONS

MEMORY MAP

Click **Proceed to Memory Map** for full accessibility to all the registers (see Figure 5). This access allows registers to be edited at a bit level (see Figure 6). The bits shaded in dark gray in Figure 6 are read only bits and cannot be accessed from ACE, and all other bits are toggled. Clicking **Apply Changes** transfers data to the ADGM3144.

All changes made in the memory map correspond to the block diagram. For example, if the internal register bit is enabled, the bit displays as enabled in the block diagram. Any bits or registers that are bold in Figure 6 are modified values not transferred to the EVAL-ADGM3144SDZ. Click **Apply Changes** to transfer data to the EVAL-ADGM3144SDZ.

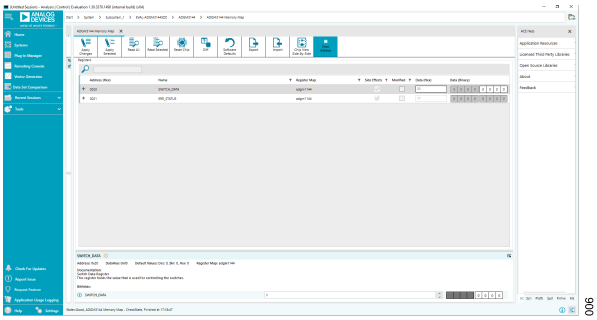

Figure 6. ADGM3144 Memory Map

MEASURING SWITCH PERFORMANCE

Figure 7 shows the connection diagram of the EVAL-ADGM3144SDZ in parallel-interface. Apply a V_{DD} supply to the EVAL-ADGM3144SDZ to measure the performance of the switch. The links are set according to the switch under test (see Table 1). After selecting the desired channel and its state, the switch performance data can be collected using a network analyzer. Terminate the RFx edge connectors of the unused switch channels into 50Ω loads to achieve the full performance of the channel under test.

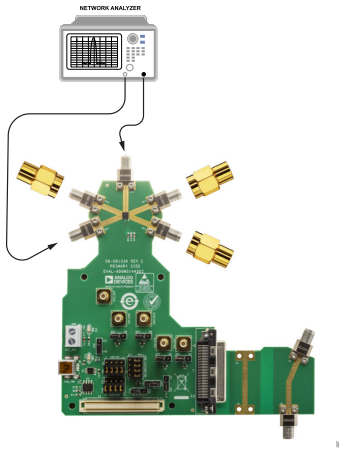

Figure 7. EVAL-ADGM3144SDZ Connection Diagram for On-Board Parallel-Interface

The EVAL-ADGM3144SDZ, shown in Figure 7, comes with a calibration thru transmission line on the PCB. This calibration line removes the insertion loss and phase offset of the PCB transmission lines connecting to the switch from the measurement. Figure 8 shows the calibration transmission line and Figure 9 shows its insertion loss and return loss up to 20GHz. The calibration line is exactly the same length as the distance from any one RFx connector to the RFx pin of the ADGM3144 plus the distance from the RFC connector to the RFC pin of the ADGM3144.

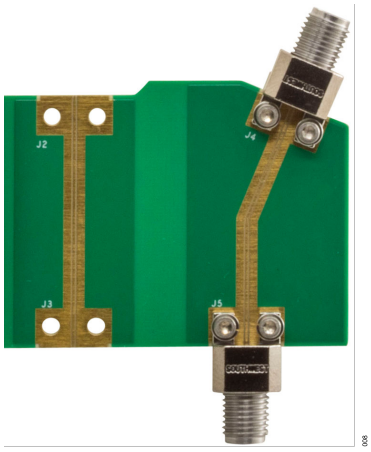

Figure 8. EVAL-ADGM3144SDZ Calibration Transmission Line Used for PCB Insertion Loss and Phase Offset Correction

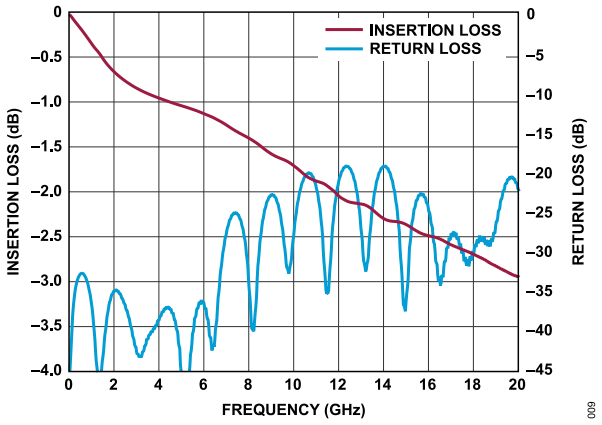

Figure 9. Calibration Transmission Line Insertion Loss and Return Loss

Figure 10 shows the calibration line length. All RF traces connecting to the ADGM3144 are of equal length.

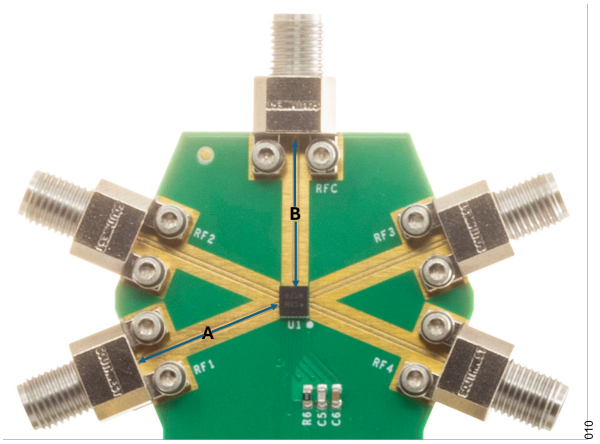

Figure 10. Calibration Transmission Line Length Equal to the A + B Length

To de-embed the PCB transmission line insertion loss from the entire switch insertion loss board measurement (the RF1 to RFC path), use the network analyzer's Auto Fixture Removal (AFR) tool. Perform this de-embedding technique using the network analyzer at the time of the measurement or after the measurement using individual measurement data files. See the Network Analyzer Calibration Procedure section for more information.

Use the network analyzer port extension function to de-embed any phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delays into the port extension menu on the network analyzer corresponding to any phase offset introduced from an RF edge connector to the switch pin. Figure 10 shows an example of these phase offsets on a typical switch measurement, labeled as A and B. Both A and B are identical in length and can be calculated by measuring the time delay of the calibration line and dividing it by two.

MEASURING SWITCH PERFORMANCE

Figure 11 shows the ADGM3144 switch insertion loss measurement results of all four channels that are de-embedded with respect to the PCB transmission line losses.

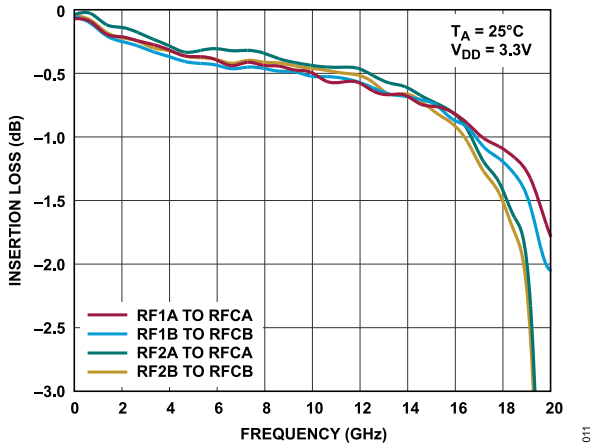

Figure 11. PCB De-Embedded ADGM3144 Insertion Loss Performance

Figure 12 shows the ADGM3144 switch return loss performance measurement results for all four channels.

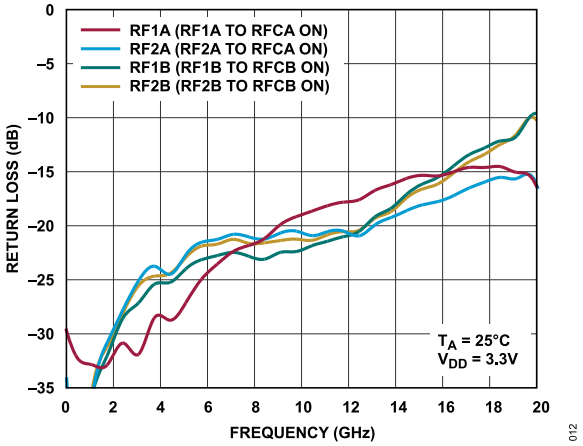

Figure 12. ADGM3144 Return Loss Performance

Figure 13 shows the ADGM3144 switch off isolation performance measurement results for all four channels.

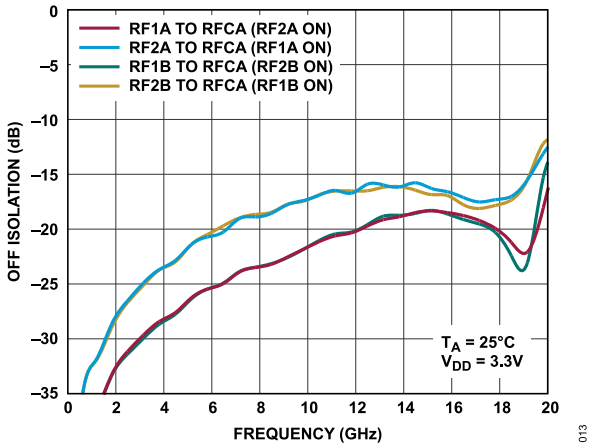

Figure 13. ADGM3144 Off-Isolation Performance

NETWORK ANALYZER CALIBRATION PROCEDURE

Use the following procedure in conjunction with the ADGM3144BCCZ for two-port measurements, assuming there is a set of manual calibration standards or an electric calibration type unit to perform a short load open through (SLOT) calibration of the network analyzer. The maximum value for the network analyzer frequency sweep for the ADGM3144 PCB can be up to 20GHz. Perform the following steps for the two-port measurements:

1. Perform a full, two-port standard SLOT calibration or an electrical calibration of the network analyzer.
2. Connect the calibration through calibration line (Connector J7 and Connector J8) to the analyzer and measure its insertion loss, S(2,1).
3. Perform an AFR to de-embed the transmission line losses or save the measured data to the network analyzer memory for later use.
4. Configure the ADGM3144 links and power up the ADGM3144, as described in the Power Supply section.
5. Connect the network analyzer to the desired MEMS switch RF connectors and apply the external control signals, if needed.
6. Measure the complete insertion loss of the ADGM3144. If an AFR has not been completed in Step 3, the measurement includes the insertion loss of the MEMS switch and test fixture (PCB transmission lines and RF connectors).
7. If an AFR has not been completed in step 3, perform an AFR by using the saved measured data of the through calibration line in step 3. Because the AFR method is dependent on the network analyzer, consult the network analyzer user manual before performing the extraction.
8. Use the network analyzer port extension function to de-embed the phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delay values into the port extension menu on the network analyzer for each RF edged connector to switch the pin path equal to the electrical length of the calibration line divided by two.

HANDLING GUIDELINES

Adhere to the following handling guidelines for the EVAL-ADGM3144SDZ:

- Always treat the ADGM3144 as a static sensitive device and observe normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps, or other electrostatic discharge (ESD) control devices.
- Take care when connecting signals. Hold the EVAL-ADGM3144SDZ from the edges to avoid any damage to the device under test (DUT).
- Avoid connecting live signal sources. Ensure that outputs are switched off (preferably grounded) before connecting to the DUT. In addition, ensure all instrumentation shares a common chassis ground.
- Avoid running measurement instruments (for example, digital multimeters (DMMs) in autorange modes). Some instruments can generate large transient compliance voltages when switching ranges.
- Use the highest practical range (that is, lowest resolution) setting for resistance measurements to minimize compliance voltages.

LAYOUT RECOMMENDATIONS

The EVAL-ADGM3144SDZ is a 4-layer board. The EVAL-ADGM3144SDZ uses 8mil Roger RO4003C dielectric. The outer copper layers have 2.2mil finish thickness with electroless nickel immersion gold (ENIG) finish. The RF transmission lines were designed using a coplanar waveguide model with a width of 14mil and ground spacing of 7mil to have a characteristic impedance of 50Ω (see Figure 14). It is recommended to use plenty of vias under the ADGM3144BCCZ and along the RF traces to provide good grounding and to avoid any resonance at high frequencies. To achieve optimum RF performance, Southwest Microwave end launch edge mount jack connectors (1092-04A-9) are used.

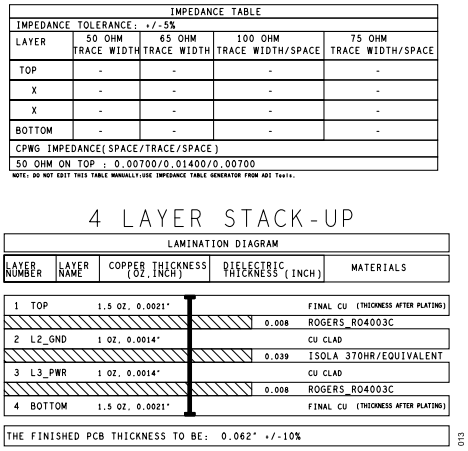

Figure 14. EVAL-ADGM3144SDZ Board Stackup and Manufacturing Information

SOLDERING RECOMMENDATIONS

To avoid solder voids under the ADGM3144BCCZ, it is recommended to use a 0.003in [0.0767mm] thick solder stencil with nano coating. The aperture size for the solder stencil must be 1:1. The stencil opening for the peripheral pins are narrower by 0.001in [0.025mm] and longer by 0.002in [0.051mm]. The stencil opening for the exposed paddle is divided with a 2 × 2 window pane openings. The opening has a 0.0025in [0.063mm] cutback from the exposed paddle landing pad. Each opening is sized 0.024in × 0.024in^2 [0.61mm × 0.61mm^2] and is separated 0.010in [0.254mm] from each other. Recommended dimensions are shown in Figure 15. Poor soldering may impact the RF performance of the ADGM3144.

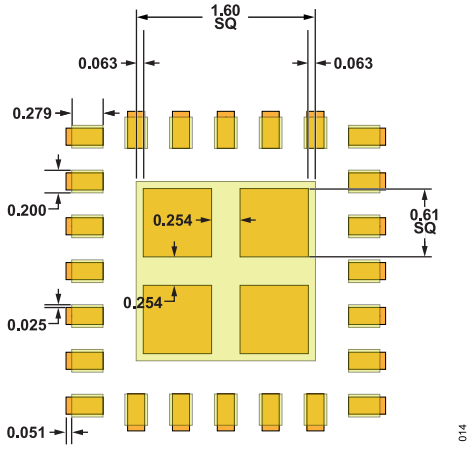

Figure 15. Solder Stencil Recommendations in Millimeters

EVALUATION BOARD SCHEMATICS AND ARTWORK

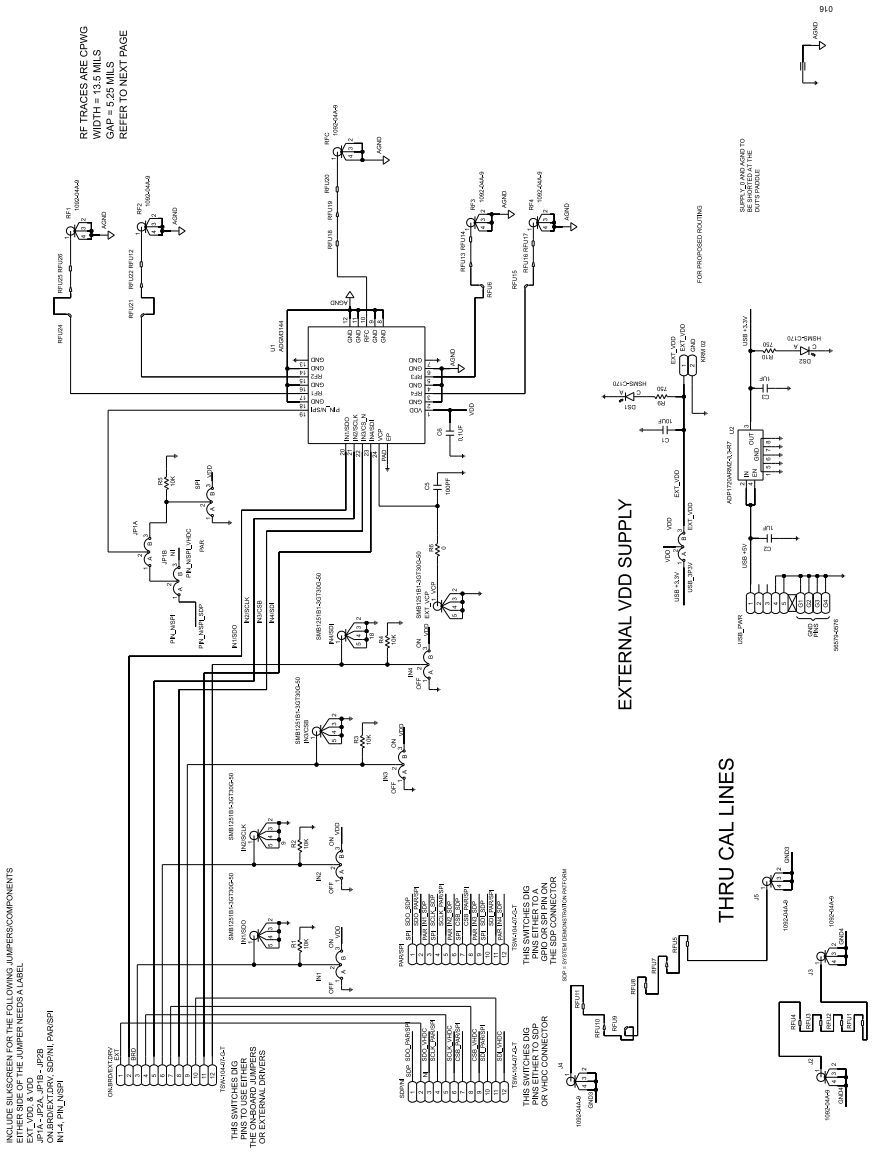

Figure 16. Schematic of the EVAL-ADGM3144SDZ

EVALUATION BOARD SCHEMATICS AND ARTWORK

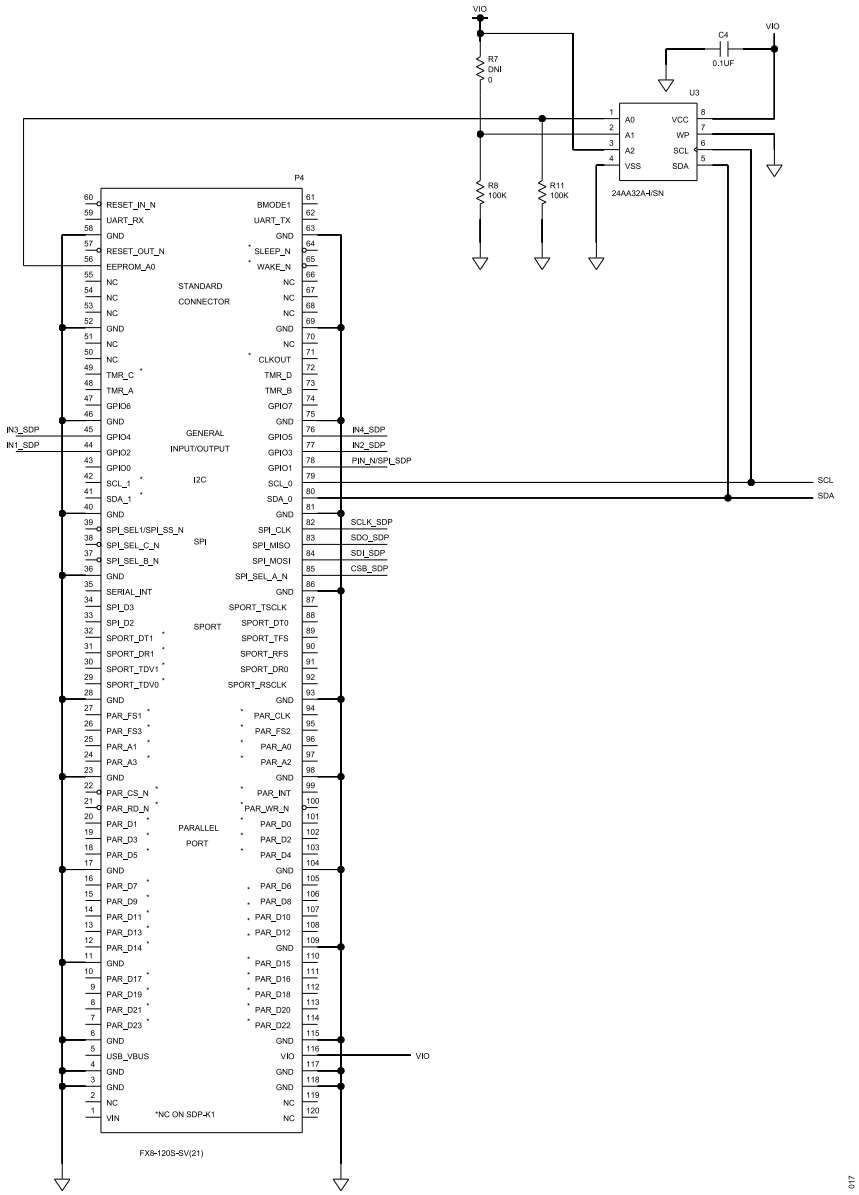

Figure 17. Schematic of the EVAL-ADGM3144SDZ with an SDP Connector

EVALUATION BOARD SCHEMATICS AND ARTWORK

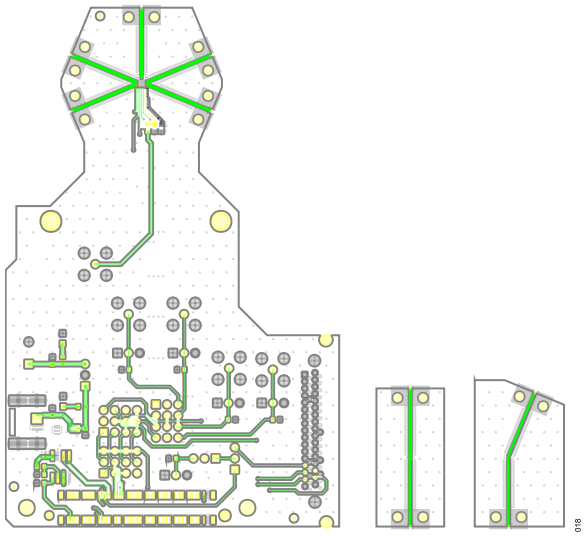

Figure 18. EVAL-ADGM3144SDZ Component Side PCB Drawing (Layer 1)

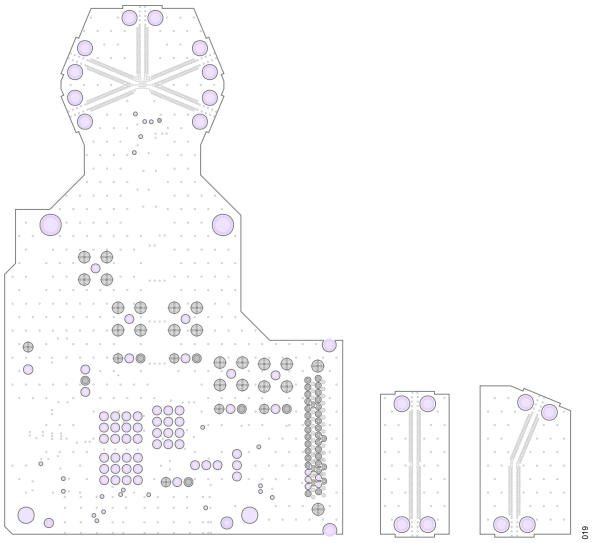

Figure 19. EVAL-ADGM3144SDZ Component Side Ground Plane PCB Drawing (Layer 2)

EVALUATION BOARD SCHEMATICS AND ARTWORK

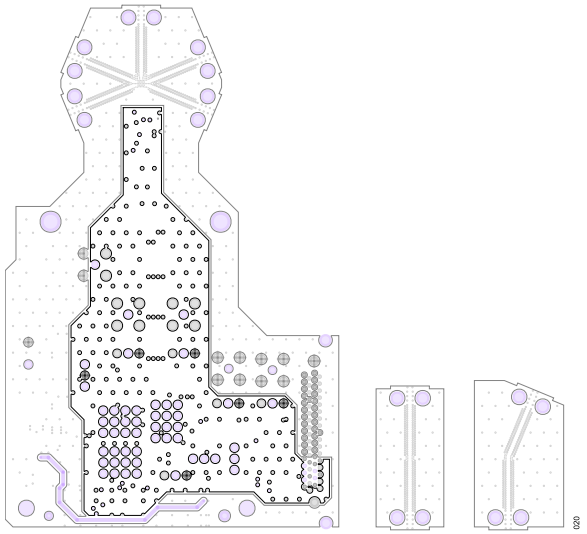

Figure 20. EVAL-ADGM3144SDZ Component Side Ground Plane PCB Drawing (Layer 3)

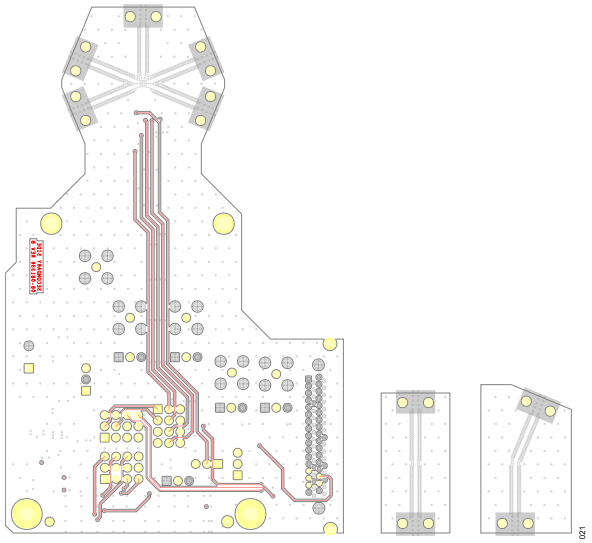

Figure 21. EVAL-ADGM3144SDZ Component Side, Bottom Side PCB Drawing (Layer 4)

EVALUATION BOARD SCHEMATICS AND ARTWORK

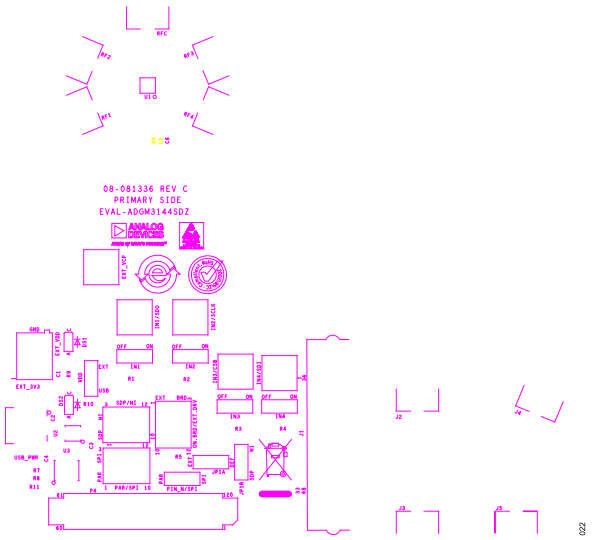

Figure 22. EVAL-ADGM3144SDZ Component Side Silkscreen PCB Drawing (Top)

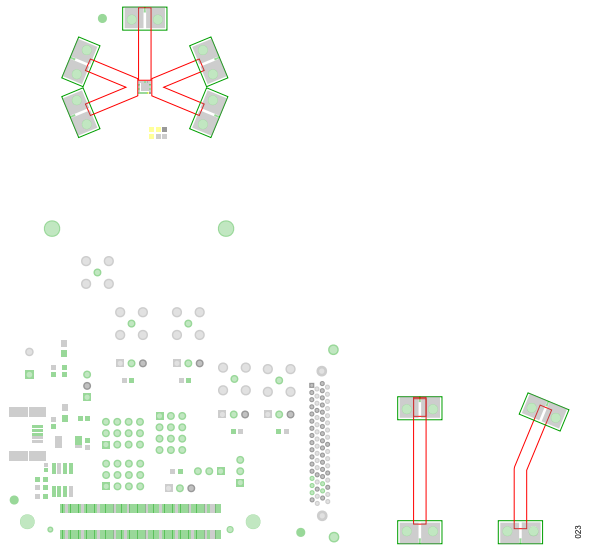

Figure 23. EVAL-ADGM3144SDZ Soldermask Top

EVALUATION BOARD SCHEMATICS AND ARTWORK

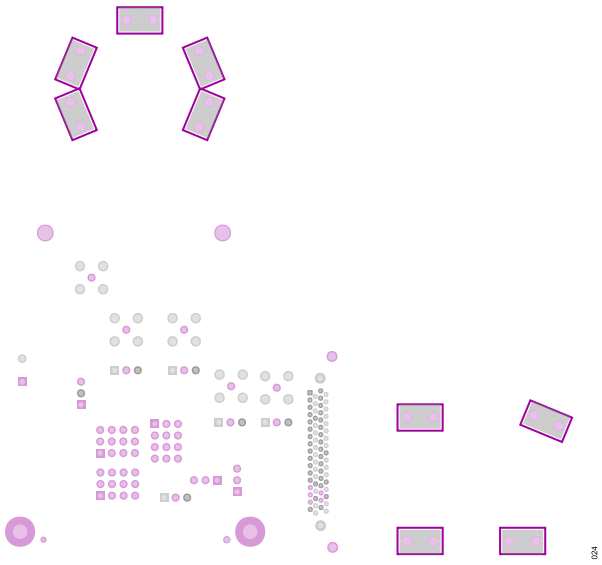

Figure 24. EVAL-ADGM3144SDZ Soldermask Bottom

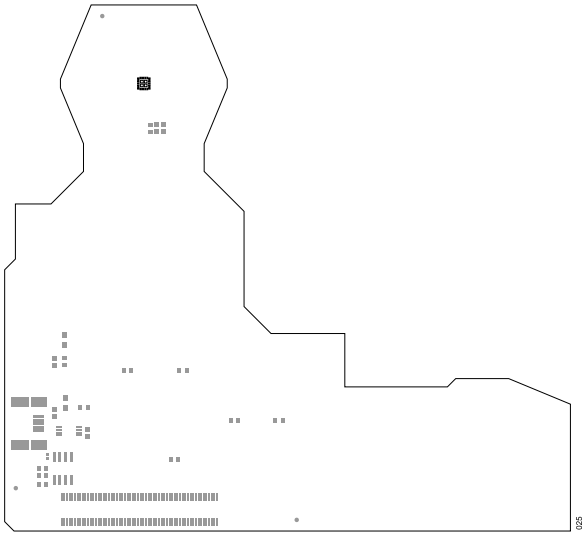

Figure 25. EVAL-ADGM3144SDZ Paste Top

ORDERING INFORMATION

EVALUATION BOARD

Model[1]	Package Description
EVAL-ADGM3144SDZ	Evaluation Board

[1] Z = RoHS Compliant Part.

BILL OF MATERIALS

Table 9. Bill of Materials

Reference Designator	Description	Manufacturer	Manufacturer Number
C1	10µF ceramic capacitor, 10V, 20%, X5R, 0603, low effective series resistance (ESR)	TDK	C1608X5R1C106M080AB
C2, C3	1µF ceramic capacitors, 16V, 10%, X7R, 0603	AVX	0603YC105KAT2A
C4	0.1µF ceramic capacitor, 16V, 10%, X7R, 0402, AEC-Q200	Murata	GCM155R71C104KA55D
C5	100pF ceramic capacitor, 100V, 5%, C0G, 0603, AEC-Q200	Murata	GCM1885C2A101JA16D
C6	0.1µF ceramic capacitor, 25 V, 10%, X7R, 0603, AEC-Q200, low ESR	TDK	CGA3E2X7R1E104K080AA
DS1, DS2	630nm light emitting diode (LED), surface-mount device (SMD), red	Broadcom Limited	HSMS-C170
EXT_VCP, IN1/SDO, IN2/SCLK, IN3/CSB, IN4/SDI	PCB connectors, Subminiature Version B (SMB), coaxial straight jack	Amphenol	SMB1251B1-3GT30G-50
EXT_VDD	PCB connector, 2-pin terminal block, 5mm pitch	Lumberg	KRM 02
IN1, IN2, IN3, IN4, JP1A, JP1B, PIN_N/SPI, VDD	PCB connectors, 3-position, male header, unshrouded single row, 2.54mm pitch, 3mm solder tail	Harwin	M20-9990345
J1	PCB connector, right angle shielded receptacle	TE Connectivity Ltd	5796055-2
J2 to J5, RF1 to RF4, RFC	Coaxial connectors, edge launch edge mount, 2.92mm jack	Southwest Microwave	1092-04A-9
ON.BRD/EXT.DRV, PAR/SPI, SDP/NI	PCB connector, 120-way, 0.6mm pitch, 2 row straight	Samtec Inc	TSW-104-07-G-T
P4	PCB connector, 120-way, 0.6mm pitch, 2 row straight	HRS	FX8-120S-SV(21)
R1 to R5	10kΩ resistors, SMD, 0.01%, 1/16W, 0603	Multicomp (SPC)	MCTF0603TTX1002
R9, R10	750Ω resistor, SMD, 1% 1/10W, 0603, AEC-Q200	Vishay	CRCW0603750RFKEA
R8, R11	100kΩ resistor, SMD, 1%, 1/16W, 0603	Multicomp (SPC)	MC 0.063W 0603 1% 100K
R6	0Ω resistor, SMD jumper, 1/3W, 0603 AEC-Q200	Vishay	CRCW06030000Z0EAHP
U1	IC, 0Hz to 17GHz, SP4T MEMS Switch	Analog Devices	ADGM3144BCCZ
U2	IC, 50mA, high voltage, micropower linear regulator	Analog Devices	ADP1720ARMZ-3.3-R7
U3	IC, 32kb serial EEPROM	Microchip Technology	24LC32A-I/MS
USB_PWR	PCB connector, USB mini-AB series	Molex	56579-0576
Not applicable[1]	Jumper, 8 (2×4) position, shunt connector, black open top, 2.54mm pitch	Samtec Inc.	MNT-104-BK-G
Not applicable[1]	Jumper, 2-position, shunt connector, black open top, 0.1in pitch	Samtec Inc.	SNT-100-BK-G-H
Not applicable[2]	Wideband 50Ω termination loads, 2.92mm	Hirose Electric Co Ltd	HK-TMP

[1] These are jumper shorts use to set headers to their desired positions.

[2] Screwed on at measurement time (see Figure 7).

ORDERING INFORMATION

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.