

## Evaluating the ADG2712, Picoamp Ultra-Low Leakage, Low Voltage, Quad SPST Switch

### FEATURES

- ▶  $\pm 1.08\text{V}$  to  $\pm 2.75\text{V}$  Dual supply
- ▶  $+1.08\text{V}$  to  $+5.5\text{V}$  Single supply
- ▶ Ultra-low leakage
  - ▶  $\pm 56\text{pA}$  typical at  $125^\circ\text{C}$
  - ▶  $\pm 8\text{pA}$  typical at  $85^\circ\text{C}$
- ▶ 16-lead,  $2\text{mm} \times 2\text{mm}$  LGA package
- ▶ 1.8V JEDEC compliant logic
- ▶ Fully specified at  $+5\text{V}$ ,  $+3.3\text{V}$ ,  $+1.8\text{V}$ , and  $\pm 2.5\text{V}$
- ▶ Rail-to-rail signal range

### EVALUATION KIT CONTENTS

- ▶ EVAL-ADG2712ARDZ evaluation board

### DOCUMENTS NEEDED

- ▶ ADG2712 data sheet
- ▶ EVAL-ADG2712ARDZ user guide

### EQUIPMENT NEEDED

- ▶ DC voltage source
  - ▶  $\pm 2.5\text{V}$  for dual-supply
  - ▶  $+5\text{V}$  for single-supply
- ▶ Optional digital logic supply
- ▶ Analog signal source
  - ▶ Source measure unit with low leakage capability or similar

### GENERAL DESCRIPTION

The EVAL-ADG2712ARDZ is the evaluation board for the ADG2712, which features a 4-channel single-pole/single-throw switch (SPST). The ADG2712 operates with a low voltage, single supply range from  $+1.08\text{V}$  to  $+5\text{V}$  or a low voltage dual supply range from  $\pm 1.08\text{V}$  to  $\pm 2.5\text{V}$ .

The signal routing and layout are optimized to minimize parasitic leakage paths and external interference, ensuring that measured performance closely reflects the intrinsic characteristics of the device.

Figure 1 shows the EVAL-ADG2712ARDZ board. The ADG2712 is soldered to the center of the evaluation board. A 4-pin wire screw terminal is provided to power the device, and for ease of use, there is also a USB-C connector to provide a  $5\text{V}$  power supply to power the ADG2712. Triaxial connectors are used to connect to the source and drain pins of the four channels of the switches.

Full specifications on the ADG2712 are available in the product data sheet, which must be consulted in conjunction with this user guide when using the evaluation board.

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**REVISION HISTORY**

**6/2026—Revision 0: Initial Version**

EVAL-ADG2712ARDZ EVALUATION BOARD LAYOUT

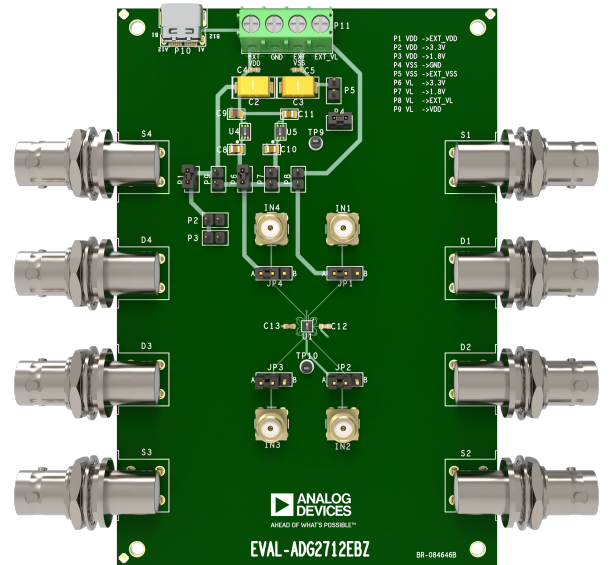


Figure 1. Evaluation Board Layout

## EVALUATION BOARD HARDWARE

### POWER SUPPLIES

For ease of use, a USB Type-C connector (P10) is supplied on the evaluation board. This connector can be used to supply 5V directly to the ADG2712 for single supply. The 5V USB connection also powers both voltage regulators providing options to power the ADG2712 with a single 3.3V supply (U4) or a single 1.8V supply (U5). The power supply can be configured using the on board jumpers listed in [Table 1](#). To power the ADG2712 with specific power-supply voltages or dual-supply voltages, the screw terminal P11 can be used to provide supply voltages from an external voltage source. For dual-supply voltages, the EVAL-ADG2712ARDZ evaluation board can be powered from  $\pm 1.08\text{V}$  to  $\pm 2.75\text{V}$ . For single-supply voltages,  $V_{DD}$  between 1.08V to 5.5V, the  $V_{SS}$  terminal must be connected to GND.

### INPUT SIGNALS

To maintain the low leakage performance of the ADG2712, triaxial connectors are provided to connect to both the source pins (S1, S2, S3, and S4) and the drain pins (D1, D2, D3, and D4) of the ADG2712.

### DIGITAL INTERFACE OPTIONS

The digital interface of the ADG2712 can be controlled either manually using the JP1, JP2, JP3, and JP4 link headers or accessed by using the corresponding Subminiature Version A (SMA) connectors. To use the Subminiature Version B (SMB) connectors, remove the JP1, JP2, JP3, and JP4 link headers.

### LINK OPTIONS

Several link options are provided on the EVAL-ADG2712ARDZ evaluation board. The functions of these link options are described in [Table 1](#).

**Table 1. Link Options**

Link Number	Options	
JP1	A = Connect IN1 to VL	B = Connect IN1 to GND
JP2	A = Connect IN2 to VL	B = Connect IN2 to GND
JP3	A = Connect IN3 to VL	B = Connect IN3 to GND
JP4	A = Connect IN4 to VL	B = Connect IN4 to GND
JP5	A = Connect IN4 to VL	B = Connect IN4 to GND
P1	Inserted = Connect Pos_Supply to VDD	Removed = Disconnect Pos_Supply from VDD
P2	Inserted = Connect Pos_Supply to 3.3V	Removed = Disconnect Pos_Supply from 3.3V
P3	Inserted = Connect Pos_Supply to 1.8V	Removed = Disconnect Pos_Supply from 1.8V
P4	Inserted = Connect Neg_Supply to GND	Removed = Disconnect Neg_Supply to GND
P5	Inserted = Connect Neg_Supply to VSS	Removed = Disconnect Neg_Supply to VSS
P6	Inserted = Connect VL to 3.3V	Removed = Disconnect VL from 3.3V
P7	Inserted = Connect VL to 1.8V	Removed = Disconnect VL from 1.8V
P8	Inserted = Connect VL to EXT_VL	Removed = Disconnect VL from EXT_VL
P9	Inserted = Connect VL to VDD	Inserted = Connect VL to VDD

### LAYOUT

To achieve the low leakage (sub 10pA) levels possible with the ADG2712 at the printed circuit board (PCB) board level, very careful consideration was given to the layout and manufacturing of the evaluation board. The PCB is a 6-layer board. All the signal traces S1, S2, S3, S4, D1, D2, D3, and D4 are connected from the ADG2712 to the triaxial connectors using fully guarded layout techniques. This signal is routed on Layer 4 with guard traces placed on both sides of the signal routing. To complete the signal guarding, further guard traces are also placed above and below the signal on Layer 3 and Layer 5. This provides complete enclosure to the signal trace in all dimensions. The guard trace is then connected to the guard pin on the triaxial connectors. Using an appropriate measurement system, the signal voltage can be buffered and connected to the guard trace. This creates a minimum voltage differential between the signal voltage and the guard trace to minimize the leakage due to the PCB traces. [Figure 2](#) shows an example of the PCB layout technique on two channels. For simplicity, only S2 to D2 and S4 to D4 connections are shown.

Also shown in [Figure 2](#) are the extra guard traces on the top layer of the board (in red). These traces are placed on multiple

## EVALUATION BOARD HARDWARE

layers and encircle the signal pins and PCB footprint to prevent any leakage between the signal pins and adjacent pins on the top layer of the PCB. This technique is also employed around the triaxial connectors pins on multiple layers and can be seen in [Figure 9](#).

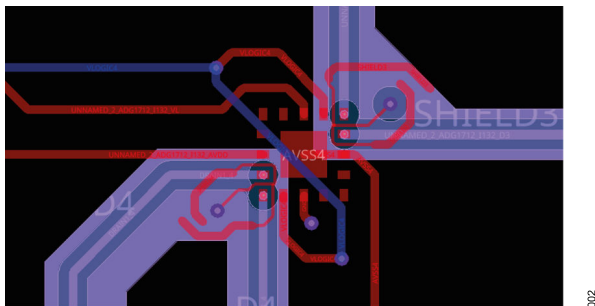


Figure 2. Guarding

## CLEANING AND HANDLING

The effective leakage of a switch input in a system can be substantially degraded if the PCB traces are contaminated. Solder flux, body oils, dust, and dirt are all possible sources of contamination. Some of these contaminants form a parallel leakage path across the surface of the existing PCB traces, effectively increasing the insulation resistance.

It is recommended that any contamination is removed by an appropriate cleaning process. The EVAL-ADG2712ARDZ evaluation boards for the ADG2712 were cleaned in an electronic PCB washing machine with deionized water on a program shown below.

Table 2. PCB Cleaning Sequence

Cycle	Time	Temp
Prewash	3 mins	30°C
Wash	15 mins	60°C
Dry	1 hour	90°C

EVALUATION BOARD SCHEMATICS AND ARTWORK

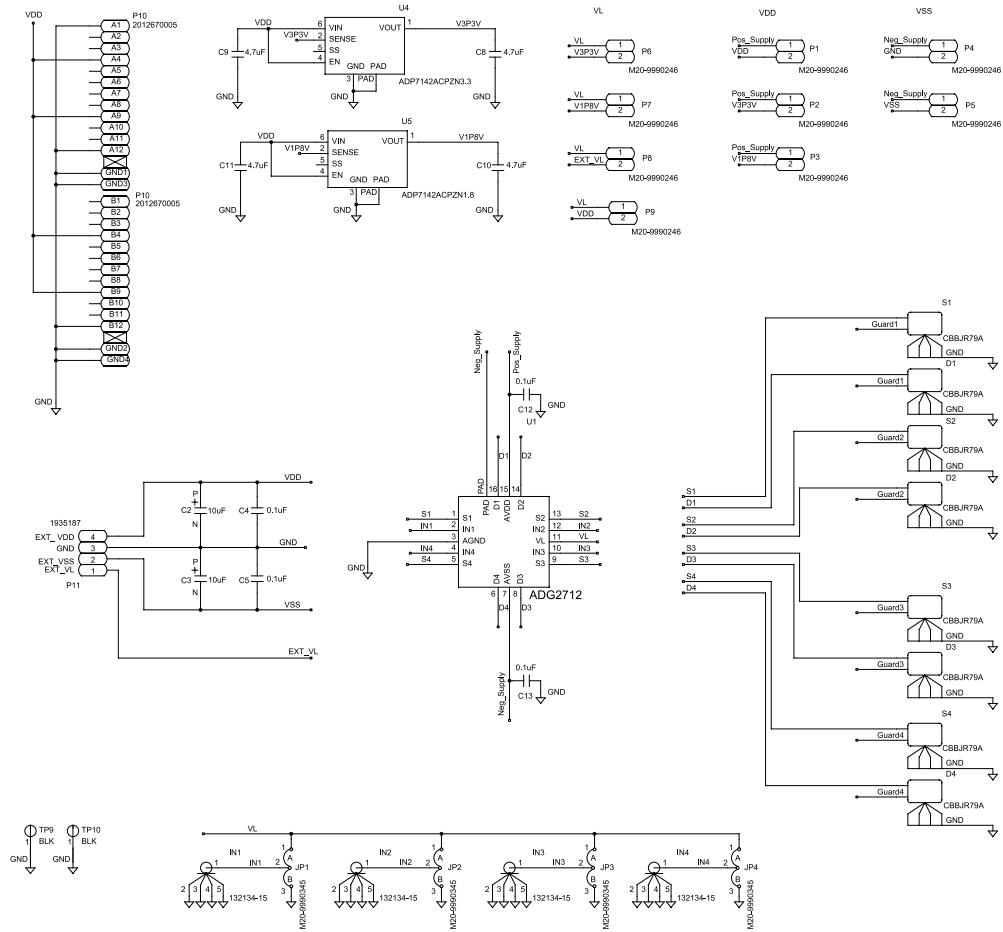


Figure 3. EVAL-ADG2712ARDZ Schematic Part 1

EVALUATION BOARD SCHEMATICS AND ARTWORK

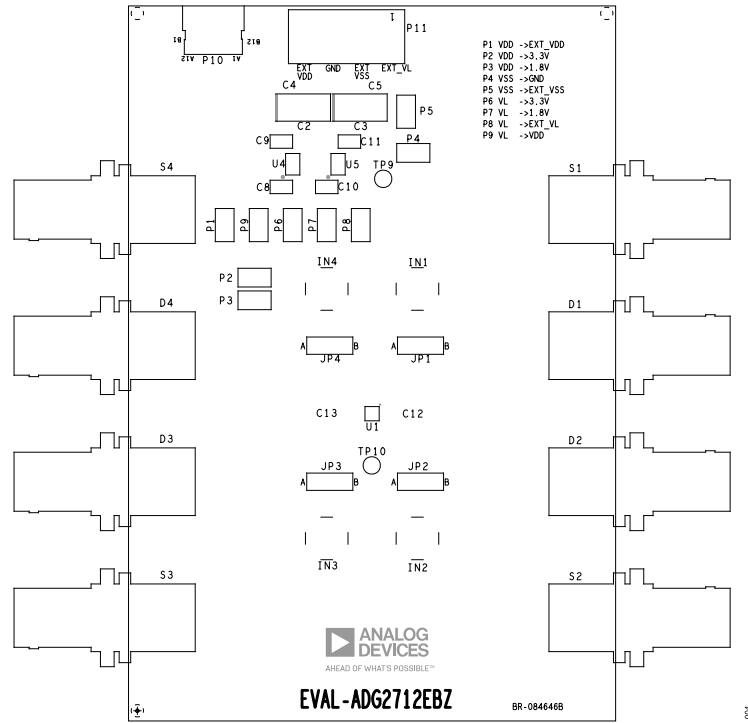


Figure 4. EVAL-ADG2712ARDZ Silkscreen

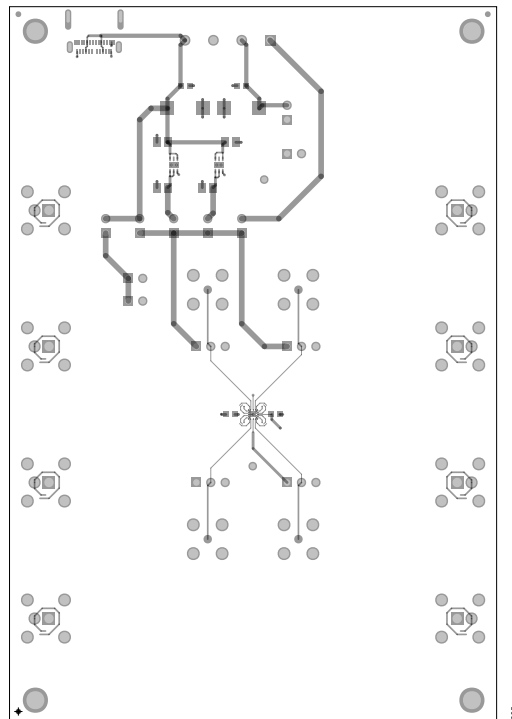


Figure 5. EVAL-ADG2712ARDZ Top Layer

EVALUATION BOARD SCHEMATICS AND ARTWORK

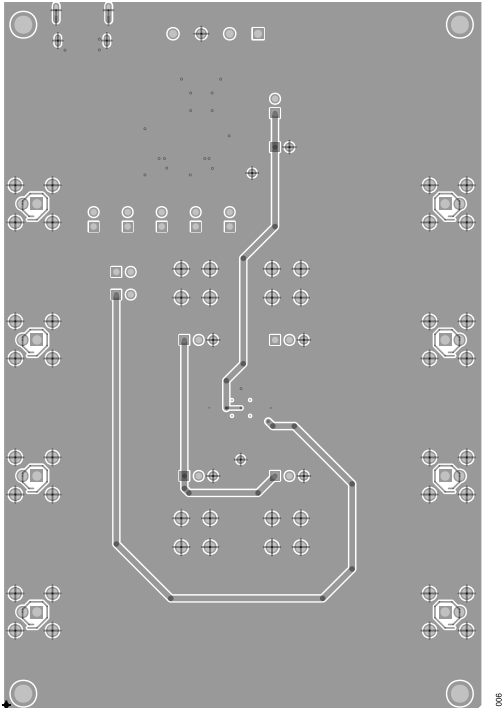


Figure 6. EVAL-ADG2712ARDZ Bottom Layer

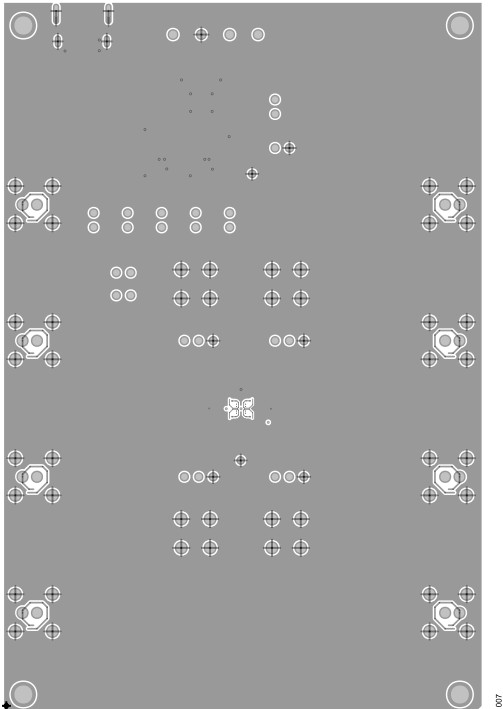


Figure 7. EVAL-ADG2712ARDZ Layer 2

EVALUATION BOARD SCHEMATICS AND ARTWORK

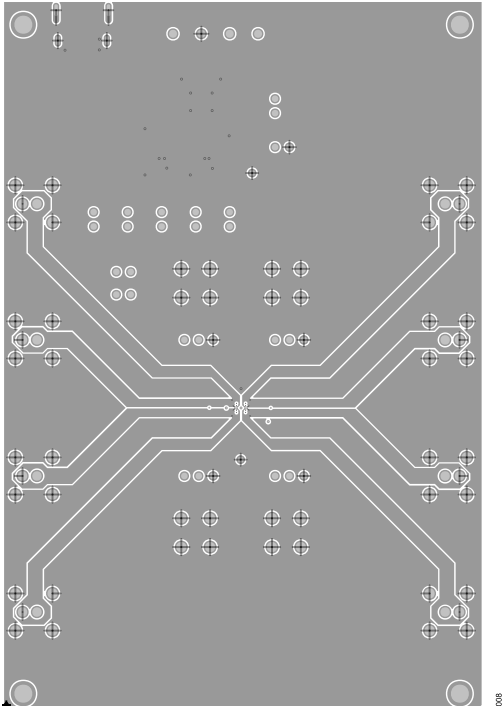


Figure 8. EVAL-ADG2712ARDZ Layer 3

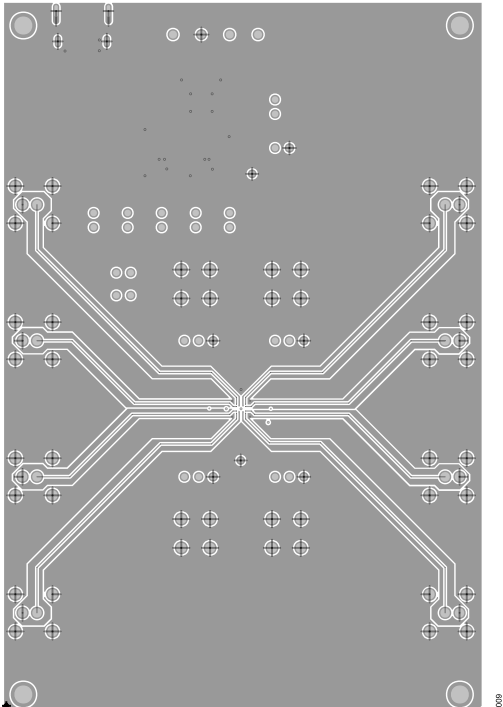


Figure 9. EVAL-ADG2712ARDZ Layer 4

EVALUATION BOARD SCHEMATICS AND ARTWORK

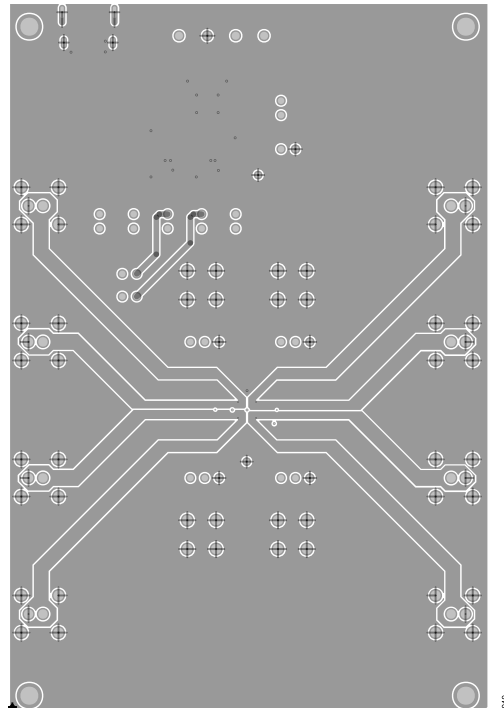


Figure 10. EVAL-ADG2712ARDZ Layer 5

## ORDERING INFORMATION

## EVALUATION BOARDS

Table 3. Evaluation Boards

Model <sup>1</sup>	Description
EVAL-ADG2712ARDZ	Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.

## BILL OF MATERIALS

Table 4. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C8, C9, C10, C11	Capacitors, ceramic, 4.7 $\mu$ F, 50V, 10%, X7R, 0805	Murata	GRM21BZ71H475KE15L
C4, C5, C12, C13	Capacitors, ceramic 0.1 $\mu$ F, 50V, 10%, X7R, 0603	Samsung	CL10B104KB8NNNC
C2, C3	Tantalum capacitors, 10 $\mu$ F, 50V, 20%, 7343-31, 0.8 $\Omega$	AVX	TAJD106M050RNJ
D1, D2, D3, D4, S1, S2, S3, S4	Connectors, PCB circuit board mount, triaxial jack, right angle, bayonet Neill-Concelman (BNC)	Cinch Connectivity Solutions	CBBJR79/A
IN1, IN2, IN3, IN4	Connectors, PCB, SMA jack, straight 50 $\Omega$ center contact, surface mount, through-hole legs	Amphenol RF	132134-15
P1, P2, P3, P4, P5, P6, P7, P8, P9	Connectors, PCB, header, single row, two position	Harwin	M20-9990246
P10	Connectors, PCB, USB Type-C, female, 24 position, right angle, surface mount, 0.25mm/0.5mm pitch, solder termination	Molex	2.01E+09
P11	Connector, PCB, terminal block, four positions, 5mm pitch	Phoenix Contact	1935187
TP9, TP10	Connectors, PCB, test point, black	Keystone Electronics	5001
U2	Picoamp ultra-low leakage, low voltage, quad SPST switch	Analog Devices, Inc.	ADG2712BCCCZ
U4	40V, 200mA, low noise, CMOS, LDO linear regulator, 3.3 output voltage	Analog Devices	ADP7142ACPZN3.3-R7
U5	40V, 200mA, low noise, CMOS, LDO linear regulator, 1.8 output voltage	Analog Devices	ADP7142ACPZN1.8-R7

**ORDERING INFORMATION****NOTES****ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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