Evaluating the ADF5612 Microwave Wideband Synthesizer with Integrated VCO

FEATURES

- Self-contained board, including ADF5612 frequency synthesizer with integrated VCO, loop filter, Type-C USB interface, on-board reference oscillator, and voltage regulators
- Windows®-based software allows control of synthesizer functions from a PC
- Externally powered by 6V

EVALUATION KIT CONTENTS

- EV-ADF5612SD1Z evaluation board

EQUIPMENT NEEDED

- Windows-based PC with USB port for evaluation software
- System demonstration platform, serial only (SDP-K1)
- EVAL-SDP-CK1Z controller board
- Power supply (6V)
- Spectrum analyzer or phase noise analyzer
- 50 Ω terminators
- Low noise REF_{IN} source (optional)

DOCUMENTS NEEDED

- ADF5612 data sheet

REQUIRED SOFTWARE

- Analysis | Control | Evaluation (ACE) Software, Version 1.30 or newer
- ADF5611 plugin, 1.2024.50401 or newer, which automatically installs the ADF5612 plugin

EV-ADF5612SD1Z EVALUATION BOARD PHOTOGRAPH

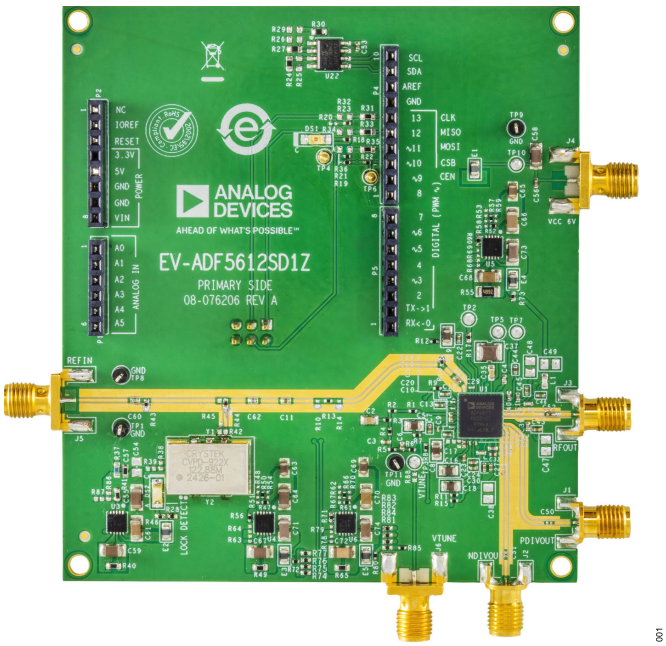

Figure 1. EV-ADF5612SD1Z Evaluation Board Photograph

GENERAL DESCRIPTION

The EV-ADF5612SD1Z evaluates the performance of the ADF5612 frequency synthesizer with an integrated voltage-controlled oscillator (VCO) for phase-locked loops (PLLs). A photograph of the EV-ADF5612SD1Z evaluation board is shown in Figure 1. The EV-ADF5612SD1Z contains the ADF5612 frequency synthesizer with an integrated VCO, a USB interface, power supply connectors, an on-board reference oscillator, and Subminiature Version A (SMA) connectors. The outputs of the EV-ADF5612SD1Z are AC-coupled with 50Ω transmission lines making them suitable to drive 50Ω impedance instruments.

The EV-ADF5612SD1Z requires an EVAL-SDP-CK1Z controller board (not supplied with the kit). The SDP-K1 allows software programming of theEV-ADF5612SD1Z with Analog Devices, Inc., ACE software.

Full specifications for the ADF5612 frequency synthesizer are available in the ADF5612 data sheet, which must be consulted in conjunction with this user guide when working with the EV-ADF5612SD1Z evaluation board.

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT
WARNING AND LEGAL TERMS AND CONDITIONS.

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REVISION HISTORY

1/2026—Rev. 0 to Rev. A

Changes to Figure 5.... 7
Changes to Figure 6.... 8

2/2025—Revision 0: Initial Version

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURES

To install the ADF5612 plug-in, take the following steps:

1. Install the latest version of the **ACE Software** platform from the Analysis | Control | Evaluation (ACE) Software web page.
2. Scroll down to the **ACE Evaluation Board Plug-ins** section of the ACE web page.
3. In the search bar within the **ACE Evaluation Board Plug-ins** section of the ACE web page, search for the ADF5612 and install the chip and board plug-ins that are found.
4. Ensure that the ADF5612 plug-ins appear when the EV-ADF5612SD1Z evaluation board is attached through the SDP-K1 connector to the PC.

EVALUATION BOARD SETUP PROCEDURES

The EV-ADF5612SD1Z uses a single 6V power supply with a SMA (J4) connector by default. On-board low noise, low dropout (LDO) regulators are used to generate the nominal 3.3 V and 5 V supplies.

For additional details on the power supply circuitry see the Power Supplies section.

To power-up the EV-ADF5612SD1Z, take the following steps:

1. Set the voltage of the power supply to 6V and the current limit to 1A.
2. Connect the power cable to J4 (a single SMA cable).
3. Turn on the power.

To run the **ACE Software**, take the following steps:

1. Select **Start** > **All Programs** > **Analog Devices** > **ACE**.
2. Under the **Select Device and Connection** tab, select the **ADF5612** and the **ADF5612 Board** then appears within the **Attached Hardware** area.
3. When connecting the EV-ADF5612SD1Z, allow 5 sec to 10 sec for the label on the **Status** bar to change.

EVALUATION BOARD HARDWARE

The EV-ADF5612SD1Z requires the SDP-K1 platform that uses the EVAL-SDP-CK1Z controller board, which is not supplied with the evaluation kit.

POWER SUPPLIES

The EV-ADF5612SD1Z is powered by a 6 V power supply connected to the SMA (J4).

The power supply circuit has one LT3045 high performance, low noise LDO regulator and three LT3042 high performance, low noise LDO regulators.

One LT3042 is used to generate 3.3V to drive the DVDD, VPPCP, VDDLS, and VCCPD supply pins, and the other two LT3042s provide 5V to drive the VCOVCC supply pin and the on-board ultralow, phase noise, sine-wave oscillator supply (XTAL). The LT3045 is used to generate 3.3V to drive the AVDD, VDD1, VDD2, VDD3, RVDD, VCCPS, and VCCHF supply pins.

REFERENCE INPUT

The EV-ADF5612SD1Z has an on-board,122.88MHz, ultralow phase noise, sine-wave oscillator to drive the ADF5612 reference input. A single-ended oscillator output is connected to the XREFP pin and a 50Ω resistor to ground is also added.

The Y1 reference footprint supports 5mm × 7.5mm and 14mm × 9mm packages in the 4-pin or 6-pin format. The R38 and R39 resistors can be populated if there is a need to set the control voltage of an alternative voltage-controlled crystal oscillator (VCXO).

The default oscillator supply voltage is set to 5V. If an alternative oscillator requires a different supply voltage, change the R40 resistor on the LT3042 to provide the desired voltage level.

The reference input can also be driven externally via a SMA connector on REFIN (J5). Note that the on-board oscillator supply must be disabled when using an external reference.

Table 1 provides the required board modifications required when using an external reference clock.

Table 1. Component Placement for Different Reference Sources

Component Location	Default On-Board Oscillator	Single-Ended External Reference
R28, R44	0Ω	Remove
R45	Do not install (DNI)	0Ω

RF OUTPUTS

The EV-ADF5612SD1Z has one SMA connector for a single-ended output RFOUT, and two SMA connectors for the differential outputs, PDIVOUT and NDIVOUT.

RFOUT (J3) is a single-ended RF output that operates from 7.3GHz to 8.5GHz.

The PDIVOUT (J1) and NDIVOUT (J2) outputs operate as a 100Ω differential pair, and as such, are sensitive to impedance mismatch.

If both of these RF outputs are used, ensure that these outputs are connected to equal load impedance. If only one port of the differential pair is used, terminate the complementary port with a 50Ω termination. The frequency range of these outputs is 7.3GHz to 8.5GHz with the divider set to 1. Additional output divider values of 1, 2, 4, 8, 16, 32, 64, and 128 allow a frequency output as low as 57MHz. The divider value can be set via the **ACE Software** using the **RFOUTDIV DIVIDER** numeric selectors (see Figure 5).

The output power of the single-ended and differential RF output channels can be adjusted via the **ACE Software Plug-ins** individually using the **RFOUT POWER** and **RFOUTDIV POWER** numeric selectors, respectively (see Figure 5).

The differential RF output channels are disabled by default in the **ACE Software Plug-ins**; however, these channels can be enabled by unchecking the **POWER DOWN RFOUTDIV** box (see Figure 5).

VCO

The ADF5612 includes dual VCO cores with enough overlap between the cores such that continuous frequency coverage from 57MHz to 8.5GHz over temperature and supply variation is possible. Each VCO core is subdivided into 128 bands for a total of 256 bands. This topology allows broadband frequency coverage with more consistent tuning sensitivity across the band. Each band has an allowable tune voltage that is applied to the VT pin (Pin 37) of 0.5V DC to 2.5V DC.

By default, autocalibration is enabled. Autocalibration utilizes an internally generated, temperature compensated voltage that is applied to the tune port of the VCO as each band is searched. Using autocalibration also ensures that, regardless of the ambient temperature during autocalibration, the synthesizer remains locked in the chosen band over the specified operating temperature range of −40°C to +105°C for the ADF5612.

LOOP FILTER

The loop filter component placement is shown in Figure 8. The footprint of the loop filter components included on the EV-ADF5612SD1Z allows up to a fifth-order loop filter configuration.

The EV-ADF5612SD1Z has one SMA connector for the VTUNE port (J6) that provides a means to verify the voltage at VT or to manually tune the VCO within its band in open-loop mode.

SERIAL PORT INTERFACE (SPI)

Connector P2 interfaces with the SDP-K1 to evaluate the ADF5612 using the **ACE Software** graphical user interface (GUI). A second connector (P3) is provided for the ability to use alternative interface boards.

EVALUATION BOARD HARDWARE

DEFAULT CONFIGURATION

All of the components necessary for local oscillator (LO) generation are placed on the EV-ADF5612SD1Z evaluation board. The EV-ADF5612SD1Z is shipped with a single-ended, 122.88MHz reference VCXO, the ADF5612 synthesizer with an integrated VCO, and a 15.9kHz loop bandwidth at 7.95GHz. When the EV-ADF5612SD1Z is powered up and connected to the **ACE Software**, click the **INITITALIZE DEFAULT STATE** button to provide a 7.95GHz output clock on the RFOUT channel with a 122.88MHz reference, a 61.44MHz phase detector input frequency (f_{PFD}), and a charge pump current of 3.2mA.

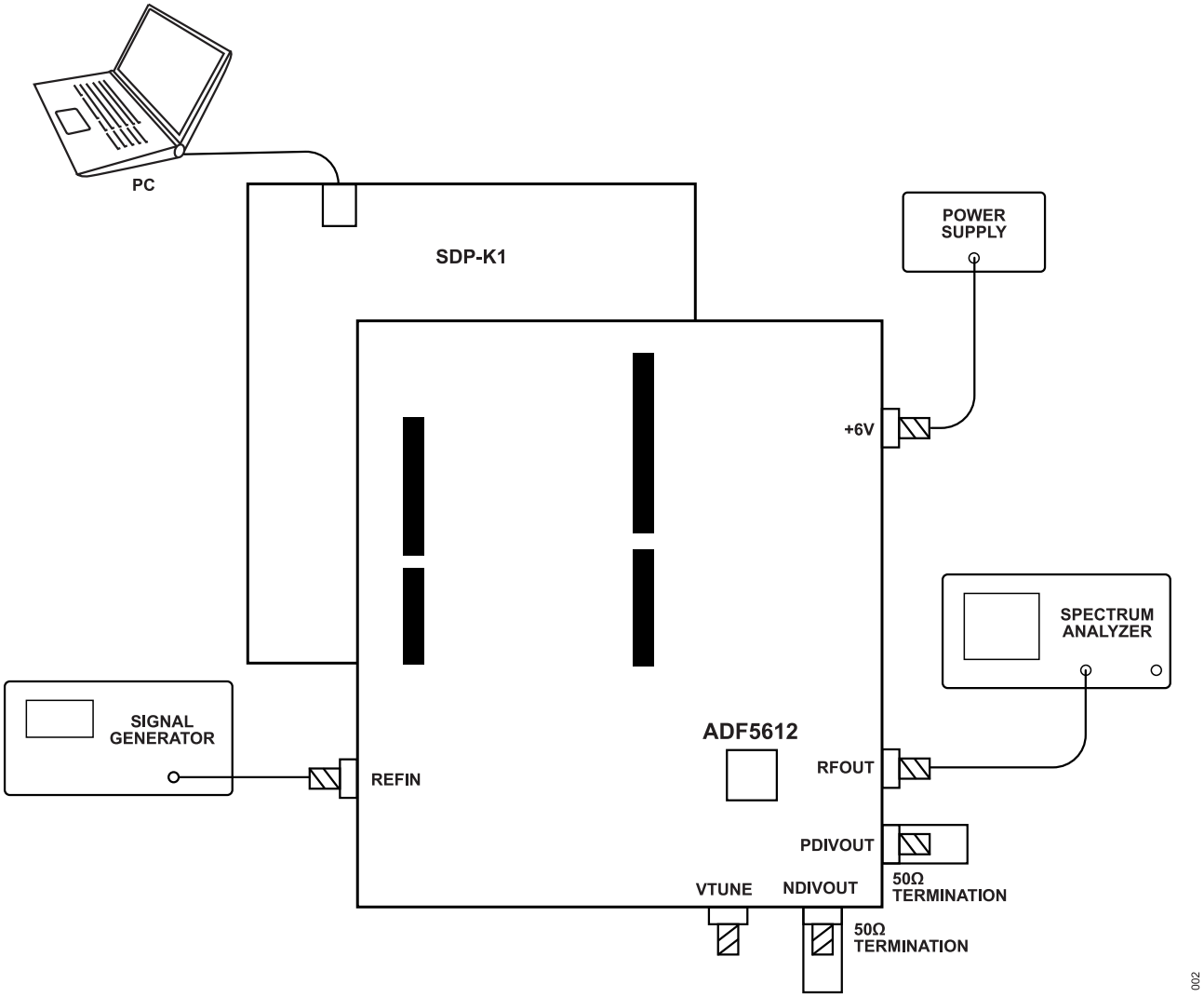

Figure 2. Evaluation Board Setup Diagram

EVALUATION BOARD SOFTWARE

The **ACE Software** is the main platform that is used to control the EV-ADF5612SD1Z. The ADF5612 plugin includes user interfaces that relate to the ADF5612 and allow evaluation of the device. Use the following steps to open the main control window for the ADF5612:

1. Launch the **ACE Software** application with the SDP-K1 controller board attached to the EV-ADF5612SD1Z. The **ADF5612 Board** then appears in the **Attached Hardware** tab as shown in Figure 3.
2. Double click the **ADF5612 Board** icon in the **Attached Hardware** tab to launch the plugin board view as shown in Figure 4 then appears.
3. Double click the **ADF5612** chip icon that appears on the ACE board view to open the main control window shown in Figure 5.

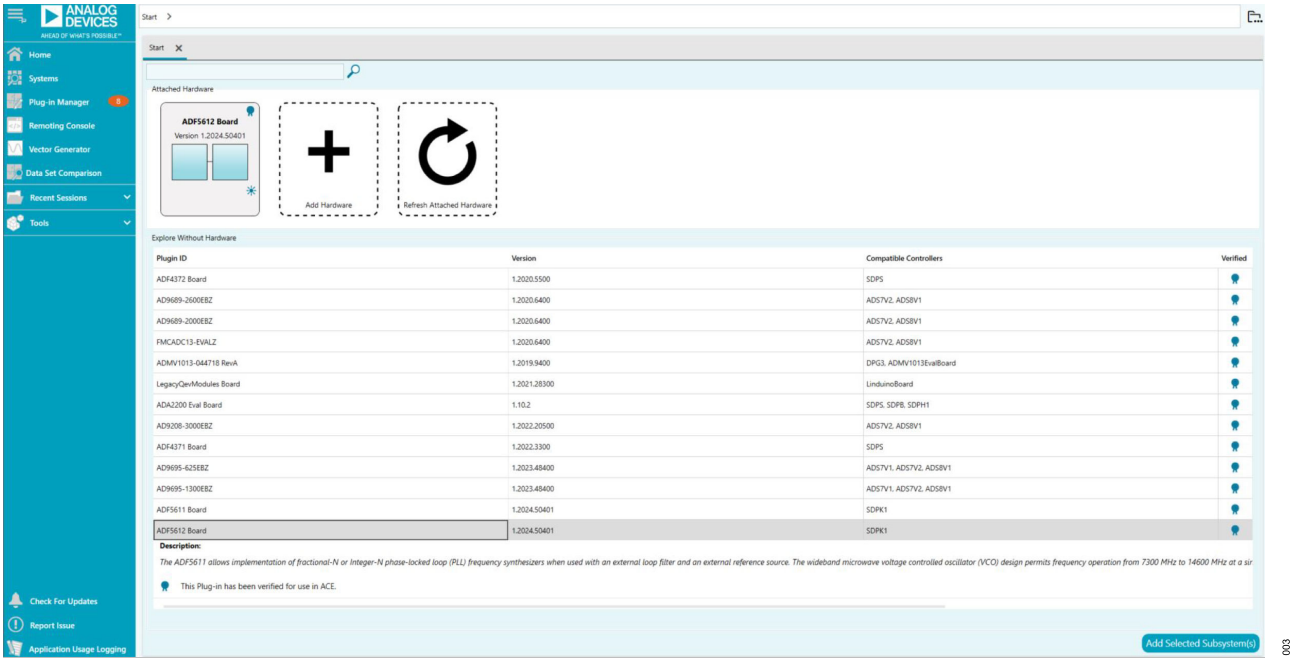

Figure 3. ACE Start Page, Attached Hardware (ADF5612 Evaluation Board)

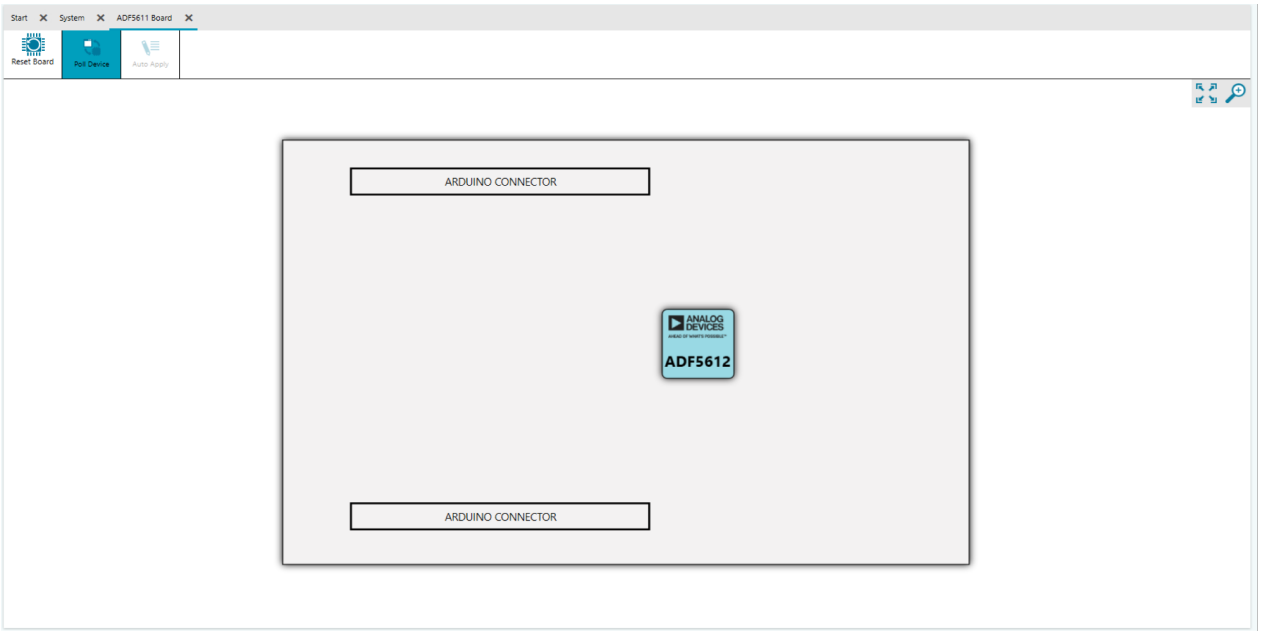

Figure 4. ACE Board Page, Device Selection

EVALUATION BOARD SOFTWARE

MAIN CONTROLS

The main controls are available in the high level register map shown in Figure 5. The **ACE Software** ADF5612 plug-in opens with uninitialized registers. Two ways to initialize the registers and the ADF5612 are as follows:

1. Click the **INITIALIZE DEFAULT STATE** button to use the default configuration settings. The ADF5612 and the front panel configuration is then set to a 122.88MHz XREF, 61.44MHz f_{PFD}, 3.2mA charge pump, and 7.95GHz RF_{OUT} clock frequency.
2. Click the **LOAD DEFAULT REGISTERS** button to load all registers in the **ACE Software Register Map**. Then, proceed to modify the front panel with your desired configuration and click **Apply Changes**.

To modify registers post initialization, perform the following steps:

1. Modify the registers as desired after performing initialization.
2. Click **Apply Changes** to load modified configuration to the ADF5612. Note that this action loads the updated registers only and triggers autocalibration if the **RFOUT FREQ.** is modified during auto calibration mode.
   a. Programs the changes from the user.
   b. Triggers an autocalibration by performing a register write to Register 0x010.

If the **RFOUT FREQ.** or any of the frequency parameters entered are outside of the operational range, a notification message will appear in the **EVALUATION MESSAGES** section (see Figure 5).

Specific blocks can be powered down by setting the corresponding power-down check box within the **POWER DOWN** section shown in Figure 5.

Digital clocks used for autocalibration can be toggled after each frequency modification, post **Apply Changes**, by clicking the **TOGGLE CLOCKS** button in the **CLOCKS** section as shown in Figure 5. This feature can be used to disable or enable digital clocks post calibration. Note that the actual state of the digital clocks is displayed in the **EVALUATION MESSAGES** box.

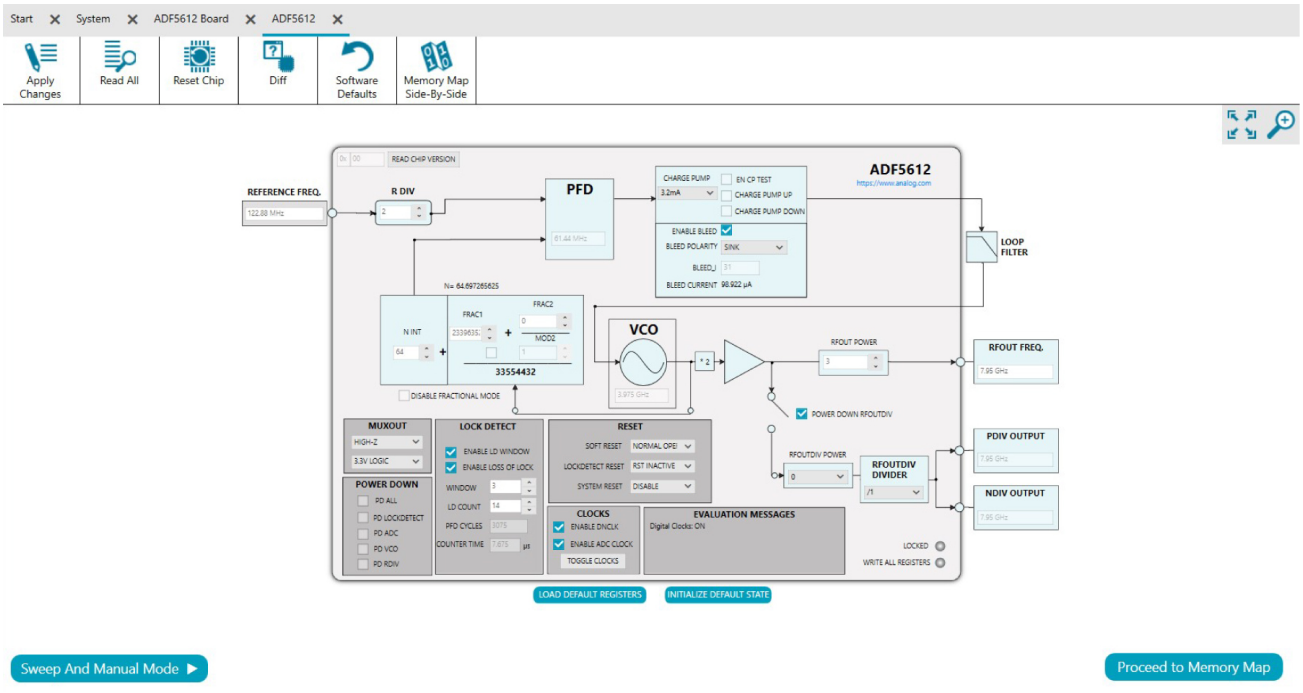

Figure 5. Main Page and Frequency Controls

EVALUATION BOARD SOFTWARE

FREQUENCY SWEEP

To use the ADF5612 to perform a frequency sweep set the **START FREQUENCY**, **STOP FREQUENCY**, **FREQUENCY SPACING**, and **ADDITIONAL DELAY ms**. The **ADDITIONAL DELAY ms** value is an added software delay for each frequency step. If the **ENABLE AUTO READ BACK** check box is selected, the **VCOCore**, **VCOBand**, and **VCOBias** values are read back from the device and populated in the **VCO CALIBRATION TABLE** with the corresponding **RFOutput Frequency** in each row. (See Figure 6).

To run a frequency sweep, perform the following steps:

1. Set the **START FREQUENCY**, **STOP FREQUENCY**, **FREQUENCY SPACING**, and **ADDITIONAL DELAY ms** boxes.
2. Check off the **ENABLE AUTO READ BACK** check box.
3. Click **START/STOP SWEEP**.

Alternatively, click **RUN SINGLE SWEEP** to perform one frequency step on each button click until it reaches the stop frequency value.

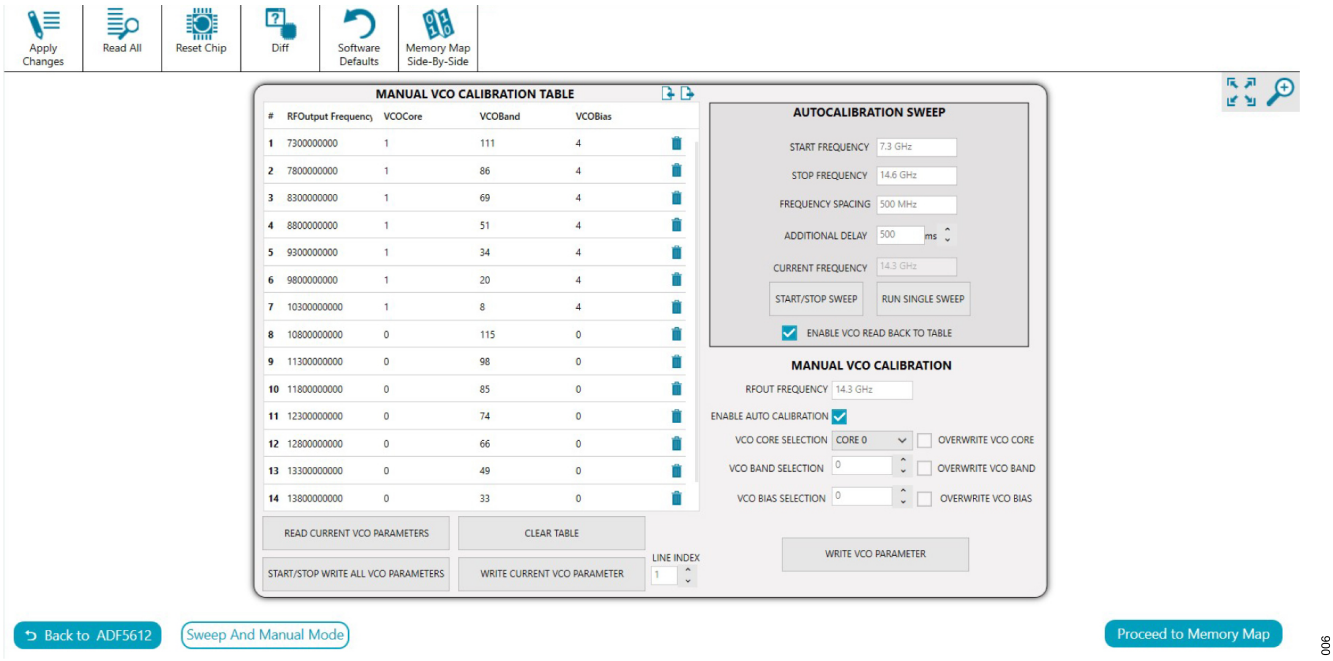

Figure 6. ACE Frequency Sweep

EVALUATION BOARD SOFTWARE

MANUAL VCO CALIBRATION

The ADF5612 can bypass autocalibration by manually programming predetermined **VCOCore**, **VCOBand**, and **VCOBias** values. The **MANUAL VCO CALIBRATION** section shown in Figure 6 of the **ACE Software** ADF5612 plugin can be used to perform an autocalibration bypass.

Take the following steps to perform an autocalibration bypass (see Figure 6):

1. Enter the target frequency in the **RFOUT FREQUENCY** text box.
2. Deselect the **ENABLE AUTO CALIBRATION** check box to disable autocalibration.
3. Select the VCO core for the target frequency by using the **VCO CORE SELECTION** drop-down menu and then check off the **OVERWRITE VCO CORE** check box.
4. Set the VCO band value by using the **VCO BAND SELECTION** text box and then check off the **OVERWRITE VCO BAND** check box.
5. Set the VCO bias value by using the **VCO BIAS SELECTION** text box and then check off the **OVERWRITE VCO BIAS** check box.
6. Click the **WRITE VCO PARAMETER** button to apply the override values onto the ADF5612.

Configure the VCO within the **VCO CALIBRATION TABLE** shown in Figure 6 as follows:

1. Click **READ CURRENT VCO PARAMETERS** to read back the VCO parameters at the current frequency. Results are displayed in the **VCO CALIBRATION TABLE**.
2. Use the **LINE INDEX** text box to select the line index of the VCO parameter intended for the target frequency displayed in the **VCO CALIBRATION TABLE**. Click **WRITE CURRENT VCO PARAMETER** to apply the VCO parameters.
3. Click **START/STOP WRITE ALL VCO PARAMETERS** to sweep through all the VCO parameters listed in the **VCO CALIBRATION TABLE**.

EVALUATION AND TEST

To evaluate and test the performance of the ADF5612, follow the hardware and software setup as explained in the Evaluation Board Hardware section and the Evaluation Board Software section.

Run the **ACE Software** and follow the steps given in Evaluation Board Software section to open the main page as shown in Figure 5.

Click **INITIALIZE DEFAULT STATE** on the **ACE Software** main page to achieve a 7.95GHz clock at the RFOUT output (see Figure 5). Measure the output spectrum and single sideband phase noise on a signal analyzer. Figure 7 shows a phase noise plot of the SMA RFOUT with an output of 7.95GHz at a reference frequency of 122.88MHz, a f_{PFD} of 61.44MHz, and a charge pump current of 3.2mA.

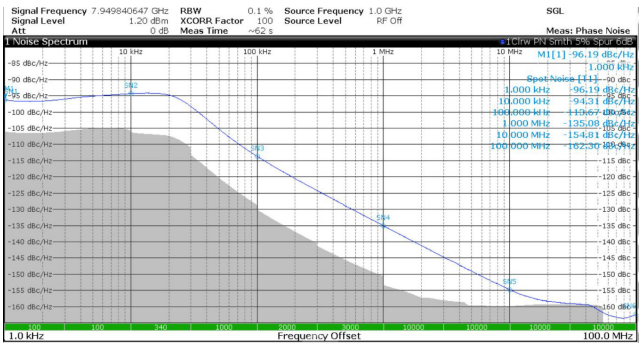

Figure 7. Single Sideband Phase Noise of 7.95GHz Output at 122.88MHz On-Board Reference

EVALUATION BOARD SCHEMATICS AND ARTWORK

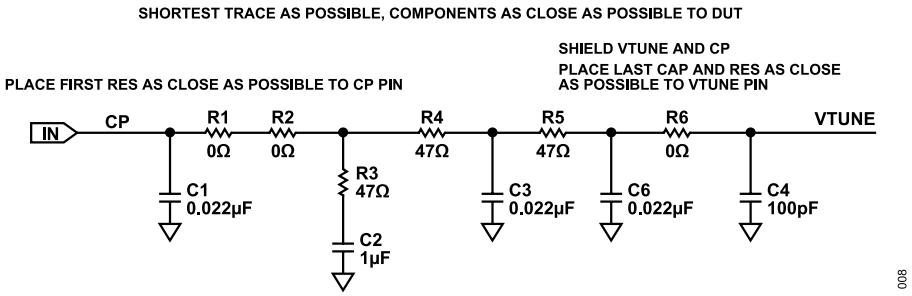

Figure 8. ADF5612 Loop Filter

EVALUATION BOARD SCHEMATICS AND ARTWORK

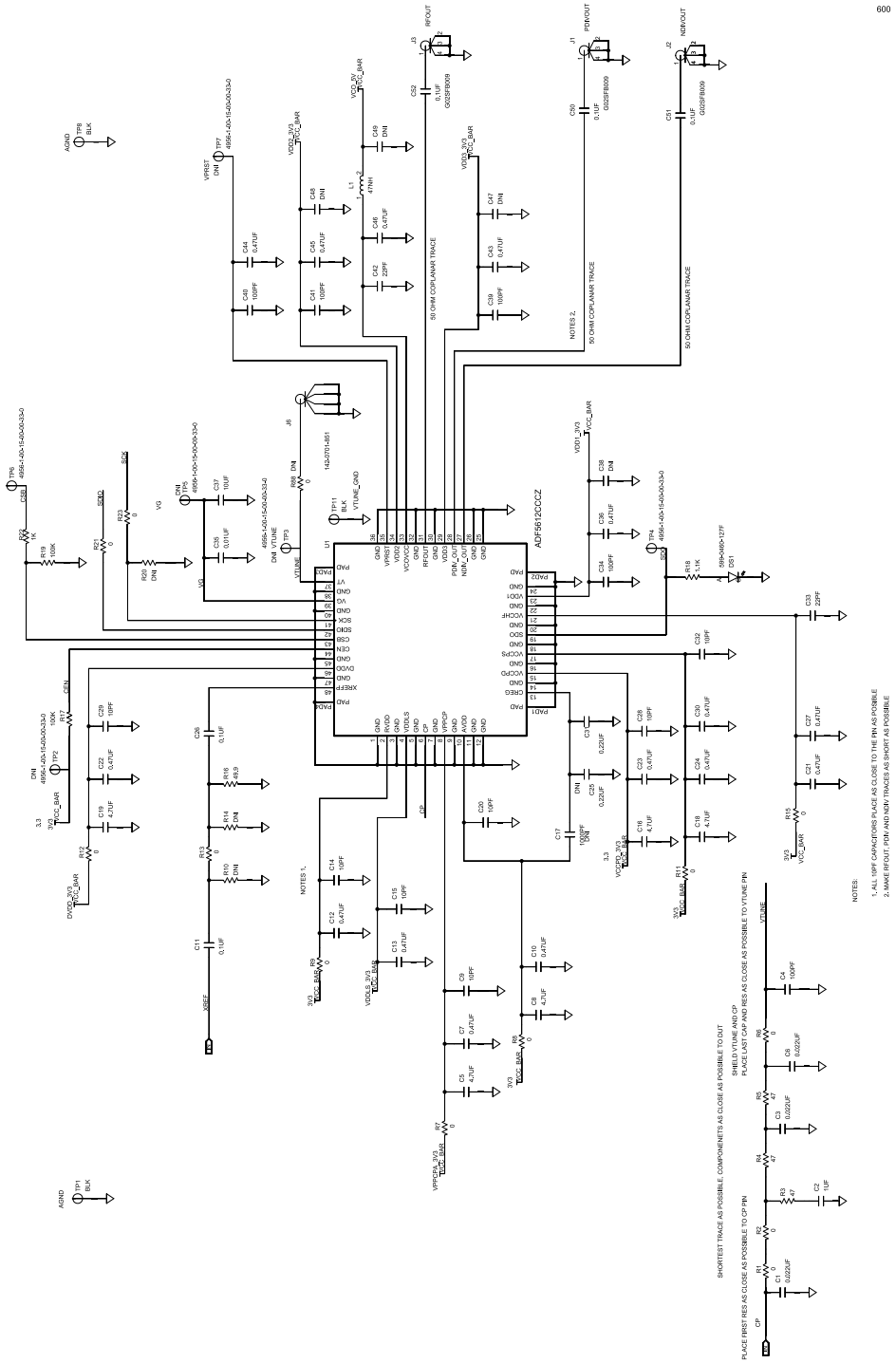

Figure 9. EV-ADF5612SD1Z Schematic of the ADF5612 Connections and Loop Filter

EVALUATION BOARD SCHEMATICS AND ARTWORK

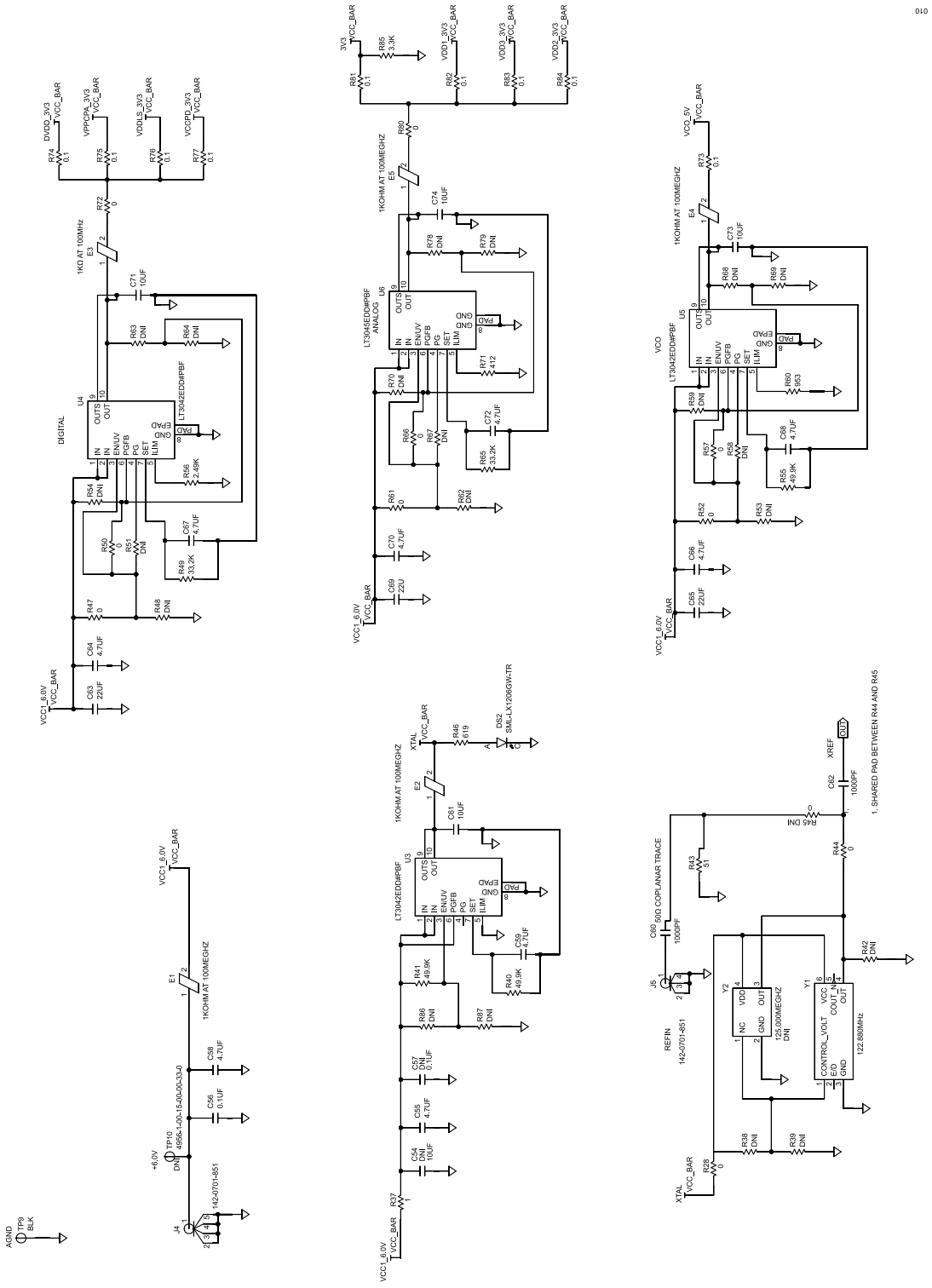

Figure 10. EV-ADF5612SD1Z Schematic of the Power Interface

EVALUATION BOARD SCHEMATICS AND ARTWORK

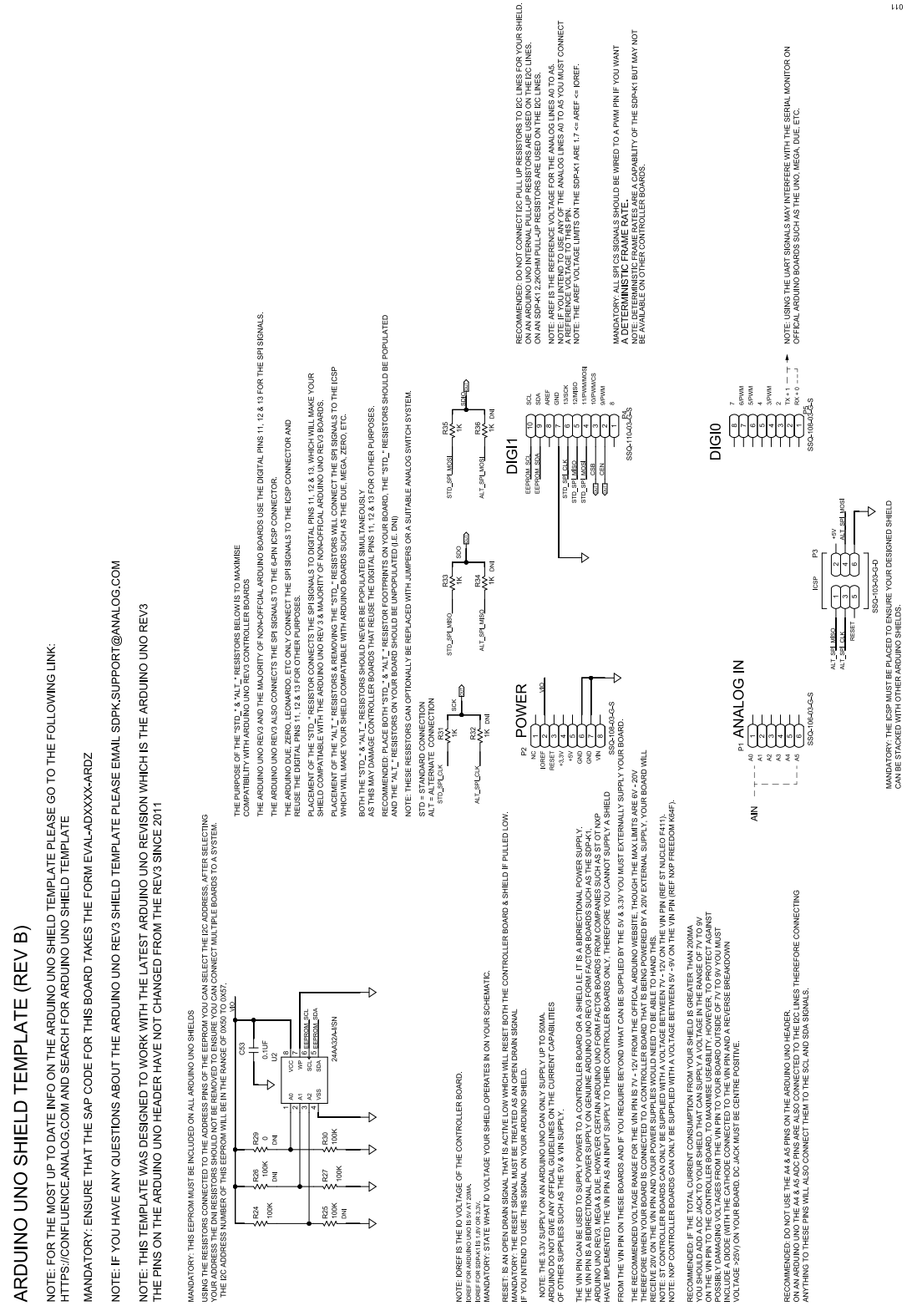

Figure 11. EV-ADF5612SD1Z Schematic of the SPI

EVALUATION BOARD SCHEMATICS AND ARTWORK

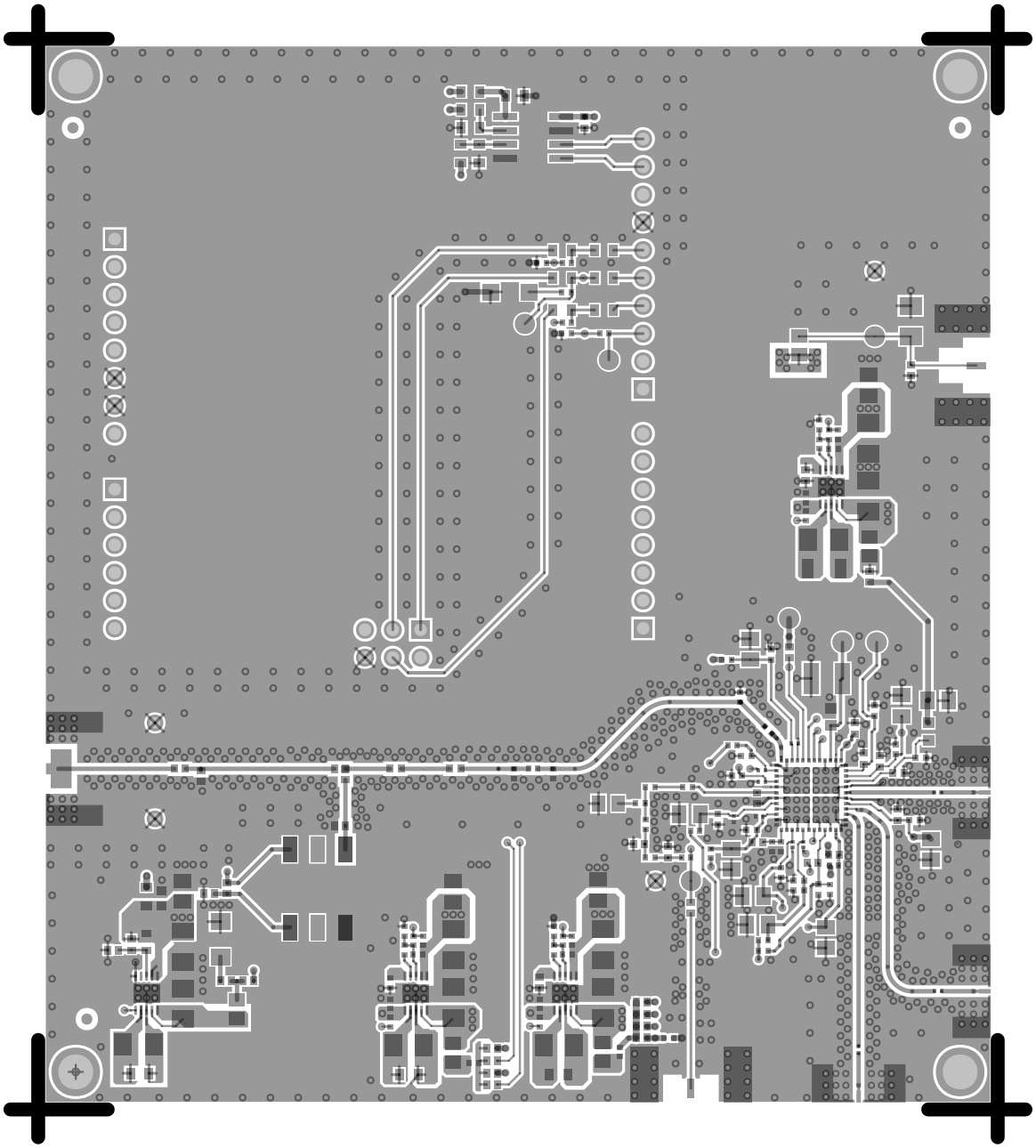

Figure 12. EV-ADF5612SD1Z Evaluation Board Layer 1, Primary

EVALUATION BOARD SCHEMATICS AND ARTWORK

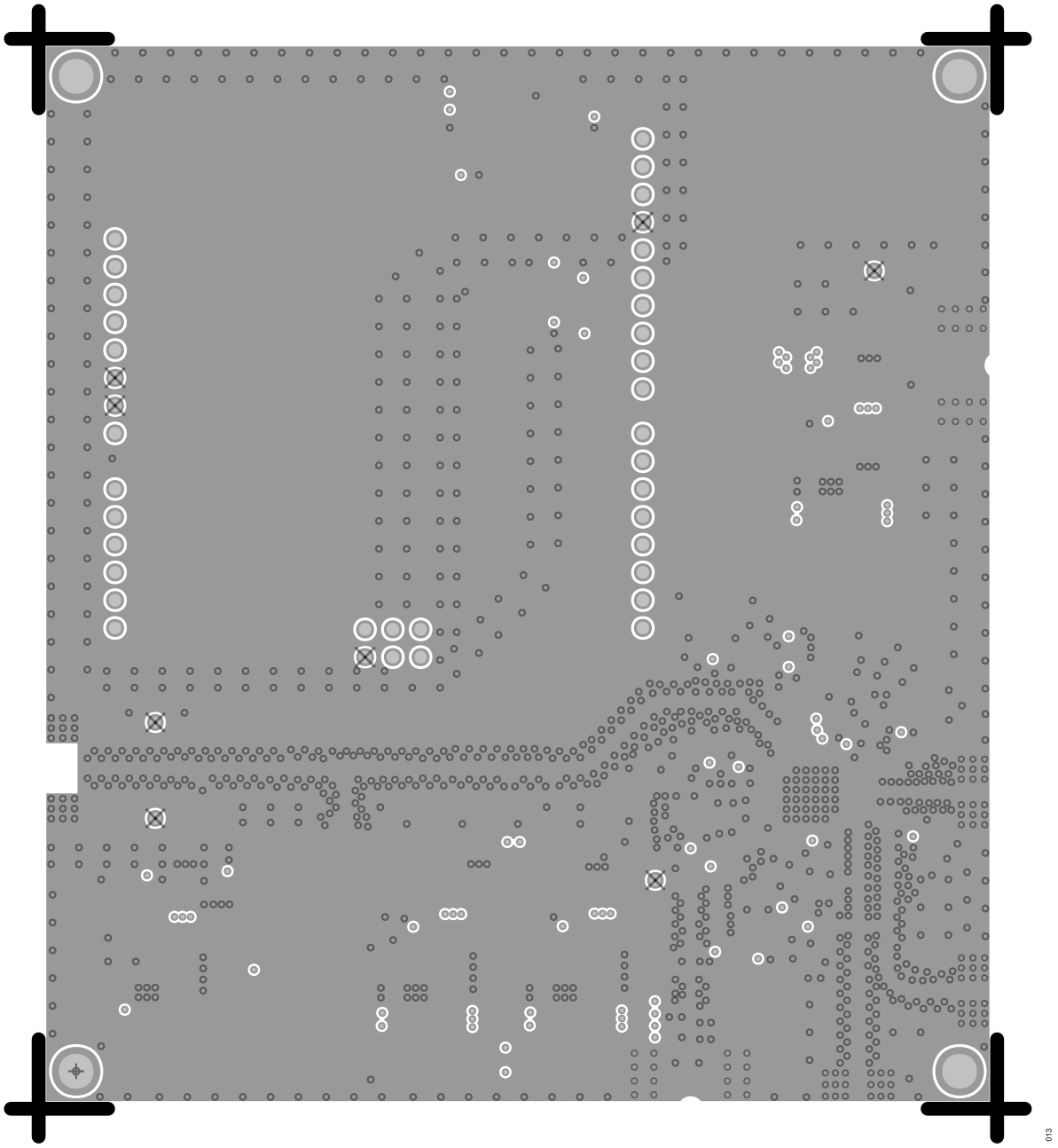

Figure 13. EV-ADF5612SD1Z Evaluation Board Layer 2, Ground

EVALUATION BOARD SCHEMATICS AND ARTWORK

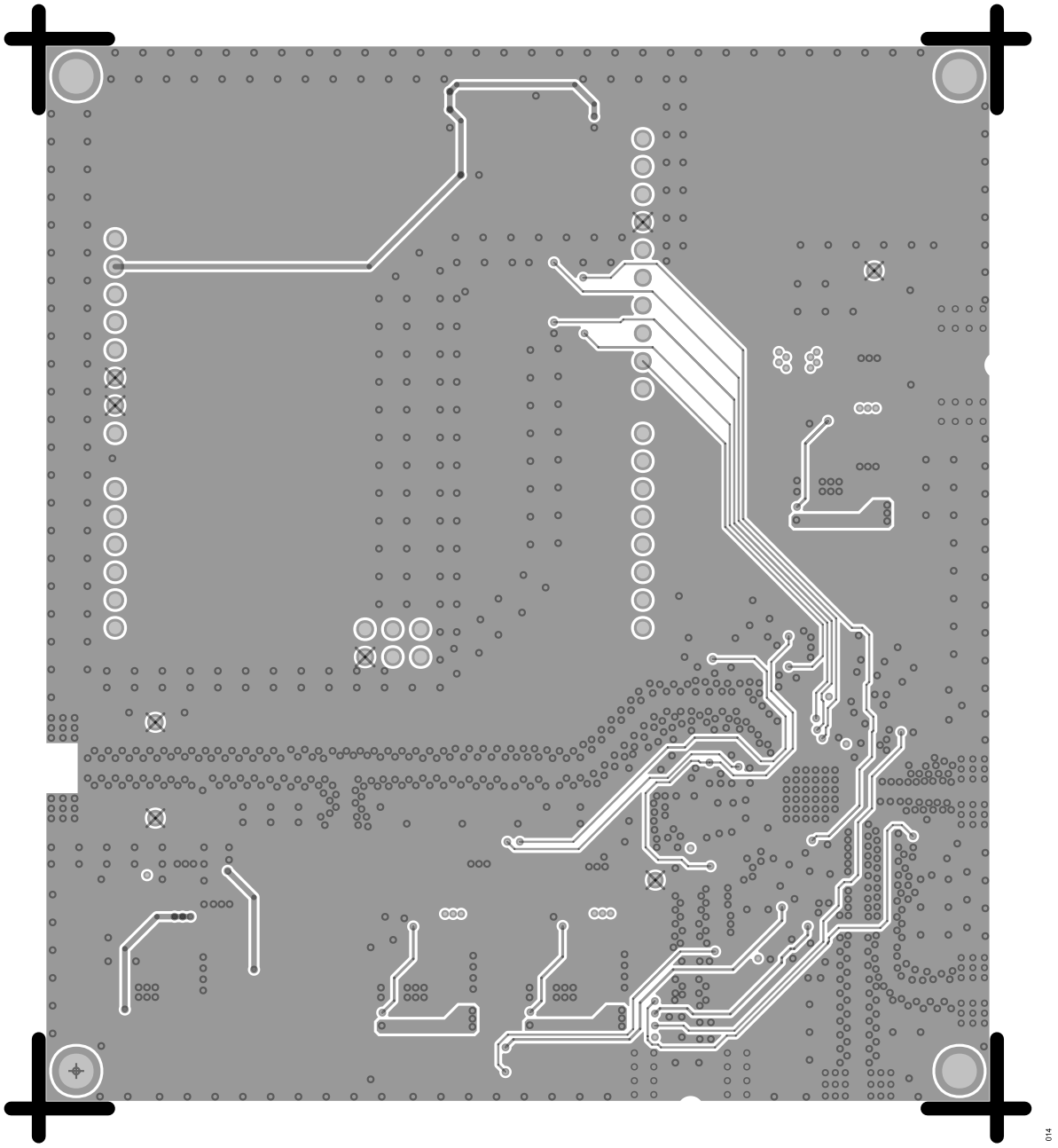

Figure 14. EV-ADF5612SD1Z Evaluation Board Layer 3, Internal

EVALUATION BOARD SCHEMATICS AND ARTWORK

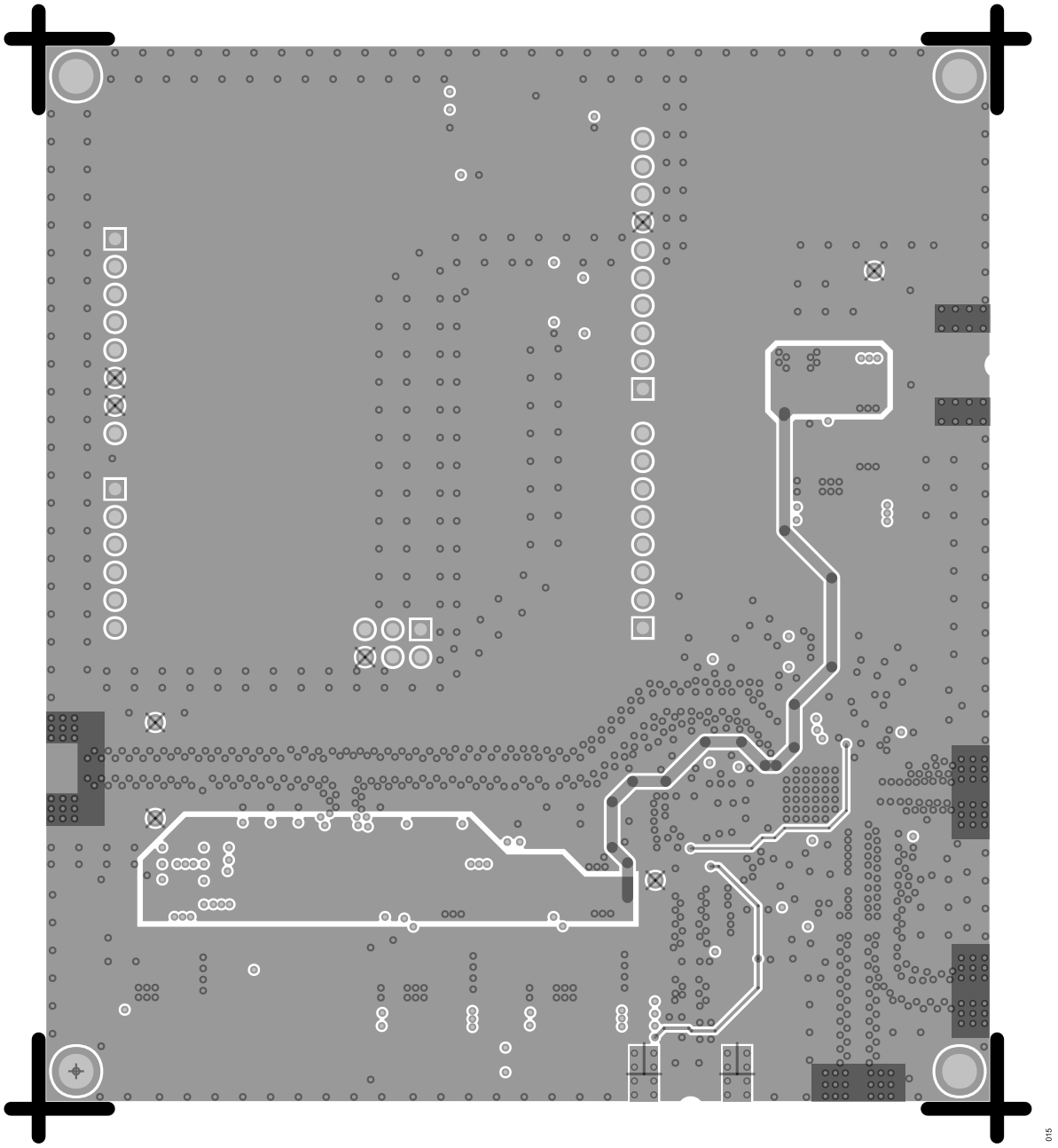

Figure 15. EV-ADF5612SD1Z Evaluation Board Layer 4, Secondary

EVALUATION BOARD SCHEMATICS AND ARTWORK

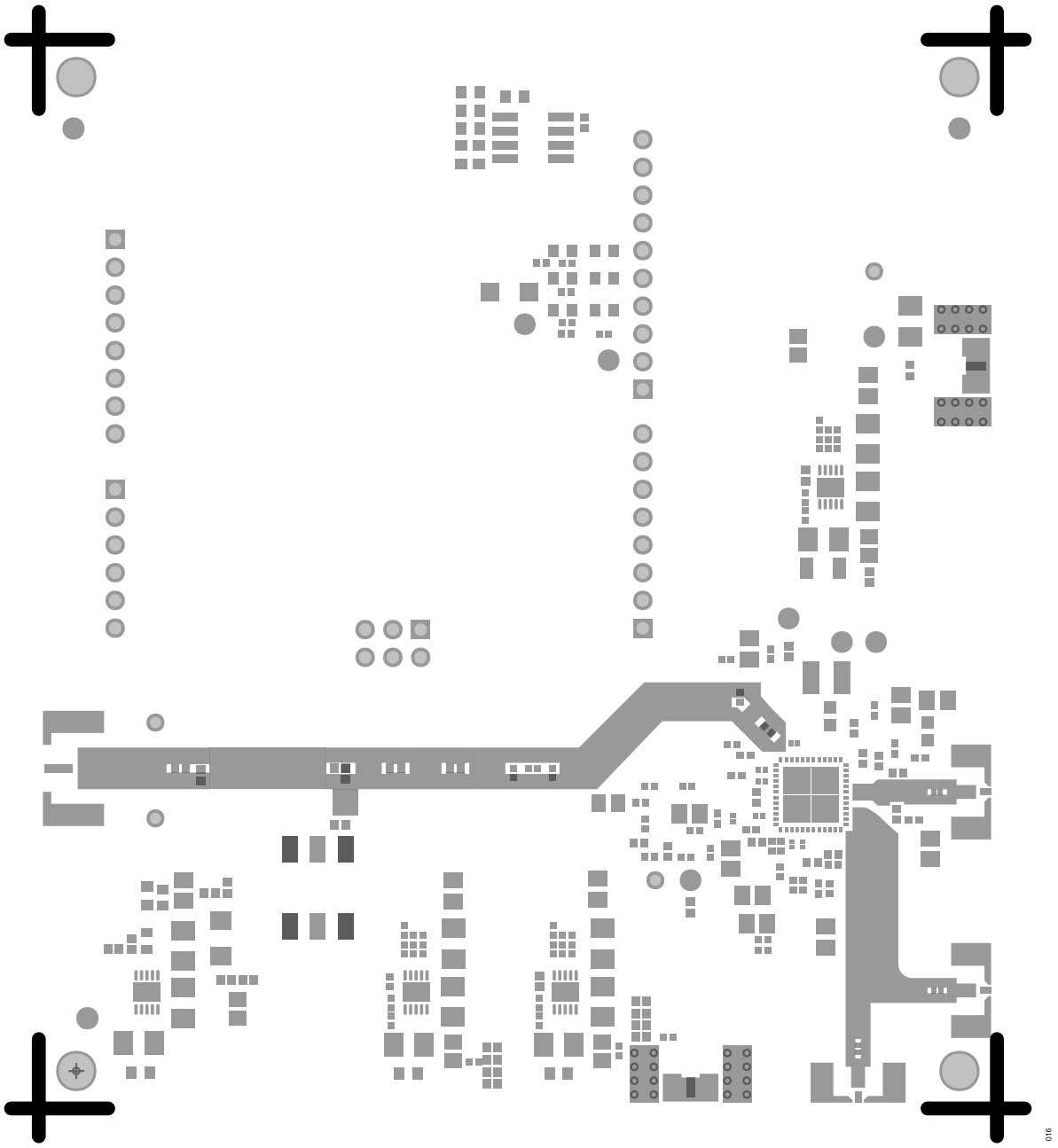

Figure 16. EV-ADF5612SD1Z Evaluation Board Silkscreen, Top Side

EVALUATION BOARD SCHEMATICS AND ARTWORK

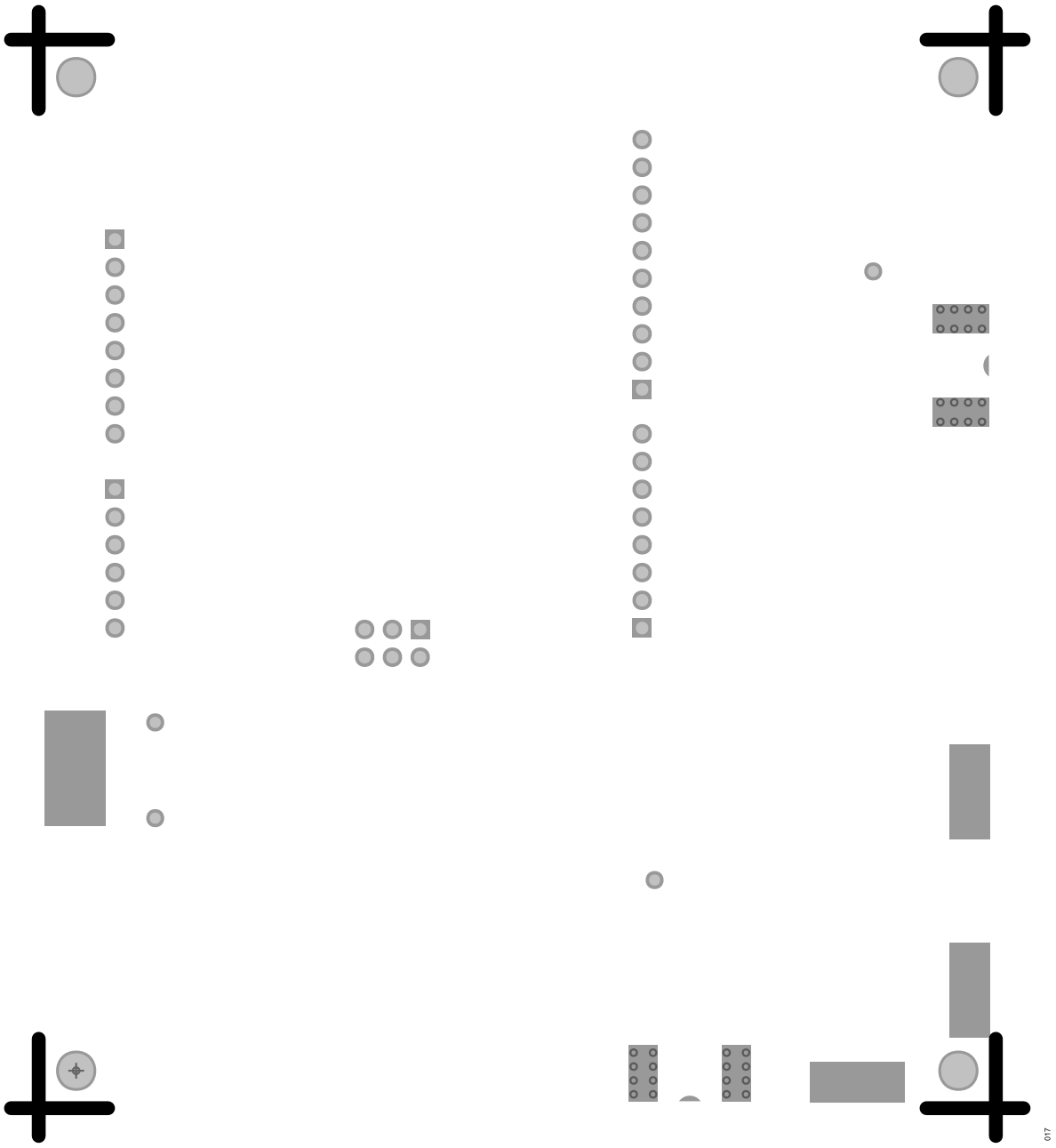

Figure 17. EV-ADF5612SD1Z Evaluation Board Silkscreen, Bottom Side

EVALUATION BOARD SCHEMATICS AND ARTWORK

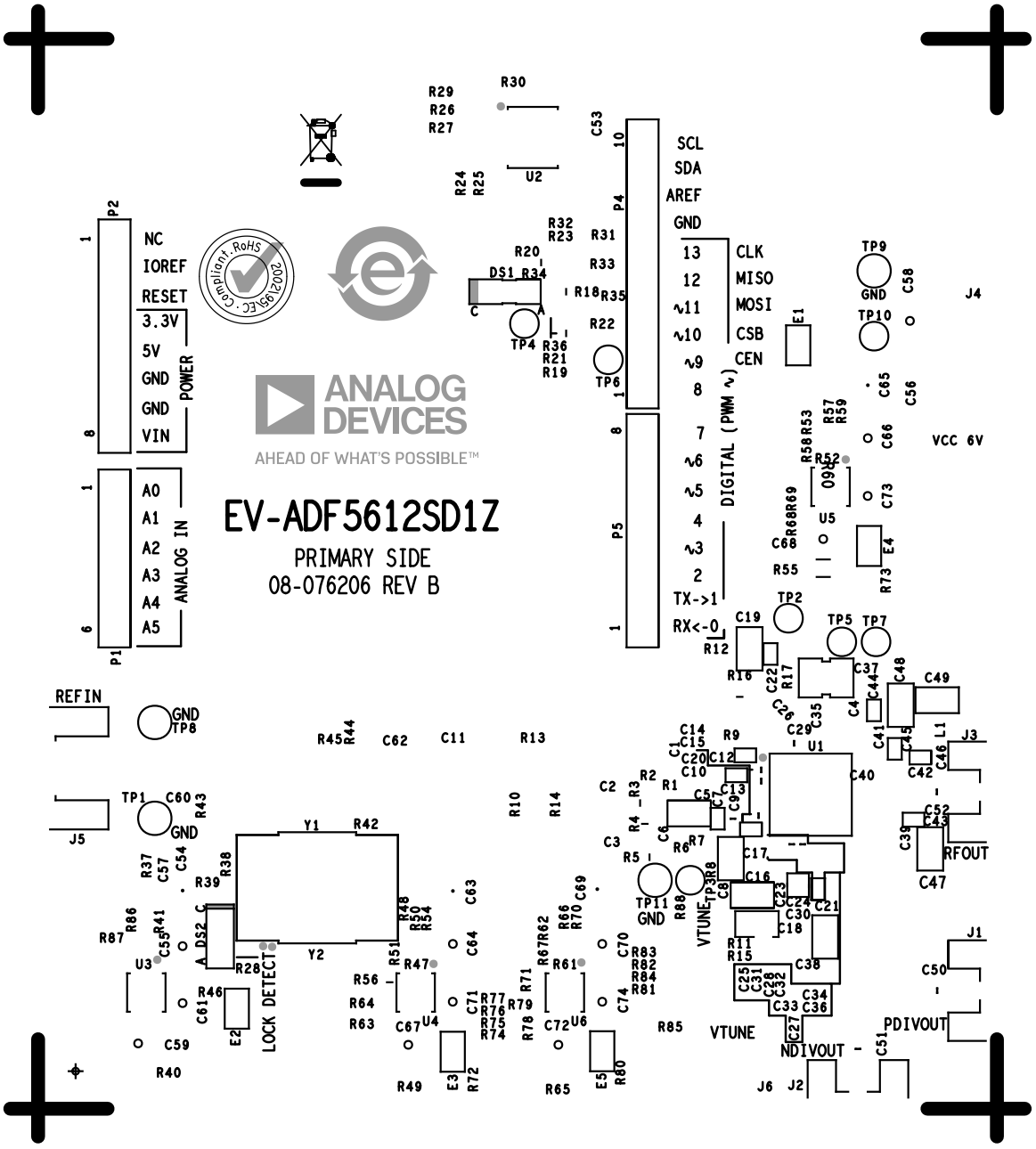

Figure 18. EV-ADF5612SD1Z Evaluation Board Solder Mask, Top Side

EVALUATION BOARD SCHEMATICS AND ARTWORK

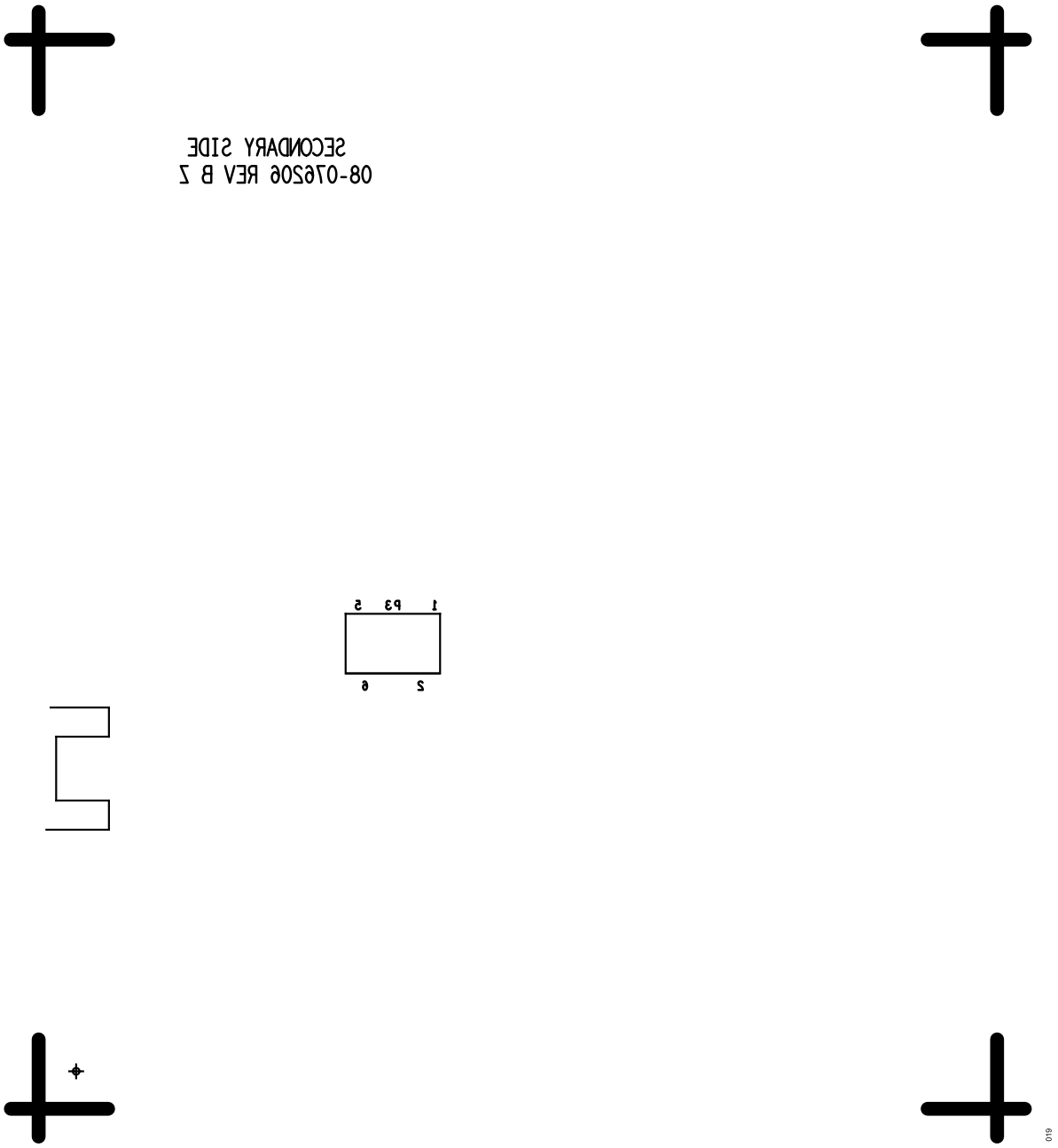

Figure 19. EV-ADF5612SD1Z Evaluation Board Solder Mask, Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C1, C3, C6	0.022µF ceramic capacitors, 16V, 5%, X7R, 0402	Murata	GRM155R71C223JA01D
C7, C10, C12, C13, C21, C22, C23, C24, C27, C30, C36, C43, C44, C45, C46	0.47µF ceramic capacitors, 6.3V, 10%, X7R, 0402, AEC-Q200	Taiyo Yuden	JMK105B7474KVHF
C11, C26, C56	0.1µF ceramic capacitors, 10V, 10%, X5R, 0402	AVX Corporation	0402ZD104KAT2A
C9, C14, C15, C20, C28, C29, C32	10pF ceramic capacitors, 25V, 5%, C0G, 0201	Murata	GRM0335C1E100JA01D
C5, C8, C16, C18, C19	4.7µF ceramic capacitors, 16V, 5%, X7R, 0805, AEC-Q200	Kemet	C0805X475J4RACAUTO
C2	1µF ceramic capacitor, 10V, 10%, X7R, 0805	Taiyo Yuden	MSASL219SB7105KTNA01
C31	0.22µF ceramic capacitor, 16V, 10%, X7R, 040,2 AEC-Q200	Murata	GCM155R71C224KE02D
C33, C42	22pF ceramic capacitors, 50V, 5%, C0G, 0402	Yageo	CC0402JRNPO9BN220
C34, C39, C40, C41	100pF ceramic capacitors, 50V, 5%, C0G, 0402	TDK	C1005NP01H101J050BA
C35	0.01µF ceramic capacitor, 50V, 10%, X7R, 0603	Yageo	CC0603KRX7R9BB103
C37	10µF ceramic capacitor, 75V, 10%, X7R, 1210, AEC-Q200, low effective series resistance (ESR)	TDK	CGA6P1X7R1N106K250AC
C4	100pF ceramic capacitor, 50V, 1%, C0G, 0402, AEC-Q200	Murata	GCM1555C1H101FA16D
C50, C51, C52	0.1µF ceramic capacitors, 16V, 20%, X7R, 0201	Murata	GRM033Z71C104ME14D
C53	0.1µF ceramic capacitor, 16V, 10%, X7R, 0402, AEC-Q200	Murata	GCM155R71C104KA55D
C55, C58, C59, C64, C66, C67, C68, C70, C72	4.7µF ceramic capacitors, 25V, 10%, X7R, 1206	Kemet	C1206C475K3RACTU
C60, C62	1000pF ceramic capacitors, 50V, 5%, C0G, 0402	Murata	GRM1555C1H102JA01
C61, C71, C73, C74	10µF ceramic capacitors, 35V, 10%, X7R, 1206	Samsung	CL31B106KLHNFNE
C63, C65, C69	22µF ceramic capacitors, 25V, 20%, X5R, 0805, AEC-Q200	Murata	GRT21BR61E226ME13L
DS1	Light emitting diode (LED), unicolor, green, 570nm	Dialight	599-0460-127F
DS2	LED, 565NM, green, diff, 1206, surface-mounted device (SMD)	Lumex	SML-LX1206GW-TR
E1, E2, E3, E4, E5	Inductors, chip, ferrite bead, multilayer, 0.5A, 0.280Ω maximum DC resistance (DCR), 1kΩ at 100MHz	Murata	BLM21AG102SN1D
J1, J2, J3	Connectors, printed circuit board (PCB), 2.92mm, edge mount jack, DC40GHz	Gigalane	G02SFB009
J4, J6	Connectors, PCB, SMA, 50Ω, end launch jack receptacle for high speed app use, ALT_SYMBOLS	Cinch	142-0701-851
J5	Connector, PCB, end launch jack, SMA, 62mils board thickness; for 30mils and 10mils, use ALT_SYMBOLS	Cinch	142-0701-851
L1	47nH inductor, RF ceramic chip, 0.9Ω, DCR, 0.3A	Johanson Technology	L-14C47NJV4T
P1	Connector, PCB, receptacle, 25mil square post, 2.54mm pitch	Samtec	SSQ-106-03-G-S
P2, P5	Connectors, PCB, receptacle, 25mil square post, 2.54mm pitch	Samtec	SSQ-108-03-G-S
P3	Connector, PCB, receptacle, 25mil square post, dual-row, 2.54mm pitch	Samtec	SSQ-103-03-G-D
P4	Connector, PCB, receptacle, 25mil square post, 2.54mm pitch	Samtec	SSQ-110-03-G-S
R1, R2, R6, R7, R8, R9, R11, R12, R13, R15, R21, R23, R28, R44, R47, R50, R52, R57, R61, R66, R72, R80	0Ω resistors, SMD, jumper, 1/10W, 040,2 AEC-Q200	Panasonic	ERJ-2GE0R00X

ORDERING INFORMATION

Table 2. Bill of Materials (Continued)

Reference Designator	Description	Manufacturer	Part Number
R16	49.9Ω SMD resistor, 1%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2RKF49R9X
R17, R19	100kΩ SMD resistors, 5%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2GEJ104X
R18	1.1kΩ SMD resistor, 5%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2GEJ112X
R22	1kΩ SMD resistor, 1%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1001X
R24, R27, R30	100kΩ SMD resistors, 1%, 1/16W, 0603	Multicomp (SPC)	MC 0.063W 0603 1% 100K
R3, R4, R5	47Ω SMD resistors,1%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2RKF47R0X
R31, R33, R35	1kΩ SMD resistors, 1%, 1/10W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1001V
R37	1Ω SMD resistor, 5%, 1/10W, 0603, AEC-Q200	Panasonic	ERJ-3GEYJ1R0V
R40, R41	49.9kΩ SMD resistors, 1%, 1/10W, 0603, AEC-Q200	Panasonic	ERJ-3EKF4992V
R43	51Ω SMD resistor, 5%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2GEJ510X
R46	619Ω SMD resistor, 1%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2RKF6190X
R49, R65	33.2kΩ SMD resistor, 1%, 1/10W, 0603, AEC-Q200	Panasonic	ERJ-3EKF3322V
R55	49.9kΩ SMD resistor, 0.01%, 1/4W, 1206, AEC-Q200	Stackpole Electronics, Inc.	RNCF1206TKY49K9
R56	2.49kΩ SMD resistor, 1%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2RKF2491X
R60	953Ω SMD resistor, 1%, 1/16W, 0402, AEC-Q200	Vishay	CRCW0402953RFKED
R71	412Ω SMD resistor, 1%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2RKF4120X
R73, R74, R75, R76, R77, R81, R82, R83, R84	0.1Ω SMD resistors, 1%, 1/6W, 0402, AEC-Q200	Panasonic	ERJ-2BSFR10X
R85	3.3kΩ SMD resistor, 1%, 1/10W, 0402, AEC-Q200	Panasonic	ERJ-2RKF3301X
TP1, TP8, TP9, TP11	Connectors, PCB, black test points	Keystone Electronics	5001
TP4, TP6	Connectors, PCB, surface-mount contact pin	Mill-Max	4956-1-00-15-00-00-33-0
U1	IC, microwave wideband synthesizer with integrated VCO	Analog Devices, Inc.	ADF5612CCCZ
U2	IC, 32KBIT serial electrically erasable programmable read-only memory (EEPROM)	Microchip Technology	24AA32A-I/SN
U3, U4, U5	IC, 20V, 200mA, ultralow noise, ultrahigh power supply rejection ratio (PSRR) RF linear regulators	Analog Devices	LT3042EDD#PBF
U6	IC, 20V, 500mA, ultralow noise, ultrahigh PSRR linear regulator	Analog Devices	LT3045EDD#PBF
Y1	IC, VCXO differential oscillator, 122.880MHz	Crystek Corporation	CVPD-922X-122.880

ORDERING INFORMATION

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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