Evaluating the ADF4383 Microwave Wideband Synthesizer with Integrated VCO

FEATURES

- Self-contained evaluation board, including the ADF4383 frequency synthesizer with integrated VCO, loop filter, USB interface, propagation delay calibration paths, and voltage regulators
- Windows®-based software allows control of synthesizer functions from a PC
- Externally powered by 6 V

EVALUATION KIT CONTENTS

- EV-ADF4383SD1Z evaluation board

EQUIPMENT NEEDED

- A Windows-based PC with USB port for the evaluation software
- A system demonstration platform, serial only EVAL-SDP-CS1Z controller board (SDP-S) or EVAL-SDP-CK1Z (SDP-K1)
- Power supply (6 V)
- Spectrum analyzer or phase noise analyzer
- 50 Ω termination
- Low noise input reference (REF_{IN}) source (125MHz output frequency)

DOCUMENTS NEEDED

- ADF4383 data sheet
- EV-ADF4383SD1Z user guide

REQUIRED SOFTWARE

- Analysis | Control | Evaluation (ACE) Software, Version 1.30 or newer
- ADF4383 plug-in, 1.2024.17500 or newer

GENERAL DESCRIPTION

The EV-ADF4383SD1Z evaluates the performance of the ADF4383 frequency synthesizer with an integrated voltage-controlled oscillator (VCO) for phase-locked loops (PLLs). A photograph of the evaluation board is shown in Figure 1. The EV-ADF4383SD1Z contains the ADF4383 frequency synthesizer with an integrated VCO, a USB interface, power supply connectors, propagation delay calibration paths, and Subminiature Version A (SMA) connectors. The outputs of the EV-ADF4383SD1Z are AC-coupled with 50 Ω transmission lines, making these outputs suitable to drive 50 Ω impedance instruments. The reference source is provided externally via SMA connectors (REFP/REFN).

The EV-ADF4383SD1Z requires an SDP-S controller board, which is not supplied with the evaluation board kit). The SDP-S allows software programming of the EV-ADF4383SD1Z with Analog Devices, Inc., ACE software.

Full specifications for the ADF4383 frequency synthesizer are available in the ADF4383 data sheet, which must be consulted in conjunction with this user guide when working with the EV-ADF4383SD1Z.

EV-ADF4383SD1Z EVALUATION BOARD PHOTOGRAPH

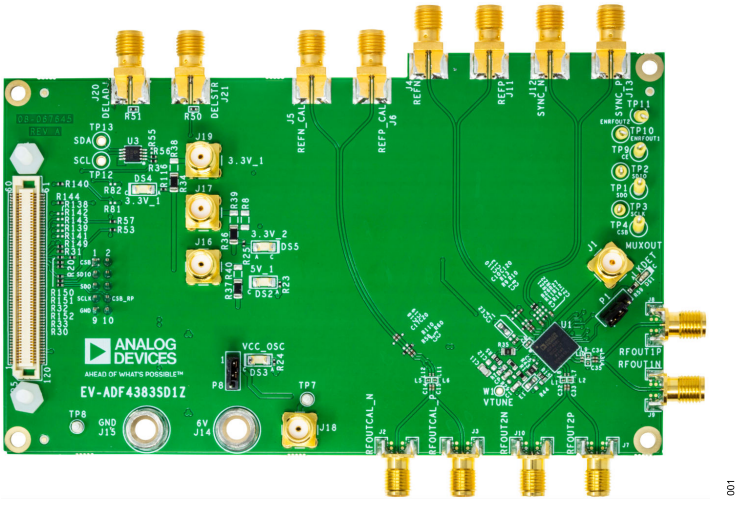

Figure 1. EV-ADF4383SD1Z Evaluation Board Photograph

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REVISION HISTORY

7/2026—Rev. 0 to Rev. A

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1/2025—Revision 0: Initial Version

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURE

To install the ADF4383 plug-in, take the following steps:

1. Install the latest version of the ACE software platform from the Analysis | Control | Evaluation (ACE) Software web page.
2. Scroll to the **ACE Evaluation Board Plug-ins** selection of the ACE web page
3. In the search bar within the **ACE Evaluation Board Plug-ins** section of the ACE web page, search for the ADF4383 and install the chip and board plug-ins that appear.
4. Ensure that the ADF4383 plug-ins appear when the EV-ADF4383SD1Z board is attached through the SDP-S connector to the PC.

EVALUATION BOARD SETUP PROCEDURES

The EV-ADF4383SD1Z uses a single 6 V power supply with J14 and J15 banana plugs or J18 SMA connector by default. On-board low noise, low dropout (LDO) regulators are used to generate nominal 3.3 V and 5 V supplies.

Details of the power supply circuitry are given in the Power Supplies section.

To power-up the EV-ADF4383SD1Z, perform the following steps:

1. Set the voltage of the power supply to 6 V and the current limit to 1 A.
2. Connect the power cables to J14 and J15 (two banana cables) or to J18 (single SMA cable).
3. Turn on the power.

To run the **ACE Software**, take the following steps:

1. Select **Start/All Programs/Analog Devices/ACE**.
2. Under the **Select Device and Connection** tab, select the **ADF4383** and the **ADF4383 Board** then appears within the **Attached Hardware** section.
3. When connecting the EV-ADF4383SD1Z, allow 5 seconds to 10 seconds for the label on the **Status** bar to change.
4. Within the **ADF4383 Board** plug-in, use the dropdown menu to select the **ADF4383** before opening the chip plug-in.

EVALUATION BOARD HARDWARE

The EV-ADF4383SD1Z requires the SDP-S platform that uses the EVAL-SDP-CS1Z, which is not supplied with the evaluation kit.

POWER SUPPLIES

The EV-ADF4383SD1Z is powered by a 6 V power supply connected to the J18 SMA connector or the J14 banana plug and GND to the J15 banana plug.

The power supply circuitry has three LT3045 high performance, low noise, and low dropout (LDO) regulators and one LT3042 high performance, low noise, and LDO regulator.

One LT3045 is used to generate 5 V to drive the VCO supply pins (V_{5V_VCO}), and the other two LT3045 regulators provide 3.3 V supplies for the 3.3 V Supply Group 1 ($V_{3.3V\_1}$) and 3.3 V Supply Group 2 ($V_{3.3V\_2}$).

The EV-ADF4383SD1Z provides the flexibility to use external 3.3 V and 5 V supplies with the component placement changes detailed in Table 2.

Table 1. 6 V Component Placement for Power Supplies (DNI Stands for Do Not Install)

	$V_{3.3V\_1}$		$V_{3.3V\_2}$		V_{5V_VCO}	
6 V Supply	**R34**	**R38**	**R36**	**R39**	**R37**	**R40**
Component	0 Ω	DNI	0 Ω	DNI	0 Ω	DNI
Connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector

Table 2. External Supply Component Placement for Power Supplies (DNI Stands for Do Not Install)

	$V_{3.3V\_1}$		$V_{3.3V\_2}$		V_{5V_VCO}	
External Supply	**R34**	**R38**	**R36**	**R39**	**R37**	**R40**
Component	DNI	0 Ω	DNI	0 Ω	DNI	0 Ω
Connector	J19	J19	J17	J17	J16	J16

EVALUATION BOARD HARDWARE

REFERENCE INPUT

An external oscillator or signal generator signal must be applied to the REFP SMA connector (and REFN for differential configurations) in order to drive the ADF4383 reference input.

Table 3 provides the required board modifications for different reference clock configuration options.

See the ADF4383 data sheet for detailed reference buffer amplitude and frequency considerations.

Note that earlier revisions of the evaluation board included an on-board reference oscillator option. The information in this user guide applies to the latest revision of the board, which requires an externally supplied reference.

Table 3. Component Placement for Different Reference Sources

		Differential External Reference	
Component	**Default Single-Ended External Reference**	**CML/LVPECL**	**LVDS**
C13	1 µF	1 µF	1 µF
C110	Remove	1 µF	1 µF
R9	0 Ω	Remove	Remove
R10	49.9 Ω	Remove	Remove
R13	Do not install	100 Ω	100 Ω

EVALUATION BOARD HARDWARE

RF OUTPUTS

The EV-ADF4383SD1Z has two pairs of SMA connectors for differential clock outputs: RFOUT1P and RFOUT1N, and RFOUT2P and RFOUT2N.

The output power of the clock output channels can be adjusted via the **ACE Software** individually using the **RFOUT1 POWER** and **RFOUT POWER** numeric selectors (see Figure 5).

The clock output channels can be powered down separately via the **ACE Software** or by hardware using the **PD RFOUT 1** and **PD RFOUT 2** check boxes (see Figure 5).

If only one port of a differential pair is used, terminate the complementary port with an equal load terminator (in general, a 50 Ω terminator). Refer to the ADF4383 data sheet for more information on output termination examples.

CALIBRATION PATH

The EV-ADF4383SD1Z has two pairs of SMA connectors for the calibration path input and output: REFN_CAL and REFP_CAL, and RFOUTCAL_N and RFOUTCAL_P. The calibration path is used to measure and calibrate out the EV-ADF4383SD1Z effect on the reference to the output delay.

LOOP FILTER

The loop filter schematic is shown in Figure 8. The fifth-order loop filter on the EV-ADF4383SD1Z is optimized for the ADF4383 low noise amplifier (LNA) reference, a 6 dBm sine-wave reference frequency of 125 MHz, a phase frequency detector (PFD) frequency of 250 MHz, and a charge pump current of 11.1 mA. A fourth-order loop filter can be used with faster slew-rate reference signals that allow the use of the delayed match amplifier (DMA) reference of the ADF4383. Refer to the ADF4383 data sheet for more information on loop filter design.

SERIAL PERIPHERAL INTERFACE (SPI)

Connector P5 interfaces with the SDP-S or SDP-K1 to evaluate the ADF4383 using the **ACE Software** graphical user interface (GUI). A second connector (P2) is provided to enable use with other interface boards. This P2 connector allows a common, open source hardware (OSH)-compatible board, such as PMOD, Raspberry Pi, and Arduino, to interface directly with the EV-ADF4383SD1Z.

EVALUATION BOARD HARDWARE

DEFAULT CONFIGURATION

The EV-ADF4383SD1Z interfaces with the SDP-S or SDP-K1 interface boards. An external reference frequency must be applied from a suitable low noise reference source of 125 MHz frequency to the REFP connector. When the EV-ADF4383SD1Z is powered up and connected to the ACE Software, click **INITIALIZE DEVICE** to provide a 20 GHz output clock on the RFOUT1 channel.

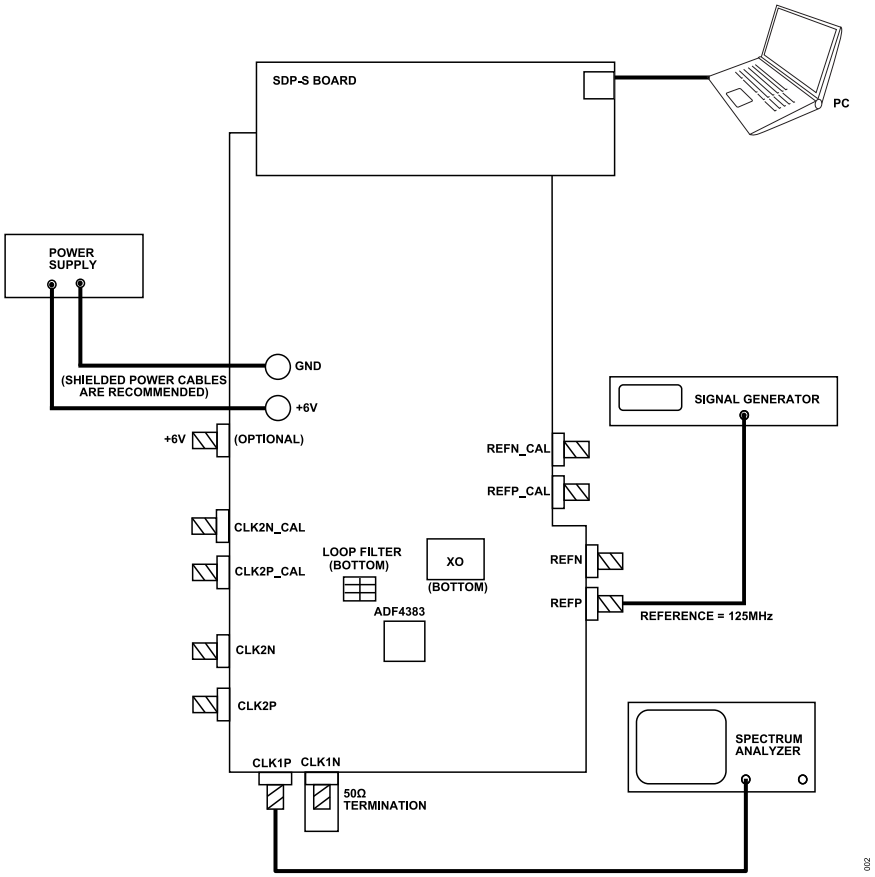

Figure 2. Evaluation Board Setup Diagram

EVALUATION BOARD SOFTWARE

The **ACE Software** is the main platform that is used to control the EV-ADF4383SD1Z. The ADF4383 plug-in includes user interfaces that relate to the ADF4383 and allow evaluation of the device. Use the following steps to open the main control window of the ADF4383:

1. Launch the **ACE Software**. With the SDP-S controller board connected to the EV-ADF4383SD1Z, the **Attached Hardware** section appears in the GUI, as shown in Figure 3.
2. Double-click the **ADF4383 Board** icon and the tab shown in Figure 4 then appears.
3. Double-click the **ADF4383** icon that appears on the board GUI to open the main control window shown in Figure 5.

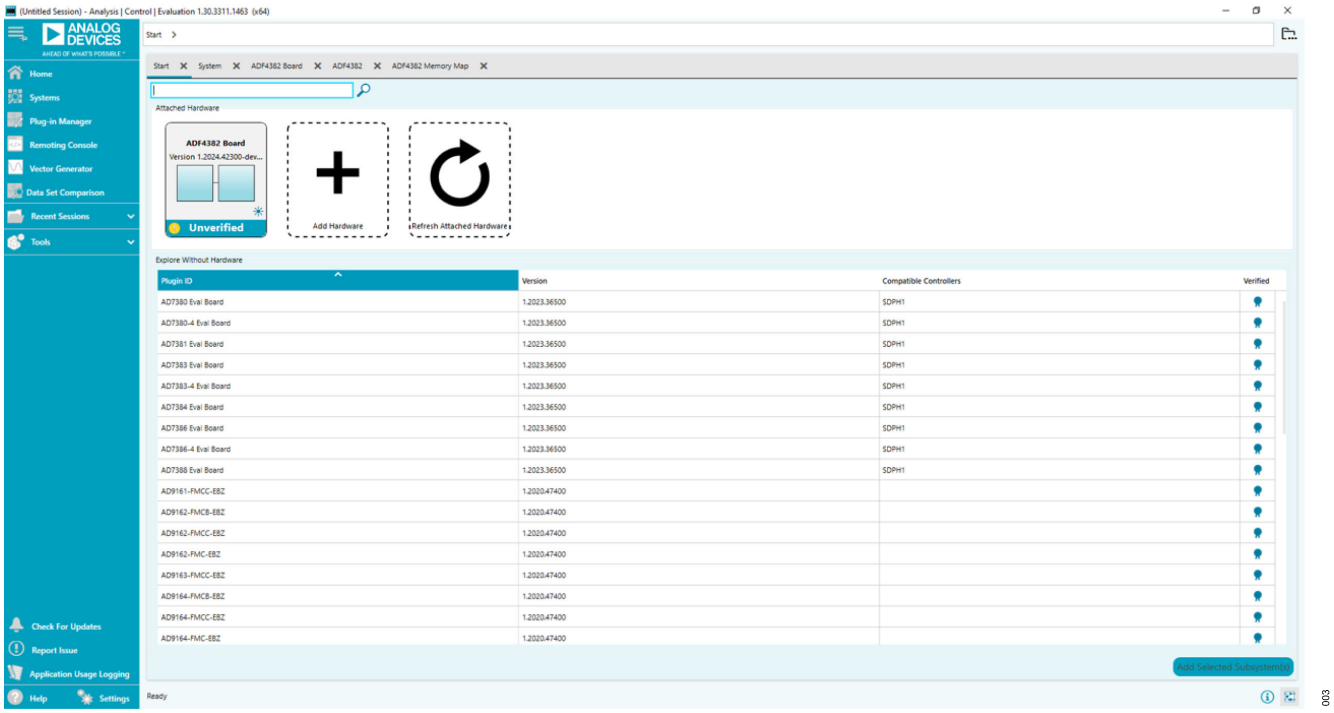

Figure 3. ACE Main Window, Attached Hardware (ADF4383 Evaluation Board)

EVALUATION BOARD SOFTWARE

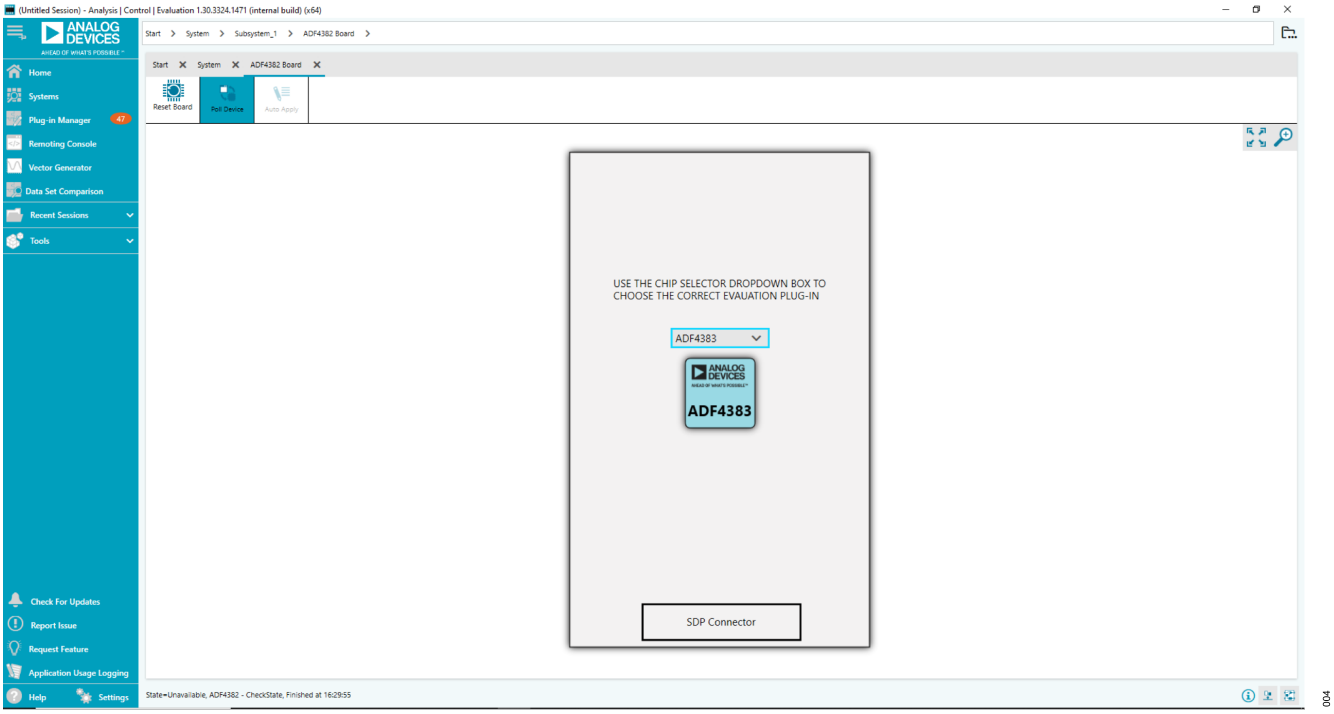

Figure 4. ACE ADF4383 Board Page, Device Selection

EVALUATION BOARD SOFTWARE

MAIN CONTROLS

The main controls are available in the high level register map shown in Figure 5. To modify registers, perform the following steps:

1. Any configuration changes must be done before initializing. The **ACE Software** plug-in opens with the default register settings for a 125 MHz reference frequency, 250 MHz PFD, and 20 GHz output clock frequency.
2. Click **INITIALIZE DEVICE** to write to all of the registers and to initialize the device (see Figure 5).
3. Modify the front panel settings as required.
4. Click **APPLY CHANGES** to load the modified settings to the device. Clicking this button performs the following write sequence:
   a. Programs the changes from the user.
   b. Turns on the clocks necessary for autocalibration.
   c. Triggers an autocalibration by performing a register write to Register 0x010.

If the RFOUT frequency selected is outside of the operational range, an error message appears within the **WARNINGS/ERRORS** section (see Figure 5).

Specific blocks can be powered down by setting the corresponding power-down check box within the **POWER-DOWN** section shown in Figure 5.

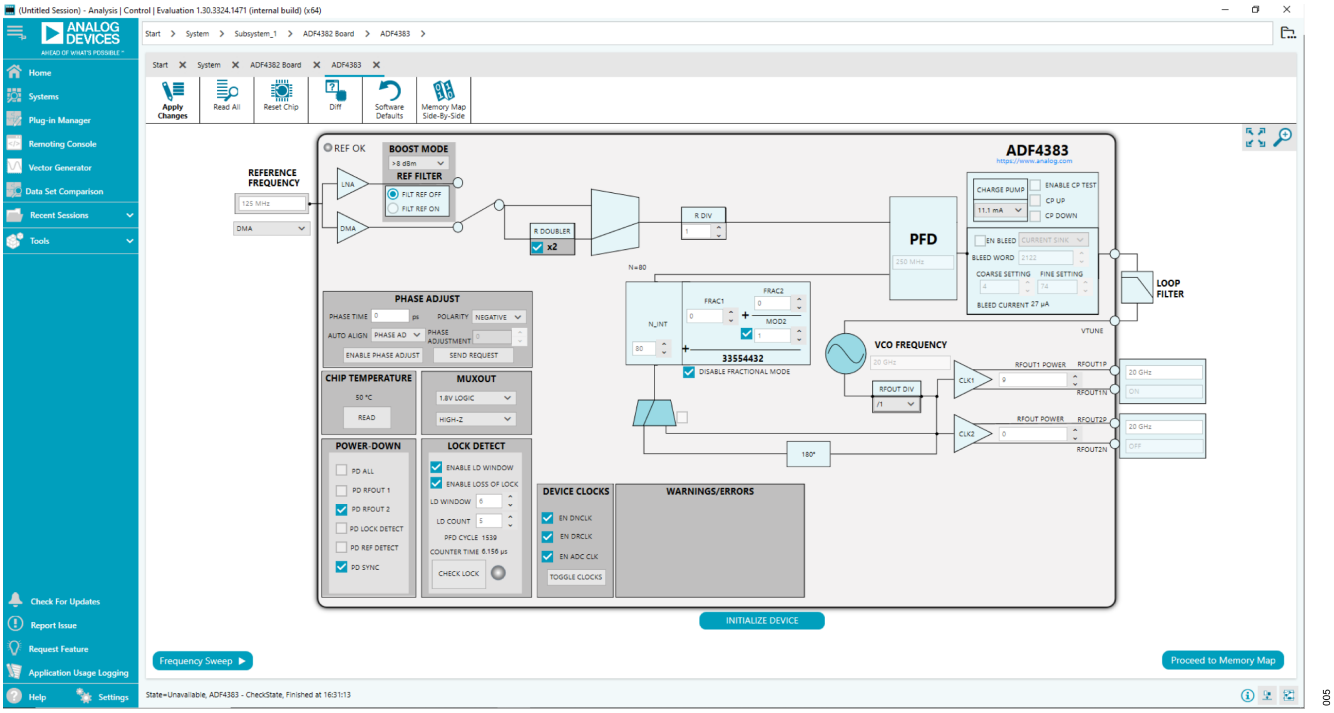

Figure 5. Front Panel

EVALUATION BOARD SOFTWARE

PHASE ADJUSTMENT

The RFOUT phase can be controlled within the **PHASE ADJUST** section in the **ACE Software** (see Figure 5). To adjust the phase, perform the following steps:

1. Click **ENABLE PHASE ADJUST**, to enable the phase adjust feature.
2. Type in the desired phase adjustment in picoseconds in the **PHASE TIME** box.
3. Select **POSITIVE** or **NEGATIVE** polarity for the written phase time using the **POLARITY** dropdown menu.
4. Select **DISABLED** in the **AUTO ALIGN** dropdown menu.
5. Click **SEND REQUEST**.

The actual phase adjustment value is then recorded in the **PHASE ADJUSTMENT** numeric box. Note that the **PHASE TIME** value in picoseconds cannot exceed the period of the **RFOUT** used. For calculations, see the Bleed Current Phase Adjustment section in the ADF4383 data sheet.

FREQUENCY SWEEP

To use the ADF4383 to perform a frequency sweep set the **START FREQUENCY**, **STOP FREQUENCY**, **FREQUENCY SPACING**, and **ADDITIONAL DELAY (ms)**. If the **ENABLE VCO READ BACK** check box is selected, the corresponding **VCOCore**, **VCOBand**, and **VCOBias** of the configured frequencies is written to the **VCO CALIBRATION TABLE** (see Figure 6).

To perform a frequency sweep, take the following steps:

1. Set the **START FREQUENCY**, **STOP FREQUENCY**, and **FREQUENCY SPACING**.
2. Check off the **ENABLE VCO READ BACK** check box.
3. Click **START/STOP SWEEP**.

Alternatively, click **RUN SINGLE SWEP** instead to perform one frequency step on each button click.

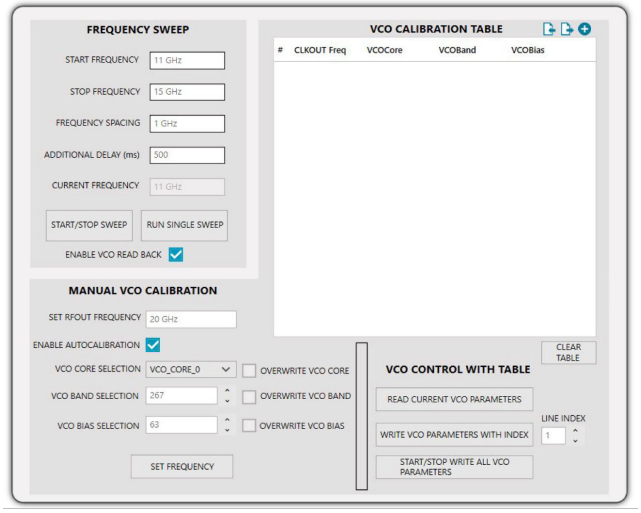

Figure 6. ACE Frequency Sweep

MANUAL VCO CONTROL

The ADF4383 can bypass autocalibration by manually writing predetermined VCO core, band, and bias information. The **MANUAL VCO CALIBRATION** section shown in Figure 6 of the ADF4383 plug-in can be used to perform an autocalibration bypass.

Take the following steps, to perform the autocalibration bypass:

1. Disable the **ENABLE AUTOCALIBRATION** check box by deselecting the check box.
2. Select the **VCO CORE SELECTION** by using the dropdown menu and check off the **OVERWRITE VCO CORE** check box.
3. Set the **VCO BAND SELECTION** value and check off the **OVERWRITE VCO BAND** check box.
4. Set the **VCO BIAS SELECTION** value and check off **OVERWRITE VCO BIAS** check box.
5. Click **SET FREQUENCY**.

Configure the VCO within the **VCO CALIBRATION TABLE**:

1. Click **READ CURRENT VCO PARAMETERS** to read the VCO parameters at the current frequency.
2. Click **WRITE VCO PARAMETERS WITH INDEX** to apply the VCO parameters. Use the **LINE INDEX** box to select the line to apply from the **VCO CALIBRATION TABLE**.
3. Click **START/STOP WRITE ALL PARAMETERS** to apply all the VCO parameters from the **VCO CALIBRATION TABLE**.

EVALUATION AND TEST

To evaluate and test the performance of the ADF4383, prepare the hardware and software setup as outlined in the Evaluation Board Hardware section and the Evaluation Board Software section.

Run the software and follow the steps given in Evaluation Board Software section to open the main controls shown in Figure 5.

Click **INITIALIZE DEVICE** to provide a 20 GHz clock at the RFOUT1P and RFOUT1N output. Then, measure the output spectrum and single sideband phase noise on a signal analyzer.

Figure 7 shows a phase noise plot of the SMA RFOUT1P output equal to 20 GHz with a 125 MHz external reference oscillator (250 MHz PFD frequency, buffer selection: DMA buffer, and doubler: disabled).

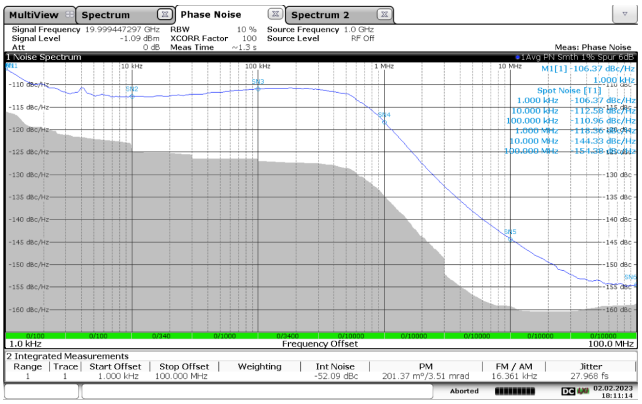

Figure 7. Single Sideband Phase Noise of 20 GHz Output

EVALUATION BOARD SCHEMATIC AND ARTWORK

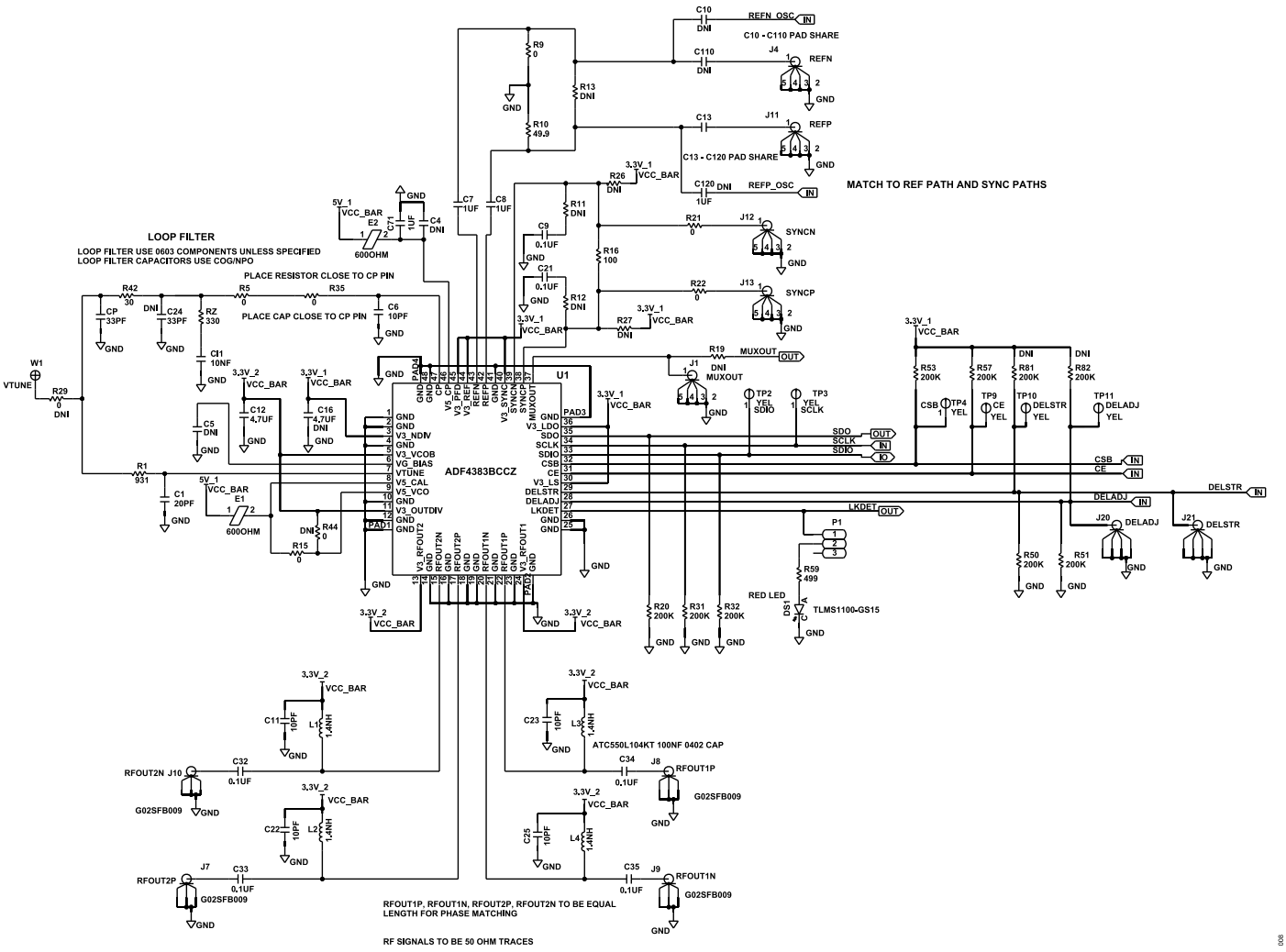

Figure 8. EV-ADF4383SD1Z Schematic, ADF4383 Connections and Loop Filter

EVALUATION BOARD SCHEMATIC AND ARTWORK

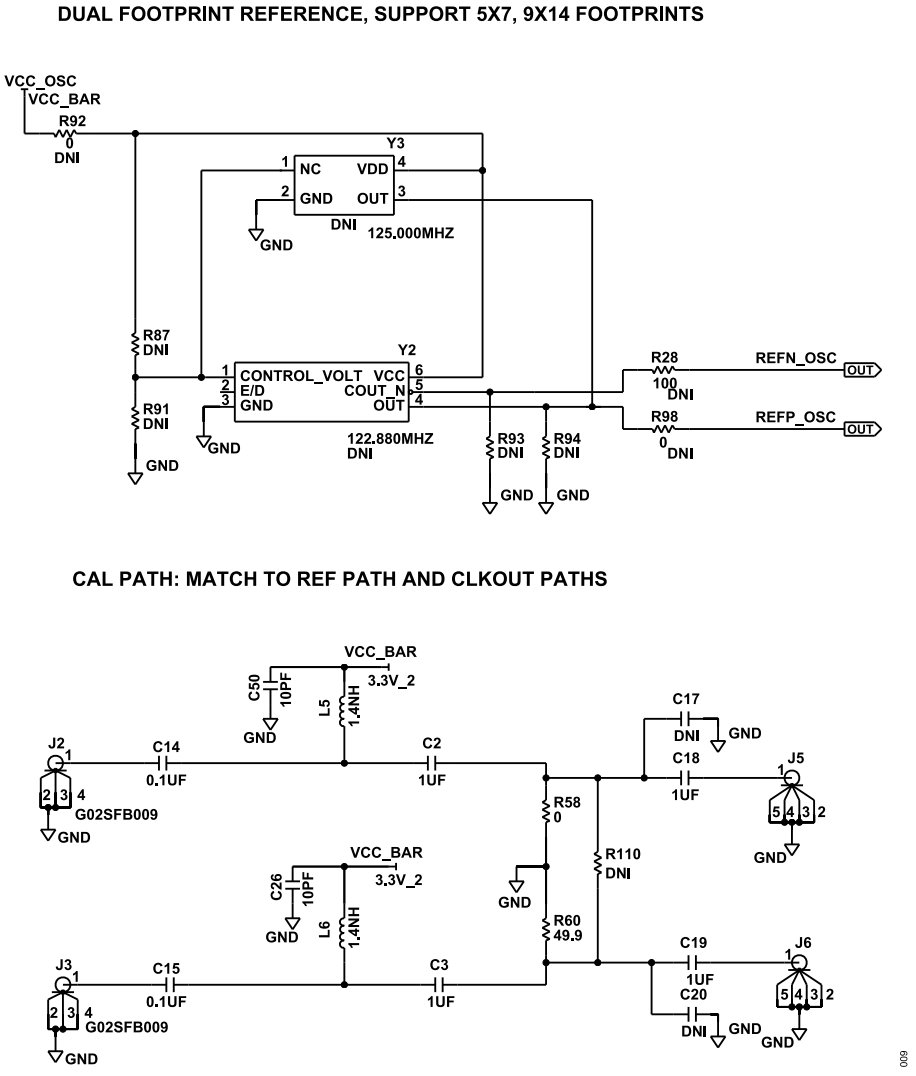

Figure 9. EV-ADF4383SD1Z Schematic, ADF4383 On-Board Ultra-Low Noise Oscillator and Calibration Path

EVALUATION BOARD SCHEMATIC AND ARTWORK

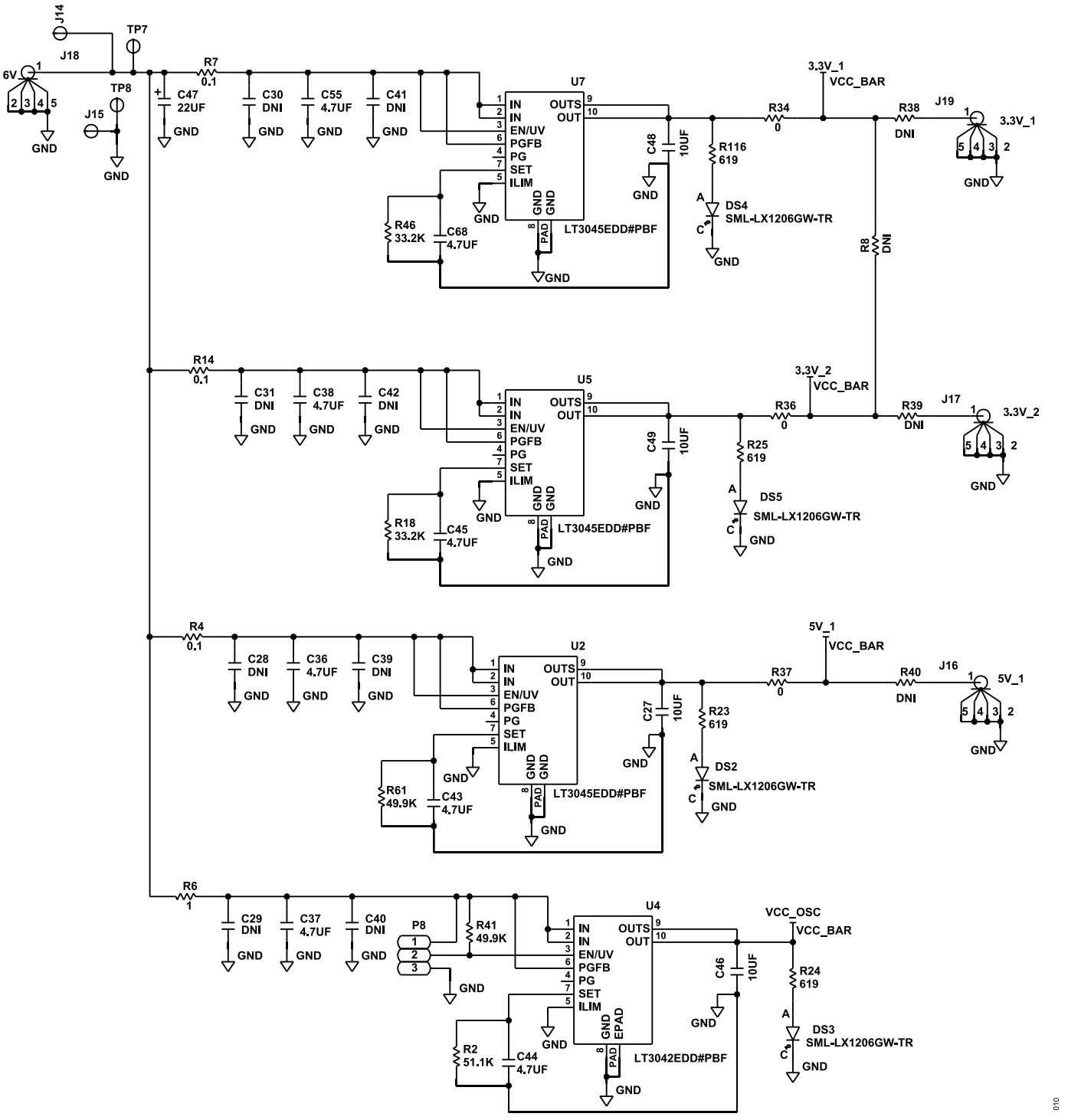

Figure 10. EV-ADF4383SD1Z Schematic, ADF4383 LDO Regulators

EVALUATION BOARD SCHEMATIC AND ARTWORK

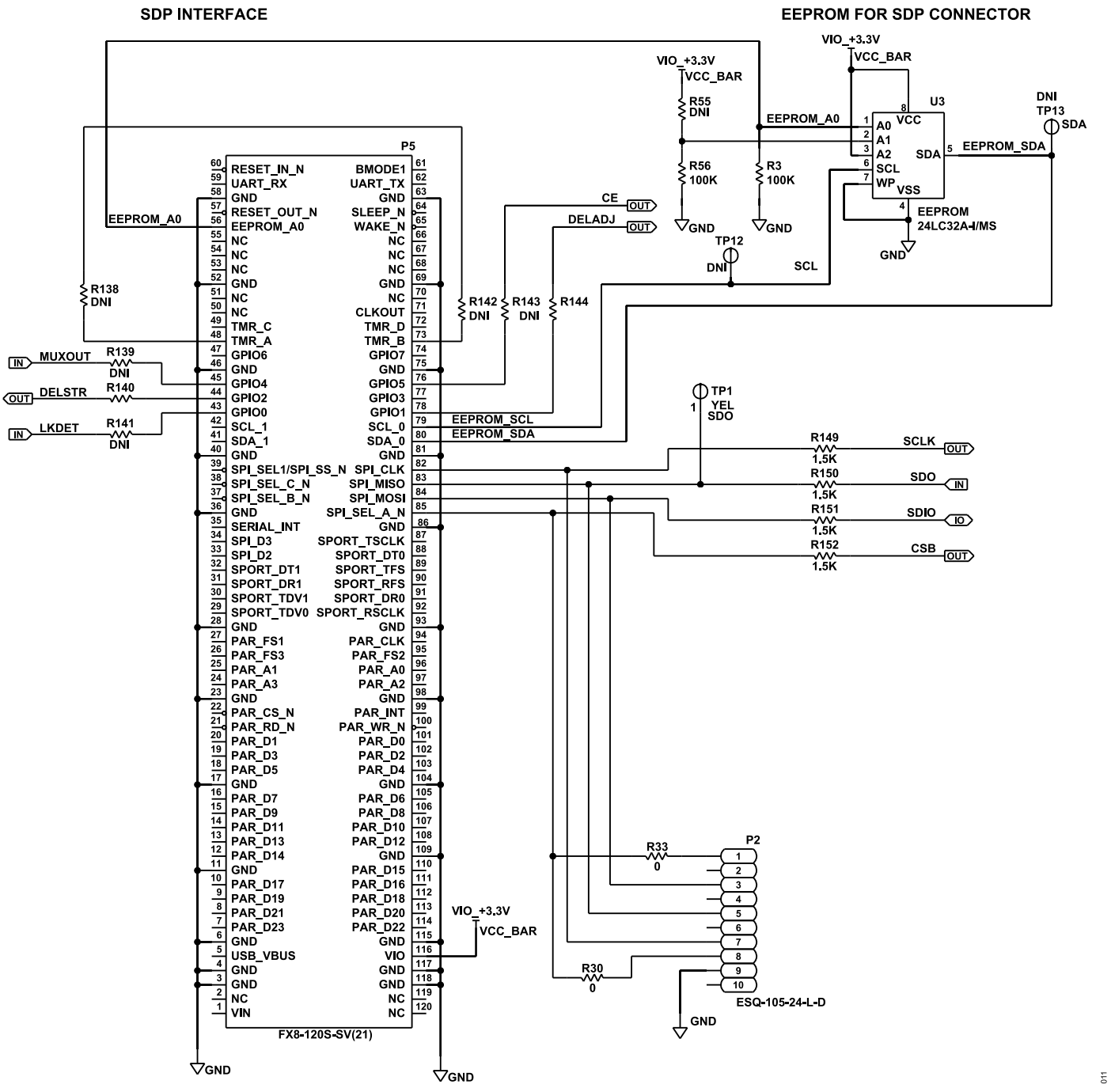

Figure 11. EV-ADF4383SD1Z Schematic, ADF4383 SDP Interface

EVALUATION BOARD SCHEMATIC AND ARTWORK

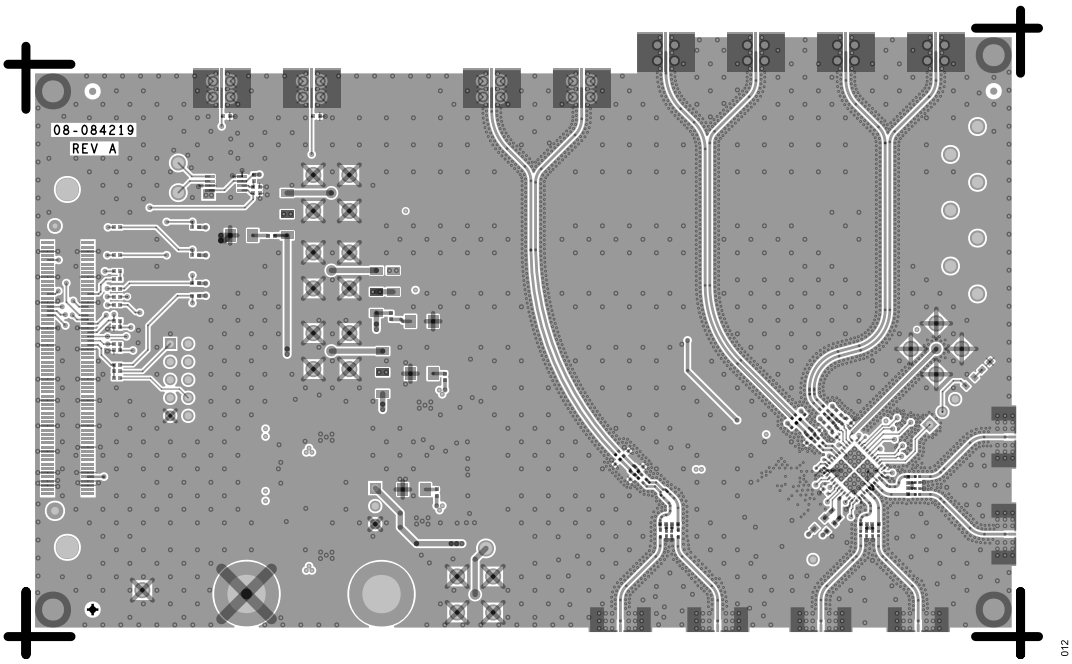

Figure 12. EV-ADF4383SD1Z Layer 1, Primary

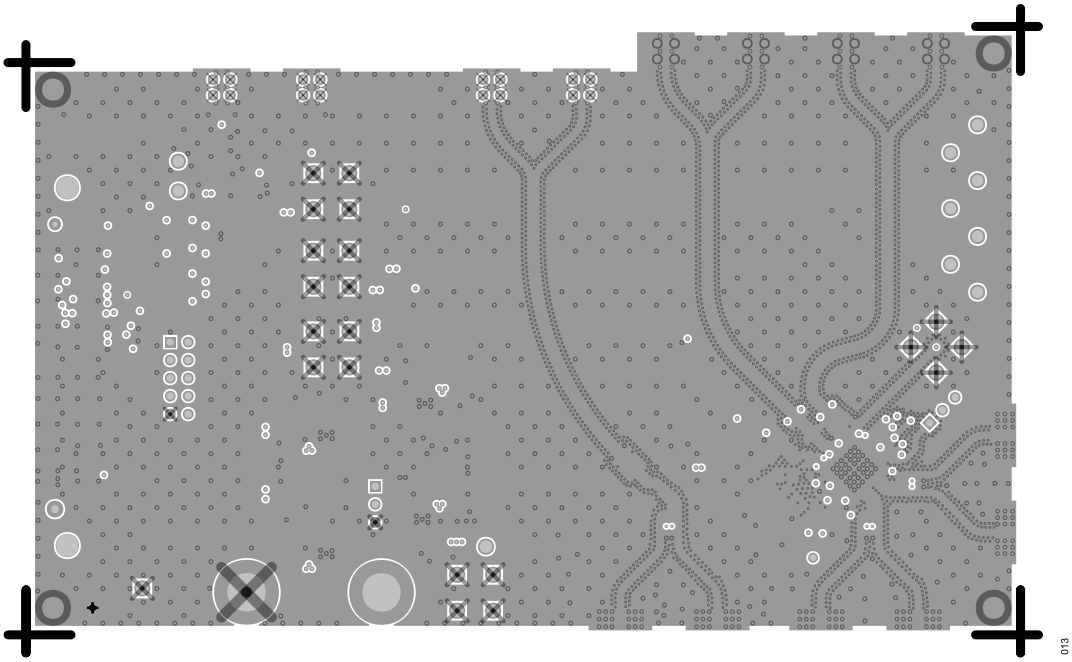

Figure 13. EV-ADF4383SD1Z Layer 2, Ground

EVALUATION BOARD SCHEMATIC AND ARTWORK

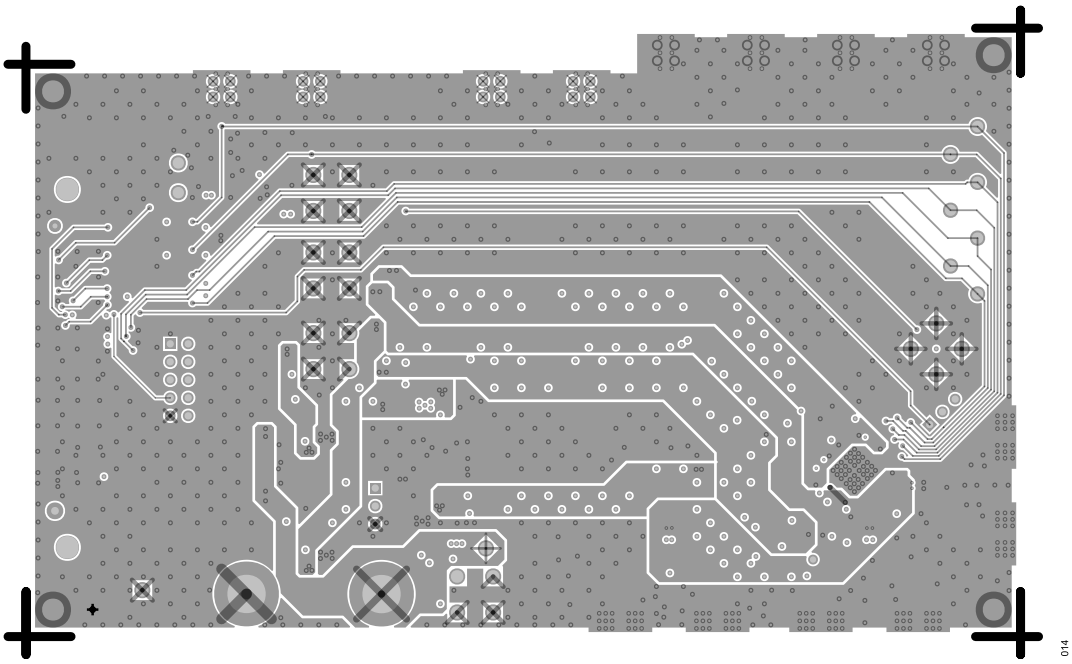

Figure 14. EV-ADF4383SD1Z Layer 3, Power

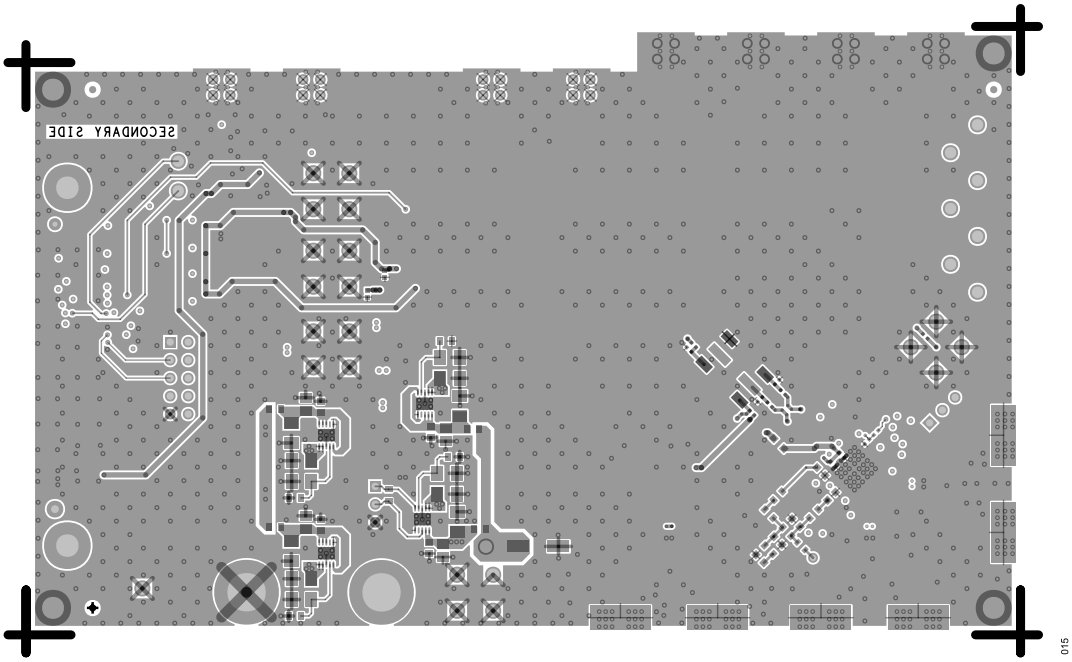

Figure 15. EV-ADF4383SD1Z Layer 4, Secondary

EVALUATION BOARD SCHEMATIC AND ARTWORK

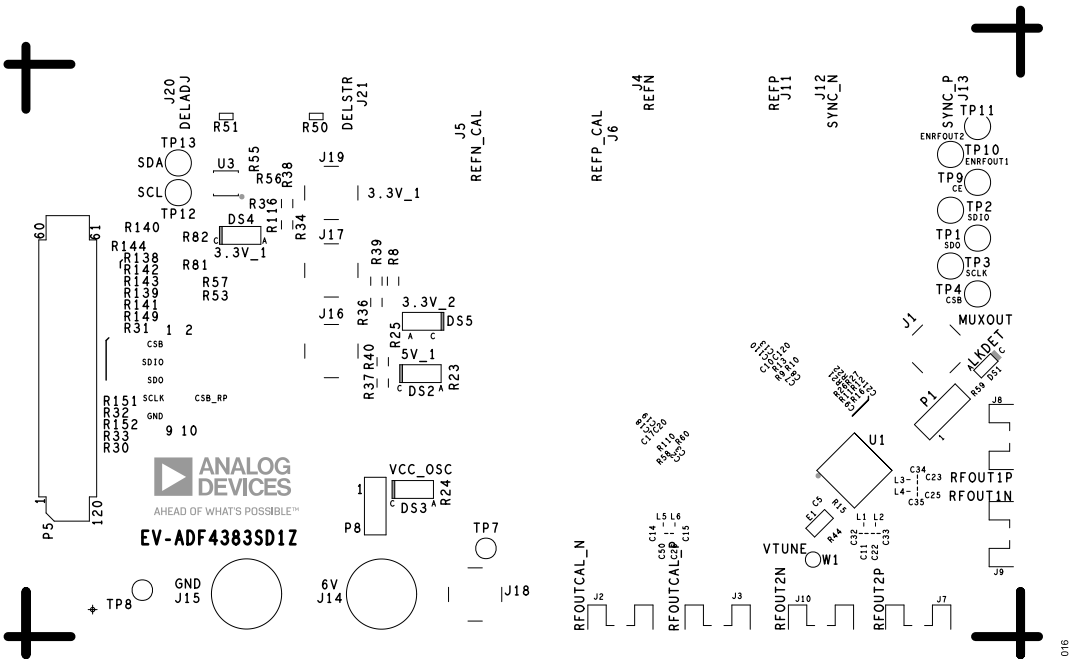

Figure 16. EV-ADF4383SD1Z Silkscreen, Top Side

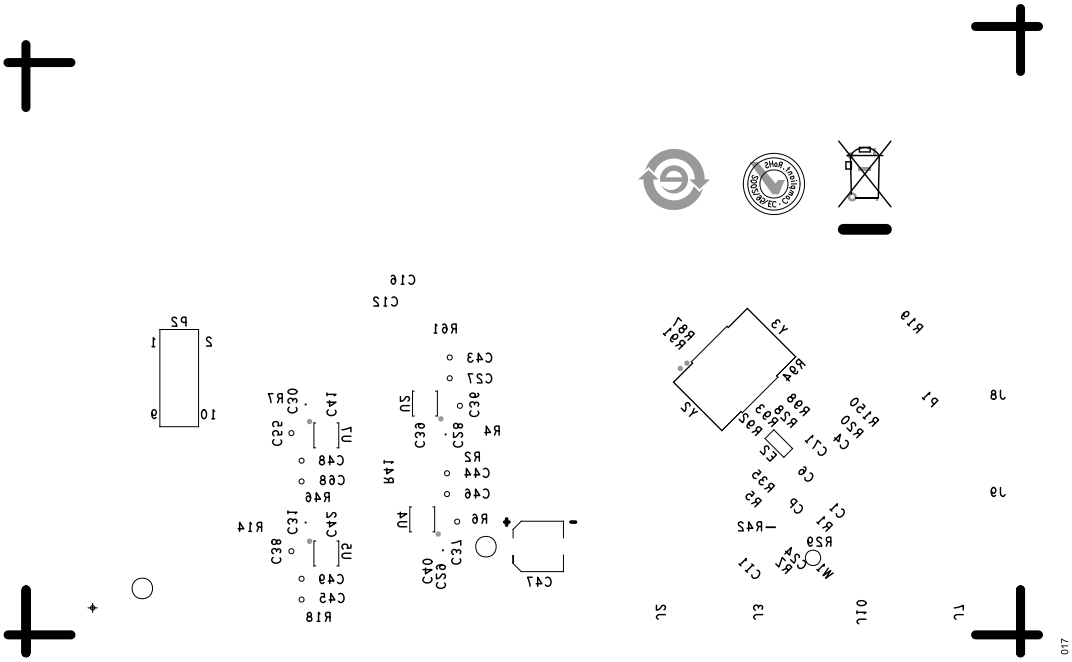

Figure 17. EV-ADF4383SD1Z Silkscreen, Bottom Side

ORDERING INFORMATION

ORDERING GUIDE

Table 4. Evaluation Boards

Model[1]	Description
EV-ADF4383SD1Z	Evaluation Board

[1] Z = RoHS-Compliant Part.

BILL OF MATERIALS

Table 5. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C1	Ceramic capacitor, 20 pF, 250 V, 2%, C0G, 0603, ultra-low equivalent series resistance (ESR)	Johanson Technology	251R14S200GV4T
C11, C22, C23, C25, C26, and C50	Ceramic capacitors, 10 pF, 25 V, 5%, C0G, 0201	Murata	GRM0335C1E100JA01D
C12	Ceramic capacitor, 4.7 µF, 4 V, 20%, X6S, 0402, low ESR	TDK	C1005X6S0G475M050BC
C2, C3, C7, C8, C18, and C19	Ceramic capacitors, 1 µF, 6.3 V, 10%, X7R, 0402	Murata	GRM155R70J105KA12D
C9, C14, C15, and C21	Ceramic capacitors, 0.1 µF, 16 V, 10%, X7R, 0402	KEMET	C0402C104K4RACTU
C27, C46, C48, and C49	Ceramic capacitors, 10 µF, 35 V, 10%, X7R, 1206	Taiyo Yuden	GMK316AB7106KL-TR
C32, C33, C34, and C35	Ceramic capacitor, 0.1 µF, 16 V, 10%, X5R, 0201	Kyocera AVX	531Z104KT16T
C36, C37, C38, C43, C44, C45, C55, and C68	Ceramic capacitor, 4.7 µF, 25 V, 10%, X7R, 1206	KEMET	C1206C475K3RACTU
C47	Aluminum electrolytic capacitor, 22 µF, 63 V, 20%, 6.3 mm × 7.7 mm, AEC-Q200	Sun Electronic Industries Corporation	63CE22BS
C6	Ceramic capacitor, 10 pF, 50 V, 0.5 pF, C0G, 0603, low ESR	TDK	C1608C0G1H100D080AA
C71	Ceramic capacitor, 1 µF, 16 V, 10%, 0402, low ESR	TDK	C1005X6S1C105K050BC
CI1	Ceramic capacitor, 10 nF, 16 V, 10%, X5R, 0603	AVX Corporation	0603YD103KAT2A
CP	Ceramic capacitor, 33 pF, 50 V, 5%, C0G, 0603	Yageo	CC0603JRNPO9BN330
DS1	Light emitting diode (LED), surface-mounted device (SMD), 0603, red, AEC-Q101	Vishay	TLMS1100-GS15
DS2, DS3, DS4, and DS5	LED, 565 nm, green, diffused, 1206, SMD	Lumex	SML-LX1206GW-TR
E1 and E2	Inductors, bead chip for power lines	Taiyo Yuden	FBMH1608HL601-T
J1, J16, J17, J18, and J19	Connector-printed circuit board (PCB), Subminature Version A (SMA), straight jacks, 50 Ω contact center, surface mount with thru hold legs	Amphenol RF	132134-15
J2, J3, J7, J8, J9, and J10	Connector-PCB, 2.92 mm edge-mounted jacks, DC 40 GHz	Gigalane	G02SFB009
J4, J5, J6, J11, J12, J13, J20, and J21	Connector-PCB, end launch, SMA, edge-mount, square	Emerson Network Power	142-0761-811
J14 and J15	Connector-PCB, banana jacks, female, noninsulated, THT, swage, 0.218 inches length	Keystone Electronics	575-4

ORDERING INFORMATION

Table 5. Bill of Materials (Continued)

Reference Designator	Description	Manufacturer	Part Number
L1, L2, L3, L4, L5, and L6	Inductors, RF, chip, unshielded, 1.4 nH ± 0.2 nH, 100 MHz, 1.1 A, 0.019 Ω DC resistance (DCR), AEC-Q200	Murata	LQW15AN1N4C1ZD
P1, P8	Connector-PCB, 3-position male headers, unshrouded, single row straight, 2.54 mm pitch, 5.84 mm post height, 5.08 mm solder tail	Samtec, Inc.	TSW-103-08-T-S
P2	Connector-PCB, 10-position female, header, elevated socket, dual row straight, 0.64 mm square post, 9.65 mm solder tail, 2.54 mm pitch	Samtec, Inc.	ESQ-105-24-L-D
P5	Connector-PCB, vertical type receptacle for the system demonstration platform (SDP) breakout board, for electromagnetic compatibility (EMC) test use, alt_symbols	HRS	FX8-120S-SV(21)
R1	Resistor, SMD, 931 Ω, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF9310V
R10 and R60	Resistors, SMD, 49.9 Ω, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF49R9X
R23, R24, R25, and R116	Resistors, SMD, 619 Ω, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF6190X
R4, R7, and R14	Resistors, SMD, 0.1 Ω, 1%, 1/3 W, 0603, AEC-Q200	Panasonic	ERJ-3BWFR100V
R140, R144, R149, R150, R151, and R152	Resistors, SMD, 1.5 kΩ, 1%, 1/16 W, 0402, AEC-Q200	Stackpole Electronics, Inc.	RMCF0402FT1K50
R5, R15, and R35	Resistors, SMD, 0 Ω, jumper, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3GEY0R00V
R16	Resistor, SMD, 100 Ω, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1000X
R18 and R46	Resistors, SMD, 33.2 kΩ, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF3322V
R2	Resistor, SMD, 51.1 kΩ, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF5112V
R20, R31, R32, R50, R51, R53, and R57	Resistors, SMD, 200 kΩ, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF2003X
R9, R21, R22, R30, R33, and R58	Resistors, SMD, 0 Ω, jumper, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2GE0R00X
R3 and R56	Resistors, SMD, 100 kΩ, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1003X
R34, R36, and R37	Resistors, SMD, 0 Ω, 5%, 1/4 W, 1026, AEC-Q200	Vishay	CRCW12060000Z0EA
R41 and R61	Resistors, SMD, 49.9 kΩ, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF4992V
R42	Resistor, SMD, 30 Ω, 0.5%, 1/16 W, 0603	Susumu Co, Ltd.	RR0816Q-300-D
R59	Resistor, SMD, 499 Ω, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF4990V
R6	Resistor, SMD, 1 Ω, 5%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3GEYJ1R0V
RZ	Resistor, SMD, 330 Ω, 5%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3GEYJ331V
TP1, TP2, TP3, TP4, TP9, TP10, and TP11	Connector-PCB, yellow test points	Components Corporation	TP-104-01-04

ORDERING INFORMATION

Table 5. Bill of Materials (Continued)

Reference Designator	Description	Manufacturer	Part Number
TP7 and TP8	Connector-PCB, solder terminal turrets for clip leads	Mill-Max	2308-2-00-80-00-00-07-0
U1	IC, Microwave wideband synthesizer with integration VCO	Analog Devices, Inc.	ADF4383BCCZ
U2, U5, and U7	IC, 20 V, 500 mA, ultra-low noise, ultra-high power supply rejection ratio (PSRR) linear regulator	Linear Technology	LT3045EDD#PBF
U3	IC, 32KBIT serial, electrically erasable programmable read-only memory (EEPROM)	Microchip Technology	24LC32A-I/MS
U4	IC, 20 V, 200 mA, ultra-low noise, ultra-high PSRR RF linear regulator	Analog Devices	LT3042EDD#PBF

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.