Evaluating the ADAR4002 0.5GHz to 19GHz, 1-Channel, Bidirectional True Time Delay Unit

FEATURES

- Standard single-ended 50Ω interfacing
- Supply voltage easily applied to test loops or headers
- SPI signals available on the P1 and P10 headers

EVALUATION KIT CONTENTS

- ADAR4002-EVALZ evaluation board

EQUIPMENT AND HARDWARE REQUIRED

- 20GHz VNA
- 2-channel power supply
- EVAL-SDP-CS1Z (SDP-S) controller board
- PC
- Digital multimeter (DMM) or voltmeter

SOFTWARE REQUIRED

- **Analysis | Control | Evaluation (ACE) Software**
- ADAR4002 ACE plug-in evaluation software

DOCUMENTS NEEDED

ADAR4002 data sheet

EVALUATION BOARD PHOTO

GENERAL DESCRIPTION

This user guide describes the ADAR4002-EVALZ evaluation board kit for the ADAR4002 0.5GHz to 19GHz, 1-channel bidirectional true time delay unit and variable attenuation device for phased array applications. The ADAR4002 features a digital stepped attenuator (DSA) block and a time delay unit (TDU) block. The TDU has two programmable time delay ranges. Range 0 offers a 508ps time delay range and 4ps step size, while Range 1 offers a 254ps time delay range and 2ps step size. See device block diagram in the ADAR4002 data sheet.

The ADAR4002-EVALZ allows the user to test all the functions and features offered by the ADAR4002 chip including variable gain, variable time delay, and both digital modes (serial peripheral interface (SPI) and shift register). RF signal traces are a 50Ω coplanar waveguide design and are connected to the RF1 port and RF2 port of the device, which provides simple interfacing with test equipment or other printed circuit boards (PCBs). The EVAL-SDP-CS1Z (SDP-S) controller board programs the SPI port or shift register using the ADAR4002 ACE plug-in.

A full description and complete specifications for the ADAR4002 are provided in the data sheet and should be consulted in conjunction with this user guide when using the ADAR4002-EVALZ evaluation board.

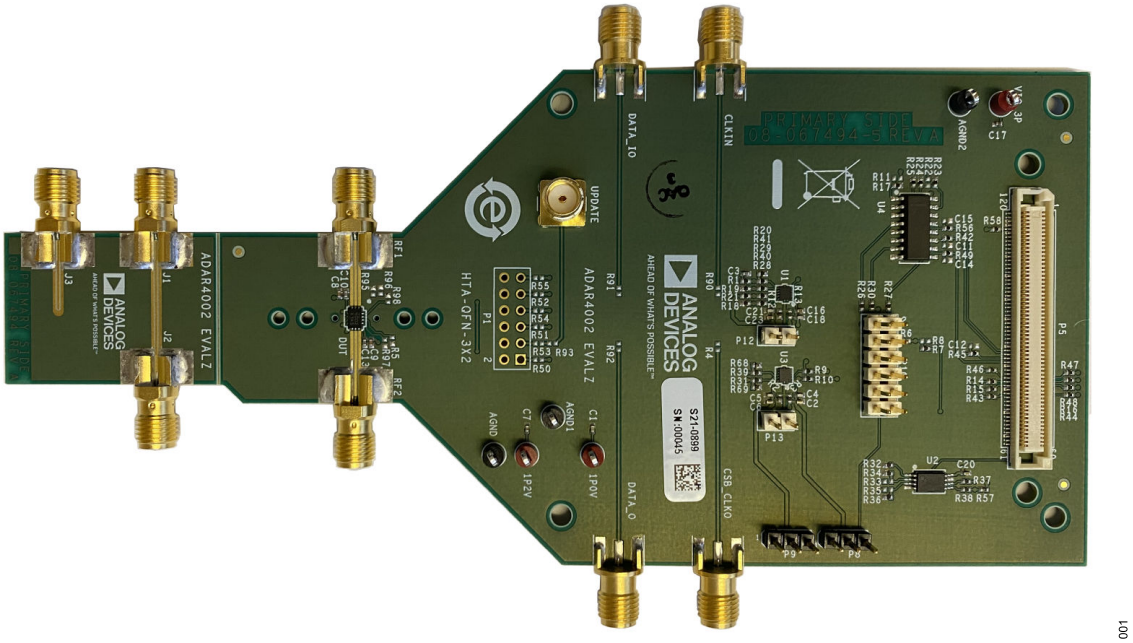

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Figure 1. ADAR4002-EVALZ Evaluation Board

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REVISION HISTORY

8/2025—Revision 0: Initial Version

EVALUATION BOARD LAYOUT

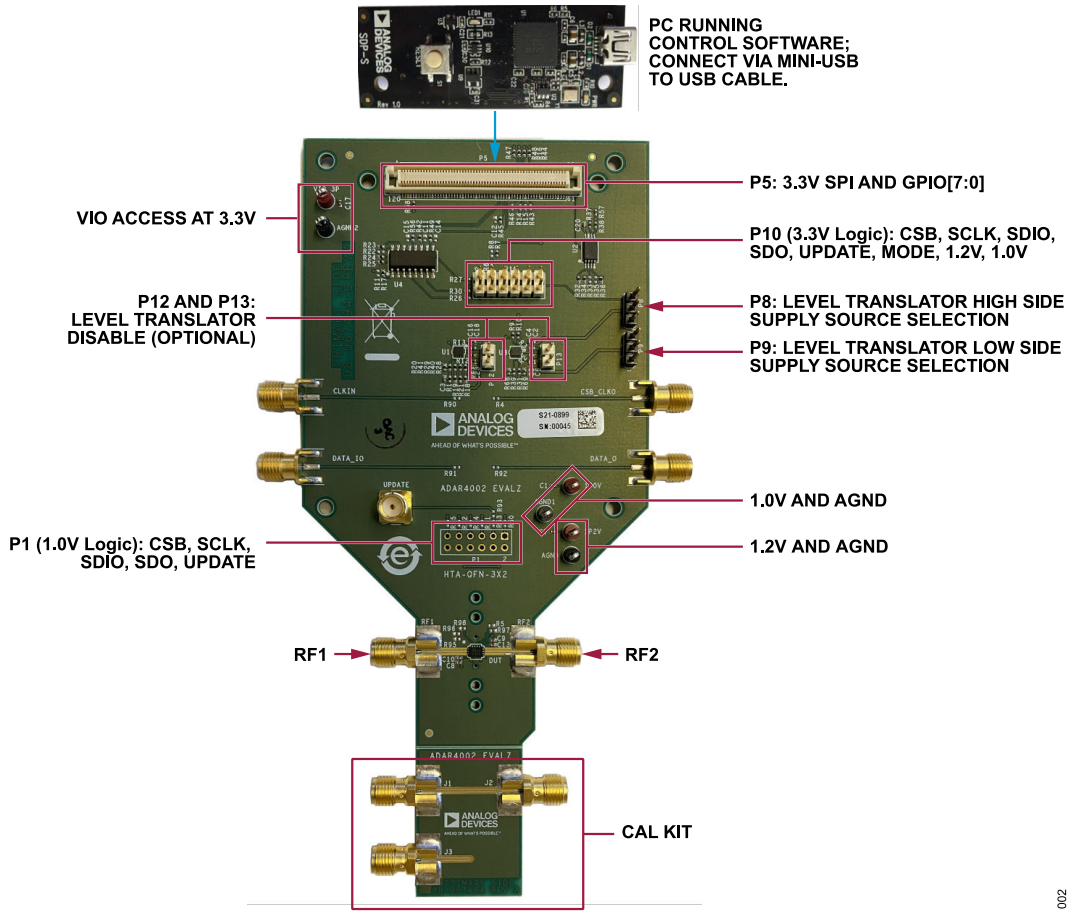

Figure 2. Layout of the ADAR4002-EVALZ Evaluation Board and the SDP-S Controller Board (Commonly Used Headers and Test Loops Highlighted)

EVALUATION BOARD HARDWARE

Figure 3 shows a typical ADAR4002-EVALZ board test setup for RF measurements using a network analyzer. Note that any loss in the test setup must be calibrated out for accurate insertion loss measurements of the ADAR4002 device.

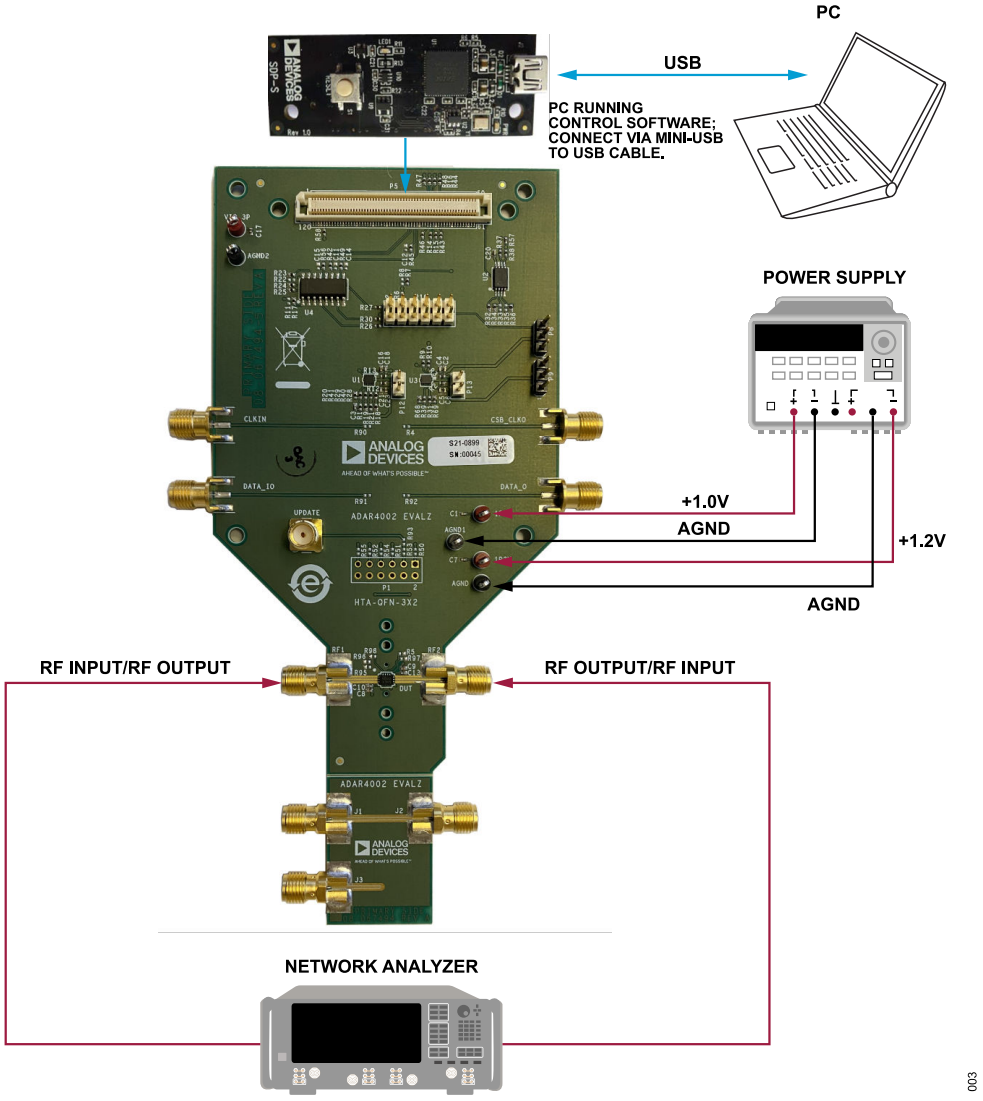

Figure 3. Typical ADAR4002-EVALZ Board Test Setup

EVALUATION BOARD HARDWARE

SETTING UP THE EVALUATION BOARD

Setting up the ADAR4002-EVALZ evaluation board includes the following steps:

1. Connect a vector network analyzer (VNA) to RF1 and RF2.
2. Connect a 1.2V power supply capable of 2mA between the red 1P2V test loop and AGND test loop.
3. Connect a 1.0V power supply capable of 2mA between the red 1P0V test loop and AGND test loop.
4. Ensure that the ADAR4002-EVALZ has solid connections at all Subminiature Version A (SMA) connectors and test point locations before using the ADAR4002-EVALZ.

POWER SUPPLY CONNECTIONS AND NOMINAL CURRENT

The ADAR4002-EVALZ has an analog voltage supply (1.2V) and a digital voltage supply (1.0V). Both voltage supplies use a common analog ground (AGND).

The analog 1.2V supply is connected to the following:

- The red 1P2V test loop
- Pin 11 of the P10 header

AGND is connected to the following:

- The black AGND test loops
- Pin 2, Pin 4, Pin 6, Pin 8, Pin 10, and Pin 12 of the P1 header
- Pin 8, Pin 10, and Pin 12 of the P10 header

The digital 1.0V supply is connected to the following:

- The red 1P0V test loop
- Pin 9 of the P10 header

If the ADAR4002-EVALZ is connected and working properly, upon power-up and after a soft reset, the evaluation board draws approximately the following:

- 0.25mA for the 1.2V analog supply voltage
- 0.55mA for the 1.0V digital supply voltage

RF INPUTS AND OUTPUTS

The ADAR4002-EVALZ is bidirectional with a single-ended configuration for simple evaluation and testing with 50Ω test equipment. The RF connectors are RF1 and RF2 on the evaluation board.

PROGRAMMING THE SPI PORT

To program the SPI port of the ADAR4002 while using the ADAR4002-EVALZ evaluation board, connect an SDP-S controller board to the 120-pin P5 connector, then connect the SDP-S board to a PC via a USB cable that is running the **ACE Software** ADAR4002 plug-in. For exact programming and power-up sequencing requirements, see the Evaluation Board Software Quick Start Procedures section.

The **ACE Software** ADAR4002 plug-in controls every function on the device, including the digital stepped attenuator, variable time delay unit, digital modes, and sequencing through the DSA and TDU states with update commands.

SPI PIN ACCESS

Users can access the four SPI pins (DATA_IO, DATA_0, CLKIN, and CSB/CLKO) and the traces associated with each pin with the P1 and P10 headers. The P1 header provides access to the 1.0V logic signals after they have gone through the level translators, while P10 offers access to the 3.3V logic signals before the level translators. The user can either monitor the signals from these headers or use their own microcontroller to drive the SPI signals from these headers. For more information, see the Driving the ADAR4002-EVALZ with an External Controller section.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

The following procedures detail how to power-up the evaluation board and begin using the **ACE Software** ADAR4002 plug-in. The ADAR4002 plug-in can be installed with the **ACE Plug-in Manager**.

1. Connect SDP-S controller board to the ADAR4002-EVALZ evaluation board via the P5 connector. Do not connect to the SDP-S to the PC yet.
2. Connect a supply cable from the red 1P2V test loop to a black AGND test loop. Set Channel 1 of the power supply to 1.2V. Do not turn on the power supply at this point.
3. Connect Channel 2 of the power supply to the red 1P0V and a AGND black test loop and set Channel 2 to 1.0V. Still keep the power supply turned off.
4. Connect the VNA to the RF1 and RF2 SMA connectors. Ensure that the VNA RF power is set to at least 15dB less than the minimum ADAR4002 input P1dB, or about −10dBm.
5. Turn on the power supply.
6. Plug the USB miniconnector of the USB cable (provided with the SDP-S controller board) into the SDP-S controller board and the USB connector into the PC.
7. Launch the **ACE Software**. If the PC is connected to the SDP-S via the USB cable and the SDP-S is connected to the ADAR4002-EVALZ board, the **ADAR4002 Board** plug-in will be shown in the **Attached Hardware** area of the **ACE Software** window. See Figure 6. Double click the **ADAR4002 Board** plug-in.
8. The **ADAR4002 Board** tab opens, with the **ADAR4002** chip plug-in icon, shown in Figure 7. Double click the **ADAR4002** chip icon to open the **ADAR4002 Chip Plugin (Main GUI)** (see Figure 8).
9. Click **Soft Reset** to initialize the chip to its default settings.
10. On the main GUI, the user can set all the **DSA** and **Time Delay Unit** values of the variable attenuation and phase (VAP) block. Note upon power up, the VAP is set to the maximum attenuation and minimum time delay, as seen in Figure 8. After changing any value, click **Load Single DSA/TDU State** to write the new values over the SPI onto VAP.

Typical gain and return loss performance are shown in Figure 4 and Figure 5, respectively.

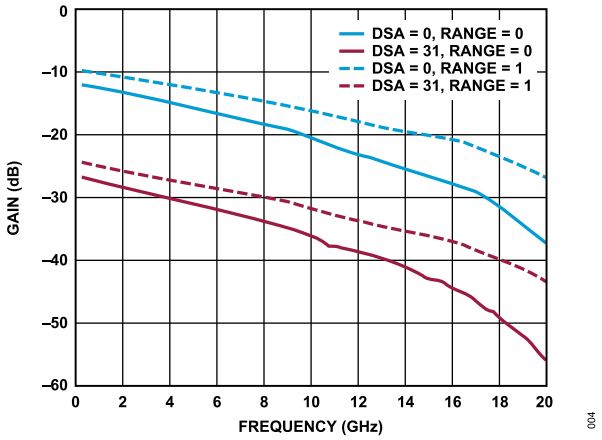

Figure 4. ADAR4002 Typical Gain vs. Frequency over DSA Code 0 and DSA Code 31, and Time Delay Range = 0 and Time Delay Range = 1

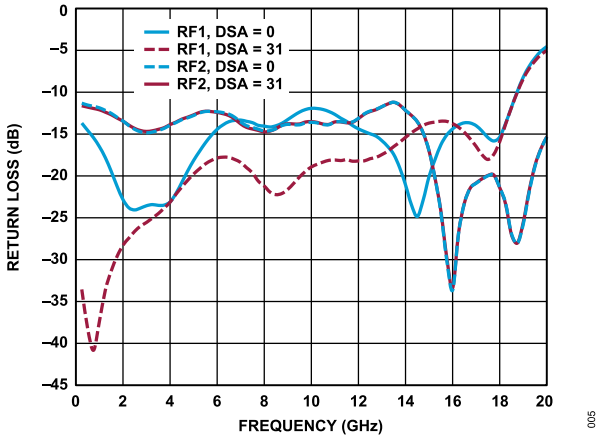

Figure 5. ADAR4002 Return Loss vs. Frequency for RF1 and RF2 and DSA Code 0 and DSA Code 31

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

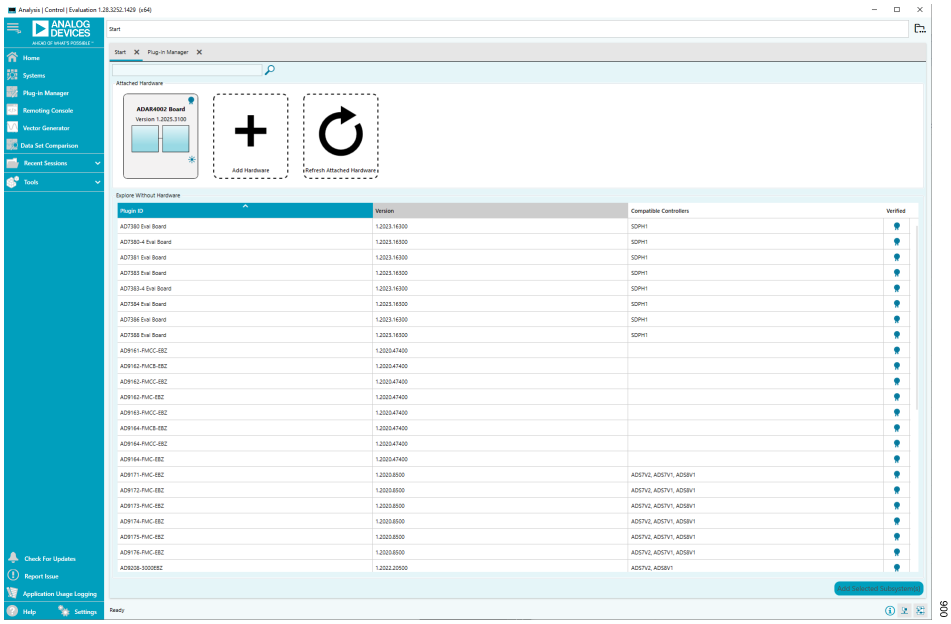

Figure 6. ACE Upon Startup If ADAR4002 Evaluation Is Connected

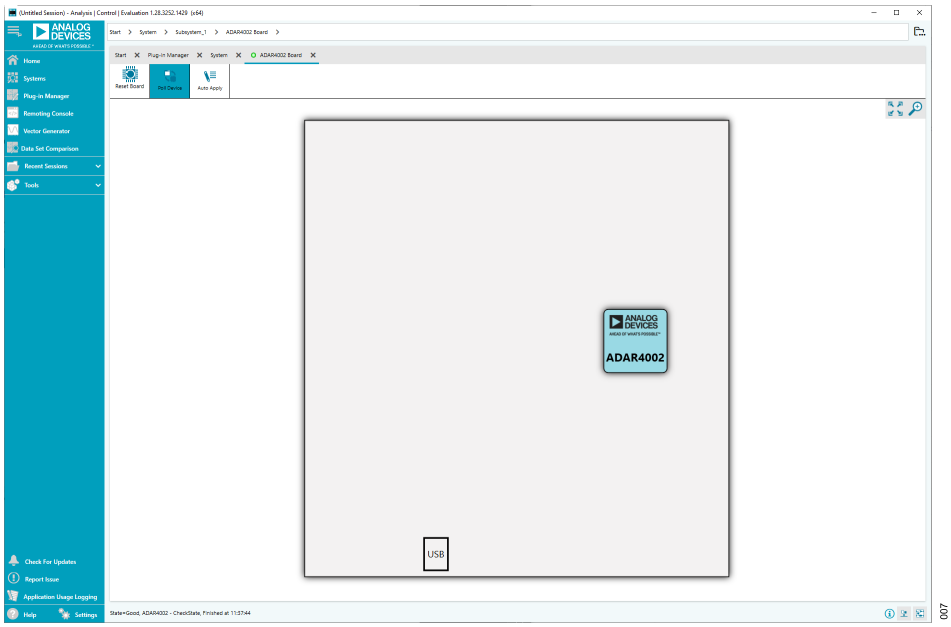

Figure 7. Click on the ADAR4002 Chip Plugin to Launch the Main GUI

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

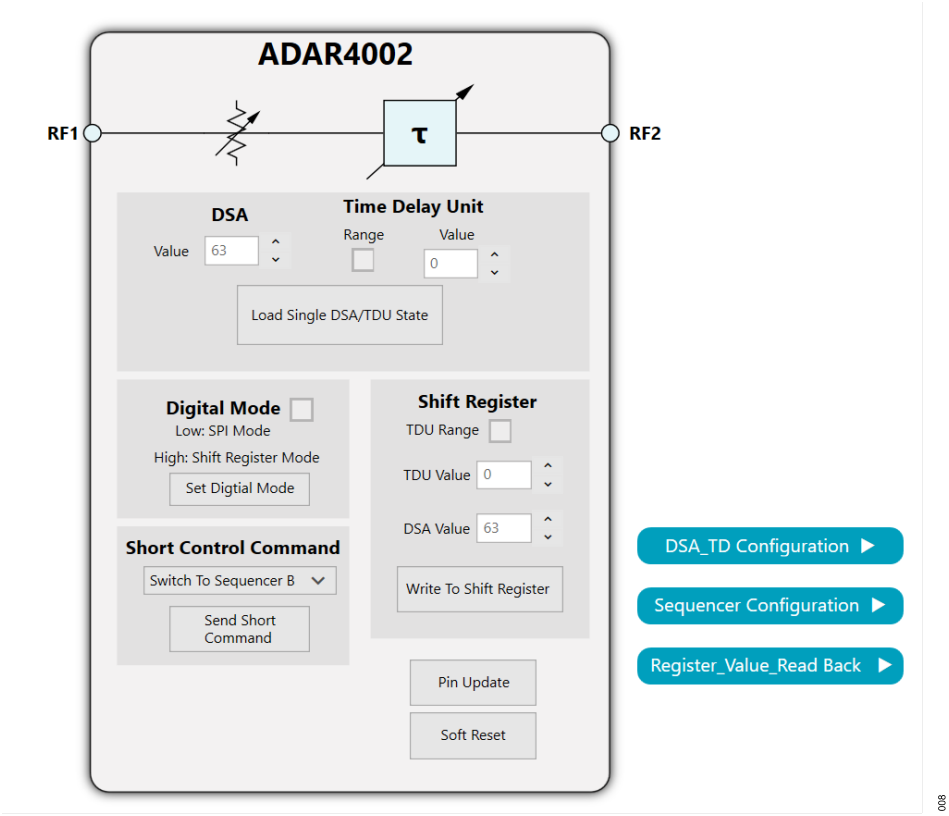

Figure 8. ADAR4002 Chip Plugin (Main GUI)

ADAR4002 PLUGIN OVERVIEW

MAIN GUI

The main GUI shown in Figure 8 controls the following ADAR4002 functions:

- **Soft Reset**.
  - Initializes the device to its default settings.
  - Sets attenuation at maximum and time delay at minimum.
- **Digital Mode**.
  - Sets the device in SPI mode or shift register mode.
  - Sets time delay and attenuation through either digital mode.
- The **Time Delay Unit** has two delay ranges:
  - Range 0: **Time Delay Unit Range** box unchecked selects the 508ps range and 4ps step size.
  - Range 1: **Time Delay Unit Range** box checked selects the 254ps range and 2ps step size.
- **DSA** programmable range **Value** in decimal from 0 (minimum attenuation) to 63 (maximum attenuation).
- **Short Control Command**.
  - **Switch to Sequencer B**: sources DSA and TDU data using Sequencer B.
  - **Switch to Sequencer A**: sources DSA and TDU data using Sequencer A.
  - **Reset Sequencer A**: resets sequencer to start position.
  - **Reset Sequencer B**: resets sequencer to start position.
  - **Toggle direction of Sequencer A**: ascends or descends through the DSA and TDU states.
  - **Toggle direction of Sequencer B**: ascends or descends through the DSA and TDU states.
  - **Data Load Command**: load DSA and TDU register data from first rank to second rank registers.
  - **Update Command**: advances the sequencer.
- Update command (**Pin Update**) with the ADAR4002 UPDATE pin.

The main GUI also has the following three subviews as shown in Figure 8 that open when clicked and give access to control of the various other functions of the chip.

- **DSA_TD Configuration** (seen in Figure 10).
  - Sets the 32 time delay (**TD**) and attenuation (**Attn**) states in the registers.
- **Register_Value_Read Back** (seen in Figure 11).
  - Reads back time delay **TD** and attenuation (**Attn**) on second rank registers.
  - Reads back current VAP data (**Read TD_DSA_VAP**).
- **Sequencer Configuration** (seen in Figure 12.)
  - **Sequencer_Reset** allows the user to select the sequencer (A or B) by using the check boxes.
  - **Sequencer Selection**: **uncheck: descend** and **check: ascend**.
  - **Sequencer Pointer Start** and **Stop**.

SUBVIEW ACCESS

To access the three subviews click their buttons, as shown in Figure 9. Each subview opens in a new tab and can be closed when the user is finished.

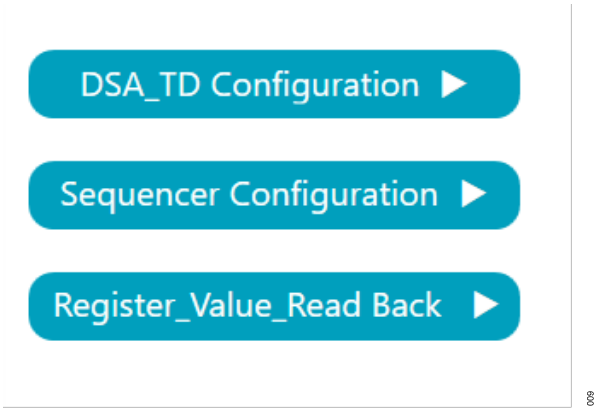

Figure 9. Subview Accessed via the Three Buttons Shown

ADAR4002 PLUGIN OVERVIEW

CONFIGURE ATTENUATION AND TIME DELAY DATA

Click **DSA_TD Configuration** in the main GUI to open the subview that controls the first rank registers shown in Figure 10. There are two sets of 32 decimal data input boxes, one set for attenuation (**Attn**) control and one set for time delay (**Time Delay**) control. One pair of data input boxes is for each DSA and TDU state. Click **Load_Update** at the bottom of this subview after setting up to 32 DSA and TDU states to write the data into the first rank registers, to load the data from the first rank registers to the second rank registers, and to perform an update command.

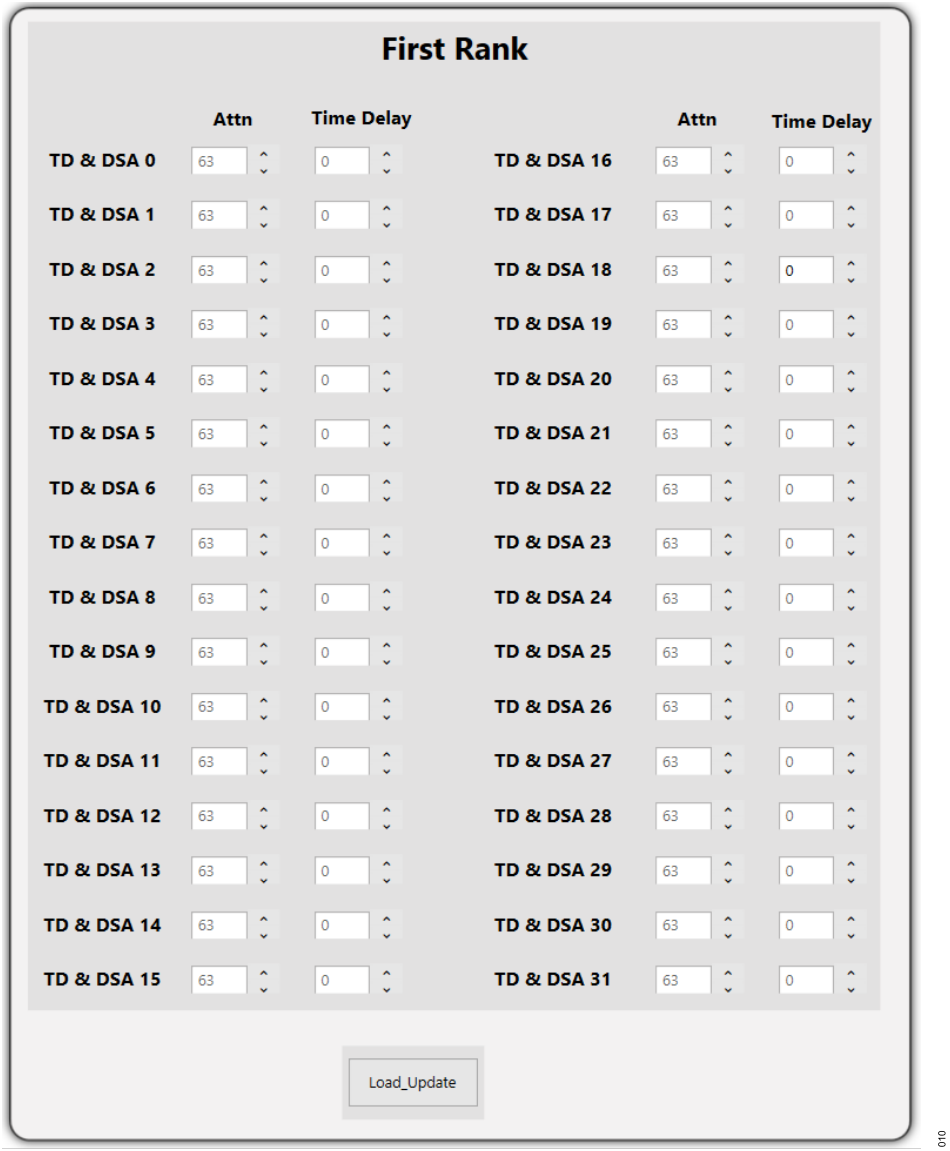

Figure 10. Setting the DSA and TDU States

ADAR4002 PLUGIN OVERVIEW

READ BACK REGISTER VALUES

Click **Register_Value_Read Back** in the main GUI to open the **Read Back TD & DSA on Second Rank** subview. Data that is loaded from the first rank registers to the second rank registers by issuing a load command can be read back in this subview. The two sets of 32 decimal data boxes, one set each for the attenuation and time delay data, display the read back second rank register data.

One pair of data boxes for each DSA and TDU state. In the bottom left **Read Back on VAP** area of this subview, there are data boxes to show the current **Time Delay Code** and **DSA Code** on the VAP. Click **Read TD_DSA_VAP** for the data of the second rank registers and current VAP data to be read back and shown in the decimal data boxes.

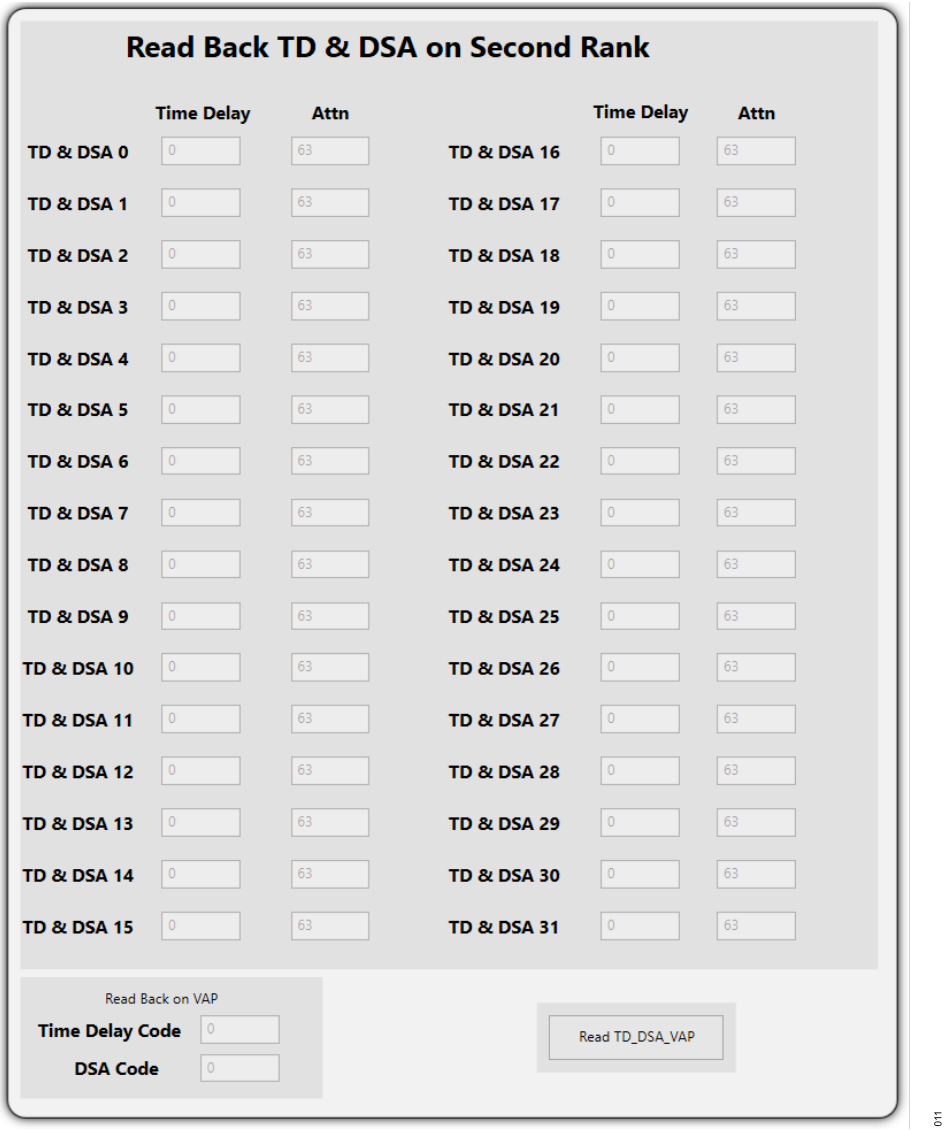

Figure 11. Read Back the DSA and TDU Data

ADAR4002 PLUGIN OVERVIEW

SEQUENCER CONFIGURATION

Click **Sequencer Configuration** in the main GUI to open the **Sequencer Configuration** subview shown in Figure 12. This subview allows a user to reset Sequencer A and Sequencer B (**Sequencer_Reset**), select Sequencer A or Sequencer B as the active sequencer (**Sequencer Selection**), set the active sequencer direction (**ascend** or **descend**), and set the **Start** and **Stop** for each **Sequencer Pointer**. To apply the sequencer settings, click **Write Start/Stop Values**. Click **Update Sequencer** to advance the active sequencer to the next TDU and DSA state in the register memory.

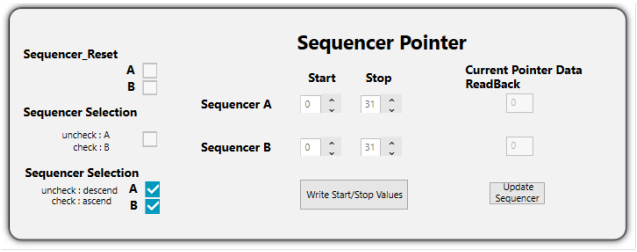

Figure 12. Sequencer Configuration Subview

The following is an example that details how to configure and operate Sequencer A, and Figure 13 also shows Step 1, Step 2, and Step 3 of this example:

1. Configure TDU and DSA values for TDU and DSA State 0 through TDU and DSA State 7 in the **DSA_TD Configuration** subview:
   - State 0: TDU code = 0 and DSA code = 0
   - State 1: TDU code = 0 and DSA code = 11
   - State 2: TDU code = 0 and DSA code = 21
   - State 3: TDU code = 0 and DSA code = 31
   - State 4: TDU code = 0 and DSA code = 41
   - State 5: TDU code = 0 and DSA code = 51
   - State 6: TDU code = 0 and DSA code = 61
   - State 7: TDU code = 0 and DSA code = 63

   Then, click **Load_Update** in the **DSA_TD Configuration** subview to write the data into the first rank registers, to load the data from the first rank to the second rank registers, and to perform an update command.
2. Read back the data from the second rank registers by clicking **Read TD_DSA_VAP** in the **Register_Value_Read Back** subview. The attenuation and time delay data that was set in Step 1 displays in the readout boxes if the data was written and loaded correctly.
3. Set up and update the sequencer by doing the following in the **Sequencer Configuration** subview:
   - Check the **Sequencer_Reset** box for **A**.
   - Uncheck the **Sequencer Selection** box to select **A** as the active sequencer.
   - Check the **Sequencer Selection** (**check: ascend**) box to ascend through the states in the register memory.
   - Set **Sequencer A Start** pointer to 0
   - Set **Sequencer A Stop** pointer to 7.
   - Click **Write Start/Stop Values** to program the sequencer settings.
   - Click **Update Sequencer** to load State 0 onto the VAP. Click **Update Sequencer** again to advance to State 1 and click a third time to advance to State 2. Continuing to click **Update Sequencer** to sequence through the remaining states.

The output signal power changes from state to state due to the different attenuation settings of each state. When **Update Sequencer** is clicked while at State 7, the sequencer advances back to the **Start** pointer value, which is 0.

ADAR4002 PLUGIN OVERVIEW

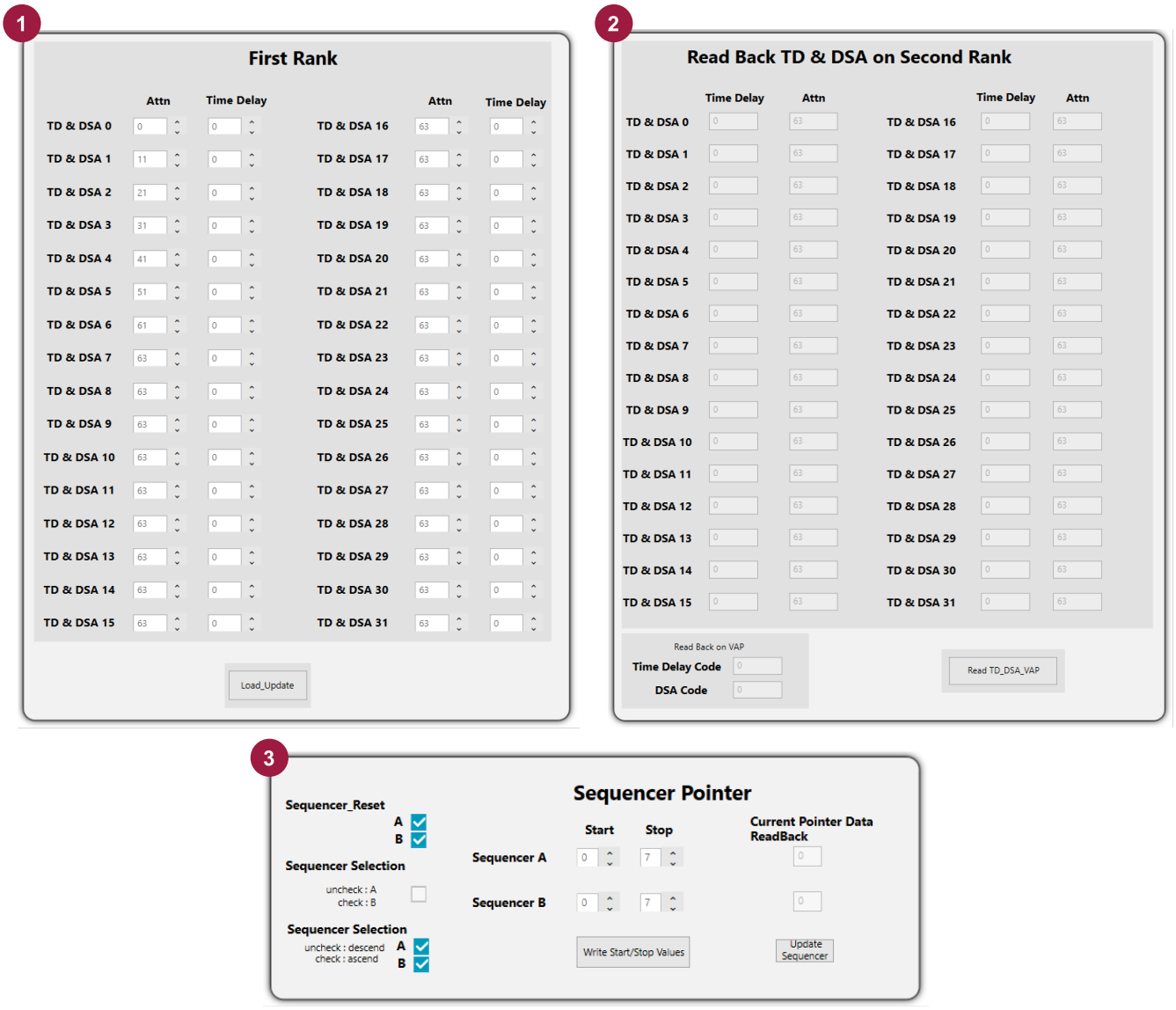

Figure 13. Example of Configuring and Operating Sequencer A

DRIVING THE ADAR4002-EVALZ WITH AN EXTERNAL CONTROLLER

It is possible to drive the ADAR4002-EVALZ evaluation board with a different microcontroller other than the SDP-S or with a digital pattern generator. Information and instructions are given on how to drive the following access points:

- Via P10
- Via P1
- SMA connectors

DRIVING VIA P10

The P10 header is placed between the U4 mux and the U1 level translator. If the user only wants to control the SPI port and use 3.3V logic, use this header. The user can also power the ADAR4002 on this header as well with the 1.2V and 1.0V connections. Pin 8, Pin 10, and Pin 12 are connected to ground. The remaining pin connections are:

- Pin 1: SCLK_LS_IN
- Pin 2: MOSI_LS_IN
- Pin 3: CSB_LS_IN
- Pin 4: MISO_LS_IN
- Pin 9: 1.0V
- Pin 11: 1.2V

If using P10, the user must do the following:

- Drive 3.3V on the red VIO_3P test loop, which is required to power the U1 and U3 level translators. Note that, when connected, the SDP-S provides this voltage.
- Disable the outputs of the mux (U4) by removing R23 and adding 10kΩ on R22.
- Disable U3 by shorting Pin 1 and Pin 2 together on P13.

DRIVING VIA P1

The P1 header is placed between the level translators (U1 and U3) and the ADAR4002. If the user wants to control the SPI pins, MODE pin, and UPDATE pin and to use 1.0V logic, use this header. Pin 2, Pin 4, Pin 6, Pin 8, Pin 10, and Pin 12 are connected to ground. The remaining pin connections are the following:

- Pin 1: MODE
- Pin 3: UPDATE
- Pin 5: SDO
- Pin 7: CSB
- Pin 9: SDI
- Pin 11: SCLK

If using P1, the user must do the following:

- Drive 3.3V on the red VIO_3P test loop, which is required to power the U1 and U3 level translators. Note that, when connected, the SDP-S provides this voltage.
- Populate with a 0Ω resistor R50, R51, R52, R53, R54, and R55.
- Disable U1 by shorting Pin 1 and Pin 2 together on P12.
- Disable U3 by shorting Pin 1 and Pin 2 together on P13.

DRIVING VIA THE SMA CONNECTORS

The SMA connectors are provided for all the SPI pins and the UPDATE pin. From the SMA connectors to the ADAR4002, there-are 50Ω transmission lines. To use all the SMA connectors, the following components must be populated and depopulated:

- Populate with a 0Ω resistor: R4, R90, R91, R92, and R93.
- Depopulate R28, R29, R31, R39, R40, and R41.
- Populate with a 50Ω resistor (optional, to terminate lines) R5, R95, R96, R97, and R98.

The 50Ω terminations can be increased if the microcontroller or pattern generator cannot source the required current and/or if reflections from the impedance mismatch can be tolerated, assuming the SMA connectors are driven with a 50Ω source.

CALIBRATION BOARD

The ADAR4002 evaluation kit comes with a calibration board that is fabricated with the main evaluation board and can be broken off the main board after assembly with a V-score (see Figure 14). The calibration board contains a through line that mimics the length of the combined RF1 + RF2 lines (J1 to J2) and one open line that mimics the RF1 line or RF2 line (J3).

This calibration board can be used to remove the insertion loss and phase shift of the evaluation board traces and connectors.

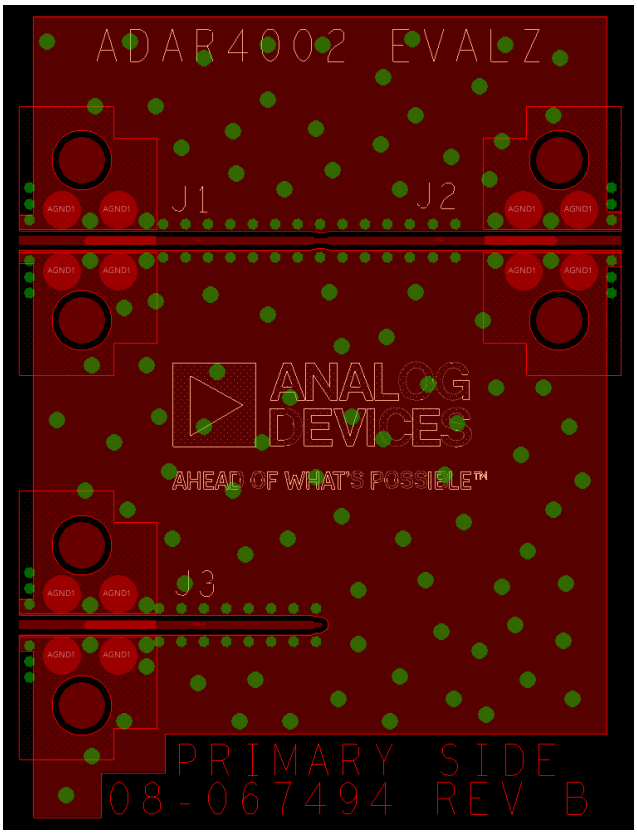

Figure 14. ADAR4002 Calibration Board

EVALUATION BOARD SCHEMATICS AND ARTWORK

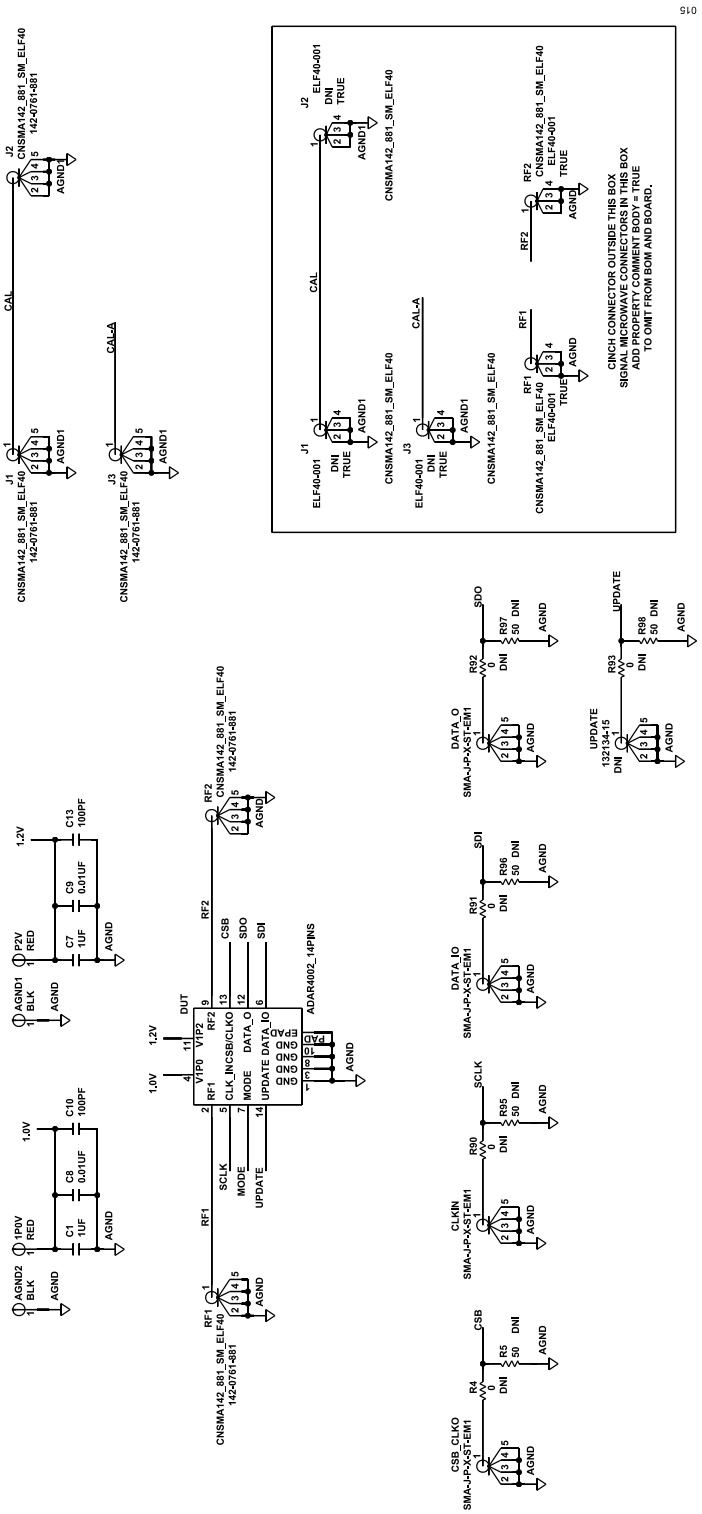

Figure 15. ADAR4002-EVALZ Main Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

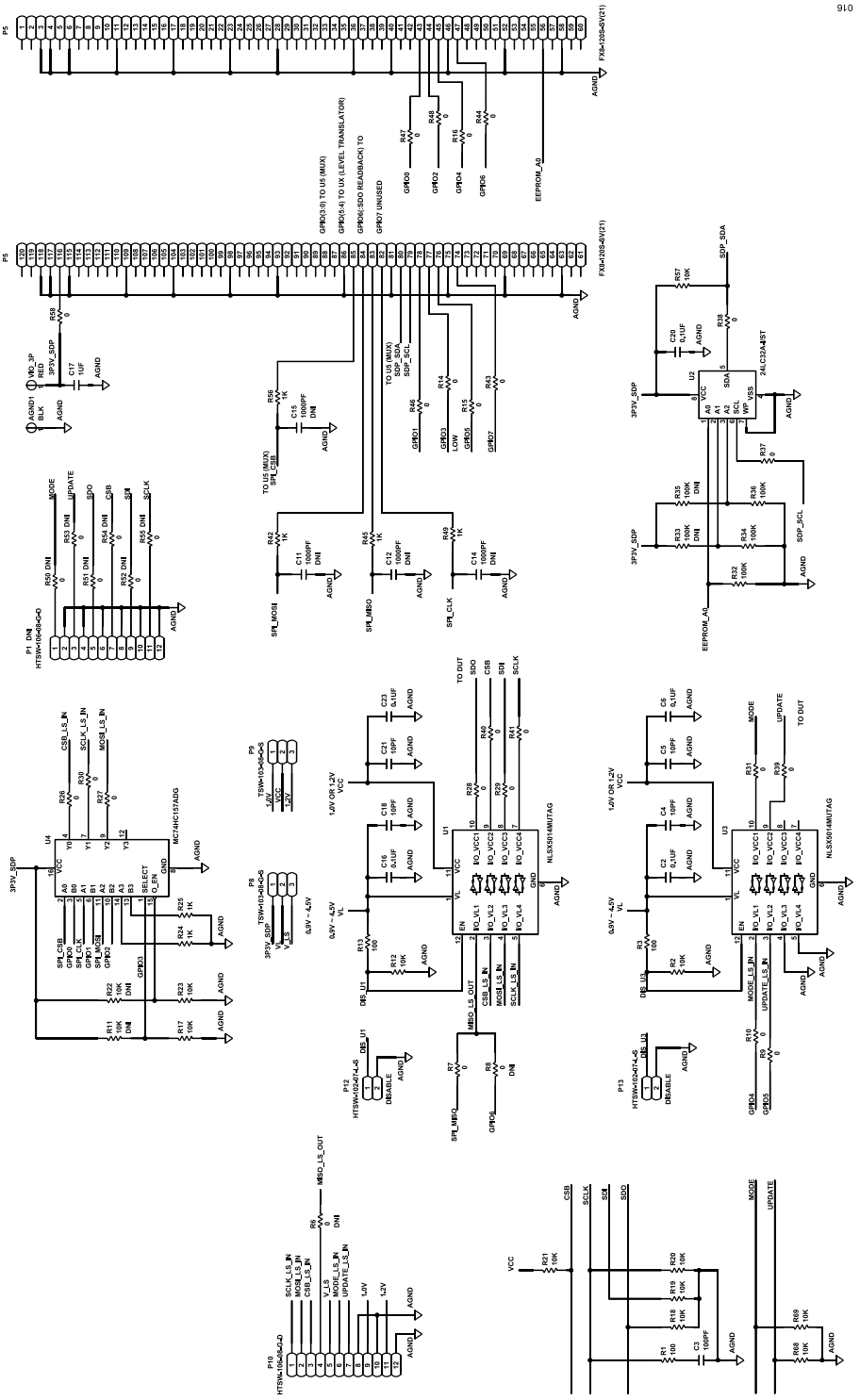

Figure 16. ADAR4002-EVALZ Schematic of Components Required for Use with SDP-S Controller Board

EVALUATION BOARD SCHEMATICS AND ARTWORK

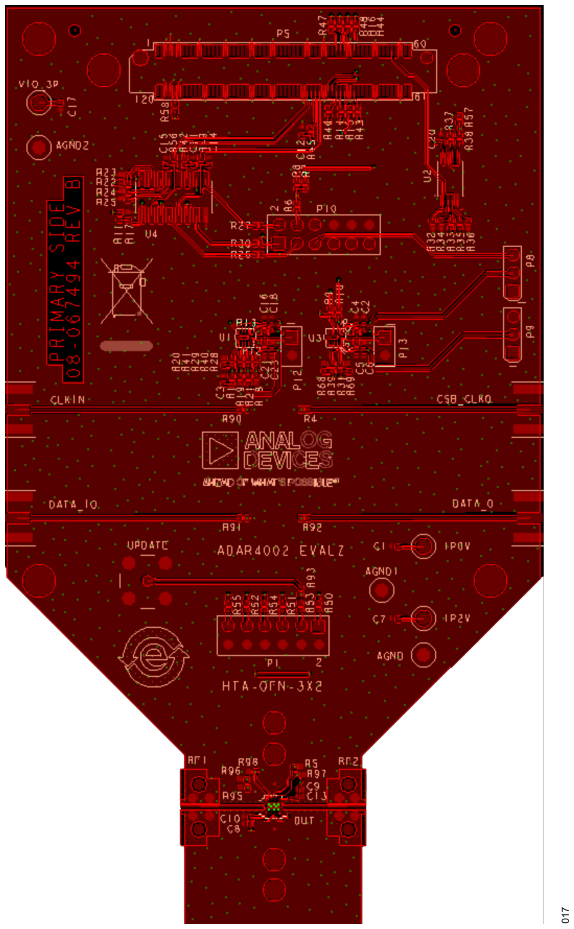

Figure 17. ADAR4002-EVALZ Silkscreen, Top View

EVALUATION BOARD SCHEMATICS AND ARTWORK

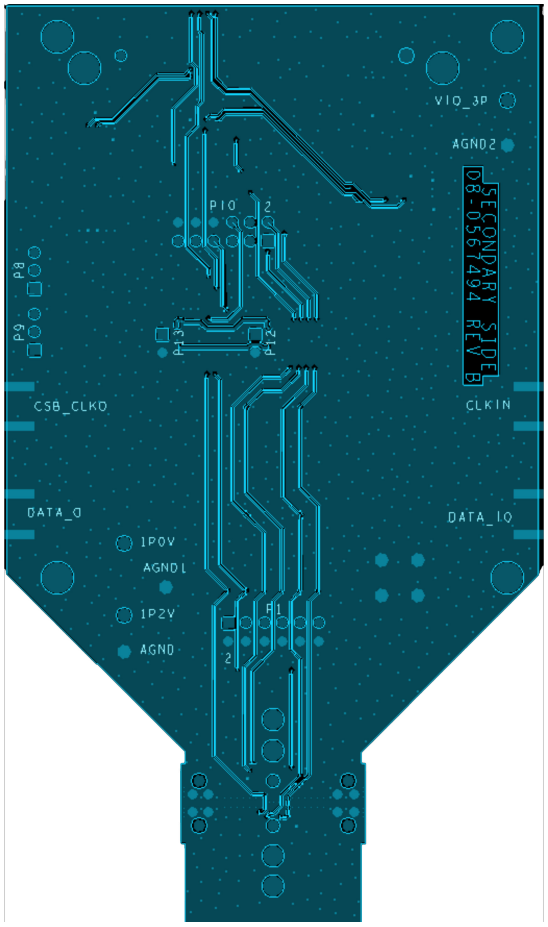

Figure 18. ADAR4002-EVALZ Silkscreen, Bottom View

ORDERING INFORMATION

EVALUATION BOARDS

Table 1. Evaluation Boards

Model[1]	Description
ADAR4002-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

BILL OF MATERIALS

Table 2. ADAR4002-EVALZ Evaluation Board Bill of Materials (Installed)

Reference Designator	Description	Part Number	Manufacturer
1P0V, 1P2V, VIO_3P	Connector, PCB, test points, red	TP-104-01-02	Components Corporation
AGND, AGND1, and AGND2	Connector, PCB, test points, black	TP-104-01-00	Components Corporation
C1, C7, and C17	Ceramic capacitors, 1µF, 6.3V, 10%, X5R, 0402	04026D105KAT2A	AVX
C3, C10, and C13	Ceramic capacitors, 100pF, 50V, 5%, C0G, 0402	C1005NP01H101J050BA	TDK
C2, C6, C16, C20, and C23	Ceramic capacitors, 0.1µF, 16V, 10%, X7R, 0402, AEC-Q200	GCM155R71C104KA55D	Murata
C4, C5, C18, and C21	Ceramic capacitors, 10pF, 50V, 5%, C0G, 0402	CC0402JRNPO9BN100	Yageo
C8 and C9	Ceramic capacitors, 0.01µF, 25V, 10%, X8R, 0402	C1005X8R1E103K	TDK
CLKIN, CSB_CLKO, DATA_IO, and DATA_O	Connectors, PCB, SMA, straight edge mount	SMA-J-P-X-ST-EM1	Samtec
DUT	IC, 0.5GHz to 19GHz 1-channel, bidirectional true time delay unit	ADAR4002	Analog Devices, Inc.
J1, J2, J3, RF1, and RF2	Connectors, PCB, end, launch, SMA edge mount, 50Ω, 0GHz to 26.5GHz, for tight GND holes use ALT_SYMBOLS	142-0761-881	Cinch
P10	Connector, PCB, header, straight, male	HTSW-106-08-G-D	Samtec
P12 and P13	Connector, PCB, two position, unshrouded, 0.635mm square post header, 5.84mm post height, 2.54mm solder tail, 2.54mm pitch	HTSW-102-07-L-S	Samtec
P5	Connector, PCB, board to board receptacle, straight, 0.60mm pitch	FX8-120S-SV(21)	Hirose Electric
P8 and P9	Connector, PCB, BERG header straight male, 3 position	TSW-103-08-G-S	Samtec
R1, R3, and R13	Resistor, surface-mounted device (SMD), 100Ω, 5%, 1/10W, 0402, AEC-Q200	ERJ-2GEJ101X	Panasonic
R7, R9, R10, R14, R15, R16, R26, R27, R28, R29, R30, R31, R37, R38, R39, R40, R41, R43, R44, R46, R47, R48, and R58	Resistors, SMD, 0Ω, jumper, 1/10W, 0402, AEC-Q200	ERJ-2GE0R00X	Panasonic
R2, R12, R17, R18, R19, R20, R21, R23, R57, R68, and R69	Resistors, SMD, 10kΩ, 1%, 1/10W, 0402, AEC-Q200	ERJ-2RKF1002X	Panasonic
R24, R25, R42, R45, R49, and R56	Resistors, SMD, 1kΩ, 5%, 1/16W, 0402	RC0402JR-071KL	Yageo
R32, R34, and R36	Resistors, SMD, 100kΩ, 1%, 1/10W, 0402 AEC-Q200	ERJ-2RKF1003X	Panasonic
U1 and U3	IC, 4-bit, 100MBPS, configurable, dual-supply, level translators	NLSX5014MUTAG	On Semiconductor
U2	IC, 32KBIT, serial, electrically erasable programmable read-only memory (EEPROM)	24LC32A-I/ST	Microchip Technology
U4	IC, transistor-transistor logic (TTL), quad, 2-input data selector/mutliplexer	MC74HC157ADG	On Semiconductor
UPDATE	Connector, PCB, SMA, straight jack, 50Ω, contact center surface mount with thru hole legs	132134-15	Amphenol RF

ORDERING INFORMATION

Table 3. ADAR4002-EVALZ Evaluation Board Bill of Materials (Not Installed)

Reference Designator	Description	Part Number	Manufacturer
C11, C12, C14, and C15	Not recommended for new designs (NRND): ceramic capacitors, 1000pF, 50V, 10%, X7R, 0402	GRM155R71H102KA01D	Murata
P1	Connector, PCB, header straight male	HTSW-106-08-G-D	Samtec
R11 and R22	Resistors, SMD, 10kΩ, 1%, 1/10W, 0402, AEC-Q200	ERJ-2RKF1002X	Panasonic
R33 and R35	Resistors, SMD, 100kΩ, 1%, 1/10W, 0402, AEC-Q200	ERJ-2RKF1003X	Panasonic
R4, R90, R91, R92, and R93	Resistors, SMD, 0Ω, jumper, 1/5W, 0402, AEC-Q200	CRCW04020000Z0EDHP	Vishay
R5, R95, R96, R97, and R98	Resistors, SMD, 50Ω, 1%, 1/20W, 0402, high frequency	FC0402E50R0FST1	Vishay
R6, R8, R50, R51, R52, R53, R54, and R55	Resistors, SMD, 0Ω, jumper, 1/10W, 0402, AEC-Q200	ERJ-2GE0R00X	Panasonic