Evaluating the ADAQ7769-1 High Input Impedance, Programmable Gain, Anti-Alias, 24-Bit, 1MSPS, µModule DAQ Solution

FEATURES

- Fully featured evaluation board for the ADAQ7769-1
- On-board IEPE sensor interface
- On-board reference and power supply circuits
- PC software for control and data analysis of time and frequency domain
- FMC-LPC system board connector ZedBoard™-compatible
- Optional PMOD connector

EVALUATION KIT CONTENTS

- EV-ADAQ7769-1FMC1Z evaluation board
- Micro-SD memory card (with adapter) containing system board boot software and Linux OS

EQUIPMENT NEEDED

- Digilent ZedBoard™ with 12V wall adapter power supply
- DC and AC signal source (Audio Precision® or similar high performance signal source)
- PC running Windows® 7 or later, with USB 2.0 port

SOFTWARE NEEDED

- Analysis | Control | Evaluation (ACE) Software
- ADAQ7769-1 ACE plugin

EVALUATION BOARD PHOTOGRAPH

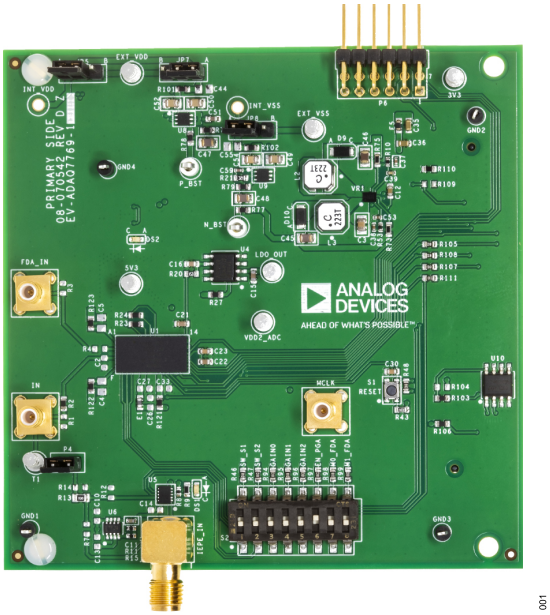

Figure 1. Evaluation Board Photograph

GENERAL DESCRIPTION

The EV-ADAQ7769-1FMC1Z evaluation kit enables simple evaluation of the ADAQ7769-1, a high input impedance, programmable gain, anti-alias, 24-bit, 1MSPS, µModule® data acquisition (DAQ) solution. The EV-ADAQ7769-1FMC1Z is used alongside a downloadable evaluation software to fully configure the features of the ADAQ7769-1 and display the conversion results in the time and frequency domains.

The EV-ADAQ7769-1FMC1Z connects to the USB port of a PC via the Digilent ZedBoard™. By default, the 3.3V rail is supplied by the ZedBoard™ and regulated by the on-board power solution to +20V, −16V, and +5.3V to power the ADAQ7769-1 and its support components. An integrated electronic piezoelectric (IEPE)-interface is included to support the evaluation of the ADAQ7769-1 using an IEPE sensor.

For a full description of the ADAQ7769-1, see the ADAQ7769-1 data sheet, which must be consulted in conjunction with this user guide when using the EV-ADAQ7769-1FMC1Z evaluation board. For the current schematic, layouts, and bill of materials, see the EVAL-ADAQ7769-1 product page.

TABLE OF CONTENTS

REVISION HISTORY

6/2025—Revision 0: Initial Version

EVALUATION BOARD SOFTWARE

EVALUATION SOFTWARE

The ACE software is a desktop software application that allows the evaluation and control of multiple evaluation systems across the Analog Devices, Inc., product portfolio. ACE provides a plug and play evaluation experience, enabling users to get up and running quickly with the product evaluation board. ACE can configure the embedded software on supported controller boards and provides a quick and easy way to get setup, configure the board and perform data capture, and analysis and/or waveform generation.

The controller board supported by ACE with this product evaluation board is the ZedBoard™.

For ACE installation and documentation instructions, see www.analog.com/ace. Follow the instructions to install the necessary evaluation board plugin support.

- If the machine that ACE is installed on has internet access, find/install/update plugins directly from the ACE application.
- For environments without internet access, download these plugins from www.analog.com/ace to portable storage and install them into ACE.

Note that the product specific documentation for the evaluation software can be found within the ACE plugin.

EMBEDDED SOFTWARE

The embedded software used for evaluation is typically built using open-source firmware examples, drivers, and hardware description language (HDL), where available, and can be found in the Software section on the product page.

Evaluation boards using Linux-based controllers come with an SD card in the box. The SD card provides a version of Analog Devices Kuiper Linux for evaluation that can boot the controller board. The ACE evaluation board plugin provides product specific configuration data and files.

If there is an issue or update available for this SD card, the image can be found in the Software section on the relevant evaluation board page.

HOST PC SOFTWARE

The embedded firmware and Linux stacks are based on the industrial I/O (IIO) architecture. This enables tools such as Python, through the pyadi-iio package, or MATLAB, with the precision toolbox, on a host PC to communicate with the evaluation and controller boards. Where available, links can be found in the Software section on the product page.

There are generic, not product specific, IIO tools, such as IIO oscilloscope, scopy, and IIO command line tools that provide basic, low-level functionality and work with any IIO platform.

QUICK START GUIDE

To begin using the EV-ADAQ7769-1FMC1Z, take the following steps:

1. For getting started with the ACE evaluation software, refer to the ACE Software Support section.
2. Ensure the ZedBoard™ boot configuration jumpers are set to use the Micro-SD card as shown in Figure 2. To avoid potential issues, ensure that the Zedboard™ VADJ SELECT = 2.5V, as shown in Figure 3.

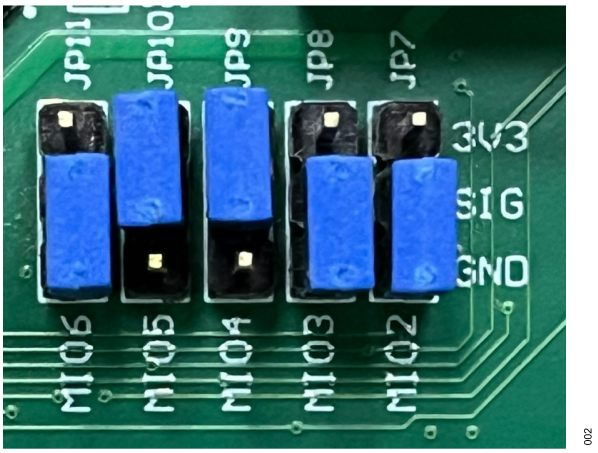

Figure 2. ZedBoard™ Boot Configuration Jumpers

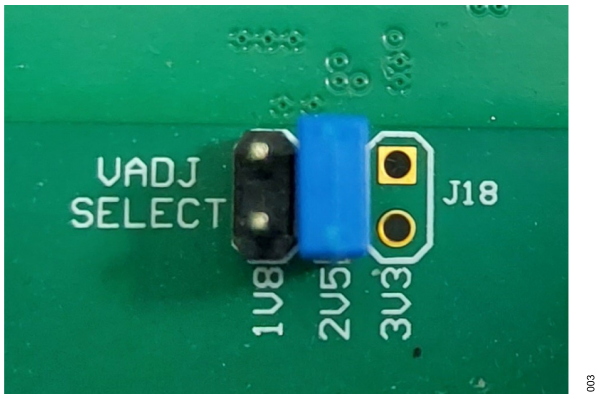

Figure 3. ZedBoard™ VADJ Link Setting

3. Connect the EV-ADAQ7769-1FMC1Z to the FMC connector on the ZedBoard™.
4. Connect the USB cable from the computer to the J13/USB OTG port of the ZedBoard™, and connect the 12V power supply to the J20/DC input of the ZedBoard™, as shown in Figure 7.
5. Slide the SW8/POWER switch in the ZedBoard™ to the on position. The green LD13/POWER light emitting diode (LED) turns on and is followed by the blue LD12/DONE LED (within the ZedBoard™). The DS2 LED in the EV-ADAQ7769-1FMC1Z also turns on, indicating board power up.
6. The LED blinks, LD0 and LD1, approximately 20 to 30 seconds later, indicating that the boot process is complete.
7. Launch the **ACE Software**. The EV-ADAQ7769-1FMC1Z appears in the **ACE Start** in the **Attached Hardware** view, as shown in Figure 4.

   If the EV-ADAQ7769-1FMC1Z does not appear on the **Attached Hardware** view, the plugin can still be launched from the **Explore Without Hardware** menu. Click **Proceed To Documentation** to open the plugin documentation for troubleshooting help as well as descriptions of each window and features within the plugin.

QUICK START GUIDE

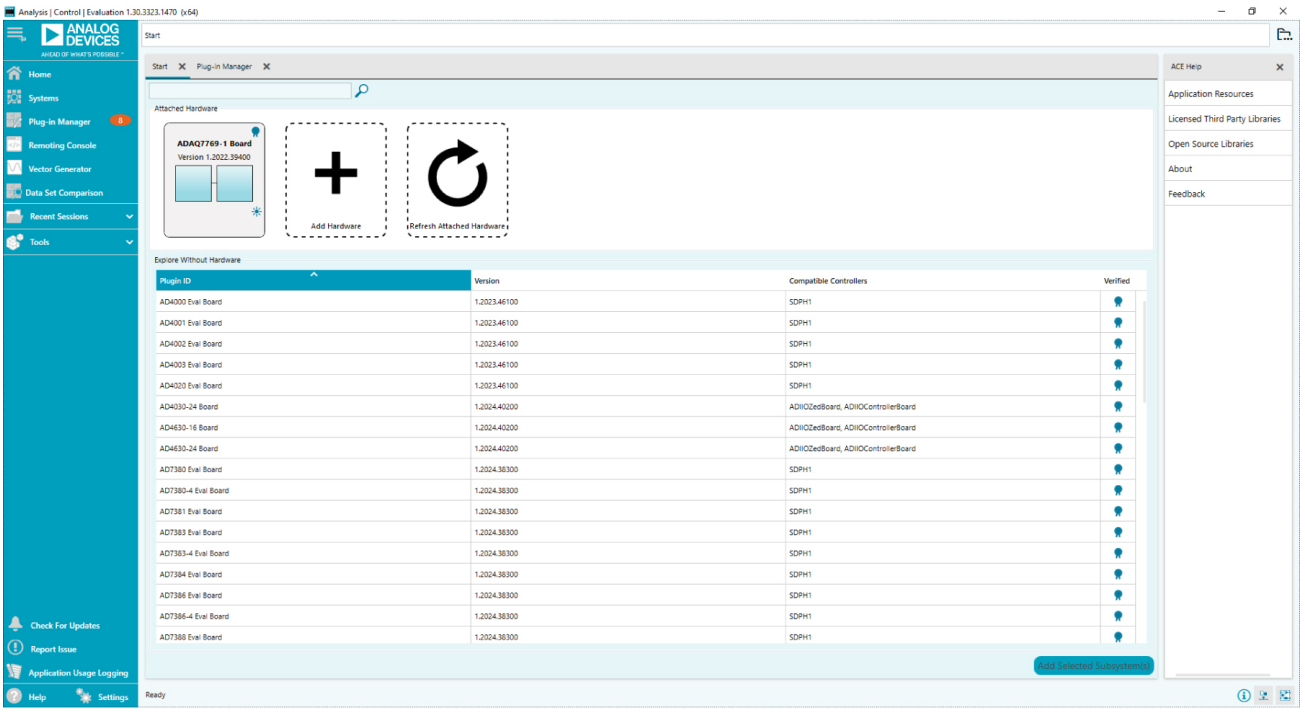

Figure 4. Attached Hardware View

EVALUATION BOARD HARDWARE

Figure 5 shows the simplified block diagram of the EV-ADAQ7769-1FMC1Z evaluation board connected to the Zed-Board™. The EV-ADAQ7769-1FMC1Z is installed with the featured ADAQ7769-1 µModule® (U1), the ADR444 4.096V reference (U4), and the on-board power solution consisting of the ADP5076 (VR1), ADP7142 (U8), ADP7182 (U9), and LTC3526LB-2 (U7). The on-board IEPE interface with 4mA current source, LT3092 (U6), can be used to bias the IEPE sensor used as an input to the µModule®.

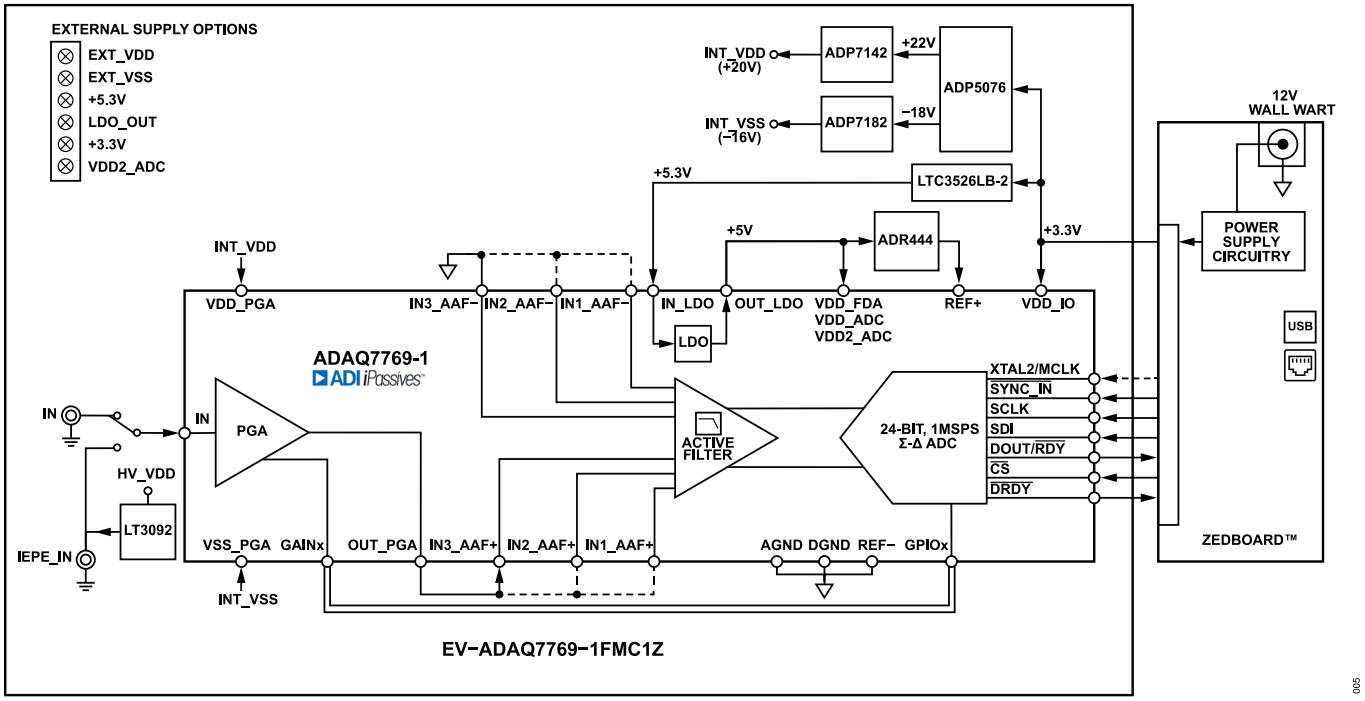

Figure 5. Simplified Evaluation Board Block Diagram

EVALUATION BOARD HARDWARE

ANALOG INPUTS

The analog input, IN, is accessible either through the Subminiature Version B (SMB) connectors, or the turret (T1). A Subminiature Version A (SMA) connector is also provided to connect to an IEPE sensor, which receives its current bias from the on-board IEPE interface.

The default settings of the board are as follows:

- Analog input to the ADAQ7769-1 obtained from IN; IEPE_IN is disconnected by P4.
- Using the ADR444 (U4) as a 4.096V reference, software default of PGA_GAIN = 1 V/V, and the hardware default of AAF_GAIN = 1/7 V/V (IN3_AAF), the full-scale input range is ±28.672V (but the input is limited to ±15.9V by default due to the PGA supply rails and common mode range headroom requirement).

See Table 3 for the suggested power supply rails and Table 4 for necessary jumper positions and link options for different input configurations and input ranges. It is recommended to use a low distortion AC source, such as the Audio Precision APx555 series, when evaluating the dynamic performance of the ADAQ7769-1.

IEPE INTERFACE

An IEPE sensor can be used as an input to the EV-ADAQ7769-1FMC1Z through the SMA connector at IEPE_IN. The on-board IEPE interface biases the IEPE sensor, which operates by providing a 24V rail at HV_VDD via the on-board supply or an external supply, and switching on SW_S1 and SW_S2 on the mechanical switch S2. Inserting P4 connects the IEPE input to the ADAQ7769-1. With a dropout of 1.2V across the current source (LT3092, U6) delivering a 4.5mA bias to the IEPE sensor, this circuit complies to the usable excitation voltage and current bias of a typical IEPE interface (see Figure 5). For overvoltage protection from the IEPE sensor, the ADG5421F (U5) fault protection switch is placed at the IEPE input. Under normal operating conditions, the IEPE LED indicator (DS1) is on.

Most IEPE sensors have their output biased at +8V to +14V, with an AC swing ±5V around the bias. The EV-ADAQ7769-1FMC1Z can be modified to allow AC-coupled or DC-coupled IEPE input. By default, the 0Ω resistor at R13 configures the IEPE input to be DC-coupled. Using the default gain settings of the device (PGA_GAIN = 1 V/V, IN3_AAF_GAIN = 1/7 V/V), the ADAQ7769-1 input range captures DC-coupled signals from the IEPE sensors, which may swing greater than 20V, given a change to the default power rails. For an AC-coupled IEPE input, simply replace R13 with a ceramic capacitor, and insert a resistor at R14 to implement a high-pass filter with a cut-off frequency at the subhertz range. The AC-coupled IEPE signal swing is suitable for the 4.096V (PGA_GAIN = 1 V/V, IN1_AAF_GAIN = 1 V/V) or the 11.2V (PGA_GAIN = 1 V/V, IN2_AAF_GAIN = 4/11 V/V) input ranges of the ADAQ7769-1, depending on the AC swing of the IEPE sensor.

Table 1 summarizes the recommended jumper settings related to using an IEPE sensor input.

Table 1. Jumper Settings when Applying an IEPE Sensor Input

Function	Link	Recommended Jumper Position for IEPE Input	Comment
IEPE Input	P4	Insert jumper	Connects IEPE_IN to ADAQ7769-1.
Input Range	JP1	Position C	Recommends use of IN3_AAF (G = 1/7 V/V) input range, which is designed for a DC-coupled IEPE sensor input.
	JP2	Position C	
IEPE Input Coupling	R13	0Ω at R13	IEPE input is DC-coupled (default). Optionally, replace R13 with a capacitor to have an AC-coupled IEPE input.
IEPE Interface Supply (HV_VDD)	JP5	Position A	IEPE interface uses on-board supply INT_VDD (default). Optionally, change to Position B to use an external supply, EXT_VDD.
S2	SW_S1	High	ADG5421F Channel 1 Enable. Connects IEPE interface to IEPE_IN.
		Low	Disconnects IEPE interface from IEPE_IN.
	SW_S2	High	ADG5421F Channel 2 Enable. Connects IEPE_IN to ADAQ7769-1.
		Low	Disconnects IEPE_IN from ADAQ7769-1.
	GAIN0 to GAIN2	All low	GAIN0 to GAIN2 mechanical switches for PGA gain setting. PGA_GAIN = 1 V/V (default)
	EN_PGA	High	Enables PGA (default).

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EV-ADAQ7769-1FMC1Z obtains its power from the 3.3V rail of the Zedboard™ by default, which is boosted and regulated to provide the supply rails required by the ADAQ7769-1, voltage reference, additional signal conditioning, and the IEPE interface.

The ADAQ7769-1 contains an internal 5V low dropout (LDO) regulator with the purpose of simplifying the power solution and layout of the signal chain µModule. Together with this internal LDO regulator, the ADAQ7769-1 can operate with only a 5.3V and 3.3V rail. In the EV-ADAQ7769-1FMC1Z, the 3.3V from the Zedboard™ directly powers the VDD_IO. This 3.3V rail is boosted to 5.3V by the LTC3526LB-2, which is then regulated by the internal LDO regulator to 5V, powering VDD_FDA, VDD_ADC, VDD2_ADC, and the ADR444 voltage reference. The 5.3V LED (DS2) is on when a 5.3V rail is powered by the on-board or external 5.3V supply.

The higher voltage rails used by the PGA and the IEPE interface, VDD/VSS_BUF and HV_VDD, are connected to the on-board rails, INT_VDD and INT_VSS, which are powered by the ADP5076 dual switching regulator, ADP7142 positive LDO regulator, and ADP7182 negative LDO regulator, as shown in Figure 6. This power tree boosts and regulates the 3.3V to a default of +20V and −16V. For the larger input signal covered by the IN3_AAF (24V) range, the PGA and IEPE interface may require a higher voltage supply. In this case, the voltage of the rails can be increased to 24V by moving the 0Ω links at the feedback resistors of the ADP5076, ADP7142, and ADP7182. As an option, VDD/VSS_PGA and HV_VDD can also be connected to the external supply rails, EXT_VDD and EXT_VSS. See Table 3 for the recommended power supply rails and Table 4 for the power supply link options.

Each supply is decoupled at the point where the supply enters the EV-ADAQ7769-1FMC1Z and again at the point where the EV-ADAQ7769-1FMC1Z connects to each device. The ADAQ7769-1 has built-in, 0.1µF supply decoupling capacitors on the VDD_PGA, VSS_PGA, VDD_FDA, VDD_ADC, VDD2_ADC, and VDD_IO supply pins.

The power solution for the EV-ADAQ7769-1FMC1Z was designed with the aid of LTpowerCAD. This tool is helpful in planning and designing power systems, with component recommendations to optimize the overall power solution.

Table 2. On-Board Power Supplies

Power Supply (V)	Function
+3.3V	VDD_IO and EV-ADAQ7769-1FMC1Z main supply rail from the ZedBoard™.
+5V	VDD_FDA, VDD_ADC, VDD2_ADC, and ADR444 supply rails using internal LDO.
+20V	VDD_PGA supply rail using the ADP7142.
−16V	VSS_PGA supply rail using the ADP7182.

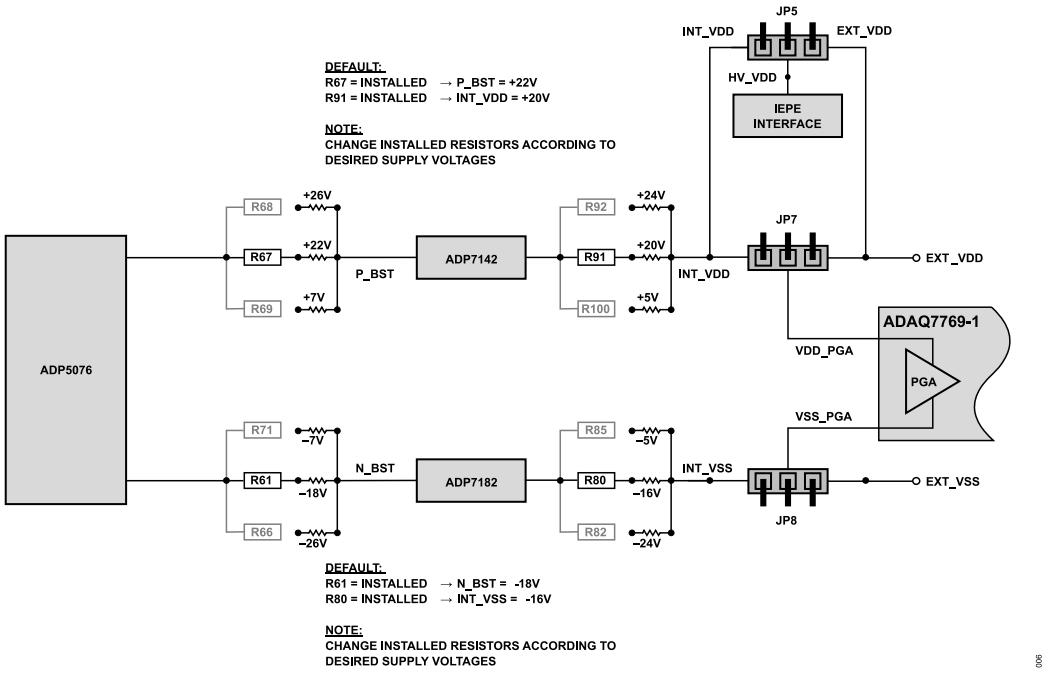

Figure 6. VDD_PGA, VSS_PGA, and HV_VDD Jumper Settings

EVALUATION BOARD HARDWARE

Table 3. Recommended Power Supply Rails Based on Input Type

PGA Input and Output Range (V)	AAF Inputs Configuration	IEPE Supply HV_VDD (V)	Buffer Supply VDD_BUF (V)		Comments
			Positive	Negative	
±4.096 (Voltage Input to IN)	OUT_PGA to IN1_AAF+ IN1_AAF− to GND	Not applicable	P_BST = 22 VDD_PGA = INT_VDD = 20	N_BST = −18 VSS_PGA = INT_VSS = −16	By default, the PGA uses on-board supplies, INT_VDD and INT_VSS, set at +20V and −16V.
±11.2 (Voltage Input to IN)	OUT_PGA to IN2_AAF+ IN2_AAF− to GND	Not applicable	P_BST = 22 VDD_PGA = INT_VDD = 20	N_BST = −18 VSS_PGA = INT_VSS = −16	By default, the PGA uses on-board supplies, INT_VDD and INT_VSS, set at +20V and −16V.
0 to +20, (Either DC-Coupled IEPE Input to IEPE_IN or Voltage Input to IN)	OUT_PGA to IN3_AAF+ IN3_AAF+ to GND	P_BST = 26 HV_VDD = INT_VDD = 24	P_BST = 26 VDD_PGA = INT_VDD = 24	N_BST = −7 VSS_PGA = INT_VSS = −5	This input range is designed for DC-coupled IEPE inputs. Change supply rails to suit input range. Caution: ensure that VDD_PGA – VSS_PGA does not exceed the PGA operating voltage of 36V.
0 to −24, (Voltage Input to IN)	OUT_PGA to IN3_AAF+ IN3_AAF+ to GND	Not applicable	P_BST = 7 VDD_PGA = INT_VDD = 5	N_BST = −26 VSS_PGA = INT_VSS = −24	Change supply rails to suit input range. Caution: ensure that VDD_PGA – VSS_PGA does not exceed the PGA operating voltage of 36V.
Negative Voltage Accelerometer	Not applicable	Not applicable	Not applicable	Not applicable	No available interface for negative voltage accelerometers. Requires 4mA IEPE current sink.

HARDWARE LINK OPTIONS

Multiple link options must be set correctly for the appropriate operating setup before applying the power and signal to the EV-ADAQ7769-1FMC1Z. Table 4 shows the default link positions for the EV-ADAQ7769-1FMC1Z.

Table 4. Default Links and Link Options

Function	Link	Default Position	Comment
AAF_GAIN setting	JP1, JP2	0Ω from COM to Position C	IN3_AAF (AAF_GAIN = 1/7 V/V) selected by default. Optionally, move both 0Ω links to Position B to use IN1_AAF. Also, optionally move both 0Ω links to Position A to use IN2_AAF.
IEPE Input	P4	No connect	The analog inputs to the ADAQ7769-1 are obtained from IN by default. Optionally, insert jumper at P4 and mechanically switch on SW_S1 and SW_S2 from S2 to use the IEPE sensor as an input.
IEPE Interface Supply (HV_VDD)	JP5	Position A	The IEPE interface uses an on-board supply, INT_VDD. Optionally, change to Position B to use the external supply, EXT_VDD.
PGA Supply (VDD_PGA)	JP7	Position A	PGA uses the on-board supply, INT_VDD, by default. Optionally, change to Position B to use the external supply, EXT_VDD.
PGA Supply (VSS_VSS)	JP8	Position A	PGA uses the on-board supply, INT_VSS, by default. Optionally, change to Position B to use the external supply, EXT_VSS.
S2	SW_S1	Low	Low: ADG5421F Channel 1 Enable. Disconnects the IEPE interface from IEPE_IN.

EVALUATION BOARD HARDWARE

Table 4. Default Links and Link Options (Continued)

Function	Link	Default Position	Comment
			High: Connects the IEPE interface to IEPE_IN
	SW_S2	Low	Low: ADG5421F Channel 2 Enable. Disconnects IEPE_IN from the ADAQ7769-1.
			High: Connects IEPE_IN to the ADAQ7769-1. To use the IEPE sensor as input, insert jumpers at P4 and switch on SW_S1 and SW_S2.
	GAIN0, GAIN1, GAIN2	All low	GAIN0 to GAIN2 mechanical switches for PGA gain setting. PGA_GAIN = 1 V/V is set by default. See the Input Range Configuration section on how to set the PGA_GAIN.
	EN_PGA	High	PGA is enabled by default.
	M0_FDA, M1_FDA	All low, disconnected	Reserved. Do not use.
IEPE Input Coupling	R13	0Ω at R13	The IEPE input is DC-coupled by default. Optionally, replace R13 with a capacitor to have an AC-coupled IEPE input.
3.3 V Supply	R106	0Ω at R106	The 3.3V supply is from the ZedBoard™ by default. Optionally, remove R106 and connect the external supply to the 3V3 turret.
5.3 V Supply	R57	0Ω at R57	The IN_LDO pin of the ADAQ7769-1 uses the on-board 5.3V supply. LED DS1 is on. Optionally, remove R57 and connect the external supply to the 5V3 turret.
VDD2_ADC Supply	R16	0Ω at R16	The VDD2_ADC pin of the ADAQ7769-1 uses the internal LDO regulator by default. Optionally, remove R16 and connect the external supply to the VDD2_ADC turret.
ADP5076 VR1 Positive Output Voltage (P_BST)	R67	0Ω at R67	P_BST is set at 22 V by default. Optionally, move 0 Ω to R68 to set P_BST = 26V. In addition, set the ADP7142 output voltage, INT_VDD, to 24V by moving the 0Ω from R91 to R92. Also, optionally move 0Ω to R69 to set P_BST = 7V. In addition, set the ADP7142 output voltage, INT_VDD, to 5V by moving the 0Ω from R91 to R100.
	R68	R68 not placed	
	R69	R69 not placed	
ADP5076 VR1 Negative Output Voltage (N_BST)	R61	0Ω at R61	N_BST is set at −18V by default. Optionally, move 0Ω to R66 to set N_BST = −26V. In addition, set the ADP7182 output voltage, INT_VSS, to −24 V by moving 0Ω from R80 to R82. Also, optionally, move 0Ω to R71 to set N_BST = −7V. In addition, set the ADP7182 output voltage, INT_VSS, to −5V by moving 0Ω from R80 to R85.
	R66	R66 not placed	
	R71	R71 not placed	
ADP7142 Output Voltage (INT_VDD)	R91	0Ω at R91	INT_VDD is at 20V by default. Optionally, move 0Ω to R92 to set INT_VDD = 24V. In addition, set the ADP5076 positive output voltage, P_BST, to 26V by moving 0Ω from R67 to R68. Also, optionally move 0Ω to R100 to set INT_VDD = 5V. In addition, set the ADP5076 positive output voltage, P_BST, to 7V by moving 0Ω from R67 to R69.
	R92	R92 not placed	
	R100	R100 not placed	
ADP7182 Output Voltage (INT_VSS)	R80	0Ω at R80	INT_VSS is at −16V by default. Optionally, move 0Ω to R82 to set INT_VSS = −24V. In addition, set the ADP5076 negative output voltage, N_BST, to −26V by moving 0Ω from R61 to R66. Also, optionally, move 0Ω to R85 to set INT_VSS = −5V. In addition, set the ADP5076 negative output voltage, N_BST, to −7V by moving 0Ω from R61 to R71.
	R82	R82 not placed	
	R85	R85 not placed	
Voltage Reference U4	R20	11Ω at R20	The ADR444 (voltage reference) output directly connects to the ADAQ7769-1 by default.

EVALUATION BOARD HARDWARE

ON-BOARD CONNECTORS

Table 5 provides information about the external on-board connectors on the EV-ADAQ7769-1FMC1Z.

Table 5. On-Board Connectors

Connector	Function
IN	SMB analog input for AC signals
FDA_IN	SMB analog input that bypasses ADAQ7769-1 PGA
T1	Turret for DC analog inputs
IEPE_IN	SMA for the IEPE sensor input
MCLK	SMB for the external MCLK
P5	FMC connects all digital signals to the ZedBoard™
P6	PMOD connector allows the user to interface with the board
LDO_OUT	Turret to connect to external V_{REF} input
3V3	Turret to connect to external 3.3V supply
5V3	Turret to connect to external 5.3V supply
VDD2_ADC	Turret to connect to external VDD2_ADC supply
EXT_VDD	Turret to connect to external positive supply for buffers and/or IEPE interface
EXT_VSS	Turret to connect to external negative supply for buffers

EVALUATION BOARD SETUP PROCEDURE

EV-ADAQ7769-1FMC1Z CONNECTION WITH ZEDBOARD™

Figure 7 shows a diagram of the evaluation setup for the EV-ADAQ7769-1FMC1Z board. After completing the steps in the Quick Start Guide section, proceed with the following to start data capture:

1. Double click the **EV-ADAQ7769-1FMC1Z** evaluation board icon to open the board view window.
2. Double click the **ADAQ7769-1** chip icon in the board view window to open the chip view window.
3. Click **Software Defaults** and then click **Apply Changes**.
4. Click the **Proceed to Analysis** button to show the analysis view window.
5. Apply an input signal at IN, or through the optional IEPE input (IEPE_IN), then click **Run Once**.

To power off, first disconnect the input signal, and close the software. Then toggle the switch SW8 to turn off the ZedBoard™ before disconnecting the USB.

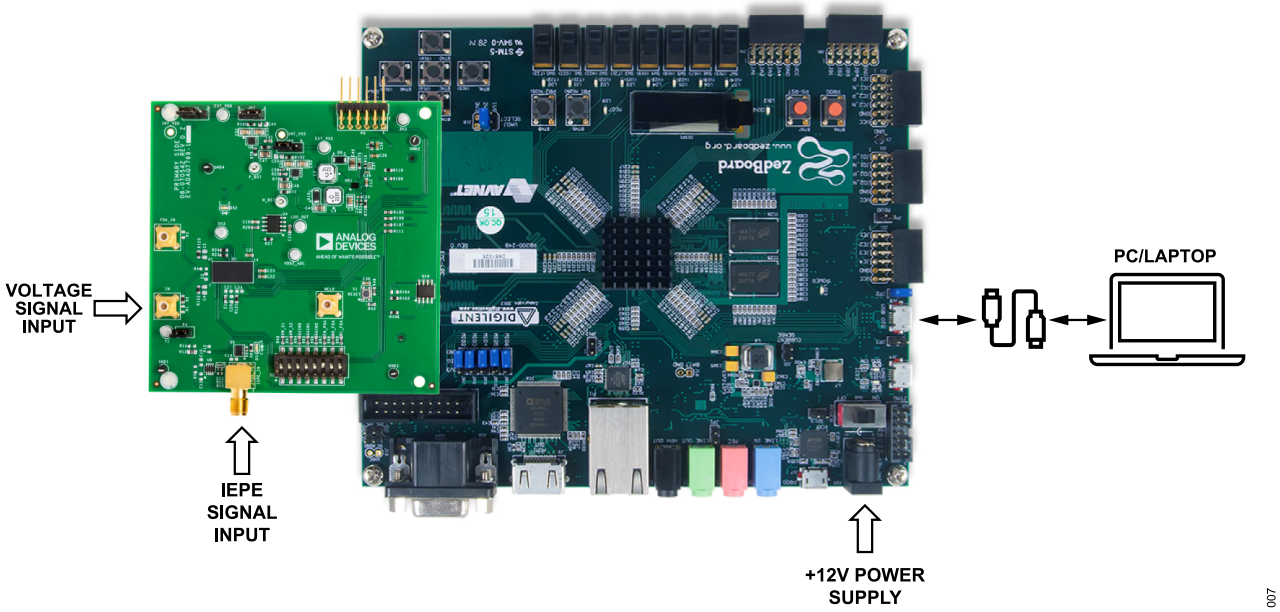

Figure 7. Evaluation Board Setup

EVALUATION BOARD SETUP PROCEDURE

INPUT RANGE CONFIGURATION

Table 6. Input Selection Table Using IN1_AAF

GAIN2 Pin Logic	GAIN1 Pin Logic	GAIN0 Pin Logic	PGA Gain (V/V)	AAF Gain (V/V)	Total Signal Chain Gain (V/V)	Full-Scale Range (V) with V_{REF} = 4.096V	Recommended Input Range (V) with V_{REF} = 4.096V
L	L	L	1	1	1	±4.096	
L	L	H	2	1	2	±2.048	
L	H	L	4	1	4	±1.024	
L	H	H	8	1	8	±0.512	
H	L	L	16	1	16	±0.256	
H	L	H	32	1	32	±0.128	
H	H	L	64	1	64	±0.064	
H	H	H	128	1	128	±0.032	

Table 7. Input Selection Table Using IN2_AAF

GAIN2 Pin Logic	GAIN1 Pin Logic	GAIN0 Pin Logic	PGA Gain (V/V)	AAF Gain (V/V)	Total Signal Chain Gain (V/V)	Full-Scale Range (V) with V_{REF} = 4.096V	Recommended Input Range (V) with V_{REF} = 4.096V
L	L	L	1	0.364	0.364	±11.264	
L	L	H	2	0.364	0.727	±5.632	
L	H	L	4	0.364	1.455	±2.816	
L	H	H	8	0.364	2.909	±1.408	
H	L	L	16	0.364	5.818	±0.704	
H	L	H	32	0.364	11.636	±0.352	
H	H	L	64	0.364	23.273	±0.176	
H	H	H	128	0.364	46.545	±0.088	

Table 8. Input Selection Table Using IN3_AAF

GAIN2 Pin Logic	GAIN1 Pin Logic	GAIN0 Pin Logic	PGA Gain (V/V)	AAF Gain (V/V)	Total Signal Chain Gain (V/V)	Full-Scale Range (V) with V_{REF} = 4.096V[1]	Recommended Input Range (V) with V_{REF} = 4.096V[2]
L	L	L	1	0.143	0.143	±28.672	±15.9
L	L	H	2	0.143	0.286	±14.336	±7.95
L	H	L	4	0.143	0.571	±7.168	±3.975
L	H	H	8	0.143	1.143	±3.584	±1.987
H	L	L	16	0.143	2.286	±1.792	±0.993
H	L	H	32	0.143	4.571	±0.896	±0.496
H	H	L	64	0.143	9.143	±0.448	±0.248
H	H	H	128	0.143	18.286	±0.224	±0.124

[1] Actual PGA input range is limited by Max = VDD_PGA − 4.4V, Min = VSS_PGA + 0.1V.

[2] PGA supplies are VDD_PGA = +20V, VSS_PGA = −16V.

EVALUATION BOARD SCHEMATICS AND ARTWORK

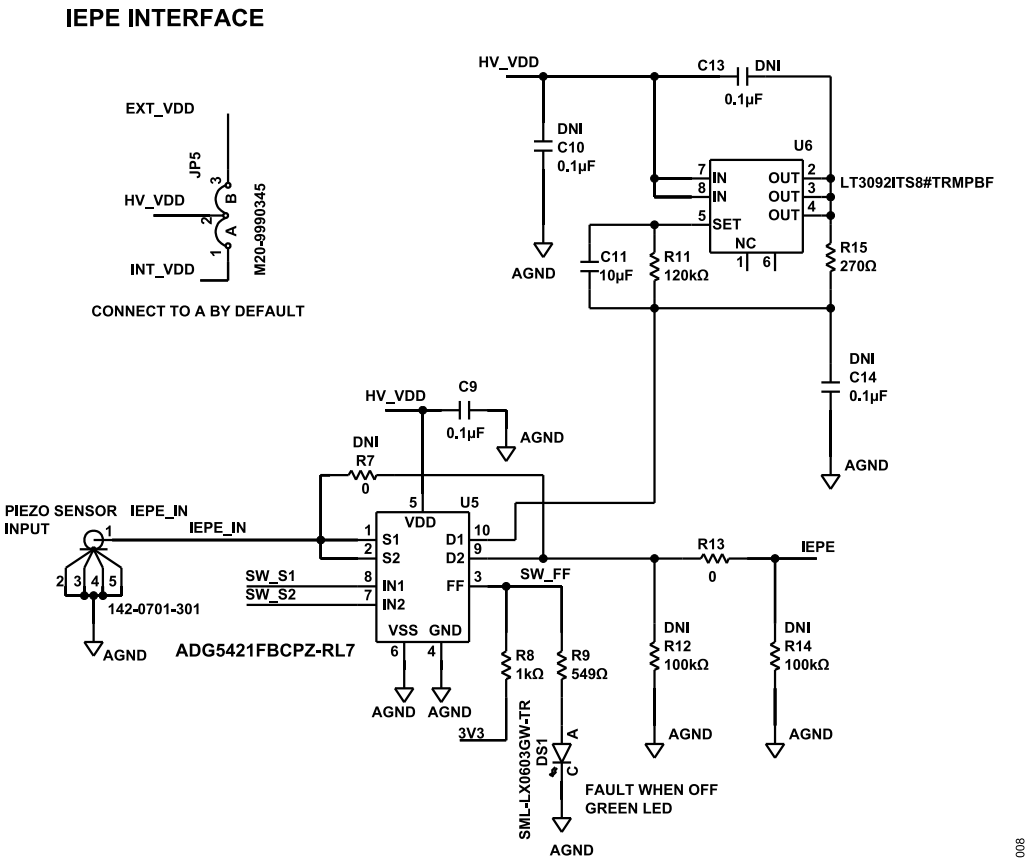

Figure 8. IEPE Interface Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

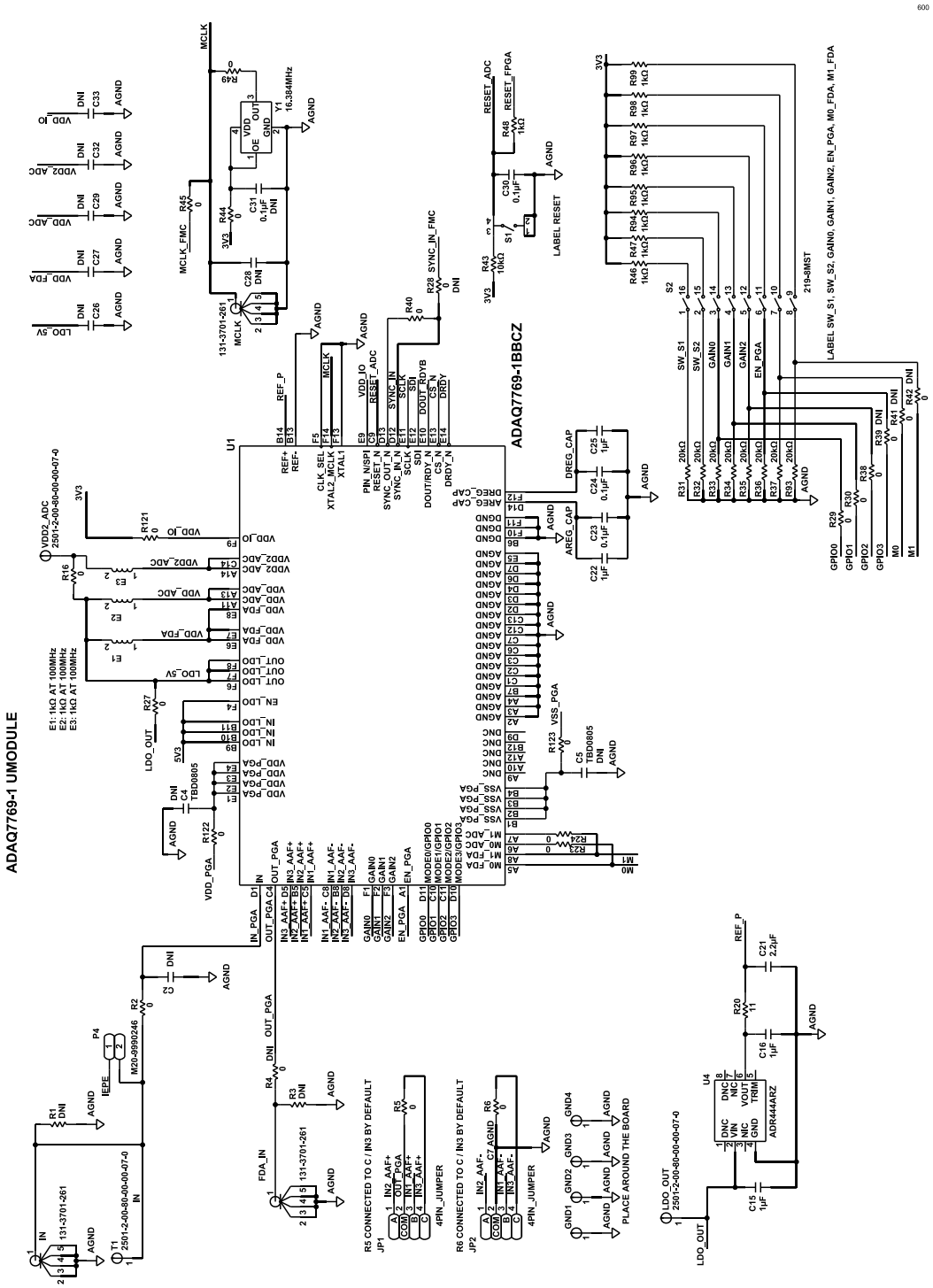

Figure 9. ADAQ7769-1 µModule® Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

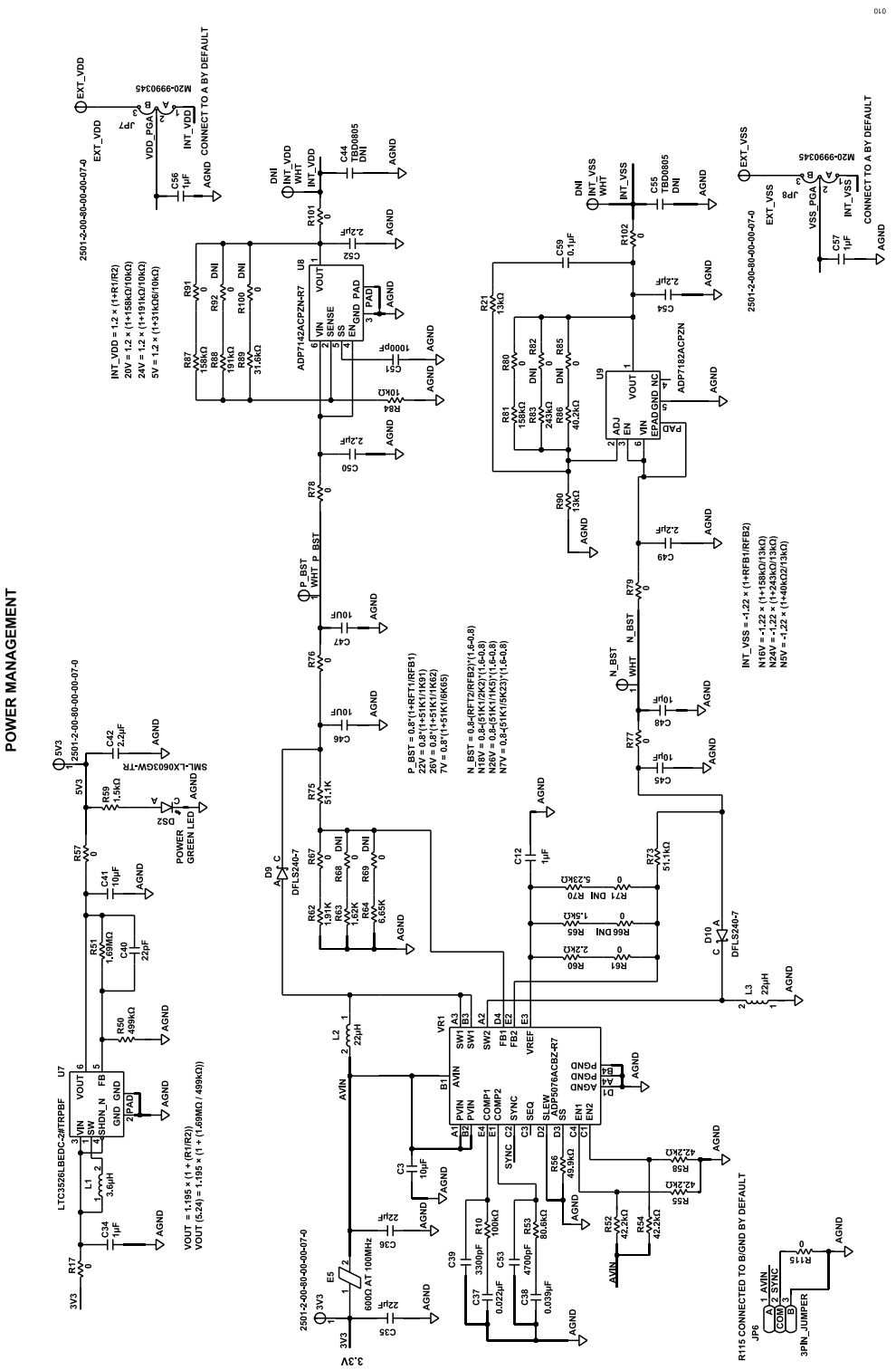

Figure 10. Power Management Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

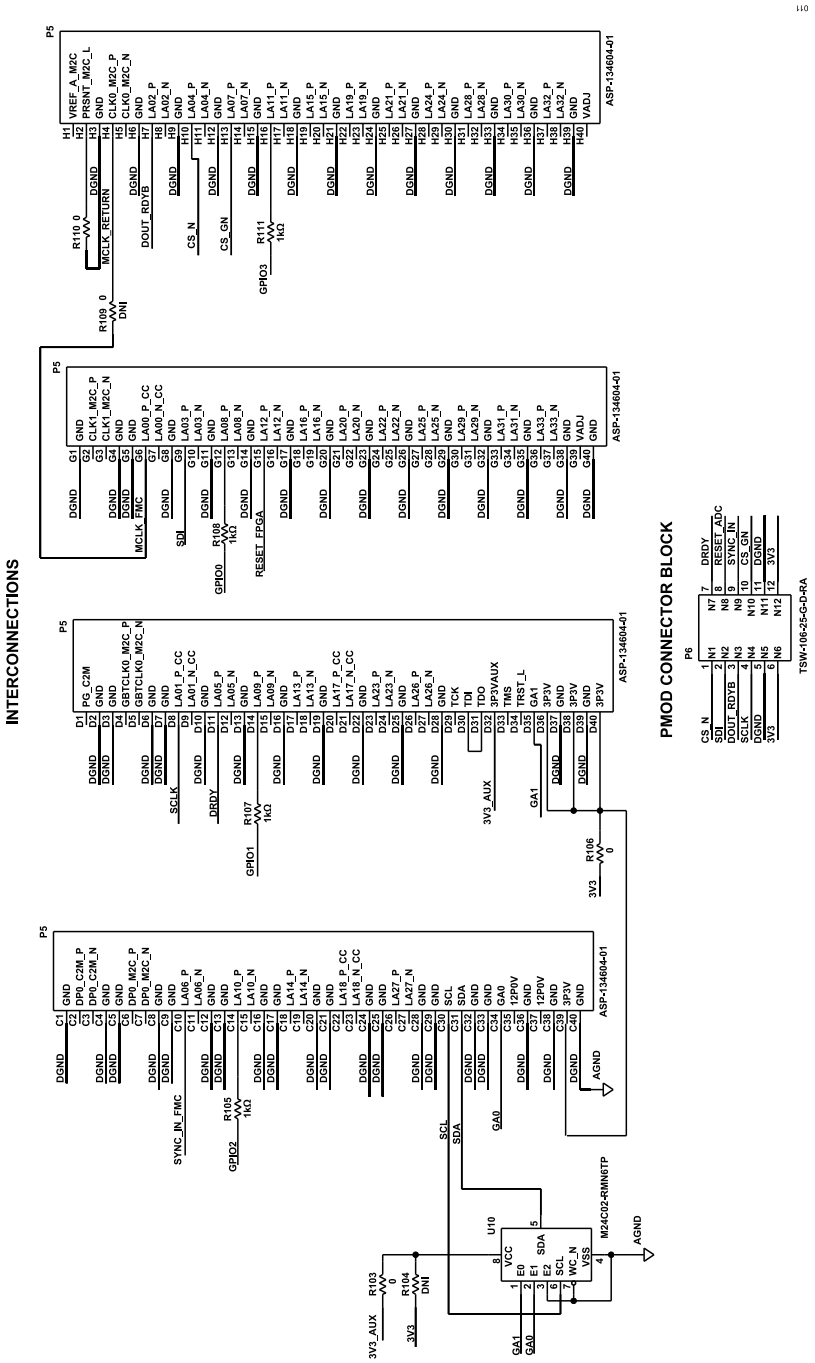

Figure 11. Digital Interconnections Schematic

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.