FEATURES

- Fully featured Pmod evaluation board with a Pmod to FMC interposer board
- Versatile analog signal conditioning circuitry
- On-board reference and ADC drivers
- PC software for control and data analysis of time and frequency domain
- System demonstration platform compatible (EVAL-SDP-CH1Z)

EVALUATION BOARD KIT CONTENTS

- EVAL-ADAQ4001PMDZ or EVAL-ADAQ4003PMDZ Pmod evaluation board
- EVAL-PMD-IB1Z Pmod to FMC interposer board

EQUIPMENT NEEDED

- PC running Windows® 10 or higher
- EVAL-SDP-CH1Z (SDP-H1) controller board
- Precision signal source
- Cable (SMB input to evaluation board)
- Standard USB A to Mini-B USB cable
- Band-pass filter suitable for 16-bit/18-bit testing (value based on signal frequency)

SOFTWARE NEEDED

- ACE evaluation software
- ADAQ4001 or ADAQ4003 ACE plugin

GENERAL DESCRIPTION

The ADAQ4001 and ADAQ4003 µModule® data acquisition system evaluation kit (EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ) contains the EVAL-ADAQ4001PMDZ or EVAL-ADAQ4003PMDZ peripheral module (Pmod) board and the EVAL-PMID-IB1Z Pmod to field programmable gate array (FPGA) mezzanine card (FMC) interposer board that interfaces with the system demonstration controller board (EVAL-SDP-CH1Z) via a 160-pin FMC connector, as shown in Figure 1.

The ADAQ4001 µModule and the ADAQ4003 µModule combine multiple common signal processing and conditioning blocks into a single device that includes a low noise, fully differential analog-to-digital converter (ADC) driver, a stable reference buffer, a high resolution, 16-bit or 18-bit, 2 MSPS successive approximation register (SAR) ADC, and the critical passive components necessary for optimum performance.

The EVAL-ADAQ4001PMDZ and the EVAL-ADAQ4003PMDZ onboard components include the following:

- The ADR4550 high precision, buffered band gap, 5.0 V voltage reference (see Figure 25)
- An optional ADA4898-1 high voltage, low noise, low distortion, unity-gain stable, high speed op amp (see Figure 26)
- An optional AD8251 programmable gain in-amp (see Figure 26)
- The LT5400-4 quad matched, low drift, resistor network

Note that J1 and J2 on the EVAL-ADAQ4001PMDZ and the EVAL-ADAQ4003PMDZ provide low noise analog signal sources.

For full details on the ADAQ4001 or the ADAQ4003, see the ADAQ4001 or the ADAQ4003 data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ.
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REVISION HISTORY

10/2022—Rev. A to Rev. B
Changes to Figure 26 ............................................... 21
Changes to Figure 27 ............................................... 22

5/2021—Rev. 0 to Rev. A
Added EVAL-ADAQ4001FMCZ ................................. 1
Added ADAQ4001 .................................................. 1
Added EVAL-ADAQ4001PMDZ .............................. 1
Changes to Software Needed Section .................. 1
Changes to Figure 2 ............................................... 5
Changes to Power Supplies Section ................... 6
Changes to Table 2 ................................................. 7
Changes to Evaluation Board Software Section .... 9
Added Figure 8 to Figure 14; Renumbered Sequentially ... 9
Deleted Figure 8 to Figure 20; Renumbered Sequentially .... 9
Added Figure 15 .................................................... 10
Deleted Figure 21, Figure 22, and Figure 23 ......... 10
Add ACE Software Operation Section .................. 12
Deleted Software Operation Section, Figure 25 to Figure 32, and Table 4; Renumbered Sequentially ..... 12
Added Figure 16, Figure 17, Figure 18, and Figure 19 .......... 12
Added Figure 20, Figure 21, and Figure 22 .......... 15
Added Figure 23 and Figure 24 ............................... 17
Changed ADAQ400x Evaluation Board Software Troubleshooting Section to Evaluation Board
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Changes to Hardware Troubleshooting Section ....... 19
Added EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ Section and Figure 25 to Figure 31 ............. 20
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9/2020—Revision 0: Initial Version
Figure 1.
**EVALUATION BOARD HARDWARE**

**SETTING UP THE EVAL-ADAQ4001FMCZ AND EVAL-ADAQ4003FMCZ EVALUATION KIT**

Figure 2 shows the simplified block diagram of the EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ. Figure 25 to Figure 26 show the EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ board schematics, which consist of the ADAQ4001 µModule or ADAQ4003 µModule (U5), the ADR4550 (U1), the ADA4898-1 (U4 and U7), the AD8251 (A1), the ADP5070 (U3), the LT3032 (U2), and the LT3023 (U6). The EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ are flexible designs that enable the user to select components and operate the evaluation boards from an adjustable bench top power supply.

**EVAL-SDP-CH1Z (SDP-H1) BOARD**

The EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ evaluation kit uses a serial port interface (SPI) and requires the system demonstration platform (SDP-H1) to capture the data via a graphic user interface (GUI) (see Figure 1). The SDP-H1 requires power from a 12 V wall adapter. The SDP-H1 has a Xilinx® Spartan®-6 and an ADSP-BF527 processor with connectivity to the PC through a USB 2.0 high speed port.

The SDP-H1 has an FMC low pin count connector with fully differential low voltage differential signaling (LVDS) and singled-ended, low voltage, CMOS support. The SDP-H1 also has a 120-pin connector that exposes the Blackfin® processor peripherals. This connector provides a configurable serial, parallel I2C and SPI and general-purpose input/output (GPIO) communication lines to the attached daughter board.
EVALUATION BOARD HARDWARE

POWER SUPPLIES

The SDP-H1 supplies 3.3 V to power the rails for the different components on the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ.

The ADAQ4001 µModule and the ADAQ4003 µModule use four power supply pins: the ADC driver positive supply (VS+), the ADC driver negative supply (VS−), the core ADC supply (VDD), and the digital input and output interface supply (VIO). The VIO pin allows the direct interface with any logic between 1.8 V and 5.5 V. To reduce the number of supplies required, VIO and VDD can be tied together for a 1.8 V operation. A combination of the ADP5070 (dual, high performance dc-to-dc switching regulator), the LT3032 (dual, low noise, positive and negative low dropout voltage linear regulator), and the LT3023 (dual, micropower, low noise, low dropout regulator) can generate independently regulated positive and negative rails for all four power supply pins, including ±15 V rails for any additional signal conditioning.

Table 1. Default Power Supplies Available on the EVAL-ADAQ4001PMDZ and the EVAL-ADAQ4003PMDZ

<table>
<thead>
<tr>
<th>Power Supply (V)</th>
<th>Function</th>
<th>Components Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>+5.5</td>
<td>Reference rail</td>
<td>ADP5070, LT3032, LT3023</td>
</tr>
<tr>
<td>±15</td>
<td>Amplifier rails</td>
<td>ADP5070, LT3032</td>
</tr>
<tr>
<td>+1.8, +3.3, or +5.5</td>
<td>µModule rails</td>
<td>ADP5070, LT3032, LT3023</td>
</tr>
</tbody>
</table>

Each supply is decoupled at the EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ entrance and device connection. A single, on-board ground plane minimizes the effect of the high frequency noise interference.

In addition, the EVAL-ADAQ4001PMDZ and the EVAL-ADAQ4003PMDZ can be powered from a benchtop power supply of ±15.5 V. The +15.5 V, −15.5 V, and GND test points are available on board to support this function. When bench power is used, the on-board power supplies are no longer required, and the link between the output pin of the ADP5070 must be removed, that is, uninstall R20 and R22.

Take the following steps to set up the EVAL-ADAQ4001PMDZ or the EVAL-ADAQ4003PMDZ when using a benchtop power supply of ±15.5 V:

1. Connect the EVAL-ADAQ4001PMDZ or the EVAL-ADAQ4003PMDZ to the EVAL-PMD-IB1Z interposer board at the P1 header (see Figure 1).
2. Connect the EVAL-PMD-IB1Z interposer board to the SDP-H1 via the 160-pin FMC connector.
3. Connect the USB and a 12 V power adapter to the SDP-H1. Ensure that the software and drivers are installed.
4. Connect the +15.5 V and −15.5 V bench supplies to the +15.5 V and −15.5 V test points on the EVAL-ADAQ4001PMDZ or the EVAL-ADAQ4003PMDZ (see Figure 3). Connect the bench supply ground to the GND test point as shown in Figure 3.

5. Power up the benchtop supply. The +15.5 V supply rail draws approximately 25 mA, and the −15.5 V supply rail draws approximately 20 mA.

The EVAL-ADAQ4001PMDZ or the EVAL-ADAQ4003PMDZ is now ready to use. See the Evaluation Board Software section for details on using the Analysis | Control | Evaluation (ACE) software. Note that by default, the EVAL-ADAQ4001PMDZ and the EVAL-ADAQ4003PMDZ are set up to accept a differential input at J1 and J2 with a 22 V range.

Figure 3. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ External Supply (Optional) Connections
The analog inputs of the EVAL-ADAQ4001PMDZ and the EVAL-ADAQ4003PMDZ, J1 and J2, are Subminiature Version B (SMB) connectors. These inputs are fed to the ADA4898-1. J1 and J2 are buffered with dedicated amplifier circuitry, U4 and U7, as shown in Figure 26. The circuit enables different configurations, input range scaling, filtering, amplifiers and supplies, and the addition of a dc component. The analog input amplifiers are set as unity-gain buffers at the factory.

The analog inputs are fully differential by default. If a single-ended bipolar input is desired, such as ±10 V, the EVAL-ADAQ4001PMDZ or the EVAL-ADAQ4003PMDZ can be configured for single-ended to differential conversion by changing JP6 to Pin B to Pin COM and by applying the single-ended input at Connector J1 (see Table 2).

For dynamic performance, a fast Fourier transform (FFT) test can be performed by applying a low distortion ac source. For low frequency testing, the audio precision source, such as the SYS-2700 series, can be used directly with the evaluation boards. Different precision sources can be used with additional filtering.

### Table 2. Jumper Details with Factory Default Setting

<table>
<thead>
<tr>
<th>Link</th>
<th>Default</th>
<th>Function</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP1</td>
<td>Not populated</td>
<td>Gain options</td>
<td>Fully differential or single-ended configuration.</td>
</tr>
<tr>
<td>JP2</td>
<td>B1 and B2, A1 and A2</td>
<td>µModule input</td>
<td>The ADAQ4001 or the ADAQ4003 has a gain of 0.454 (22 V range). See the ADAQ4001 or the ADAQ4003 data sheet for other gains.</td>
</tr>
<tr>
<td>JP3</td>
<td>B1 and B2, A1 and A2</td>
<td>µModule input</td>
<td>The ADAQ4001 or the ADAQ4003 has a gain of 0.454 (22 V range). See the ADAQ4001 or the ADAQ4003 data sheet for other gains.</td>
</tr>
<tr>
<td>JP4</td>
<td>Pin A to Pin COM</td>
<td>Synchronize the switching frequency to CNV</td>
<td>To set the switching frequency to 1.2 MHz, pull the SYNC/FREQ pin of the ADP5070 low or Pin B to Pin COM.</td>
</tr>
<tr>
<td>JP5</td>
<td>Pin A to Pin COM</td>
<td>Op amp or in-amp</td>
<td>Connect the J1 input to the ADA4898-1 op amp.</td>
</tr>
<tr>
<td>JP6</td>
<td>Pin A to Pin COM</td>
<td>Op amp or in-amp</td>
<td>Connect the J2 input to the ADA4898-1 op amp.</td>
</tr>
<tr>
<td>JP8</td>
<td>Pin A to Pin COM</td>
<td>Amplifier or in-amp</td>
<td>Connect Pin A to Pin COM to the output of the AD8251.</td>
</tr>
<tr>
<td>JP9</td>
<td>Pin B to Pin COM</td>
<td>Gain setting pin (LSB)</td>
<td>Refer to the AD8251 data sheet for the truth table logic levels for transparent gain mode.</td>
</tr>
<tr>
<td>JP10</td>
<td>Pin B to Pin COM</td>
<td>Gain setting pin (MSB)</td>
<td>Refer to the AD8251 data sheet for the truth table logic levels for transparent gain mode.</td>
</tr>
<tr>
<td>JP11</td>
<td>Pin A to Pin COM</td>
<td>Power</td>
<td>Differential amplifier positive supply. Tied to ground.</td>
</tr>
<tr>
<td>JP12</td>
<td>Pin A to Pin COM</td>
<td>Differential amplifier power mode</td>
<td>Differential amplifier positive supply. Tied to ground.</td>
</tr>
<tr>
<td>JP13</td>
<td>Pin A to Pin COM</td>
<td>Differential amplifier power down</td>
<td>Normal mode. See the ADAQ4001 or the ADAQ4003 data sheet.</td>
</tr>
<tr>
<td>JP14</td>
<td>Pin A to Pin COM</td>
<td>Reference buffer power down</td>
<td>Powered up. See the ADAQ4001 or the ADAQ4003 data sheet.</td>
</tr>
<tr>
<td>JP15</td>
<td>Pin A to Pin COM</td>
<td>Differential amplifier power down</td>
<td>Powered up. See the ADAQ4001 or the ADAQ4003 data sheet.</td>
</tr>
</tbody>
</table>
EVALUATION BOARD HARDWARE

LINK CONFIGURATION FOR DIFFERENT GAIN OPTIONS

Multiple link options must be set correctly for the appropriate gain configuration of the ADAQ4001 or the ADAQ4003. Table 3 details the different gain positions for the links of the EVAL-ADAQ4001PMDZ and the EVAL-ADAQ4003PMDZ.

Table 3. The Different Gain Positions Available for the Links of the EVAL-ADAQ4001PMDZ or the EVAL-ADAQ4003PMDZ

<table>
<thead>
<tr>
<th>Gain</th>
<th>Input Range (V)</th>
<th>Input Signal on Pins</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.454</td>
<td>±11</td>
<td>R1K1− and R1K1+</td>
<td>For JP2, tie A1 to A2 and tie B1 to B2, and for JP3, tie A1 to A2 and tie B1 to B2 (see Figure 4).</td>
</tr>
<tr>
<td>0.9</td>
<td>±5.5</td>
<td>R1K− and R1K+</td>
<td>For JP2, tie B1 to B2, and for JP3, tie B1 to B2 (see Figure 5).</td>
</tr>
<tr>
<td>1</td>
<td>±5</td>
<td>R1K− and R1K+</td>
<td>For JP2, tie A2 to B1, and for JP3, tie A1 to B2 (see Figure 6).</td>
</tr>
<tr>
<td>1.9</td>
<td>±2.6</td>
<td>R1K1−, R1K−, R1K1+, and R1K+</td>
<td>For JP2, tie B1 to A2 and B2, and for JP3, tie B2 to A1 and B1 (see Figure 7).</td>
</tr>
</tbody>
</table>
SOFTWARE INSTALLATION PROCEDURES

Download the ACE evaluation software from the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ evaluation kit page. Install the software on a PC before using the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ kit. Download the ADAQ4001 or ADAQ4003 ACE plugin from the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ page or from the plugin manager in ACE.

Perform the following steps to complete the installation process:

1. Install the ACE evaluation software.
2. Install the SDP-H1 drivers.
3. Install the ADAQ4001 or ADAQ4003 plugin. The ACE Quick-start page shows the plugin installation guide.

Warning

Install the ACE software and SDP-H1 drivers before connecting the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ and the SDP-H1 to the USB port of the PC to ensure that the evaluation system is properly recognized when it is connected to the PC.

Installing the ACE Evaluation Software

To install the ACE evaluation software, take the following steps:

1. Download the ACE software to a Windows-based PC.
2. Double click the ACEInstall.exe file to begin the installation. By default, the ACE software is saved to the following location: C:\Program Files (x86)\Analog Devices\ACE
3. A dialog box opens asking for permission to allow the program to make changes to the PC. Click Yes to start the installation process.
4. In the ACE Setup window, click Next > to continue the installation (see Figure 8).

5. Read the software license agreement and click I Agree (see Figure 9).

6. Click Browse... to choose the install location and then click Next > (see Figure 10).

7. The ACE software components to install are preselected. Click Install (see Figure 11).
8. The Windows Security window opens (see Figure 12). Click Install. Figure 13 shows the installation in progress. No action is required.

9. When the installation completes, click Next > (see Figure 14), and then click Finish.

EVALUATION BOARD SETUP PROCEDURES

The EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ connects to the SDP-H1. The SDP-H1 is the communication link between the PC and the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ. Figure 1 shows a diagram of the connections between the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ and the SDP-H1.

Connecting the EVAL-ADAQ4001FMCZ or EVAL-ADAQ4003FMCZ and the SDP-H1 to a PC

After installing the ACE software, take the following steps to set up the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ and the SDP-H1:

1. Ensure that all configuration links are in the appropriate positions, as detailed from Figure 4 to Figure 7.
2. Connect the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ securely to the 160-way connector on the SDP-H1. The EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ do not require an external power supply adapter.
3. Connect the SDP-H1 to the PC via the USB cable included in the SDP-H1 kit.

Verifying the Board Connection

After connecting the power and the USB cable from the SDP-H1 to the PC, take the following steps to verify the board connection:

1. After connecting the SDP-H1 to the PC, allow the Found New Hardware Wizard to run. If prompted by the operating system, choose to automatically search for the drivers for the SDP-H1.
2. Navigate to the Device Manager window of the PC (see Figure 15).
3. A dialog box opens asking for permission to allow the program to make changes to the computer. Click Yes.
4. The Computer Management window opens. In the list labeled System Tools, click Device Manager. If the SDP-H1 driver software is installed, and the board is properly connected to the PC, Analog Devices SDP-H1 is shown in the ADI Development Tools list in the Device Manager window, as shown in Figure 15.

Disconnected the EVAL-ADAQ4001FMCZ or the EVAL-ADAQ4003FMCZ

Disconnect power from the SDP-H1 or press the reset tact switch located alongside the mini USB port on the SDP-H1 before disconnecting the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ from the SDP-H1.
LAUNCHING THE SOFTWARE

After the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ and the SDP-H1 are properly connected to the PC, launch the ACE evaluation software by taking the following steps:

1. From the Start menu of the PC, click All Programs > Analog Devices > ACE> ACE.exe to open the ACE software main window shown in Figure 16.

2. Connect the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ and the SDP-H1 to the USB. If the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ is not connected to the USB port via the SDP-H1 when the software launches, the ADAQ4001 Eval Board or ADAQ4003 Eval Board icon does not appear in the Attached Hardware section. To make the ADAQ4001 Eval Board or ADAQ4003 Eval Board icon appear, connect the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ and the SDP-

H1 to the USB port of the PC, wait a few seconds, and then follow the instructions in the dialog box that opens.

3. Double click the ADAQ4001 Eval Board or ADAQ4003 Eval Board icon in the ACE software main window (see Figure 16) to open the board view window shown in Figure 17.

4. Double click the ADAQ4001 or ADAQ4003 chip icon in the board view window (see Figure 17) to open the chip view window shown in Figure 18. The on-board voltage reference provided by the ADR4550 is 5.0 V, as shown in the board view window. Type the value of the reference voltage in the reference voltage box in the chip view window when using the external reference.

5. Click Software Defaults and then click Apply Changes to apply the default settings.

6. Click the Proceed to Analysis button to show the Analysis view window, as shown in Figure 19.
ACE SOFTWARE OPERATION

Figure 17. Board View Window

Figure 18. Chip View Window
Figure 19. Analysis View Window
DESCRIPTION OF ANALYSIS VIEW WINDOW

The Analysis view window allows the user to showcase the performance of the ADAQ4001 or the ADAQ4003. Before performing any measurements, set the capture settings (see the CAPTURE section) and analysis settings (see the ANALYSIS SETTINGS section).

The Analysis view window contains the Waveform tab (see Figure 20), Histogram tab (see Figure 21), and FFT tab (see Figure 22).
ACE SOFTWARE OPERATION

CAPTURE

The CAPTURE pane contains the capture settings. These settings reflect onto the registers automatically before data capture.

The Throughput(ksp/s) field in the Capture Settings section allows the user to set the throughput rate of the µModule. The default maximum throughput rate is 1754 kSPS. The 2 MSPS throughput rate can only be set when the µModule is in Turbo Mode with a minimum SCK rate of 75 MHz. Refer to the ADAQ4001 data sheet and the ADAQ4003 data sheet to determine the required SCK clock frequency for the selected 3-wire or 4-wire mode.

The No. of samples pulldown menu in the Capture Settings section allows the user to select the number of samples per capture.

Select the Turbo Mode check box in the Register Control section to enable a 2 MSPS throughput rate for the µModule.

Select the Span Compression check box in the Register Control section to reduce the input range by 10% from the top and bottom of the range while still accessing the available µModule codes.

Select the Enable Status Bits check box in the Register Control section to read the status registers after every after conversion.

Select the Use Custom Reference check box in the Reference section if the 5.0 V on-board reference is not used. Set the corresponding reference value in the Reference Voltage field.

When enabled, the Oversampling Ratio pulldown menu in the Software Oversampling section can be set between 2 and 256 and provide improved signal-to-noise ratio (SNR) performance. Refer to the ADAQ4001 data sheet and the ADAQ4003 data sheet to determine the maximum oversampling ratio for the selected oversampling mode.

Click Run Once to start a data capture of the samples at the sample rate specified in the No. of samples pulldown menu. These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

Click Run Continuously to start a data capture that gathers samples continuously with one batch of data at a time. This operation runs the Run Once operation continuously.

ANALYSIS SETTINGS

The General Settings section allows the user to set up the preferred configuration of the FFT analysis, including how many tones are analyzed. The fundamental is set manually.

The Windowing section allows the user to select the Window type used in the FFT analysis, set the Number of Harmonics, and set the number of Fundamental Bins that must be included.

The Single Tone Analysis section allows the user to select the fundamental frequency included in the FFT analysis.

The INL Settings section allows the user to set the Averaging Iterations and Truncation settings during the INL measurement.

The DNL Settings section allows the user to set the Averaging Iterations and Truncation settings during the DNL measurement.
RESULTS
Click Export to export the captured data. The waveform, histogram, and FFT data is stored in .xml files along with the values of the parameters at capture.

WAVEFORM TAB
The Waveform tab displays data in form of time vs. discrete data values with the results, as shown in Figure 20.

The Waveform graph shows each successive sample of the µModule output. The user can zoom in on and pan over the Waveform graph using the embedded waveform tools above the graph. Select the channels to display in the Display Channels section.

Under the Display Units pulldown menu, select Codes above the Waveform graph to select whether the Waveform graph displays in units of Codes, Hex, or Volts. The axis controls are dynamic.

When either y-scale dynamic or x-scale dynamic is selected, the corresponding axis width automatically adjusts to show the entire range of the µModule results after each batch of samples.

HISTOGRAM TAB
The Histogram tab contains the histogram graph and the RESULTS pane, as shown in Figure 21.

The RESULTS pane displays the information related to the dc performance.

The Histogram graph displays the number of hits per code within the sampled data. This graph is useful for dc analysis and indicates the noise performance of the device.

FFT TAB
The FFT tab displays fast Fourier transform (FFT) information for the last batch of samples gathered (see Figure 22).

When performing an FFT analysis, the RESULTS pane shows the Noise and Distortion performance of the ADAQ4001 or the ADAQ4003. SNR and other noise performance measurements, such as SINAD, Dynamic Range, noise density (Noise / Hz), and SFDR, are shown in the Performance section. The THD measurements, as well as the major harmonics contributing to the THD performance, are shown in the Distortion section.

INL AND DNL TAB
The INL tab (see Figure 23) and DNL tab (see Figure 24) display the linearity analysis. To perform a linearity test, apply a sinusoidal signal with 0.5 dB full scale to the EVAL-ADAQ4001PMDZ or the EVAL-ADAQ4003PMDZ at the J1 and J2 SMB inputs.
Figure 24. DNL Tab
TROUBLESHOOTING

EVALUATION BOARD SOFTWARE TROUBLESHOOTING

To troubleshoot the ACE evaluation software, take the following steps:

1. Install the ACE software before connecting the hardware to the PC (see the Software Installation Procedures section).
2. Restart the PC after the software installation process completes (both the ACE software and SDP-H1 drivers must be installed before the process completes).
3. After connecting the SDP-H1 to the PC, allow the Found New Hardware Wizard to run before starting the ACE software.
4. If the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ does not appear to be functioning, ensure that the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ is connected to the SDP-H1 board and that the SDP-H1 is recognized in the Device Manager window, as shown in Figure 15.
5. If connected to a slower USB port where the SDP-H1 cannot read quickly, a timeout error may result. In this case, do not read continuously or lower the number of samples taken.

HARDWARE TROUBLESHOOTING

To troubleshoot the hardware, take the following steps:

1. Check that the power is applied within the power ranges described in the Setting Up the EVAL-ADAQ4001FMCZ and EVAL-ADAQ4003FMCZ Evaluation Kit section.
2. Using a voltmeter, measure the voltage present at each of the test points: +15 V, −15 V, −VS, and VIN (3.3 V). Note that the LED1 on the SDP-H1 must be lit.
3. Launch the ACE software and read the data. If nothing happens, exit the software.
4. Power down the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ and relaunch the ACE software.
5. When no data is read back, confirm that the EVAL-ADAQ4001FMCZ/EVAL-ADAQ4003FMCZ is connected to the SDP-H1 and that the SDP-H1 is recognized in the Device Manager, as shown in Figure 15.
6. When the user is working with the software in standalone or offline mode (no hardware connected) and later chooses to connect hardware, close and relaunch the software.
EVALUATION BOARD SCHEMATICS AND SILKSCREENS

EVAL-ADAQ4001PMDZ AND EVAL-ADAQ4003PMDZ

Figure 25. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ Power Supplies and Voltage Reference
Figure 26. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ µModule and Signal Conditioning
EVALUATION BOARD SCHEMATICS AND SILKSCREENS

Figure 27. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ Silkscreen, Top Layer

Figure 28. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ, Layer 1

Figure 29. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ, Layer 2
EVALUATION BOARD SCHEMATICS AND SILKSCREENS

Figure 30. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ, Layer 3 GND

Figure 31. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ, Layer 4 Secondary
EVALUATION BOARD SCHEMATICS AND SILKSCREENS

EVAL-PMD-IB1Z

Figure 32. EVAL-PMD-IB1Z Interposer Schematic Diagram
Figure 33. EVAL-PMD-IB1Z, Top Layer
Figure 34. EVAL-PMD-IB1Z Silkscreen, Primary
Figure 35. EVAL-PMD-IB1Z Silkscreen, Secondary
Figure 36. EVAL-PMD-IB1Z, Secondary
## BILL OF MATERIALS

**Table 4. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ Bill of Materials**

<table>
<thead>
<tr>
<th>Qty.</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Manufacturing</th>
<th>Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>+15.5 V, −15.5 V, −VS, GND, VIN</td>
<td>Connector printed circuit board (PCB) test points, white</td>
<td>Components Corporation</td>
<td>TP-104-01-09</td>
</tr>
<tr>
<td>2</td>
<td>C1, C7</td>
<td>22 µF ceramic capacitors, X5R, general-purpose</td>
<td>Murata</td>
<td>GRM188R61A226ME15D</td>
</tr>
<tr>
<td>1</td>
<td>C10</td>
<td>0.022 µF ceramic capacitor, X7R, general-purpose</td>
<td>TDK Corporation</td>
<td>CGA2B3X7R1H223K</td>
</tr>
<tr>
<td>1</td>
<td>C11</td>
<td>0.039 µF ceramic capacitor, X7R, 0402</td>
<td>AVX</td>
<td>0402ZC393JAT2A</td>
</tr>
<tr>
<td>2</td>
<td>C2, C12</td>
<td>1 µF ceramic capacitors, X7R, general-purpose</td>
<td>Samsung</td>
<td>CL10B105KP8NNNC</td>
</tr>
<tr>
<td>4</td>
<td>C14, C15, C20, C21</td>
<td>10 µF ceramic capacitors, X5R, general-purpose</td>
<td>Murata</td>
<td>GRM218R61E106KA73L</td>
</tr>
<tr>
<td>4</td>
<td>C8, C16, C24, C25</td>
<td>4.7 µF multilayer ceramic capacitors, X7R</td>
<td>TDK Corporation</td>
<td>C2012X7R1E475K125AB</td>
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<tr>
<td>2</td>
<td>C6, C18</td>
<td>0.1 µF ceramic capacitors, X7R, 0603</td>
<td>AVX</td>
<td>06035C104KAT2A</td>
</tr>
<tr>
<td>4</td>
<td>C19, C23, C27, C28</td>
<td>0.01 µF ceramic capacitors, X7R, general-purpose</td>
<td>KEMET</td>
<td>C0402C103J3RACTU</td>
</tr>
<tr>
<td>1</td>
<td>C4, C9</td>
<td>1 µF ceramic capacitors, X7R, general-purpose</td>
<td>Murata</td>
<td>GCM218R71E105KA56L</td>
</tr>
<tr>
<td>2</td>
<td>C5, C22</td>
<td>2.2 µF ceramic capacitors, X5R, general-purpose</td>
<td>Murata</td>
<td>GRM188R61H225KE11J</td>
</tr>
<tr>
<td>1</td>
<td>C26</td>
<td>1 µF ceramic capacitor, X7R, general-purpose</td>
<td>TDK Corporation</td>
<td>CGA3E1X7R1C105K080AC</td>
</tr>
<tr>
<td>2</td>
<td>C29, C30</td>
<td>2.2 µF ceramic capacitors, X7R, general-purpose</td>
<td>Murata</td>
<td>GRM188R71A225KE15D</td>
</tr>
<tr>
<td>1</td>
<td>C3</td>
<td>10 µF capacitor, 10%, 10 V, X7R, 0805</td>
<td>TDK Corporation</td>
<td>C2012X7R1A106K125AC</td>
</tr>
<tr>
<td>6</td>
<td>C39 to C44</td>
<td>0.1 µF ceramic capacitors, X7R, general-purpose</td>
<td>AVX</td>
<td>04023C104KAT2A</td>
</tr>
<tr>
<td>2</td>
<td>C4, C9</td>
<td>4.7 µF ceramic capacitors, X7R</td>
<td>Murata</td>
<td>GCM218R71E105KA56L</td>
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<tr>
<td>1</td>
<td>C52</td>
<td>0.0033 µF monolithic ceramic capacitor, 0402</td>
<td>Yageo</td>
<td>CC0402KR7R9BB332</td>
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<tr>
<td>1</td>
<td>C53</td>
<td>0.0047 µF ceramic capacitor, X7R, general-purpose</td>
<td>KEMET</td>
<td>C0402C472K5RACTU</td>
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<tr>
<td>2</td>
<td>D1, D2</td>
<td>Schottky diodes, barrier rectifier</td>
<td>Diodes, Inc.</td>
<td>DFLS240-7</td>
</tr>
<tr>
<td>2</td>
<td>E1, E2</td>
<td>Inductor ferrite beads, 0.150 Ω maximum dc resistance, 1 A</td>
<td>TDK Corporation</td>
<td>MPZ1608S601ATA00</td>
</tr>
<tr>
<td>2</td>
<td>J1, J2</td>
<td>0 Hz to 4 GHz, SMB connectors, 50 Ω, solder right angle thru-hole, gold over nickel</td>
<td>Cinch Connectivity Solutions</td>
<td>131-3701-301</td>
</tr>
<tr>
<td>2</td>
<td>L1, L2</td>
<td>22 µH inductors, shielded power</td>
<td>Coilcraft, Inc.</td>
<td>LPS5030-223MRC</td>
</tr>
<tr>
<td>2</td>
<td>L4, L5</td>
<td>680 nH inductors, shielded power</td>
<td>Coilcraft, Inc.</td>
<td>PFL3215-681MEB</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>Connector, unshrouded header, 12 position, 2.54 mm, solder right angle thru-hole, bulk</td>
<td>Samtec, Inc.</td>
<td>TSW-106-25-F-D-RA</td>
</tr>
<tr>
<td>1</td>
<td>R10</td>
<td>100 kΩ resistor, precision thick film chip</td>
<td>Panasonic</td>
<td>ERA-2AB104X</td>
</tr>
<tr>
<td>1</td>
<td>R11</td>
<td>80.6 kΩ resistor, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RF8062X</td>
</tr>
<tr>
<td>1</td>
<td>R12</td>
<td>2.7 kΩ resistor, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RF2701X</td>
</tr>
<tr>
<td>1</td>
<td>R13</td>
<td>54.9 kΩ resistor, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RFK5492X</td>
</tr>
<tr>
<td>2</td>
<td>R14, R15</td>
<td>11.5 Ω resistors, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RF11R5X</td>
</tr>
</tbody>
</table>
### Table 4. EVAL-ADAQ4001PMDZ and EVAL-ADAQ4003PMDZ Bill of Materials

<table>
<thead>
<tr>
<th>Qty.</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Manufacturing</th>
<th>Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R6</td>
<td>60.4 kΩ resistor, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RKF6042X</td>
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<tr>
<td>3</td>
<td>R8, R17, R31</td>
<td>698 kΩ resistors, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RKF6983X</td>
</tr>
<tr>
<td>2</td>
<td>R18, R21</td>
<td>61.9 kΩ resistors, precision thick film chip</td>
<td>Yageo</td>
<td>RC0402FR-0761K9L</td>
</tr>
<tr>
<td>4</td>
<td>R2 to R5</td>
<td>42.2 kΩ resistors, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RKF4222X</td>
</tr>
<tr>
<td>5</td>
<td>R6, R20, R22, R24, R25</td>
<td>0 Ω film resistors, surface-mount device (SMD), 0603</td>
<td>Panasonic</td>
<td>ERJ-3GEY0R00V</td>
</tr>
<tr>
<td>24</td>
<td>R7, R23, R26 to R30, R35 to R37, R40, R43 to R48, R51 to R55, R57, R60</td>
<td>0 Ω film resistors, SMD, 0402, jumper short</td>
<td>Panasonic</td>
<td>ERJ-2GE0R00X</td>
</tr>
<tr>
<td>2</td>
<td>R32, R34</td>
<td>200 kΩ resistors, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RKF2003X</td>
</tr>
<tr>
<td>1</td>
<td>R33</td>
<td>95.3 kΩ resistor, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RKF9532X</td>
</tr>
<tr>
<td>1</td>
<td>R9</td>
<td>3.3 kΩ resistor, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RKF3301X</td>
</tr>
<tr>
<td>1</td>
<td>RN1</td>
<td>Resistor network quad matched</td>
<td>Analog Devices, Inc.</td>
<td>LT5400BHMS8E-4#PBF</td>
</tr>
<tr>
<td>1</td>
<td>U1</td>
<td>Ultralow noise, high accuracy, 5.0 V voltage reference</td>
<td>Analog Devices</td>
<td>AD84550BRZ</td>
</tr>
<tr>
<td>1</td>
<td>U2</td>
<td>Dual positive and negative low noise low dropout (LDO) regulator</td>
<td>Analog Devices</td>
<td>LT3032IDE#PBF</td>
</tr>
<tr>
<td>1</td>
<td>U3</td>
<td>1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs</td>
<td>Analog Devices</td>
<td>ADP5070ACPZ-R7</td>
</tr>
<tr>
<td>2</td>
<td>U4, U7</td>
<td>High voltage, low noise, low distortion, unity-gain stable, high speed op amps</td>
<td>Analog Devices</td>
<td>ADA4898-1YRDZ</td>
</tr>
<tr>
<td>1</td>
<td>U5</td>
<td>16-bit/18-bit, 2 MSPS, µModule data acquisition solution in ball grid array</td>
<td>Analog Devices</td>
<td>ADAQ4001/ADAQ4003</td>
</tr>
<tr>
<td>1</td>
<td>U6</td>
<td>Low dropout, low noise regulator</td>
<td>Analog Devices</td>
<td>LT3023ID#PBF</td>
</tr>
<tr>
<td>1</td>
<td>A1</td>
<td>Programmable gain drift instrument amplifier</td>
<td>Analog Devices</td>
<td>AD8251ARMZ</td>
</tr>
</tbody>
</table>
ORDERING INFORMATION

Table 5. EVAL-PMD-812 Bill of Materials

<table>
<thead>
<tr>
<th>Qty</th>
<th>Reference Designator</th>
<th>Description</th>
<th>Manufacturing</th>
<th>Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>+12 V, 3P3V, 3V3AUX</td>
<td>Connector PCB test points, red</td>
<td>Keystone Electronics</td>
<td>5000</td>
</tr>
<tr>
<td>1</td>
<td>C1</td>
<td>0.1 µF ceramic capacitor, X7R</td>
<td>AVX</td>
<td>0603SC0104KAT2A</td>
</tr>
<tr>
<td>1</td>
<td>DS1</td>
<td>LED, green, clear</td>
<td>Fairchild</td>
<td>QLTP600C4TR</td>
</tr>
<tr>
<td>1</td>
<td>J1</td>
<td>Connector, PCB, straight, Subminiature Version A (SMA)</td>
<td>TE Connectivity Ltd</td>
<td>5-181432-1</td>
</tr>
<tr>
<td>3</td>
<td>P1 to P3</td>
<td>Connector headers, female, 12 position, right angle, gold, 2.34 mm pitch</td>
<td>Sullins</td>
<td>PPC062LJBN-RC</td>
</tr>
<tr>
<td>1</td>
<td>P2</td>
<td>FMA connector, single-ended array, male, 160 position</td>
<td>Samtec</td>
<td>ASP-134604-01</td>
</tr>
<tr>
<td>25</td>
<td>R1 to R25, R59</td>
<td>0.2 film resistors, SMD, 0603</td>
<td>Panasonic</td>
<td>ERJ-2RKF2003X</td>
</tr>
<tr>
<td>1</td>
<td>R26</td>
<td>2.4 kΩ resistor, precision thick film chip</td>
<td>Panasonic</td>
<td>ERJ-2RKFR4X</td>
</tr>
<tr>
<td>1</td>
<td>U1</td>
<td>2 Kb serial I²C bus electronically erasable programmable read-only memory (EEPROM)</td>
<td>ST Microelectronics</td>
<td>M24C02-WMN6TP</td>
</tr>
</tbody>
</table>

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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