Evaluating the AD9954 400MSPS, 14-Bit, 1.8V CMOS, Direct Digital Synthesizer

FEATURES

- Full-featured evaluation board for the AD9954
- PC evaluation software for control and measurement of the AD9954
- USB interface
- GUI software with frequency sweep capability for board control and data analysis
- Factory tested and ready to use

EVALUATION KIT CONTENTS

- AD9954/PCBZ-SDP-K1 evaluation board

ADDITIONAL HARDWARE

- Analog Devices, Inc., EVAL-SDP-CK1Z (SDP-K1) controller board that must be purchased separately

SOFTWARE NEEDED

- Analog Devices Analysis | Control | Evaluation (ACE) Software

EVALUATION BOARD PHOTOGRAPH

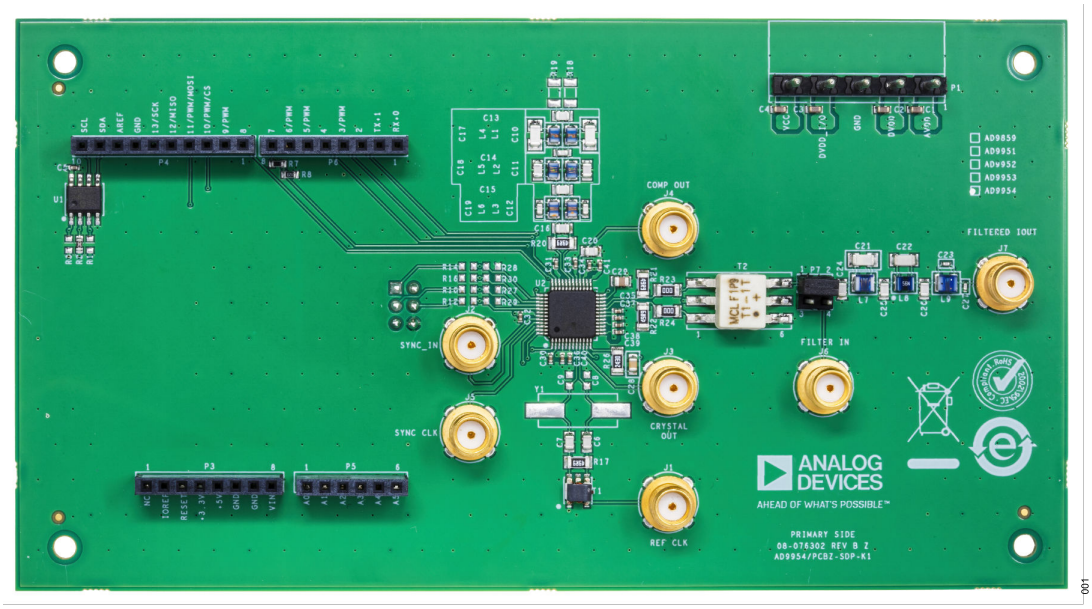

Figure 1. AD9954/PCBZ-SDP-K1 Evaluation Board Photograph

GENERAL DESCRIPTION

This user guide takes users through the setup and use of the AD9954/PCBZ-SDP-K1 evaluation board. The AD9954 is a direct digital synthesizer (DDS) that uses advanced technology, coupled with an internal high-speed, high-performance digital-to-analog converter (DAC) to form a complete, digitally programmable, high-frequency synthesizer capable of generating a frequency agile, analog output, sinusoidal waveform at up to 160MHz with many user-programmable functions.

The Analog Devices, Inc., **Analysis | Control | Evaluation (ACE) Software** provides a graphical user interface (GUI) for simple communication with the AD9954. The AD9954/PCBZ-SDP-K1 requires the use of an SDP-K1 controller board, which is not supplied with the evaluation board kit and must be purchased separately. The SDP-K1 controller board, along with the use of the **ACE Software**, allows users the ability to program the software.

For full details on the AD9954, see the AD9954 data sheet, which must be consulted in conjunction with this user guide when using the AD9954/PCBZ-SDP-K1.

TABLE OF CONTENTS

REVISION HISTORY

3/2026—Revision 0: Initial Version

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURE

To install the **ACE Software** AD9954 plug-in, take the following steps:

1. Install the latest version of the **ACE Software** platform from the Analysis | Control | Evaluation (ACE) Software web page.
2. Scroll to the **ACE Evaluation Board Plug-ins** selection of the ACE web page.
3. In the search bar within the **ACE Evaluation Board Plug-ins** section of the **ACE Software** web page, search for the AD9954 and install the chip and board plug-ins that appear.
4. Ensure that the AD9954 plug-ins appear when the AD9954/PCBZ-SDP-K1 board is attached through the SDP-K1 connector board to the PC.

EVALUATION BOARD SETUP PROCEDURE

Once the **ACE Software** has been successfully installed onto your PC, the next step is to interface the AD9954 evaluation software to the AD9954 evaluation board via the SDP-K1.

To power-up the AD9954/PCBZ-SDP-K1, perform the following steps:

1. Set the Channel 1 voltage of the power supply to 1.8V and the current limit to 1A, and set the Channel 2 voltage of the power supply to 3.3V and the current limit to 1A.
2. Exercise caution during this procedure because all equipment must be turned off. When moving to an on state, note that the following power-up sequence must be followed:
   a. Turn on the power supply.
   b. Turn on the signal generator.
   c. Connect the SDP-K1 controller board to the PC.
   d. Configure the AD9954 with the **ACE Software**.

To run the **ACE Software**, take the following steps

1. Select **Start/All Programs/Analog Devices/ACE**.
2. Under the **Select Device and Connection** tab within the **ACE Software**, select the **AD9954 Board** that appears within the **Attached Hardware** section.
3. When connecting the AD9954/PCBZ-SDP-K1, allow between 5 seconds to 10 seconds for the **Status** bar to turn green.

EVALUATION BOARD HARDWARE

REQUIREMENTS

To successfully use the AD9954/PCBZ-SDP-K1 evaluation board and run the **ACE Software**, the following requirements must be met:

- A Windows®-based PC with a USB port for the AD9954 evaluation software (**ACE Software**).
- A signal generator capable of generating sinusoidal waves at least 3dBm power, up to at least 10MHz.
- A system demonstration platform, serial only EVAL-SDP-CK1Z controller board (SDP-K).
- A power supply that has the capability to generate at least two independent DC voltages (1.8V and 3.3V).
- An appropriate measurement device, such as a spectrum analyzer or a high bandwidth oscilloscope.
- A USB-C cable and Subminiature Version A (SMA)-to-x cables (x = SMA or BNC), depending on the connector of the device interfacing with the AD9954/PCBZ-SDP-K1.

SETTING UP THE EVALUATION BOARD

Powering the AD9954/PCBZ-SDP-K1

The AD9954/PCBZ-SDP-K1 has one power supply connector: P1. P1 powers the DDS, PC interface logic, and USB circuitry. Table 1 details the necessary connections and the appropriate biasing voltage, and Figure 2 shows the AD9954/PCBZ-SDP-K1 setup diagram.

Table 1. Connections and Biasing Voltage

Connector	Pin No.	Label	Voltage (V)
P1	1	AVDD	1.8
P1	2	DVDD	1.8
P1	3	GND	0
P1	4	DVDD_I/O	3.3
P1	5	VCC	3.3

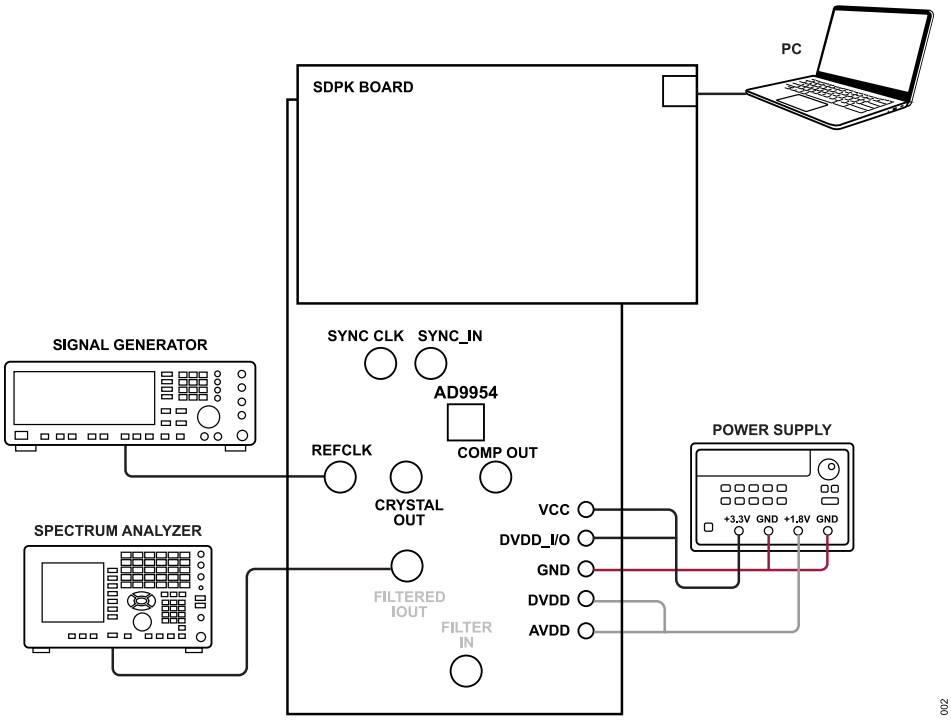

Figure 2. Evaluation Board Setup Diagram

EVALUATION BOARD HARDWARE

Clocking the AD9954

The AD9954 architecture provides the user with two options for providing an input signal to the AD9954. Figure 1 shows that users can clock the frequency synthesizer/DDS directly by connecting an external clocking signal to the REF CLK connector, J1, or by using an external crystal. If a user wants to use an external crystal as the clocking source, install the crystal at Y1 (see Figure 7).

Refer to the AD9954 data sheet for details on the maximum input speeds and input sensitivities of these two inputs.

EVALUATION BOARD LAYOUT

Manual Input and Output Control Headers

The manual input and output control headers provide interfaces for communicating with the AD9954 when the device is being controlled by an external controller (manual control).

Multidevice Synchronous Control

These control connections set up the AD9954 for multidevice synchronous operation.

DAC Channels

These DAC channel connections are the DAC filtered and unfiltered output and AVDD power supplies.

Clock Input Supply

The clock input supply powers the clock input circuitry of the AD9954.

Reference Clock Input

The reference clock input is the input for the external REF CLK signal.

Power Supply

The power supply powers the USB circuitry, input and output circuitry, digital portion (DVDD), and analog portion (AVDD) of the AD9954 DAC.

USB Port

When the AD9954 is under PC control, which is the default mode, the AD9954/PCBZ-SDP-K1 communicates with the AD9954 via this port.

EVALUATION BOARD SOFTWARE

The **ACE Software** is the main platform that is used to control the AD9954/PCBZ-SDP-K1. The AD9954 plug-in uses interfaces that connect to the AD9954 and to evaluate the device. Use the following steps to open the main control window of the **ACE Software**:

1. Launch the **ACE Software**. When the SDP-K controller board is connected to the AD9954/PCBZ-SDP-K1, the **Attached Hardware** section appears in the **ACE Software** GUI, as shown in Figure 3.
2. Double-click the **AD9954 Board** icon and the tab shown in the Figure 4 then appears.
3. Double-click the **AD9954** icon that appears on the board GUI to open the main control window shown in Figure 5.

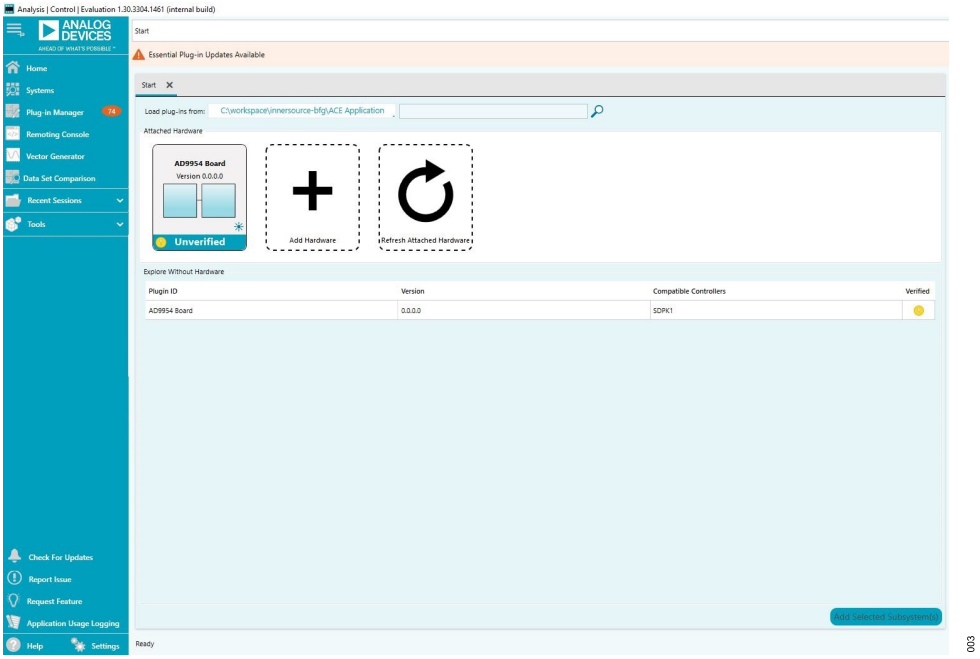

Figure 3. ACE Main Window, Attached Hardware (AD9954 Evaluation Board)

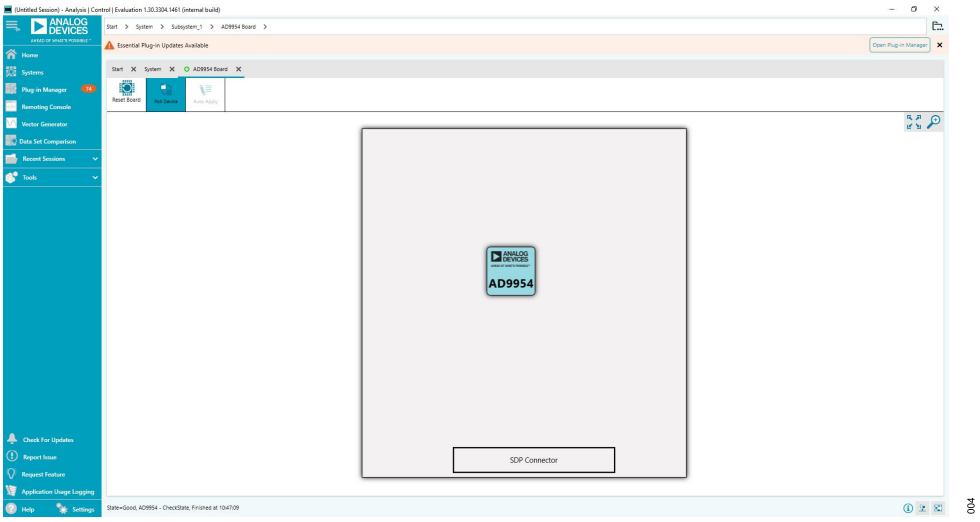

Figure 4. ACE Software AD9954 Evaluation Board Page

EVALUATION BOARD SOFTWARE

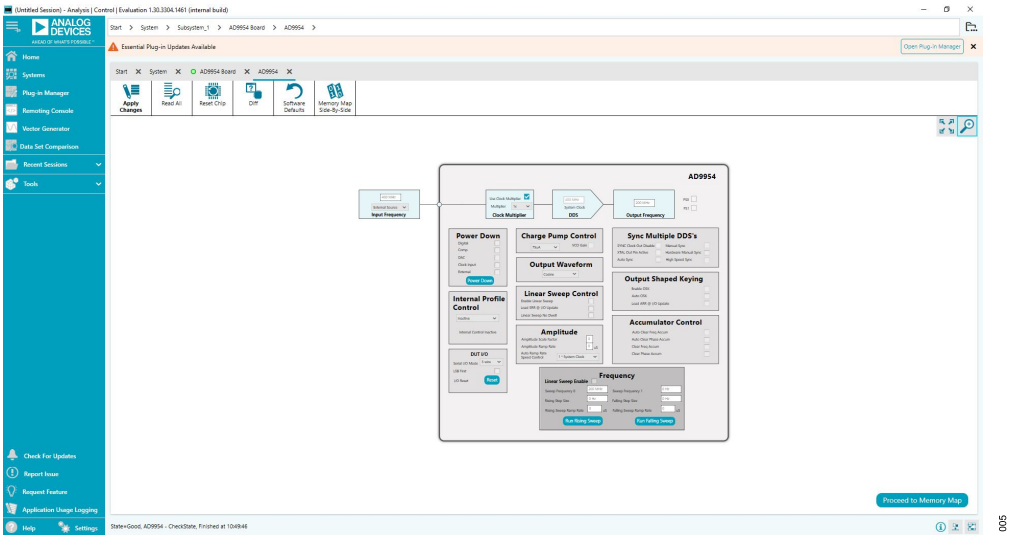

Figure 5. ACE Software Front Panel

MAIN CONTROLS

The main controls are shown in the Figure 5. To modify any controls, take the following steps:

1. Before initializing, all configuration changes must be completed. The ACE Software plug-in opens with a default 400MHz **System Clock** frequency register setting and a 200MHz **Output Frequency** register setting.
2. Modify any **ACE Software** front panel settings as required (see Figure 5).
3. Click **APPLY CHANGES** to load the modified settings to the AD9954, which then performs the write sequence. If the **System Clock** frequency and **Output Frequency** selected are outside of the operational range, an error message will appear within the GUI. Specific blocks can be powered down by setting the corresponding power-down check boxes within the **Power Down** section shown in Figure 5.

FEATURE CONTROL WINDOWS

Input Frequency

The **Input Frequency** section shown in Figure 5 allows users to configure the reference clock.

Note that the input frequency takes control of the input of the operating frequency of the external reference clock or crystal. The maximum reference clock frequency is 400MHz for the AD9954, which is the default setting of this box. If a value is entered that is out of range, an error message will appear.

Clock Multiplier

The **Clock Multiplier** section shown in Figure 5 allows users to select the phase-locked loop (PLL) multiplication factor (4× to 20×) by which to scale the input frequency. The default setting of this dropdown menu is **x1**, indicating that the **Clock Multiplier** circuitry is bypassed and that the input frequency and crystal input are piped directly to the DDS core.

System Clock

The **System Clock** section shown in Figure 5 displays the operating frequency of the DDS core (system). The value within this box is derived from the value entered and selected in the **Input Frequency** section and the **Multiplier** selected in the **Clock Multiplier** section by the user.

Output Frequency

To customize the channel output configuration, go to the **Output Frequency** section shown in Figure 5. By default, the channel output operates in single tone mode.

Power Down

Users can go to the **Power Down** section shown in Figure 5 to power down any of the following:

- Digital logic by checking off the **Digital** box
- Comparator logic by checking off the **Comp** box
- DAC logic by checking off the **DAC** box
- Clock input by checking off the **Clock Input** box
- External logic by checking off the **External** box

EVALUATION BOARD SOFTWARE

Once users select their power-down options, they must click **Power Down**. All of these boxes are unchecked by default, indicating that all of the circuitry of that channel are enabled (powered up).

Charge Pump Control

To control the current settings on the charge pump, go to the Charge Pump Control section shown in Figure 5. The default value of the charge pump current is **75µA**. Other dropdown menu options included the following: **100µA**, **125µA**, or **150µA**.

Output Waveform

In the **Output Waveform** section shown in Figure 5, users can select either a **Cosine** or a **Sine** function for the angle-to-amplitude conversion. The default setting is **Cosine**.

Linear Sweep Control

Use the **Linear Sweep Control** section shown in Figure 5 to control the linear sweep features.

Options included the following:

- Select **Enable Linear Sweep** to turn on the linear sweep function.
- Select **Load SRR @ I/O Update** for the contents of the sweep ramp rate register to be loaded into the sweep ramp rate timer every time an input and output update is sent to the device.
- Select **Linear Sweep No Dwell** to enable this device feature, see the Linear Sweep No Dwell Mode section of the AD9954 data sheet for more information regarding the no dwell feature.

Amplitude

Use the **Amplitude** section in Figure 5 to set the **Amplitude Scale Factor**, **Amplitude Ramp Rate**, and **Auto Ramp Rate Speed Control**.

The **Amplitude Scale Factor** can be set to a maximum of 1 to increment or decrement. The default setting for the **Amplitude Scale Factor** box is 1, and it can be scaled up or down by 0.0006.

Use the **Amplitude Ramp Rate** box to set the amplitude ramp rate (ARR) time. This time (entered in µs) can range from 0.01µs (minimum) to 2.55µs (maximum). If the value entered exceeds the maximum time, an alert will show in the **ACE Software** GUI.

Use the **Auto Ramp Rate Speed Control** dropdown menu to tell the output shaped keying (OSK) block how many amplitude steps to take for each increment or decrement.

Frequency

Use the **Frequency** section of Figure 5 to setup the slope of the linear sweep.

Enter the desired value for the rising step size in the **Rising Step Size** box, and enter the amount of time you want spent at each step in the **Rising Sweep Ramp Rate**.

Enter the desired value for the falling step size in the **Falling Step Size** box, and enter the amount of time you want spent at each step in the **Falling Sweep Ramp Rate** box. The **Rising Step Size** box and **Falling Step Size** box are similar to the profile registers.

The number of steps in a ramp can be calculated by determining the difference between the starting and ending points of the sweep and by dividing this difference by the step size. The time required to sweep is then the number of steps times the amount of time spent at each step.

The range of the **Rising Sweep Ramp Rate** and **Falling Sweep Ramp Rate** is computed similarly to the time range for the **Amplitude Ramp Rate** (see the Amplitude section for additional information). Note that the **Rising Sweep Ramp Rate** box and **Falling Sweep Ramp Rate** box also have an error message feature when the maximum rising and falling step interval values are exceeded.

Sync Multiple DDSs

The SYNC_CLK pin is active by default within the **Sync Multiple DDS's** section of see Figure 5. When the **SYNC Clock Out Disable** feature is enabled (checked off), the SYNC_CLK pin assumes a static Logic 0 state to minimize the noise generated by the digital circuitry. The synchronization circuitry remains active internally to maintain the device timing.

When **XTAL Out PIN Active** is enabled (checked off), the crystal oscillator circuitry output drives the CRYSTAL OUT pin, which can be used as a reference frequency for additional devices.

When **Auto Sync** is enabled (checked off), one device is chosen as a main and the other device(s) is its subordinate. All subordinates automatically synchronize their internal clocks to the SYNC_CLK output signal of the main device. Use automatic synchronization to configure each subordinate. Connect the SYNC_IN input(s) to the main SYNC_CLK output. Subordinate devices continuously update the phase relationship of their SYNC_CLKs until they are in phase with the SYNC_IN inputs. When **Auto Sync** is enabled (checked off), the **High Speed Sync** must be enabled (checked off).

When **Hardware Manual Sync** is enabled (checked off), the user can force the device to advance the SYNC_CLK rising edge one SYSCLK cycle (¼ SYNC_CLK period).

When **Manual Sync** is enabled (checked off)**,** the SYNC_IN input pin is configured such that it advances the rising edge of the SYNC_CLK signal each time the device detects a rising edge on the SYNC_CLK signal and a rising edge on the SYNC_IN pin.

EVALUATION BOARD SOFTWARE

Output Shaped Keying (OSK)

The shaped on-off keying function is enabled or disabled using the **Output Shaped Keying** section shown in Figure 5 by enabling (checking off) **Enable OSK**. The OSK function allows users to control the ramp-up time and ramp-down time when turning the DAC on or off. This function is primarily used in burst transmissions of digital data to reduce the adverse spectral impact of short, abrupt bursts of data.

When **Auto OSK** is enabled (checked off), a single-scale factor is internally generated and applied to the multiplier input for scaling the output of the DDS core block. The scale factor is the output of the 14-bit counter that increments or decrements at a rate determined by the contents of the 8-bit output ramp rate register.

When **Load ARR @ I/O Update** is enabled (checked off), the ramp rate timer is loaded when an input or output update is done, there is a change in the profile input, or a value of 1 is reached. The ramp timer can be loaded before reaching a value of 1 by three methods.

The first method is by toggling the OSK pin, sending a rising edge to the I/O UPDATE pin, or changing the state of a profile pin. For this method, the ASFR value is loaded into the ramp rate timer, which then proceeds to count down as normal.

The second method is if the load ARR control bit (Register CFR1, Bit 26) is set and an I/O update (or change in profile) is issued (see the AD9954 data sheet for additional information.

The last method is by setting the sweep enable bit (Register CFR1, Bit 21). This switches the bit from inactive autoshaped on-off keying mode to active autoshaped on-off keying mode (see the AD9954 data sheet for additional information.

Accumulator Control

In the **Accumulator Control** section of Figure 5, the following options are available:

- Select **Clear Phase Accum** to clear the phase accumulator memory and maintain it in a cleared state.
- Select **Auto Clear Phase Accum** to automatically and synchronously clear the phase accumulator for one clock cycle upon receiving an input and output update signal.
- Select **Clear Freq Accum** to clear the frequency accumulator memory elements and hold them in a cleared state.
- Select **Auto Clear Freq Accum** to automatically and synchronously clear the frequency accumulator for one clock cycle upon receiving an input and output update signal.

DUT I/O

The **DUT I/O** section shown in Figure 5 controls the I/O configuration for the device. Click the **Reset** button of the **I/O Reset** to send an I/O reset to the corresponding serial port state machine. Select the **LSB First** box to change the data format to LSB first from the default setting of MSB first. Use the **Serial I/O Mode** dropdown menu to select the desired I/O mode of operation: **2 wire** or **3 wire** (default).

EVALUATION BOARD SCHEMATICS AND ARTWORK

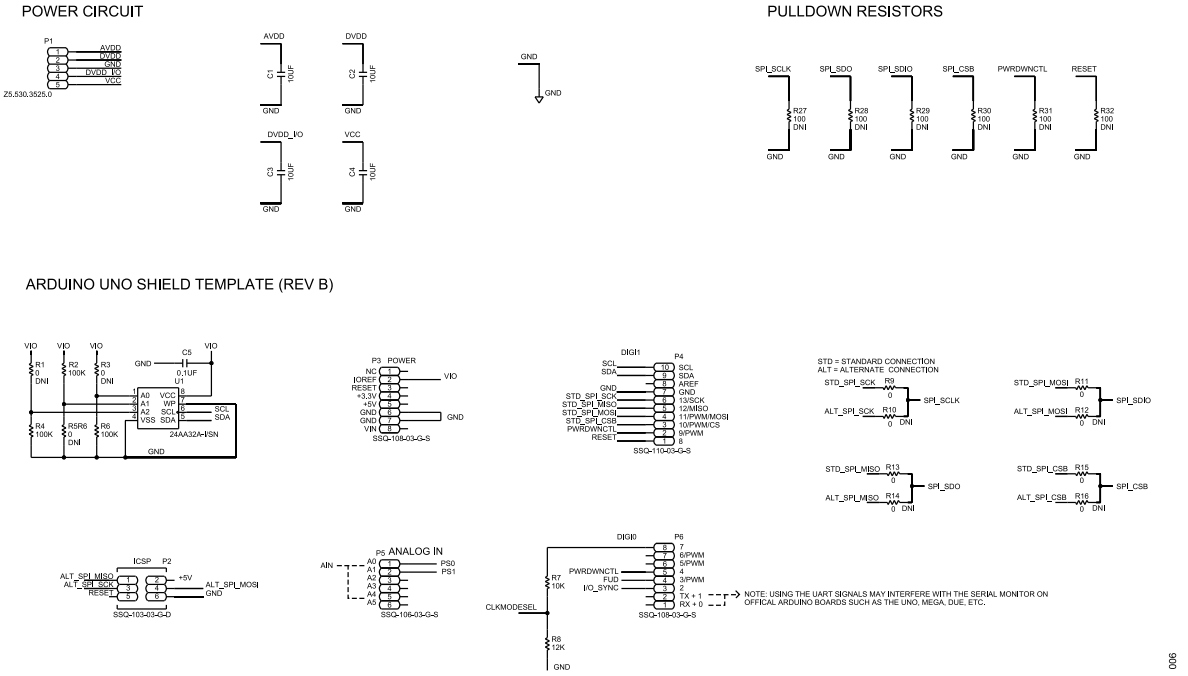

Figure 6. AD9954/PCBZ-SDP-K1 Schematic, Page 2

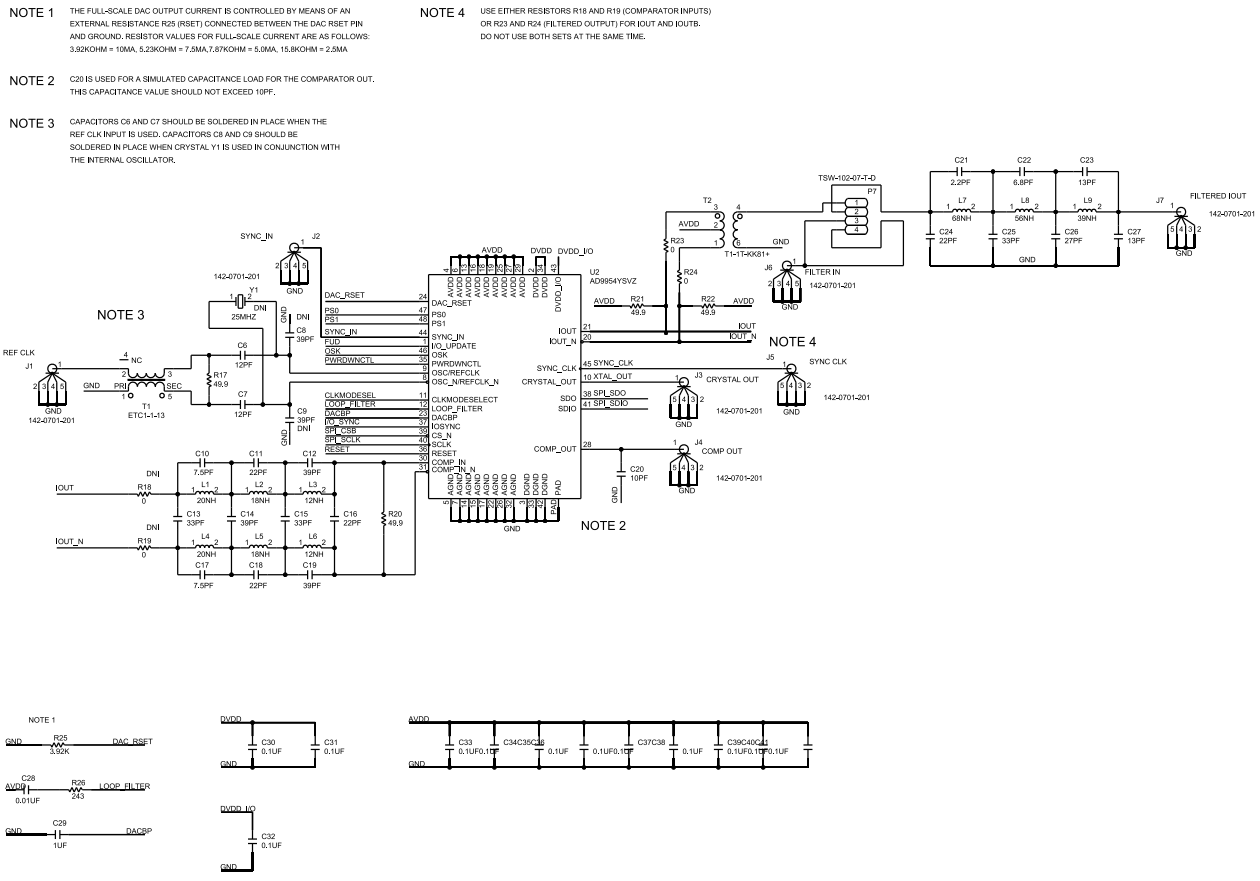

Figure 7. AD9954/PCBZ-SDP-K1 Schematic, Page 3

EVALUATION BOARD SCHEMATICS AND ARTWORK

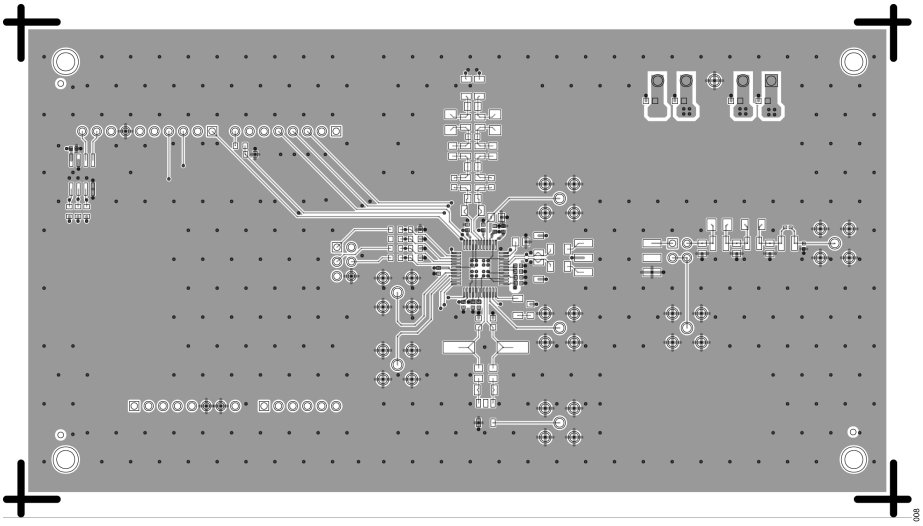

Figure 8. AD9954/PCBZ-SDP-K1 Schematic, Primary

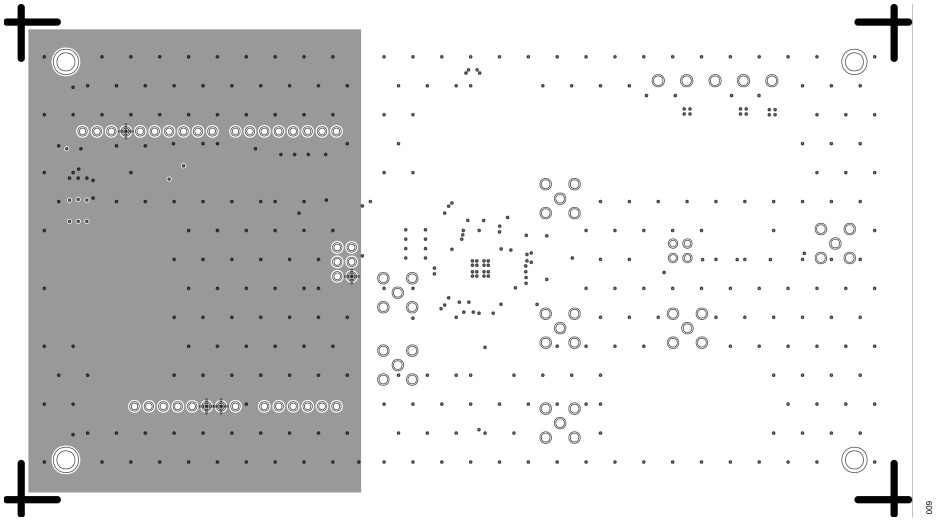

Figure 9. AD9954/PCBZ-SDP-K1 Schematic, Ground

EVALUATION BOARD SCHEMATICS AND ARTWORK

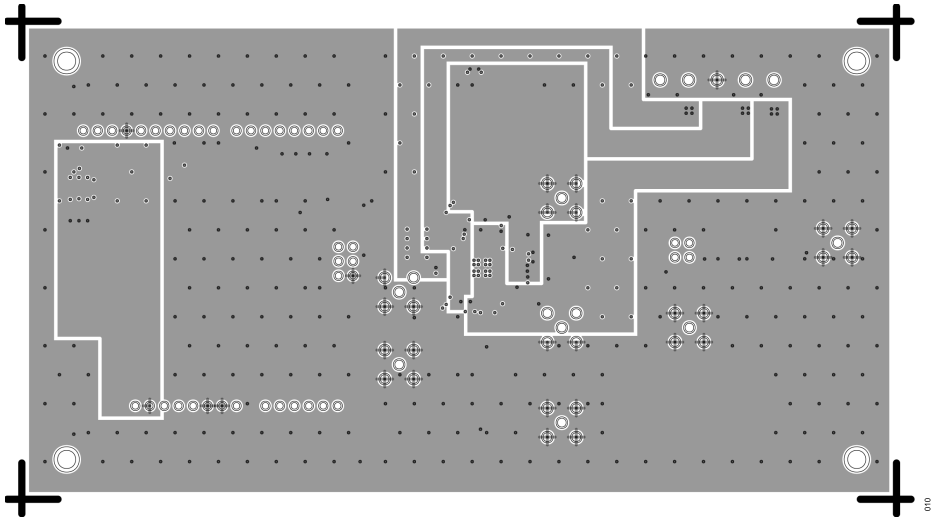

Figure 10. AD9954/PCBZ-SDP-K1 Schematic, Power

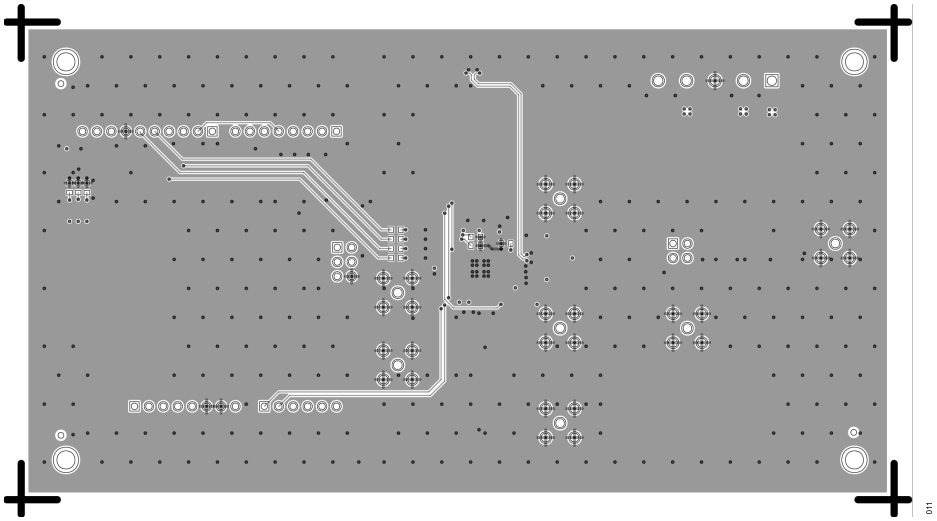

Figure 11. AD9954/PCBZ-SDP-K1 Schematic, Secondary

EVALUATION BOARD SCHEMATICS AND ARTWORK

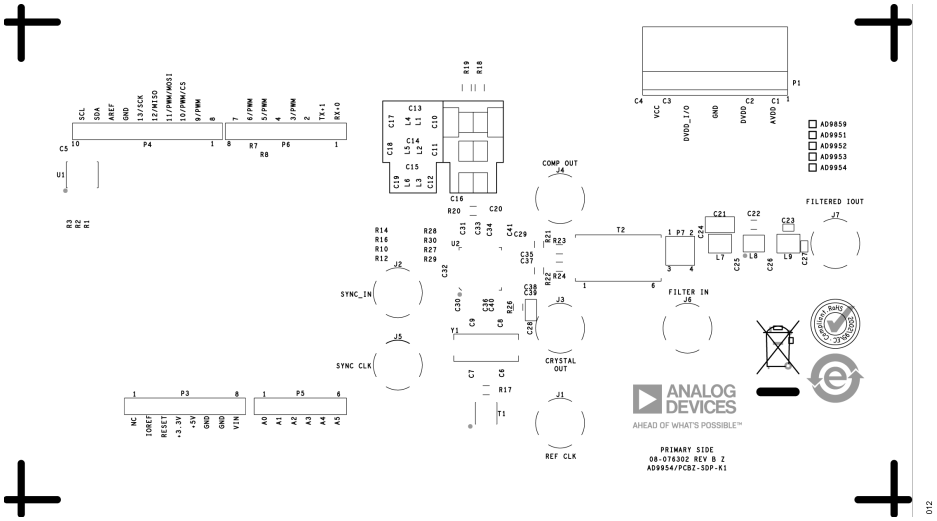

Figure 12. AD9954/PCBZ-SDP-K1 Schematic, Top Side Silkscreen

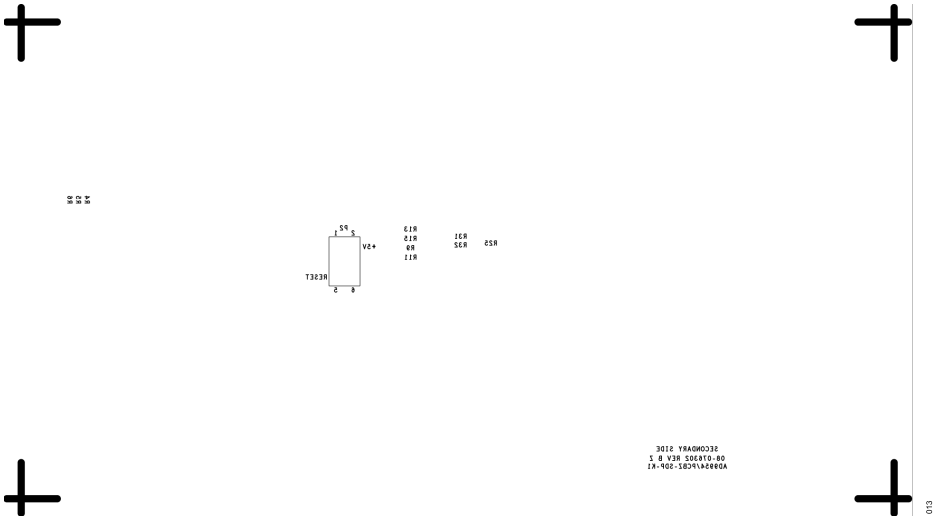

Figure 13. AD9954/PCBZ-SDP-K1 Schematic, Bottom Side Silkscreen

ORDERING INFORMATION

EVALUATION BOARDS

Table 2. Evaluation Boards

Model	Description
AD9954/PCBZ-SDP-K1	Evaluation Board

BILL OF MATERIALS

Table 3. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C1, C2, C3, C4	Ceramic capacitors, 10µF, 35V, 20%, X5R, 0603	Murata	GRM188R6YA106MA73D
C10, C17	Ceramic capacitors, 7.5pF, 50V, 0.5pF, C0G, 1206, extreme low, effective series resistance (ESR)	KEMET	C1206C759D5GACTU
C11, C16, C18, C24	Ceramic capacitors, 22pF, 50V, 5%, C0G, 0805, extreme low, ESR	KEMET	C0805C220J5GACTU
C12, C14, C19	Ceramic capacitors, 39pF, 50V, 5%, C0G, 0603	AVX Corporation	06035A390JAT2A
C13, C15, C25	Ceramic capacitors, 33pF, 50V, 5%, C0G, 0805, extreme low, ESR	KEMET	C0805C330J5GACTU
C20	Ceramic capacitor, 10pF, 50V, 0.5pF, C0G, 0805, extreme low, ESR	KEMET	C0805C100D5GACTU
C21	Ceramic capacitor, 2.2pF, 50V, 0.25pF, C0G, 1206	Yageo	CC1206CRNPO9BN2R2
C22	Ceramic capacitor, 6.8pF, 50V, 0.25pF, C0G, 1206	AVX	12065A6R8CAT2A
C23, C27	Ceramic capacitors, 13pF, 50V, 5%, C0G, 0402, extreme low, ESR	KEMET	C0402C130J5GACTU
C26	Ceramic capacitor, 27pF, 50V, 5%, C0G, 0805	Yageo	CC0805JRNPO9BN270
C28	Ceramic capacitor, 0.01µF, 100V, 5%, X7R, 0805	AVX Corporation	08051C103JAT2A
C29	Ceramic capacitor, 1µF, 100V, 10%, X7R, 0805, AEC-Q200	Kyocera	08051C105K4T2A
C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41	Ceramic capacitors, 0.1µF, 16V, 10%, X7R, 0402	Samsung	CL05B104KO5NNNC
C5	Ceramic capacitor, 0.1µF, 16V, 10%, X7R, 0402, AEC-Q200	Murata	GCM155R71C104KA55D
C6, C7	Ceramic capacitors, 12pF, 50V, 5%, C0G, 0805, extreme low, ESR	KEMET	C0805C120J5GACTU
J1, J2, J3, J4, J5, J6, J7	Connector, PCB, coax Subminiature Version A (SMA) straight	Cinch Connectivity Solutions	142-0701-201
L1, L4	Inductors, wire wound, chip, 0.055Ω DCR, 1.4A	Coilcraft Inc.	0805HQ-20NXJLB
L2, L5	Inductors, wire wound, chip, 0.06Ω DCR, 1.4A	Coilcraft Inc.	0805HQ-18NXJLB
L3, L6	Inductors, wire wound, chip, 0.045Ω, DCR, 1.6A	Coilcraft Inc.	0805HQ-12NXJLB
L7	Inductor, wire wound, chip, 0.13Ω DCR, 1.1A	Coilcraft Inc.	1008HQ-68NXGLB
L8	Inductor, surface-mounted device (SMD), 1008	Wurth Elektronik Group	744762156A
L9	Inductor, wire wound, chip, 0.09Ω DCR, 1.3A	Coilcraft Inc.	1008HQ-39NXGLB
P1	Connector, PCB, header, terminal, strip, 5.0mm pitch, 1× M026826	Wieland Electric	Z5.530.3525.0
P2	Connector, PCB, receptacle 25mil square, post, dual-row 2.54mm pitch	Samtec	SSQ-103-03-G-D
P3, P6	Connectors, PCB, receptacle 25mil square, post, 2.54mm pitch	Samtec	SSQ-108-03-G-S
P4	Connector, PCB, receptacle 25mil square, post, 2.54mm pitch	Samtec	SSQ-110-03-G-S
P5	Connector, PCB, receptacle 25mil square, post, 2.54mm pitch	Samtec	SSQ-106-03-G-S
P7	Connector, PCB, 4 position male header, unshrouded header, double row straight, 2.54mm pitch, 5.84mm post height, 2.54mm solder tail	Samtec Inc.	TSW-102-07-T-D
R9, R11, R13, R15	Resistors, SMD, 0Ω, jumper, 1/10W, 0603, AEC-Q200	Panasonic	ERJ-3GEY0R00V
R17, R20, R21, R22	Resistors, SMD, 49.9Ω, 1%, 1/4W, 1206, AEC-Q200	Panasonic	ERJ-8ENF49R9V
R2, R4, R6	Resistors, SMD, 100kΩ, 1%, 1/16W, 0603	Multicomp (SPC)	MC 0.063W 0603 1% 100K
R23, R24	Resistors, SMD, 0Ω jumper, 1/4W, 1206, AEC-Q200	Panasonic	ERJ-8GEY0R00V
R25	Resistor, SMD, 3.92kΩ, 1%, 1/10W, 0603 AEC-Q200	Panasonic	ERJ-3EKF3921V
R26	Resistor, SMD, 243Ω, 1%, 1/4W, 1206, AEC-Q200	Panasonic	ERJ-8ENF2430V
R7	Resistor, SMD, 10kΩ, 1%, 1/10W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1002V
R8	Resistor, SMD, 12kΩ, 0.1%, 1/10W, 0603, AEC-Q200, high reliability	Panasonic	ERA-3AEB123V

ORDERING INFORMATION

Table 3. Bill of Materials (Continued)

Reference Designator	Description	Manufacturer	Part Number
T1	Transformer (XFMR) RF, 1:1 transmission line, 4.5MHz to 3000MHz	Macom Technology Solutions	ETC1-1-13
T2	XFMR RF	Mini Circuits	T1-1T-KK81+
U1	IC, 32-KBIT serial, electrically erasable programmable read-only memory (EEPROM)	Microchip Technology	24AA32A-I/SN
U2	IC, 400MSPS, 14-bit, 1.8V complementary metal-oxide semiconductor (CMOS), direct digital synthesizer	Analog Devices	AD9954YSVZ