Quick Start Guide for Evaluating the AD9217 12-Bit, 6GSPS/10.25GSPS, RF ADC with the Customer Evaluation Board Using the ADS8-V1EBZ FPGA-Based Capture Board

FEATURES

- Full-featured evaluation board for the AD9217
- On-board power supplies
- On-board clocking and external clocking capabilities
- PC control in conjunction with the system demonstration platform (ADS8-V1EBZ)
- PC software for control and data analysis

EQUIPMENT NEEDED

- Signal generators
- PC running Windows
- USB port and cable to connect to a PC
- AD9217-10GEBZ-B evaluation board
- ADS8-V1EBZ FPGA-based data capture board with a power supply

DOCUMENTS NEEDED

- AD9217 data sheet
- ADS8-V1EBZ user guide

SOFTWARE NEEDED

- Analysis | Control | Evaluation (ACE) Software

GENERAL DESCRIPTION

The AD9217-10GEBZ-B is a full-featured evaluation platform for the AD9217 high-speed analog-to-digital converter (ADC). The evaluation board connects to the ADS8-V1EBZ field-programmable gate array (FPGA) carrier board through a FPGA mezzanine card (FMC) interface, while the ADS8-V1EBZ provides communication to a host PC via a USB for device configuration, data capture, and performance evaluation.

The **ACE Software** provides comprehensive dynamic performance analysis of the AD9217 ADC, including time-domain waveform capture and frequency-domain, fast Fourier transform (FFT) analysis. The software also enables configuration of device operating parameters and data processing settings, including adjustment of the ADC sampling frequency through either the on-board clock generation circuitry or an external clock source.

On-board clocking components include the HMC7044 high-performance jitter attenuator and clock distribution device and the ADF4371 wideband, microwave phased-loop loop (PLL) with an integrated voltage-controlled oscillator (VCO). The HMC7044 generates and distributes the low-jitter clock required for ADC sampling, while the ADF4371 synthesizes the high-frequency sampling clock used by the ADC and FPGA clocking system. Together, these devices provide the low phase noise and deterministic timing required for high-speed data converter operation.

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REVISION HISTORY

8/2026—Revision A: Initial Version

EVALUATION BOARD TYPICAL SETUP

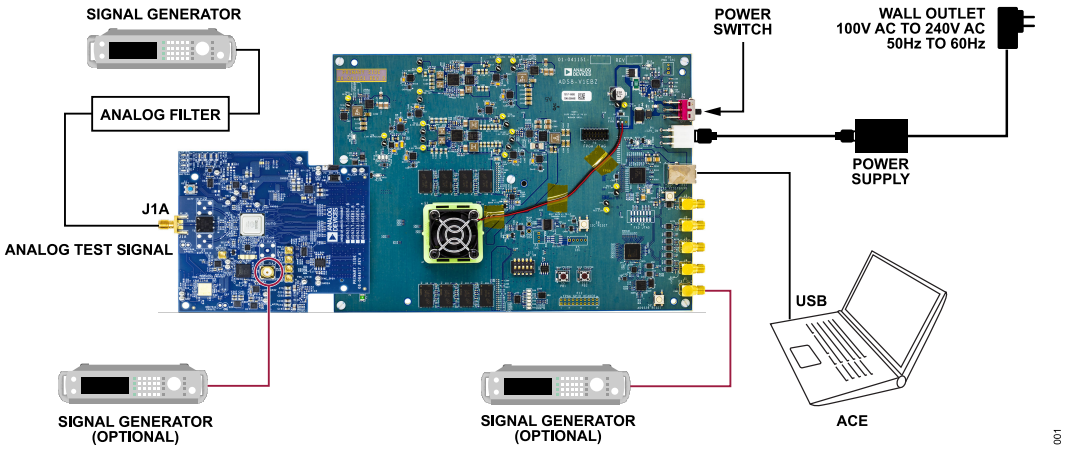

Figure 1. Evaluation Board and ADS8-V1EBZ Data Capture Board, Default Configuration with External Clocks

EVALUATION BOARD HARDWARE

CONFIGURATION FOR THE EXTERNAL CLOCKS AND LOWER FREQUENCIES

The AD9217 is able to be configured for on-board clocking or external clocking. By default, the AD9217-10GEBZ-B uses the on-board clock that ranges from 10GHz to 8GHz.

Take the following steps to enable the external clock on the AD9217-10GEBZ-B:

- Remove the C78 and C79 capacitors and populate the C6 and C18 capacitors.
- For on-board clocking frequencies lower than 8GHz, relocate the C78 and C79 capacitors to the where the C6 and C18 are placed, respectively. In addition, move the C12 and C13 capacitors to where the C14 and C15 are placed and mount C87 and C88 with 0201, 22nF capacitors.

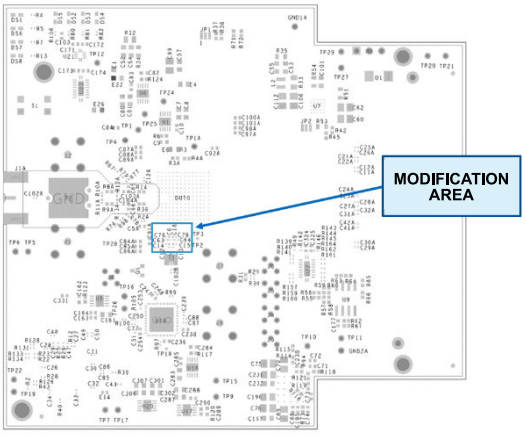

Figure 2. External Clocking Modification Area

- Figure 3 displays a zoomed in view of the clocking capacitors. Note that the capacitors outlined in orange, C78 and C79, are for on-board clocking, and the capacitors outlined in blue, C6 and C18, are for external clocking. In addition, although these capacitors are all the same package size, note that, the on-board clocking capacitors are 1nF capacitors, and the external clocking capacitors are 10nF capacitors.

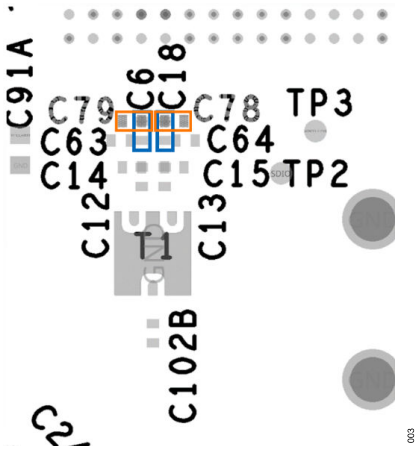

Figure 3. Clocking Capacitors View

- Figure 4 shows the on-board clock changes required to operate a clock frequency of less than 8GHz. The mounted C79 and C78 capacitors must be moved to where the C6 and C18 capacitors are, and the C12 and C13 capacitors must be moved to where the C14 and C15 are. Additionally, C87 and C88 must be mounted with 22nF capacitors.

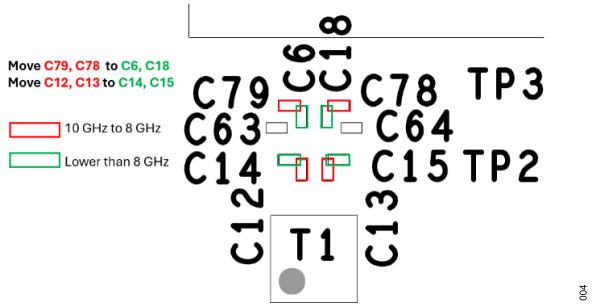

Figure 4. On-Board Clock Required Changes to Operate a Clock Frequency of Less Than 8GHz

For more information on the on-board and external clocking capacitors, see the following:

- Refer to the **Board Design and Integration Files** on the AD9217-10GEBZ-B web page for more information about the sizing and values of the components.
- See the Signal Generators section to set up the signal generators (which are optional clock sources) necessary for external clocking the AD9217-10GEBZ-B.

SIGNAL GENERATORS

Signal generator setup and options follow:

- An analog signal source. The frequency and power requirements of this source depends on the tests required. Note that a band-pass filter is typically used for single-tone tests.
- An optional sample clock source. The AD9217-10GEBZ-B is equipped with on-board sample clock generation capabilities; therefore, an external clock source is not required. If an external sample clock source is required, the clock signal generator must have low phase noise and be capable of supplying a 10GHz clock signal (or a 6GHz clock signal for the 6GSPS speed grade of the AD9217) at approximately 10dBm.
- An optional FPGA reference clock source. The AD9217-10GEBZ-B is equipped with an on-board FPGA reference clock generation capability; therefore, an external FPGA reference clock source is not required. For the AD9217, the REFCLK frequency is the sample rate divided by 16, which is the same as the digital output data rate divided by 16.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

INSTALLING THE ACE SOFTWARE

Take the following steps to install the **ACE Software** and plug-ins:

1. Go to the **ACE Software** web page to install the **ACE Software**.
2. Open the **ACE Software** and the **Start** window appears. Note that the **Start** window displays all released plug-ins.
3. Ensure that the AD9217 plug-in appears in the preinstalled list of released plug-ins. If the AD9217 plug-in does not appear in the preinstalled list, it is also available at https://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boards-kits/EVAL-AD9217.html#eb-relatedsoftware.
4. Close the **ACE Software**.

Note: The AD9213 plug-in contains the AD9217 plug-in; therefore, installing the AD9213 plug-in installs the AD9217 plug-in.

JUMPER, STANDOFF, AND SCREW INSTALLATION

Take the following steps to install a jumper and the standoffs:

1. Install a jumper on P3 as shown in Figure 5.

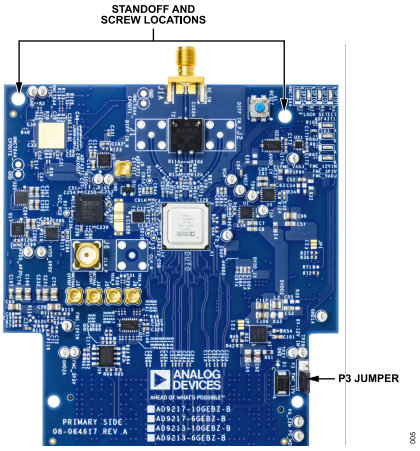

Figure 5. Standoff and Jumper Locations

2. If required, you can install standoffs at the locations (see Figure 5).

EVALUATION BOARD TESTING

Take the following steps to test the AD9217-10GEBZ-B:

1. Connect the AD9217-10GEBZ-B to the ADS8-V1EBZ evaluation board as shown in Figure 6.

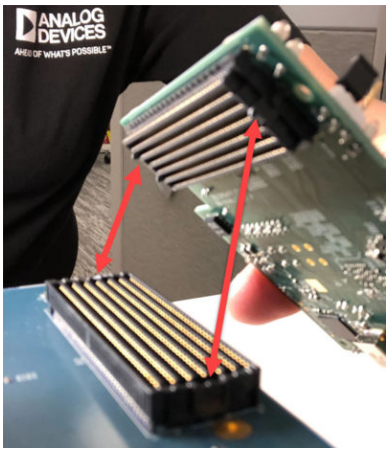

Figure 6. Connecting the AD9217-10GEBZ-B to the ADS8-V1-EBZ

2. Align the FMC+ connectors and apply even pressure across the connector and press the FMC connector onto its counterpart on the FPGA board.
3. Connect a signal, clocks (optional), power, and USB cables to the boards as shown in Figure 1.

   a. Signal (J1A). The frequency and amplitude of the test signal depends on the type of test you are performing. Full scale is typically achieved at 9dBm to 12dBm signal power at the signal generator (depending on the frequency and insertion loss of the filter used). If in doubt about which amplitude to use, start with a lower amplitude (for example, 4dBm at the signal generator) and work up or down from there.

   b. Optional sample clock (J6). The sample clock works well across a wide range of amplitudes (1dBm to 10dBm at the signal generator). Because jitter performance is likely to improve as the slew rate increases, choose an amplitude towards the upper end of the stated range.

   c. Optional FPGA reference clock (ADS8-V1EBZ, J1). Similar to the sample clock, the reference clock works well across a wide range of amplitudes (1dBm to 10dBm at the signal generator). Unlike the sample clock, the reference clock is not sensitive to jitter and phase noise. Any signal generator that meets the frequency and power requirements works. For the AD9217, the frequency of the reference clock is the (Sampling Clock Frequency)/16. The FPGA reference clock must be synchronized with the ADC sample clock.

   For example, for the default output configuration of AD9217-10GEBZ-B at 10GSPS, the reference clock frequency = 10G/16 = 625MHz, and at 6GSPS, the reference clock frequency = 6G/16 = 375MHz.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

4. Connect the USB cable from the ADS8-V1EBZ FPGA board to the Windows® PC that has the **ACE Software** installed.
5. Power on the AD28-V1EBZ FPGA board by using the S4 switch. Wait several seconds after powering on the ADS8-V1EBZ until DS17 flashes and the FPGA fan has stopped spinning.
6. Start the **ACE Software** from **Start/Programs/Analog Devices/ACE**.
7. The **ACE Software** automatically detects the AD9217-10GEBZ-B and brings up the correct ACE plug-in, which will appear in the upper left portion of the graphical user interface (GUI). If the plug-in does not appear in the upper left, select the **Plug-in Manager**, select the AD9217-10GEBZ-B, and then add the selected plug-in (see Figure 7).

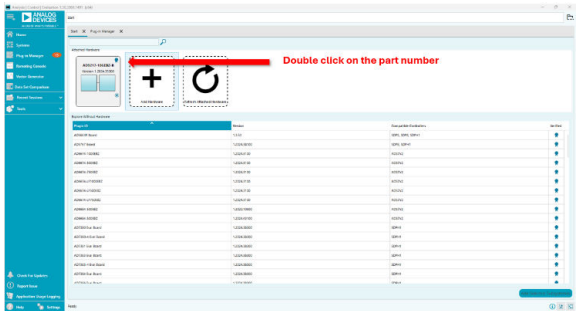

Figure 7. ACE Software Plug-In

8. Double-click the **AD9217-10GEBZ-B** icon in the **Attached Hardware** section of the GUI (see Figure 7).
9. **State=Unknown** initially appears in the lower left corner; however, wait until this status changes to **State=Good** (see Figure 8).

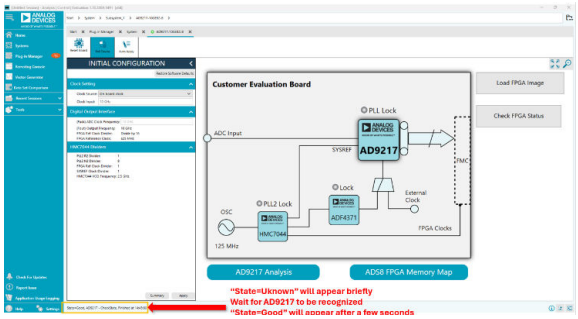

Figure 8. On-Board Clocking Board View

10. After **State=Good** appears in the lower left (see Figure 8), turn on the signal generator for the input signal.
11. Go to the **INITIAL CONFIRGURATION** tab and click the **Apply** button to configure the AD9217 in its default 10G mode.

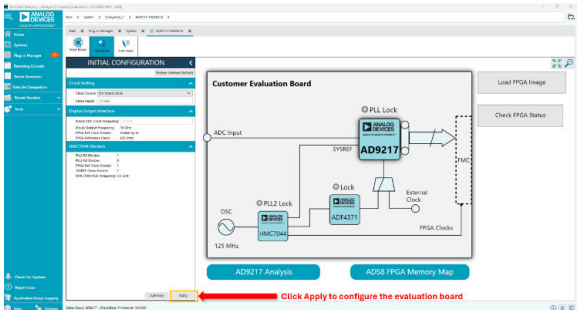

Figure 9. INITIAL CONFIRGURATION Tab

After clicking **Apply**, the configuration is applied to both the on-board clocks and the AD9217. If the on-board clock settings are successful, and the link initializes correctly, the lock indicators, including the PLL locks, turn green (see Figure 10).

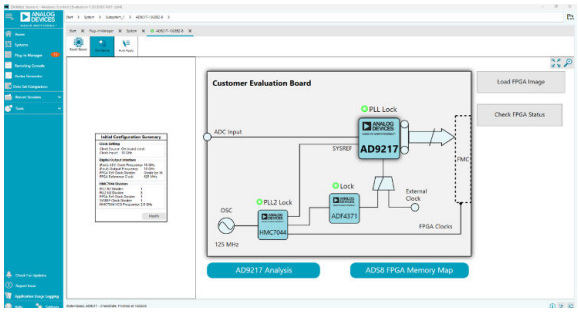

Figure 10. Successful Implementation

12. Double-click on the **AD9217** icon to proceed to check the chip internal status (see Figure 11).

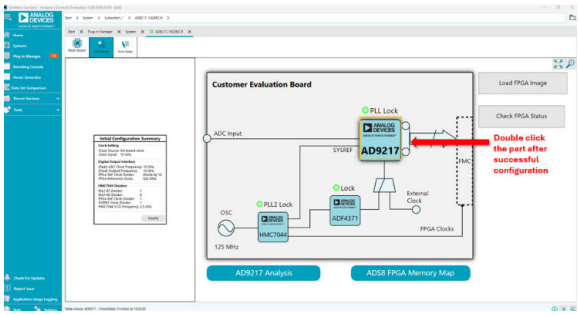

Figure 11. Icon

13. **Output Interface PLL Locked** appears in green (see Figure 12). Confirm that **Common Mode** is set to **Startup: Internal VCM control** and then click **Proceed to Analysis**. Note that you can also monitor the device temperature.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

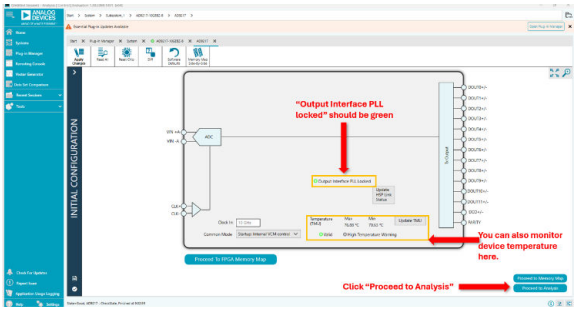

Figure 12. Output Interface PLL Locked (Green)

14. The analysis page then appears. Click **Run Once** to get a time domain view of the converted data (see Figure 13).

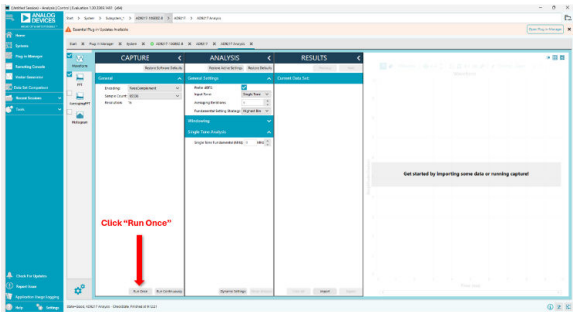

Figure 13. Time Domain View of the Converted Data

15. When using full bandwidth mode, the time domain analysis of the converted data appears (see Figure 14).

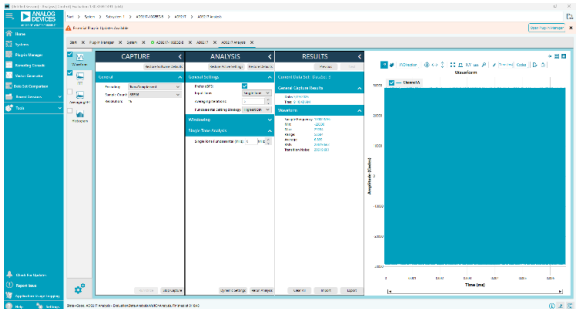

Figure 14. Time Domain Analysis of the Converted Data

16. Click the **FFT** icon (see Figure 15) to display the frequency domain view (FFT).

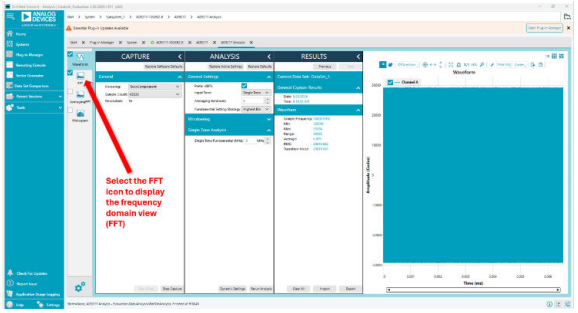

Figure 15. FFT Icon

17. Click **Run Continuously** to view repetitive FFTs (see Figure 16).

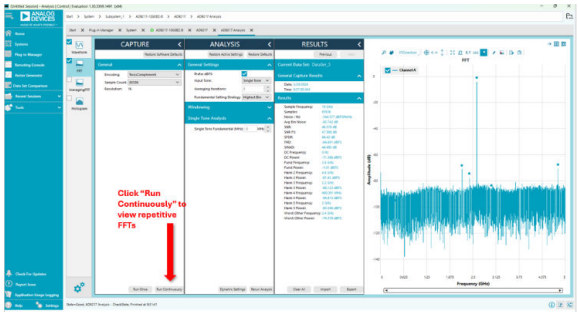

Figure 16. Run Continuously

If the **ACE Software** start-up procedure does not proceed as described or expected, take the following steps:

1. Close the **ACE Software**.
2. Power down the ADS8-V1EBZ by using the S4 switch.
3. Repeat the **ACE Software** start-up procedure (see the Evaluation Board Software Quick Start Procedures section).

If after repeated attempts the **ACE Software** start-up procedure is not successful, take the following steps:

1. Verify that the jumper is placed on the AD9217-10GEBZ-B as shown in Figure 5.
2. If using external clocks, verify that all signal generators are on and at the correct frequencies and power levels.

If data capture cannot be established after power-up, power-cycle the ADS8V1-EBZ, and retry. In rare cases, multiple power cycles may be required. Once data capture is successful, subsequent operation is stable and reliable.

EXPECTED WAVEFORM

The capture in Figure 17 shows the AD9217 operating at 10GSPS with a 2.6GHz input signal at –1.0 dBFS, acquired using the AD9217-10GEBZ-B. The on-board clock source was used for sampling, while an Rhode & Schwarz (R&S) SMA100B signal generator provides the analog input signal.

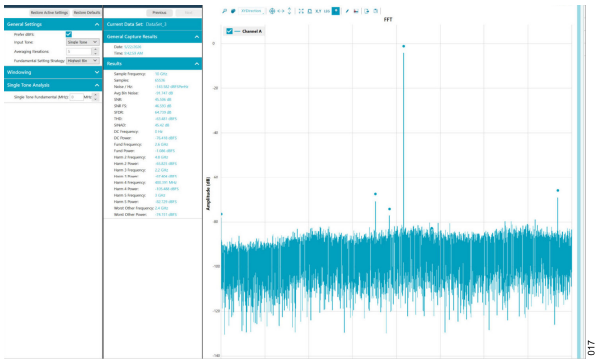

Figure 17. Expected Waveform Capture

EVALUATION BOARD SCHEMATICS, BILL OF MATERIALS (BOM), AND LAYOUTS

For additional information on the schematics, BOM, and layout files, go to the AD9217-10GEBZ-B user guide web page.

ORDERING INFORMATION

ORDERING GUIDE

Model[1]	Description
AD9217-10GEBZ-B	AD9217-10 Evaluation Board, Version B

[1] Z = RoHS-Compliant Part.

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.