Evaluating the AD5529R, 16-Channel, 16-Bit, High-Voltage Output DAC

FEATURES

- Fully-featured evaluation board for the AD5529R
- PC control in conjunction with the SDP-K1 controller board through Analysis | Control | Evaluation (ACE) Software
- On-board power solution can generate all power rails from a single external bench supply
- Various link options for configurable or external DAC output supplies
- On-board optional ADR4540 precision reference
- On-board optional Pmod™ interface

EVALUATION KIT CONTENTS

- EVAL-AD5529R-ARDZ evaluation board

DOCUMENTS NEEDED

- AD5529R data sheet

HARDWARE NEEDED

- SDP-K1 controller board (must be purchased separately)
- Bench DC power supply (with 6V to 12V, 1A ratings)
- PC running Windows® 10 operating system or higher

SOFTWARE NEEDED

- ACE Software available to download from the Analog Devices, Inc. website

GENERAL DESCRIPTION

This user guide explains the operation of the EVAL-AD5529R-ARDZ evaluation board for the AD5529R, 16-channel, 16-bit, high-voltage output DAC (digital-to-analog converter).

The EVAL-AD5529R-ARDZ includes a full power system that generates all necessary power rails, which require only one external bench supply for operation. The power tree generates two sets of DAC output voltage rails, which allow half the DAC channels to operate under one configuration, and the other half under another. The voltages for each bank can be configured to preset values by jumper configuration. It is also possible to provide the voltage for the DAC outputs externally.

The EVAL-AD5529R-ARDZ includes an optional ultra-low noise, high-accuracy ADR4540 4.096V voltage reference, disabled by default, that can be enabled for use instead of the internal AD5529R on-chip reference.

The EVAL-AD5529R-ARDZ evaluation board is intended for use along with the SDP-K1 controller board. This arrangement facilitates quick evaluation through the ACE Software. Alternatively, a Pmod connector is available to interface with the AD5529R, which allows the creation of custom hardware and software solutions to control and evaluate the AD5529R.

Full specifications on the AD5529R are available in the AD5529R data sheet available from Analog Devices, Inc., and must be consulted with this user guide when using the EVAL-AD5529R-ARDZ evaluation board.

For the current schematics, printed circuit board (PCB) layouts, and bill of material (BOM), refer to the EVAL-AD5529R-ARDZ product page.

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REVISION HISTORY

3/2026—Revision 0: Initial Version

EVAL-AD5529R-ARDZ EVALUATION BOARD PHOTOGRAPH

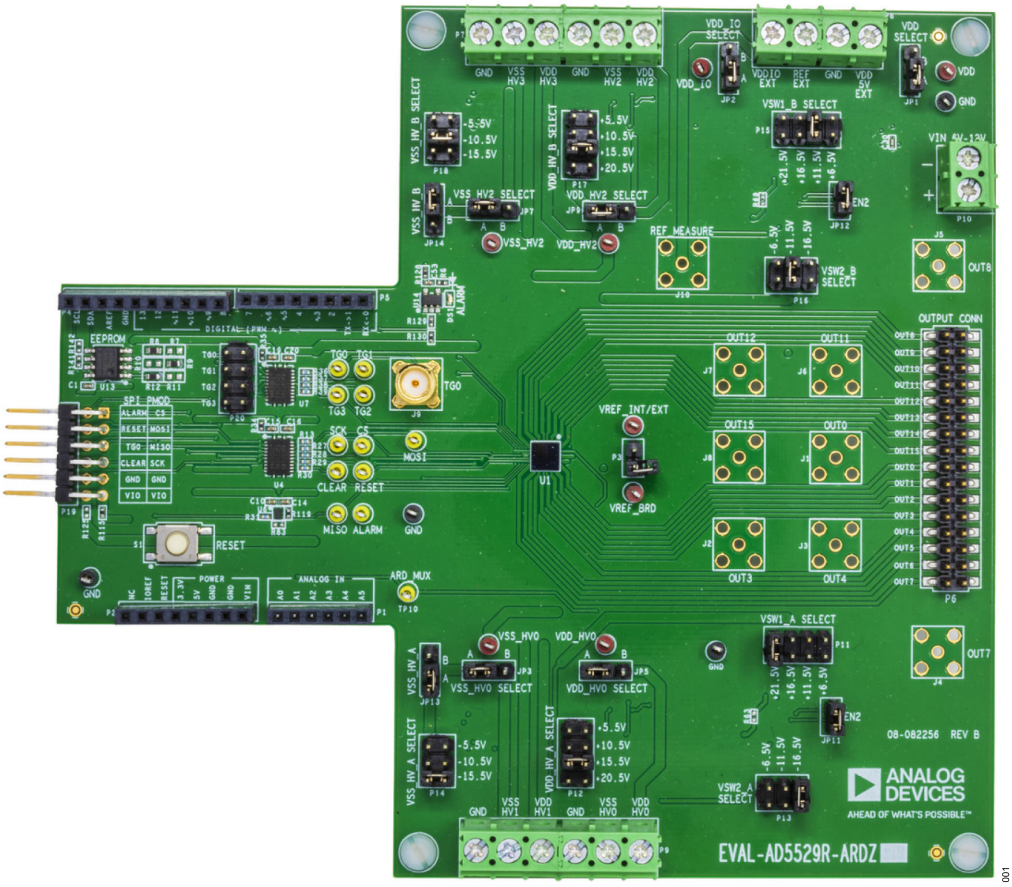

Figure 1. EVAL-AD5529R-ARDZ Evaluation Board Photograph

EVALUATION BOARD HARDWARE

UNBOXING HARDWARE AND QUICK SETUP

For a quick evaluation of the board, do the following steps:

1. Check that all the jumpers are placed by default, as shown in Table 4.
2. Plug the EVAL-AD5529R-ARDZ evaluation board onto the SDP-K1 controller board.
3. Connect a power supply set to a voltage between 6V to 12V and capable of providing 1A to the screw connector P10 of the EVAL-AD5529R-ARDZ evaluation board.
4. Connect the SDP-K1 board to the PC with a USB-C cable.
5. Install and run the ACE Software (see the Evaluation Board Software Support section).

POWER SUPPLIES

The main power input to the EVAL-AD5529R-ARDZ evaluation board is the P10 screw connector. An external bench supply with a voltage set between 6V and 12V, and capability to provide 1A must be used to supply this connector. The power tree that spans this input is shown in Figure 2 with the voltages generated in the default configuration (note that defaults are different for the DAC0 to DAC7 bank and the DAC8 to DAC15 bank).

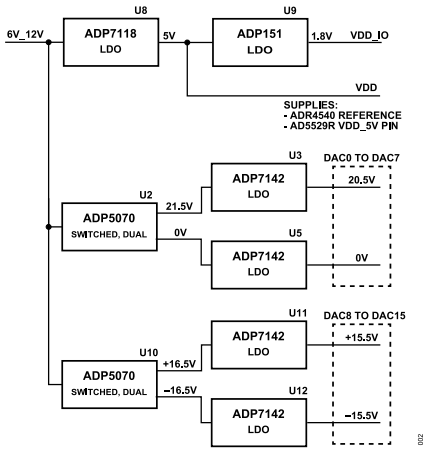

Figure 2. Evaluation Board Power Tree, Default Voltage Settings

The 5V (U8) and 1.8V (U9) rails are fixed. The switched and LDO regulators whose function is to generate the positive and negative supply rails for the DAC outputs (U2, U10, U3, U5, U11, U12) can have their output voltages changed by jumper settings. Jumper configuration permits values for the DAC output positive rails of +20.5V, +15.5V, +10.5V or +5.5V, and values of −15.5V, −10.5V, −5.5V, or 0V for the negative rails. For jumper configuration needed to produce these voltages, see the On-Board DAC Output Voltage Rails section.

ON-BOARD DAC OUTPUT VOLTAGE RAILS

By default, the EVAL-AD5529R-ARDZ evaluation board jumper setting configuration from factory results in the DAC output voltage rails, as shown in Figure 2. To use this default setting, no action is required and the steps described in Unboxing Hardware and Quick Setup section can be directly followed. Table 1 details the default jumper positions and resulting voltages.

Table 1. DAC Output Voltage Rails Default Configuration

Device	Default Output Voltage	Jumper Name	Default Jumper Position
U2	SW1 output: +21.5V	SW1 output: P11	P11: 1-2.
	SW2 output: disabled	SW2 output: P13, JP11	P13: not inserted, JP11: open (SW2 disable).
U3	+20.5V	P12	1-2.
U5	0V	P14, JP13	P14: not inserted, JP13: position B (rail grounded).
U10	SW1 output: +16.5V	SW1 output: P15	P15: 3-4.
	SW2 output: −16.5V	SW2 output: P16	P16: 1-2.
U11	+15.5V	P17	3-4.
U12	−15.5V	P18	1-2.

To change the supply voltage of the DAC output stages to values different to the default ones, jumper adjustments have to be made both at the first switching voltage conversion stage (regulators U2 for DAC0 to DAC7, and U10 for DAC8 to DAC15) and at the final linear regulation stage (U3 and U5 for DAC0 to DAC7, and U11 and U12 for DAC8 to DAC15). All jumper adjustments must be applied with the board powered off.

The linear regulators directly generate the voltage level supplied to the DAC output stages, use Table 2 to select the required supply level for each DAC output bank and make the corresponding jumper adjustments. The switched regulators (U2, U10) must be configured in correspondence to the selected values for the linear regulators, with voltage levels 1V above/below the DAC output rail for positive/negative rails respectively. For the jumper settings needed, see Table 3.

As shown in Table 2 and Table 3, it is possible to generate custom voltages for the supply rails different to the provided presets. This is done by populating the indicated resistors on the evaluation board. To calculate the necessary resistor values, refer to the EVAL-AD5529R-ARDZ evaluation board schematic with the data sheets of the involved regulator ICs.

EVALUATION BOARD HARDWARE

Table 2. Jumper Settings for DAC Output Rail Linear Voltage Regulators (U3, U5, U11, U12)

Affected DAC Output Channels	Device and Rail	DAC Output Rail Voltage Setting	Jumper Position
DAC0 to DAC7	U3, positive rail	+20.5V	P12: 1-2 (default).
		+15.5V	P12: 3-4.
		+10.5V	P12: 5-6.
		+5.5V	P12: 7-8.
		Custom	P12: no jumper. Populate R112 with calculated value.
	U5, negative rail	−15.5V	P14: 1-2.
		−10.5V	P14: 3-4.
		−5.5V	P14: 5-6.
		0V	JP13: position B (rail grounded) (default). P14: do not care (U5 not driving rail).
		Custom	P14: no jumper. Populate R120 with calculated value.
DAC8 to DAC15	U11, positive rail	+20.5V	P17: 1-2.
		+15.5V	P17: 3-4 (default).
		+10.5V	P17: 5-6.
		+5.5V	P17: 7-8.
		Custom	R124.
	U12, negative rail	−15.5V	P18: 1-2 (default).
		−10.5V	P18: 3-4.
		−5.5V	P18: 5-6.
		0V	JP13: position B (rail grounded). P18: do not care (U12 not driving rail).
		Custom	P18: no jumper. Populate R126 with calculated value.

Table 3. Jumper Settings for Switched Regulators (U2, U10)

Affected DAC Output Channels	Device and Output	Output Voltage	Jumper Position
DAC0 to DAC7	U2, SW1 (positive)	+21.5V	P11: 1-2 (default).
		+16.5V	P11: 3-4.
		+11.5V	P11: 5-6.
		+6.5V	P11: 7-8.
		Custom	P14: no jumper. Populate R110 with calculated value.
	U2, SW2 (negative)	−16.5V	P13: 1-2.
		−11.5V	P13: 3-4.
		−6.5V	P13: 5-6.
		Disable	JP11: open (default).
		Custom	P13: no jumper. Populate R118 with calculated value.
DAC8 to DAC15	U10, SW1 (positive)	+21.5V	P15: 1-2.
		+16.5V	P15: 3-4 (default).
		+11.5V	P15: 5-6.
		+6.5V	P15: 7-8.
		Custom	P15: no jumper. Populate R116 with calculated value.
	U10, SW2 (negative)	−16.5V	P16: 1-2 (default).
		−11.5V	P16: 3-4.

EVALUATION BOARD HARDWARE

Table 3. Jumper Settings for Switched Regulators (U2, U10) (Continued)

Affected DAC Output Channels	Device and Output	Output Voltage	Jumper Position
		−6.5V	P16: 5-6.
		Disable	JP12: open.
		Custom	P16: no jumper.
			Populate R122 with calculated value.

EXTERNAL VOLTAGE RAILS OPTION

It is possible to bypass the on-board generated voltage rails and supply them externally. This requires adjustment of jumper links, as shown in Table 4 according to the *External Supply* configuration. The *External Supply* configuration facilitates direct external driving of the AD5529R DAC output supply pins (VDD_HV0/1/2/3, VSS_HV0/1/2/3) as well as the main 5V supply rail (VDD_5V) and the logic interface supply (VDD_IO). For the full link options, see Table 5.

For the DAC output supply rails, note that by default the positive supply pins are shorted as follows on the evaluation board: VDD_HV0 is connected to VDD_HV1, and VDD_HV2 is connected to VDD_HV3. Similarly, for the negative supply pins, VSS_HV0 is connected to VSS_HV1, and VSS_HV2 is connected to VSS_HV3. This arrangement results in two possible supply configurations, one for DAC0 to DAC7, and another for DAC8 to DAC15. It is possible to remove the shorting resistors to have up to four different supply configurations (externally provided), do the following steps:

1. Remove R121 to disconnect VDD_HV0 from VDD_HV1.
2. Remove R123 to disconnect VDD_HV2 from VDD_HV3.
3. Remove R109 to disconnect VSS_HV0 from VSS_HV1.
4. Remove R111 to disconnect VSS_HV2 from VSS_HV3.

Removal of the resistors above allow to use the maximum of four different output voltage rail configurations (one for each set of four DAC outputs).

Table 4. Quick Start Link Configuration for Power Solution and External Supply

Supply Rail	Link	Link Position for On-Board Power Solution (Default)	Link Position for External Supply
VDD_5V	JP1	A	B
VDD_IO	JP2	A	B
VSS_HV0/1	JP3	A	B
VDD_HV0/1	JP5	A	B
VSS_HV2/3	JP7	A	B
VDD_HV2/3	JP9	A	B

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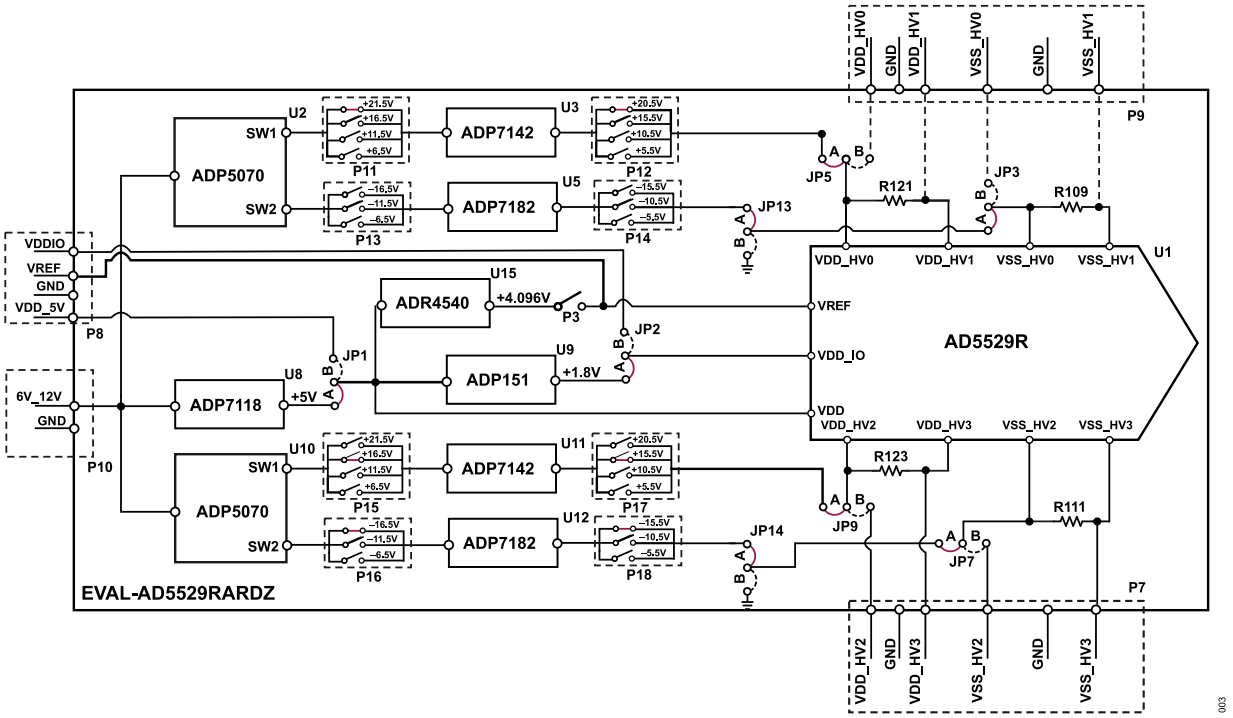

Figure 3. Jumper and Link Options for EVAL-AD5529R-ARDZ Evaluation Board Power Rails

Table 5. Jumper and Link Options Full Description

Jumper/Link	Description	Positions
JP1	VDD (5V) rail selection between on-board or external.	A (default): on-board. Source U15, U9, and AD5529R VDD_5V pin from U8. B: external. Source AD5529R VDD for terminal P8, Pin 1.
JP2	VDD_IO rail selection between on-board or external.	A (default): on-board. Source AD5529R VDD_IO pin from U9. B: external. Source AD5529R VDD_IO from terminal P8, Pin 4.
JP3	VSS_HV0 and VSS_HV1 rails selection between on-board or external.	A (default): on-board. Source AD5529R VSS_HV0/HV1 from the signal selected in JP13 (U5 or ground, see JP13). B: external. Source AD5529R VSS_HV0/HV1 from terminal P9, Pin 2 and Pin 5.
JP5	VDD_HV0 and VDD_HV1 rails selection between on-board or external.	A (default): on-board. Source AD5529R VDD_HV0/HV1 from U3 (see P12). B: external. Source AD5529R VDD_HV0/HV1 from terminal P9, Pin 4 and Pin 6.
JP7	VSS_HV0 and VSS_HV1 rails selection between on-board or external.	A (default): on-board. Source AD5529R VSS_HV2/HV3 from the signal selected in JP14 (U12 or ground, see JP14). B: external. Source AD5529R VSS_HV2/HV3 for terminal P7, Pin 2 and Pin 5.
JP9	VDD_HV0 and VDD_HV1 rails selection between on-board or external.	A (default): on-board. Source AD5529R VDD_HV2/HV3 from U11 (see P17). B: external. Source AD5529R VDD_HV2/HV3 for terminal P7, Pin 4 and Pin 6.
JP11	Enables or disables the negative output of switched regulator U2.	Removed (default): output disabled. Inserted: output enabled.
JP12	Enables or disables the negative output of switched regulator U10.	Removed (default): output disabled. Inserted: output enabled.
JP13	On-board VSS_HV0 and VSS_HV1 rail generation selection between U5 or ground.	A (default): U5 linear regulator (see P14 for voltage). B: GND.
JP14	On-board VSS_HV2 and VSS_HV3 rail generation selection between U12 or ground.	A (default): U5 linear regulator (see P17 for voltage). B: GND.
P3	On-board ADR4540 reference connection to AD5529R: connect or disconnect.	Inserted: connect, U15 driving AD5529R REF pin. Removed (default): disconnect. Internal AD5529R reference used.
P11	Voltage setting for U2 switching regulator positive output (SW1).	1-2 (default): +21.5V.

EVALUATION BOARD HARDWARE

Table 5. Jumper and Link Options Full Description (Continued)

Jumper/Link	Description	Positions
		3-4: +16.5V. 5-6: +11.5V. 7-8: +6.5V.
P12	Voltage setting for U3 linear regulator.	1-2 (default): +20.5V. 3-4: +15.5V. 5-6: +10.5V. 7-8: +5.5V.
P13	Voltage setting for U2 switching regulator negative output (SW2).	Removed by default. 1-2: −16.5V. 3-4: −11.5V. 5-6: −6.5V.
P14	Voltage setting for U5 linear regulator.	Removed by default. 1-2: −15.5V. 3-4: −10.5V. 5-6: −5.5V.
P15	Voltage setting for U10 switching regulator positive output (SW1).	1-2 (default): +21.5V. 3-4: +16.5V. 5-6: +11.5V. 7-8: +6.5V.
P16	Voltage setting for U10 switching regulator positive output (SW1).	1-2 (default): −16.5V. 3-4: −11.5V. 5-6: −6.5V.
P17	Voltage setting for U11 linear regulator.	1-2 (default): +20.5V. 3-4: +15.5V. 5-6: +10.5V. 7-8: +5.5V.
P18	Voltage setting for U12 linear regulator.	1-2 (default): −15.5V. 3-4: −10.5V. 5-6: −5.5V.

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ON-BOARD REFERENCE

The EVAL-AD5529R-ARDZ evaluation board contains an ADR4540 ultra-low noise, high-accuracy 4.096V voltage reference (U15), which by default is not connected to the AD5529R REF pin. To make use of this on-board reference, insert P3 and disable the AD5529R internal reference by writing the appropriate value in the Reference Source Select Register (for more details, refer to the AD5529R data sheet).

MONITOR MULTIPLEXER

The AD5529R features a buffered monitor multiplexer that enables the user to monitor signals including DAC output voltages, DAC output currents, and chip temperature measurements by the MUX-OUT pin. The AD5529R MUXOUT pin is routed to the A0 pin (connector P1) in the Arduino header for easy access. For a detailed explanation of the monitor multiplexer functionality, refer to the AD5529R data sheet.

ON-BOARD CONNECTORS

Table 6 shows the functionality of all connectors present on the EVAL-AD5529R-ARDZ evaluation board.

Table 6. On-Board Connector Description

Connector Identifier	Description
P1, P2, P4, P5	These four connectors form the Arduino header. For more details, see the Arduino Connector section.
P6	Provides access to all DAC outputs (DAC0 to DAC15).
P7	Allows externally supplying the VDD_HV2/HV3 and VSS_HV2/HV3 pins of the AD5529R.
P8	Allows externally supplying the VDD_5V, VREF and VDD_IO pins of the AD5529R.
P9	Allows externally supplying the VDD_HV0/HV1 and VSS_HV0/HV1 pins of the AD5529R.
P10	Main power input to the board, must be supplied with a fixed voltage between 6V to 12V (1A maximum current draw).
P19	Digilent Pmod compatible digital interface pin header connector. Optional use for custom interfacing with AD5529R. For more details, see the Pmod Connector section.
J1, J2, J3, J4, J5, J6, J7, and J8	Alternative access to DAC0, DAC3, DAC4, DAC7, DAC8, DAC11, DAC12, and DAC15 outputs. Not populated by default.
J9	Allows external access to the AD5529R TG0 (Toggle0) pin.
J10	Allows external access to the AD5529R REF (Reference) pin. Not populated by default.

Arduino Connector

The EVAL-AD5529R-ARDZ evaluation board digital interface signals are transmitted by the controller board by the Arduino header, formed by connectors P1, P2, P4, and P5. The interface includes SPI bus lines for reading and writing data, and several GPIOs with multiple functions. Table 7 shows the digital signal names, functions, and digital header pin assignments.

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Table 7. Arduino Header Connections

Signal Name	Function	Header Pin	Arduino Pin Name	Pull-Up
ARD_SPI_CS	SPI chip-select.	P4 Pin 3	10/PWM/CSB	10kΩ (R1)
SDI	SPI serial data in (MOSI).	P4 Pin 4	11/PWM/MOSI	
SDO	SPI serial data out (MISO).	P4 Pin 5	12/MISO	10kΩ (R119)
SCLK	SPI serial clock.	P4 Pin 6	13/SCK	
SDA	I^2C serial data. Used to read board ID data from the EEPROM.	P4 Pin 9	SDA	2.1kΩ (R142)
SCL	I^2C serial clock. Used to read board ID data from the EEPROM.	P4 Pin 10	SCL	2.1kΩ (R141)
ARD_TG0	This pin has several functionalities, it can act as LDAC for an asynchronous load, as the clock for the DCK dither or as a toggle pin TGP0.	P4 Pin 2	9/PWM	
ARD_RESET	Active Low Device Reset. Asserting this pin low resets the device to its default configuration.	P4 Pin 1	8	1kΩ (R32)
ARD_CLEAR	Active Low. A logic low at this level-triggered input clears the device to the defaults values.	P5 Pin 8	7	10kΩ (R33)
ARD_TG1	This pin has several functionalities, it can act as LDAC for an asynchronous load, as the clock for the DCK dither or as a toggle pin TGP1.	P5 Pin 7	6/PWM	
ARD_TG2	This pin has several functionalities, it can act as LDAC for an asynchronous load, as the clock for the DCK dither or as a toggle pin TGP2.	P5 Pin 6	5/PWM	
ALARM	The AD5529R active low, open collector ALARM output pin is made available for monitoring via this pin.	P5 Pin 5	4	
ARD_TG3	This pin has several functionalities, it can act as LDAC for an asynchronous load, as the clock for the DCK dither or as a toggle pin TGP3.	P5 Pin 4	3/PWM	
ARD_MUX	An external analog-to-digital converter (ADC) reads voltages on this pin for diagnostic purposes.	P1 Pin 1	A0	

EVALUATION BOARD HARDWARE

Pmod Connector

A 12-pin, Digilent Pmod compatible connector (P19) is available on the EVAL-AD5529R-ARDZ evaluation board and can be optionally used for custom interfacing with AD5529R. Figure 4 lists the signal assignment to the connector pins, which corresponds to a Pmod Interface Type 2A (expanded SPI) according to the Pmod 1.3.1 Interface Specification from Digilent.

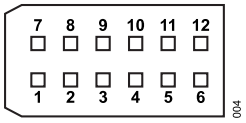

Figure 4. Pmod Connector Pinout

Table 8. Pmod Connector (P19) Signal Assignment

Pin Number	Mnemonic
1	$\overline{CS}$
2	SDI
3	SDO
4	SCLK
5	GND
6	IOVDD
7	$\overline{ALARM}$
8	$\overline{RESET}$
9	TG0
10	$\overline{CLEAR}$
11	GND
12	IOVDD

EVALUATION BOARD SOFTWARE SUPPORT

The ACE Software is a desktop software application that provides a plug-and-play evaluation experience for multiple evaluation systems from across the Analog Devices, Inc., product portfolio. An SDP-K1 controller board (which must be purchased separately) is necessary to control the EVAL-AD5529R-ARDZ evaluation board through ACE.

For ACE installation and documentation instructions, go to the ACE Software web page. The first time that ACE runs with the SDP-K1 controller board connected with the EVAL-AD5529R-ARDZ evaluation board attached and powered, a prompt may appear informing about a required firmware update, as shown in Figure 5. If this is the case, press OK to accept the update.

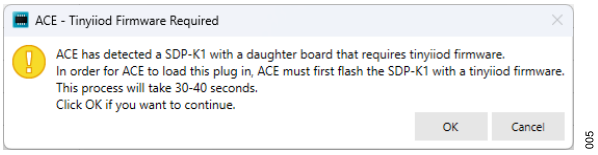

Figure 5. SDP-K1 Firmware Update ACE Prompt

After the SDP-K1 firmware is updated, ACE can autodetect a connected EVAL-AD5529R-ARDZ evaluation board, and prompts for installation of the specific plug-in required to control this board (see Figure 6).

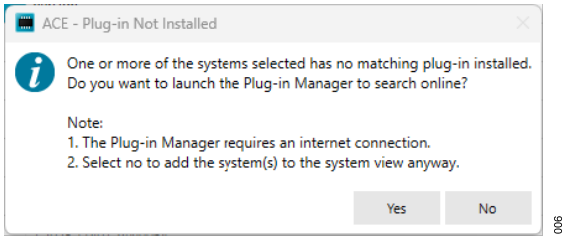

Figure 6. Plug-In Install ACE Prompt

Accepting this prompt takes the user to the **Plug-In Manager** menu. As shown in Figure 7, the **Board.AD5529R** plug-in appears in the **Available Packages** section by the search box, and to install it, click the **Install Selected** button.

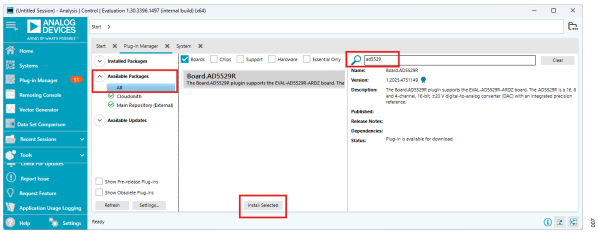

Figure 7. Plug-In Installation

With the plug-in installed, then to run the plug-in, double-click the detected **EVAL-AD5529R-ARDZ** board icon (see Figure 8).

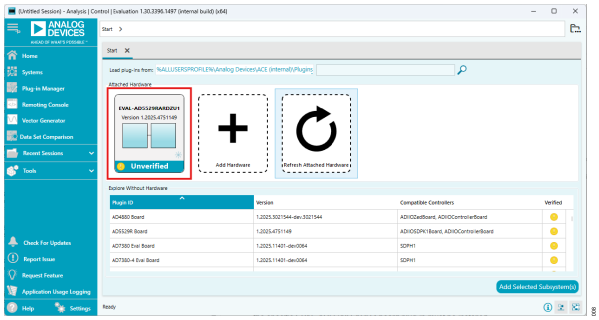

Figure 8. Autodetected EVAL-AD5529R-ARDZ Evaluation Board

With the plug-in opens, then to open the **Chip View** and access all attributes and functionality, double-click the **AD5529R** icon, as shown in Figure 9.

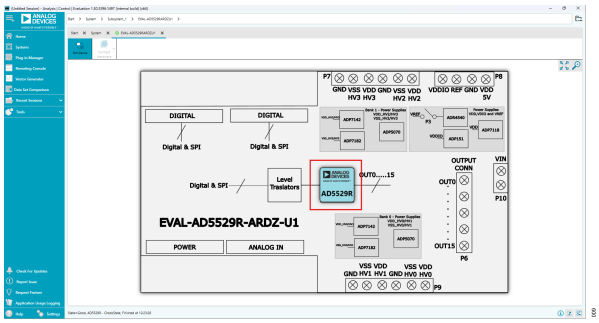

Figure 9. AD5529R ACE Plug-In

For an additional documentation for controlling the EVAL-AD5529R-ARDZ evaluation board, see within the plug-in.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.