Evaluating the AD5144 Digital Potentiometer

FEATURES

- Full featured evaluation board for the AD5144 in conjunction with low voltage digital potentiometer (digiPOT) motherboard (EVAL-AD5144-2DBZ)
- Various test circuits
- Various power solutions
- Various AC/DC input signals
- PC control in conjunction with the Analog Devices, Inc., EVAL-SDP-CK1Z (SDP-K1) controller board

EVALUATION KIT CONTENTS

- EVAL-AD5144-2DBZ: AD5144 daughter board

HARDWARE REQUIRED

- EVAL-MB-LV-ARDZ digiPOT motherboard (purchased separately)
- EVAL-SDP-CK1Z (SDP-K1) controller board (purchased separately)
- PC running on Windows® 10 (32-bit or 64-bit) or later

SOFTWARE REQUIRED

- Analysis | Control | Evaluation (ACE) software, available for download from the EVAL-AD5144-2DBZ product page
- Dedicated firmware for EVAL-MB-LV-ARDZ compatible boards, available for download from the EVAL-AD5144-2DBZ product page.

GENERAL DESCRIPTION

This user guide describes the evaluation board for evaluating the AD5144—a digital potentiometer with 256 positions and nonvolatile memory. With versatile programmability, the AD5144 allows multiple modes of operation, including read/write access to the RDAC and electrically erasable programmable read-only memory (EEPROM) registers, increment/decrement of resistance, resistance changes in ±6dB scales, wiper setting readback, and extra EEPROM for storing user-defined information, such as memory data for other components or a lookup table.

The AD5144 supports dual supply (±2.25V to ±2.75V) operation and single supply (2.3V to 5.5V) operation, making the device suitable for battery-powered and other applications. The EVAL-MB-LV-ARDZ incorporates an internal power supply from the USB and provides on-board 5V, 3V, and +2.5V/−2.5V supplies to EVAL-AD5144-2DBZ.

The EVAL-MB-LV-ARDZ interfaces with the USB port of a PC through the system demonstration platform (SDP-K1) controller board. The ACE software is available for download on the EVAL-AD5144-2DBZ product page. This software enables the user to program the AD5144. A peripheral module interface (PMOD) connection is also available that allows the connection of different microcontrollers to the EVAL-MB-LV-ARDZ without the SDP-K1 controller board. Note that when a microcontroller is used through the PMOD connection, the SDP-K1 board must be disconnected, and the user cannot use the ACE software.

Complete specifications for the AD5144 part can be found in the AD5144 data sheet, which is available from Analog Devices and must be consulted in conjunction with this user guide when using the evaluation board.

TYPICAL EVALUATION SETUP

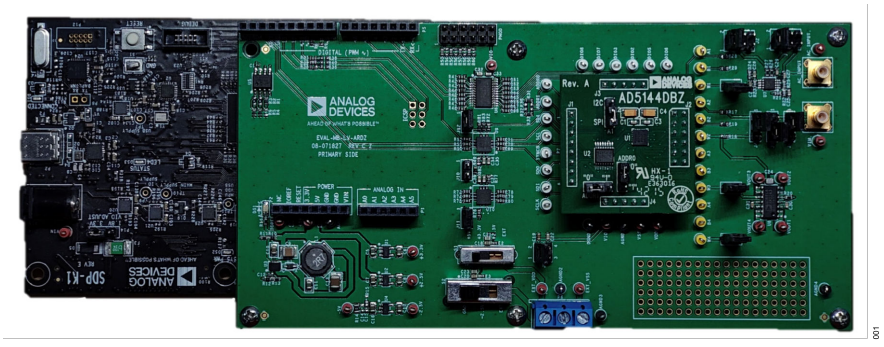

Figure 1. Evaluation Board with Low Voltage DigiPOT Motherboard and System Demonstration Platform Photograph

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REVISION HISTORY

9/2025—Revision 0: Initial Version

EVALUATION BOARD SOFTWARE

INSTALLING ACE

The EVAL-AD5144-2DBZ uses the ACE evaluation software that allows the evaluation and control of multiple evaluation systems.

The ACE installer comes with the necessary SDP-K1 drivers and the Microsoft® .NET Framework 4 by default. The ACE software is available for download from the ACE software page and must be installed before connecting the SDP-K1 board to the USB port of the PC to ensure that the SDP-K1 board is recognized as soon as it is connected to the PC. For full instructions on how to install and use this software, see the ACE software page on the Analog Devices website.

LOADING SDP-K1 FIRMWARE

A dedicated firmware to control the EVAL-AD5144-2DBZ is required to be loaded to the SDP-K1. This is simply done by right-clicking the ***.bin** file, hovering over **Send to** and sending the file to the drive named **SDP-K1**, see Figure 2. A dialogue box pops up showing the progress which takes few seconds. The dialogue box automatically disappears once the firmware is loaded.

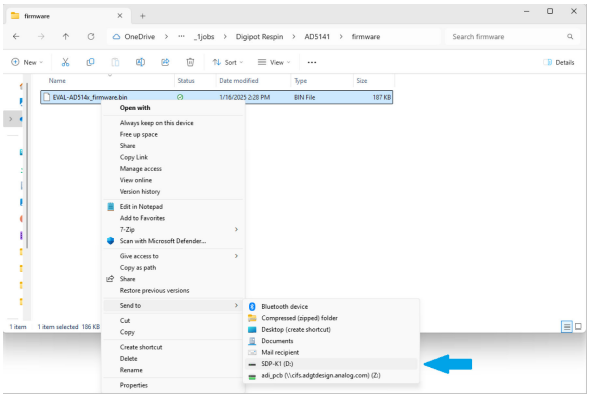

Figure 2. Loading SDP-K1 Firmware

INSTALLING EVAL-AD5144-2DBZ PLUG-IN

A plug-in for the EVAL-AD5144-2DBZ is required to be installed on ACE to communicate with the firmware loaded on SDP-K1. Take the following steps:

1. Connect the evaluation board to the SDP-K1 board, and connect the USB cable between the SDP-K1 board and the PC.
2. Open ACE, go to **Plug-in Manager**. A dialogue box occasionally pops up asking to reprogram the SDP-K1 with a standard firmware, always select **No** or **Cancel**. See Figure 3.

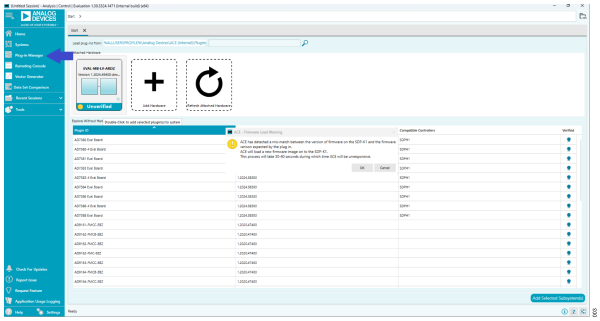

Figure 3. Opening Plug-in Manager

3. Within **Plug-in Manager**, go to **Available Packages**. Then, search for **Boards.ADDigipots**. Select the available plug-in and click **Install Selected**. For reference, see Figure 4.

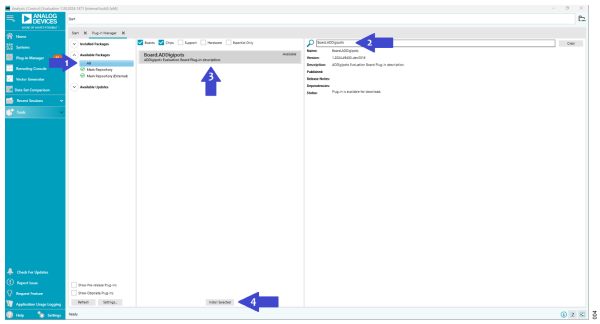

Figure 4. Installing Board.ADDigipots Plug-in

INITIAL SETUP

To set up the evaluation board, take the following steps:

1. Connect the evaluation board to the SDP-K1 board, and connect the USB cable between the SDP-K1 board and the PC.
2. Load the SDP-K1 firmware.
3. Run the ACE application. The **EVAL-MB-LV-ARDZ** plug-in appears in the attached hardware section of the **Start** tab.

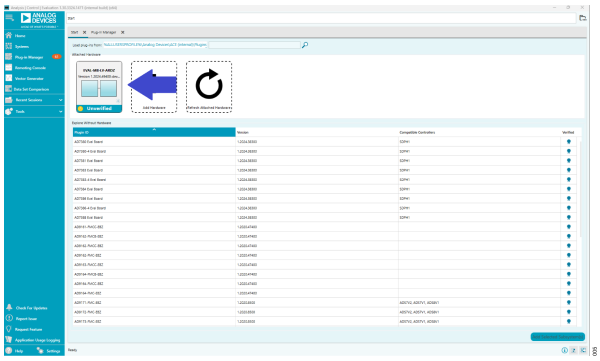

Figure 5. EVAL-MB-LV-ARDZ as Attached Hardware

4. Double-click the board plug-in to open the board view. If the correct firmware in the SDP-K1 controller is missing or does not match, a dialogue box pops up and gives the option to flash the correct firmware. Click **Cancel** since the firmware has been loaded previously.

EVALUATION BOARD SOFTWARE

5. In the device **system_config** attributes section, set the following information:
   a. device_generic: **AD5144**
   b. comm_interface: **SPI**
   c. operating_mode: **potentiometer**
6. Click on **Reconfigure System** at the bottom of the system configuration window. When the **System Config Summary** shows up, click **Modify**.

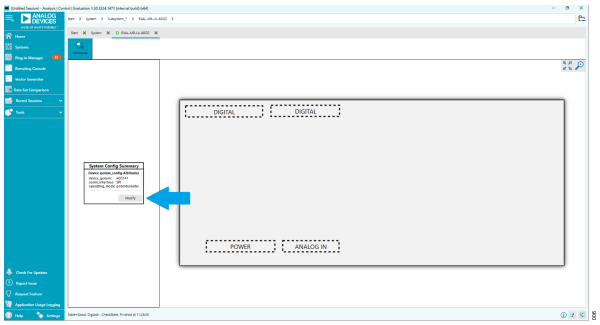

Figure 6. EVAL-MB-LV-ARDZ Board View Configuration Window

7. Restart the ACE software and repeat Step 4. The board view shows the **Digipot** block. Double-click the block.

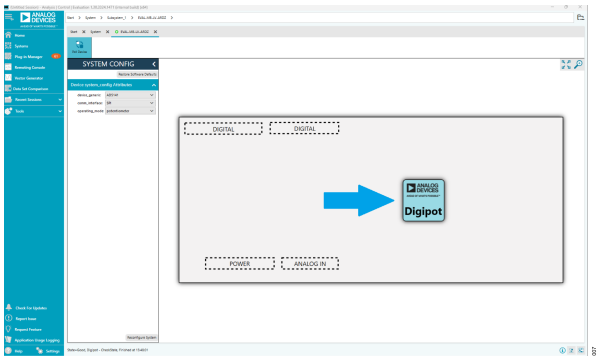

Figure 7. EVAL-MB-LV-ARDZ Board View to Chip View

8. You can now control the device. Type the values you want to modify and press the enter key to send it to the device.

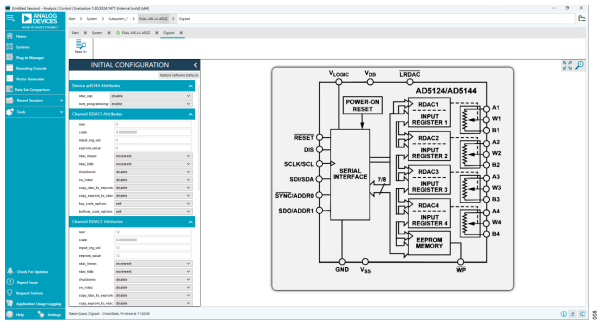

Figure 8. EVAL-AD5144-2DBZ Chip View

For more information about the ACE functionality for AD5144, refer to the markdown documentation in ACE software.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EVAL-MB-LV-ARDZ motherboard provides both on-board single (5V, 3.3V) and dual (+2.5V/−2.5V) power supplies. Users can choose between voltages using the switches S1 and S2. The output of S1 is connected to V_{DD}, while S2 is connected to V_{SS}. For safety precaution, use the switch only if there is no power connected to the motherboard. V_{LOGIC} is connected to V_{DD} via J9 jumper pins by default. For the switch options, check Table 1.

The EVAL-AD5144-2DBZ can also be powered externally through the P6 connectors, as described in Table 2. This is used if a different voltage supply is needed or if the PMOD connector is used. If using an external supply, remove the shunt connection of J9.

All supplies are decoupled to ground using 10µF and 0.1µF capacitors

Table 1. On-board Power Supply Switch Options

Switch - Position	Options
S1 - 1	5V
S1 - 2	3.3V (default)
S1 - 3	2.5V
S1 - 4	EXT_VDD
S2 - 1	GND (default)
S2 - 2	−2.5V
S2 - 3	EXT_VSS

Table 2. External Power Supply Connectors

Connector Label	Voltage
EXT_VDD	External analog positive power supply.
	Recommended supply is +15V.
GND	Ground.
EXT_VSS	External analog negative power supply.
	Recommended supply is −15V.

LINK OPTIONS

Several link and switch options are incorporated into the EVAL-MB-LV-ARDZ motherboard and the EVAL-AD5144-2DBZ daughterboard, and the options must be set up before using the board. The default positions of the links are configured to control the evaluation board via the SDP-K1 board using a PC. The functions of these link options are described in detail in Table 3.

The EVAL-AD5144-2DBZ has many on-board configuration options, one of which is the ability to switch between I^2C and SPI as its communication interface via the A2 link. For more information, refer to Table 4.

Table 3. Motherboard Link Functions

Link No.	Option
J9	This link selects the V_{LOGIC} connection
	Position 1-2 Connects V_{LOGIC} to V_{DD} (default)
	Position 3-4 Connects V_{LOGIC} to IO_{REF} pin from SDP-K1
J10	Enables the step down translator for open drain lines
	Must be disconnected if V_{DD} is greater than 3.3 V (default)
	Must be connected if V_{DD} is less than 3.3 V
J11	Enables the step up translator for open drain lines
	Must be connected if V_{DD} is greater than 3.3 V (default)
	Must be disconnected if V_{DD} is less than 3.3 V
J12	Enables the translator for push-pull lines.
	Must be connected when using SDP-K1 (default)
	Must be disconnected when using PMOD

Table 4. Daughterboard Link Functions

Link No.	Option	Description
A1	I^2C	Selects the communication interface
	SPI	
ADDR0	0 or 1	See Table 5
ADDR1	0 or 1	See Table 5

Table 5. I^2C Address Selection Table

A3 Jumper Position	A4 Jumper Position	Device Address
0	0	0101111 (default)
0	1	0100011
1	0	0101100
1	1	0100000

EVALUATION BOARD HARDWARE

TEST CIRCUITS

The EVAL-MB-LV-ARDZ incorporates several test circuits in the output to evaluate the performance of the AD5144 in typical applications.

DAC

The digiPOT can be operated as a digital-to-analog converter (DAC), as shown in Figure 9. Table 6 describes the options available for the voltage references. This test circuitry is connected to Channel 1.

The output voltage is defined in Equation 1.

$$V_{OUT} = (V_A - V_B) \times \frac{RDAC1}{256} \quad (1)$$

where:
RDAC1 is the code loaded in the RDAC1 register.
V_A is the voltage applied to the A terminal via J1.
V_B is the voltage applied to the B terminal via J2.

However, by changing the R28 and R29 external resistor values, the voltage of the voltage references can be reduced. In this case, use the A1 and B1 test points to measure the voltage applied to the A and B terminals and to recalculate V_A and V_B in Equation 1.

Table 6. DAC Voltage References

Terminal	Link	Position	Description
A1	J1	1 and 2	Connects Terminal A1 to V_{DD}.
		3 and 4	Connects Terminal A1 to $V_{DD}/2$. Do not apply AC signal.
W1	J3		Connects Terminal W1 to an output buffer.
B1	J2	1 and 2	Connects Terminal B1 to $V_{DD}/2$.
		3 and 4	Connects Terminal B1 to V_{SS}.
		5 and 6	Connects Terminal B1 to analog ground.

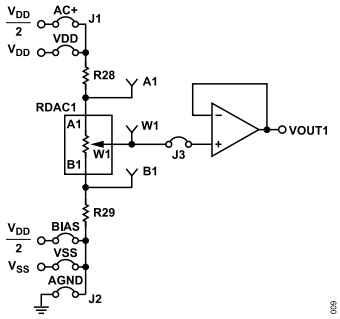

Figure 9. DAC

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AC Signal Attenuation

The RDAC can be used to attenuate an AC signal, which must be provided externally using the AC_INPUT connector, as shown in Figure 10.

Depending on the voltage supply rails and the DC offset voltage of the AC signal, various configurations can be used as described in Table 7.

The signal attenuation is defined in Equation 2.

$$Attenuation\ (\text{dB}) = 20 \times \log\left(\frac{R_{WB1} + R_W}{R_{AB}}\right) \quad (2)$$

where:
R_W is the wiper resistance.
R_{AB} is the end-to-end resistance value.
R_{WB1} is the resistor between the W1 and B1 terminals.

Table 7. AC Signal Attenuation Link Options

Voltage Supply	Maximum AC Signal Amplitude	Link	Position	Conditions
Single	V_{DD}	J1	Position 3 and 4 (AC + Bias)	No DC offset voltage. The AC signal is outside of the voltage supply rails due to the DC offset voltage or the DC offset voltage ≠ V_{DD}/2.[1]
			Position 5 and 6 (AC_Input)	All other conditions.
		J2	Position 3 and 4 (Bias)	Use in conjunction with the AC + bias link.
			Position 1 and 2 (GND)	All other conditions.
Dual	V_{DD}/V_{SS}	J1	Position 3 and 4 (AC + Bias)	The AC signal is outside the voltage supply rails due to the DC offset voltage, and the DC offset voltage ≠ 0 VDD.[1]
			Position 5 and 6 (AC_Input)	All other conditions.
		J2	Position 1 and 2 (GND)	Use in conjunction with the AC + bias link.
			Position 5 and 6 (Vss)	All other conditions.

[1] Recommended to ensure optimal total harmonic distortion (THD) performance.

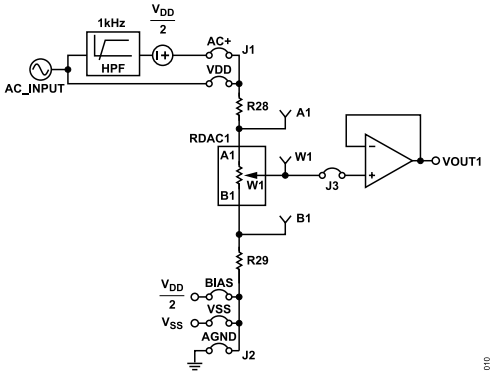

Figure 10. AC Signal Attenuator

EVALUATION BOARD HARDWARE

Signal Amplifier

The RDAC can be operated as an inverting or noninverting signal amplifier supporting linear or pseudologarithmic gains. Table 8 shows the available configurations. This test circuitry is connected to Channel 2.

The noninverting amplifier with linear gain is shown in Figure 11, and the gain is defined in Equation 3.

$$G = 1 + \frac{R_{WB2}}{R_{AW2}} \quad (3)$$

where:
R_{WB2} is the code loaded for the R_{WB2} resistance.
R_{AW2} is the code loaded for the R_{AW2} resistance.

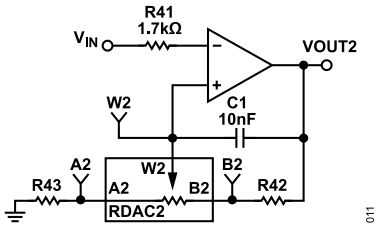

Figure 11. Linear Noninverting Amplifier

R17 and R19 can be used to set the maximum and minimum gain limits.

The noninverting amplifier with pseudologarithmic gain is shown in Figure 12, and the gain is defined in Equation 4.

$$G = 1 + \frac{RDAC2}{256 - RDAC2} \quad (4)$$

where *RDAC2* is the code loaded in the RDAC2.

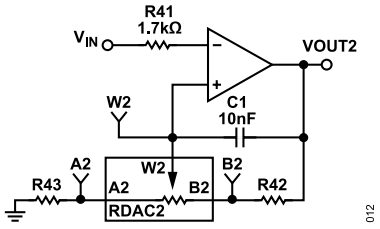

Figure 12. Pseudologarithmic Noninverting Amplifier

R17 and R19 can be used to set the maximum and minimum gain limits.

The inverting amplifier with linear gain is shown in Figure 13, and the gain is defined in Equation 5.

Note that the input signal, V_{IN}, must be negative.

$$G = -\frac{R_{WB2}}{R_{AW2}} \quad (5)$$

where:
R_{WB2} is the code loaded for the R_{WB2} resistance.
R_{AW2} is the code loaded for the R_{AW2} resistance.

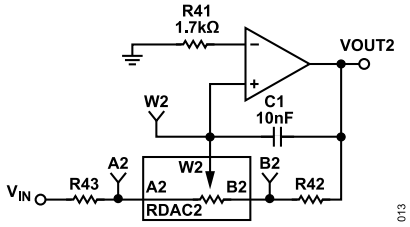

Figure 13. Linear Inverting Amplifier

R17 and R19 can be used to set the maximum and minimum gain limits.

The inverting amplifier with pseudologarithmic gain is shown in Figure 14, and the gain is defined in Equation 6.

$$G = -\frac{RDAC2}{256 - RDAC2} \quad (6)$$

where *RDAC2* is the code loaded in the RDAC2.

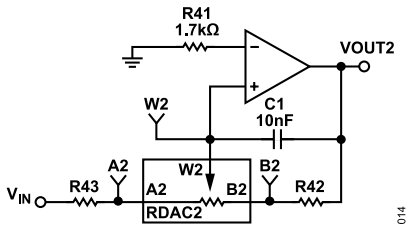

Figure 14. Pseudologarithmic Inverting Amplifier

R17 and R19 can be used to set the maximum and minimum gain limits.

Table 8. Amplifier Selection Link Options

Amplifier	Gain	Linear Setting Gain Mode Enabled	Link	Label
Noninverting	Linear	Yes	A7	LIN
			A6	N-INV
			A8	N-INV
	Pseudologarithmic	No	A7	LOG
			A6	N-INV
			A8	N-INV

EVALUATION BOARD HARDWARE

Table 8. Amplifier Selection Link Options (Continued)

Amplifier	Gain	Linear Setting Gain Mode Enabled	Link	Label
Inverting	Linear	Yes	A7	LIN
			A6	INV
			A8	INV
	Pseudologarithmic	No	A7	LOG
			A6	INV
			A8	INV

EVALUATION BOARD HARDWARE

Output Buffers

RDAC3 and RDAC4 can be connected to an output buffer as shown Figure 15 and Figure 16.

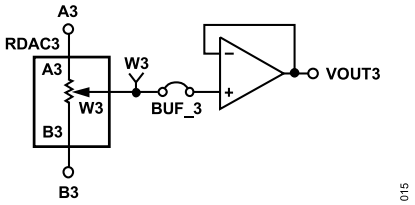

Figure 15. RDAC3

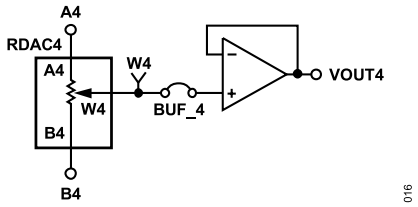

Figure 16. RDAC4

EVALUATION BOARD SCHEMATICS AND ARTWORK

EVAL-MB-LV-ARDZ (MOTHERBOARD)

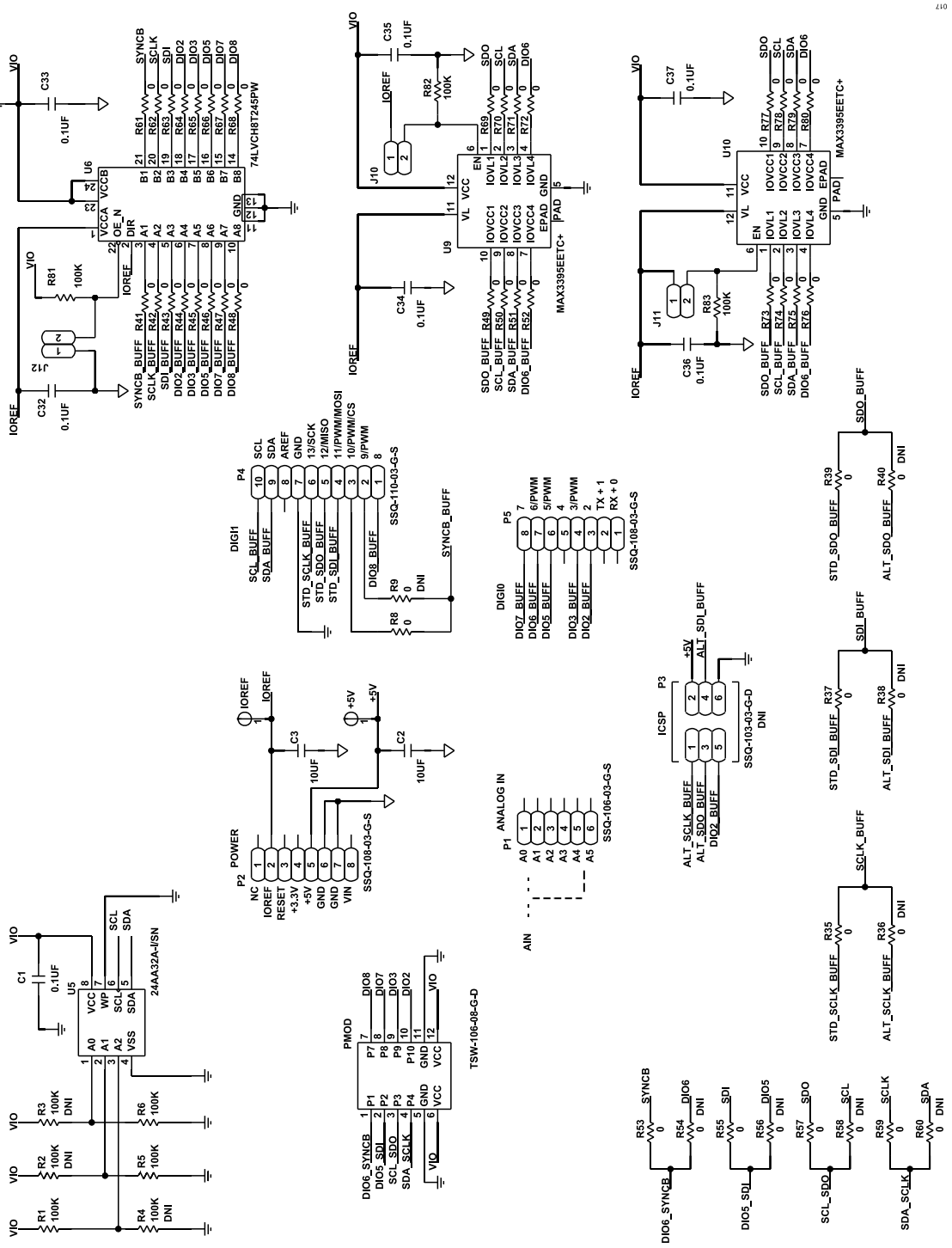

Figure 17. EVAL-MB-LV-ARDZ Schematic, SDP, Arduino-Compatible, PMOD Connectors, and Translators

EVALUATION BOARD SCHEMATICS AND ARTWORK

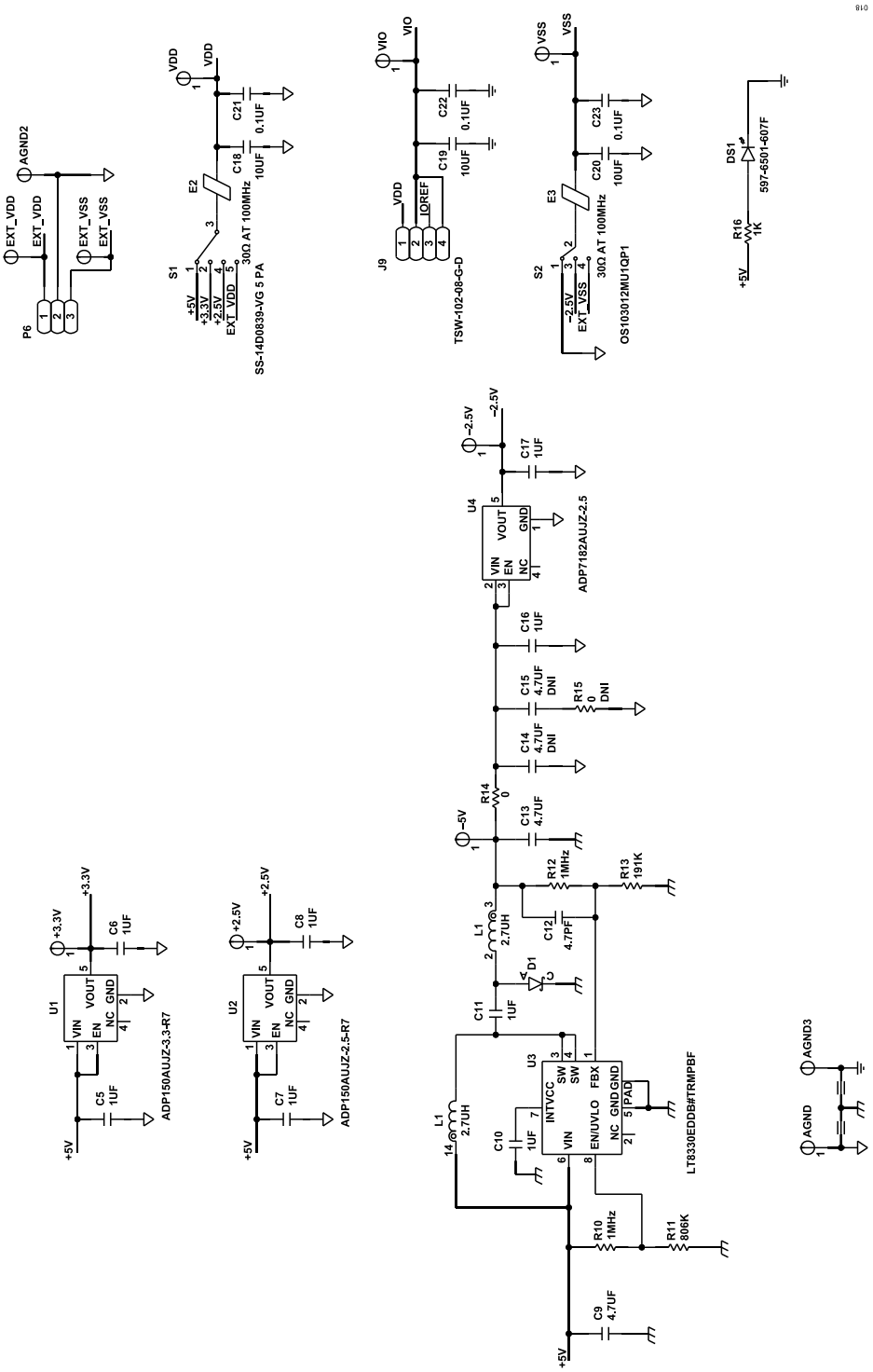

Figure 18. EVAL-MB-LV-ARDZ Schematic, Power Circuitry

EVALUATION BOARD SCHEMATICS AND ARTWORK

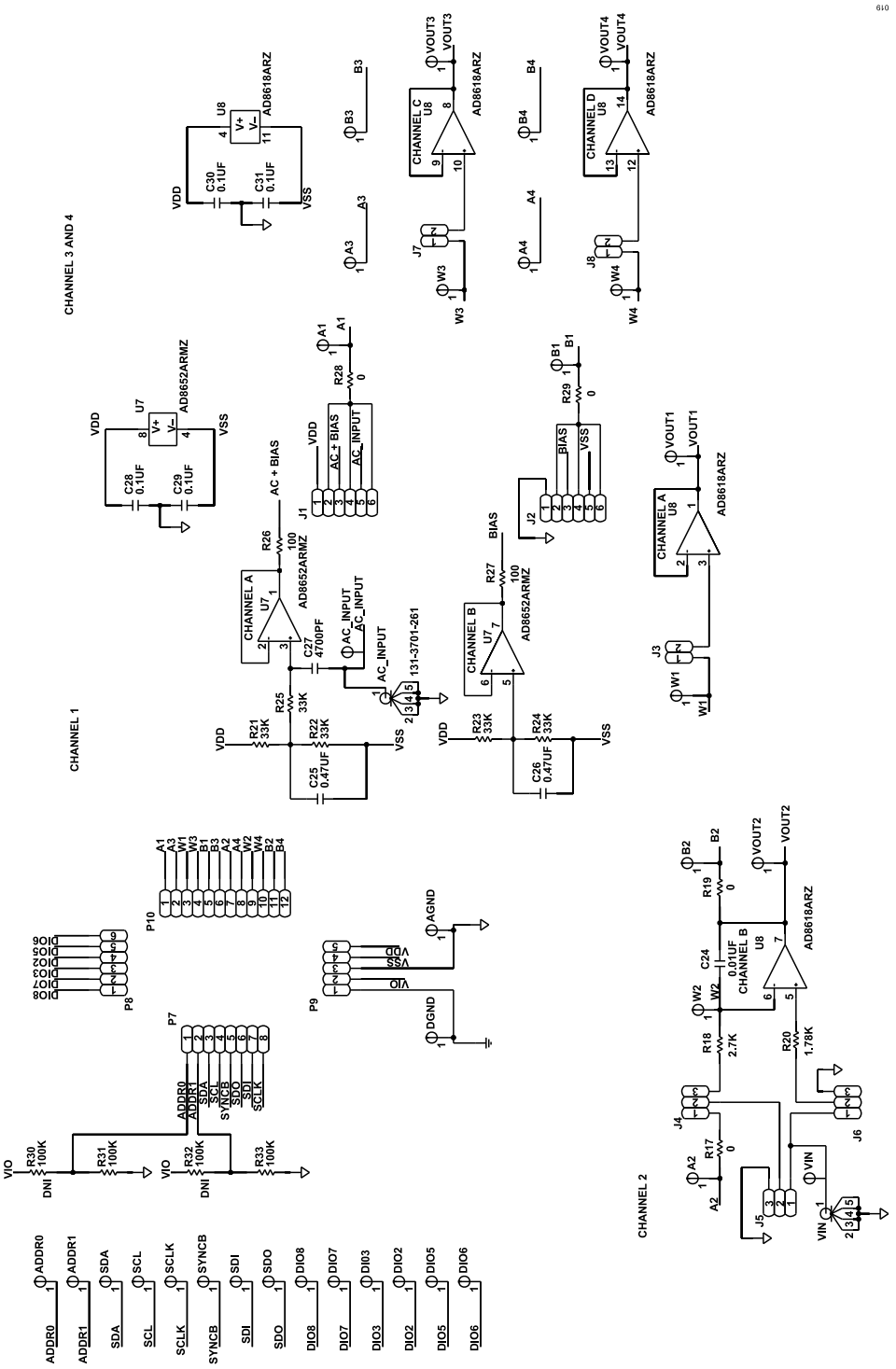

Figure 19. EVAL-MB-LV-ARDZ Schematic, Daughterboard Connectors, Test Points, and Output Circuitry

EVALUATION BOARD SCHEMATICS AND ARTWORK

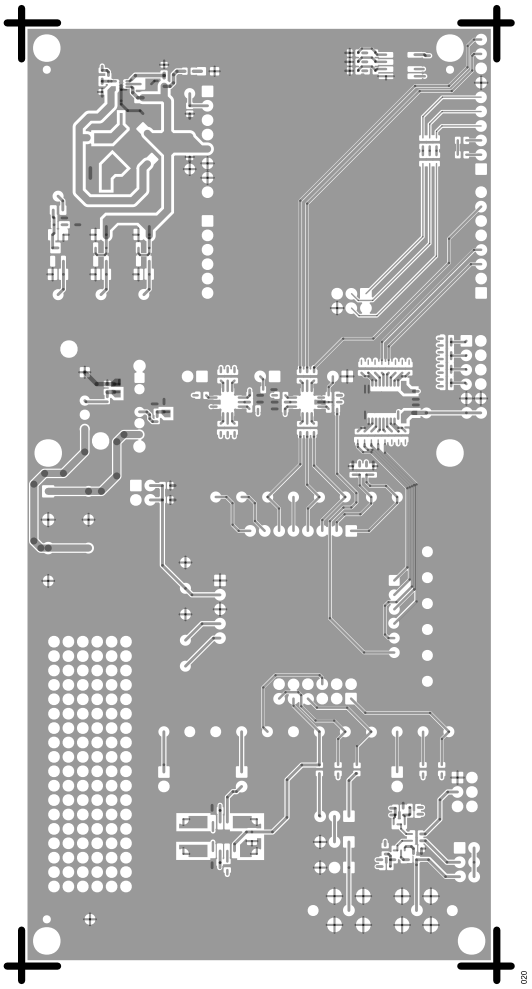

Figure 20. EVAL-MB-LV-ARDZ Board Layout L1 Primary

EVALUATION BOARD SCHEMATICS AND ARTWORK

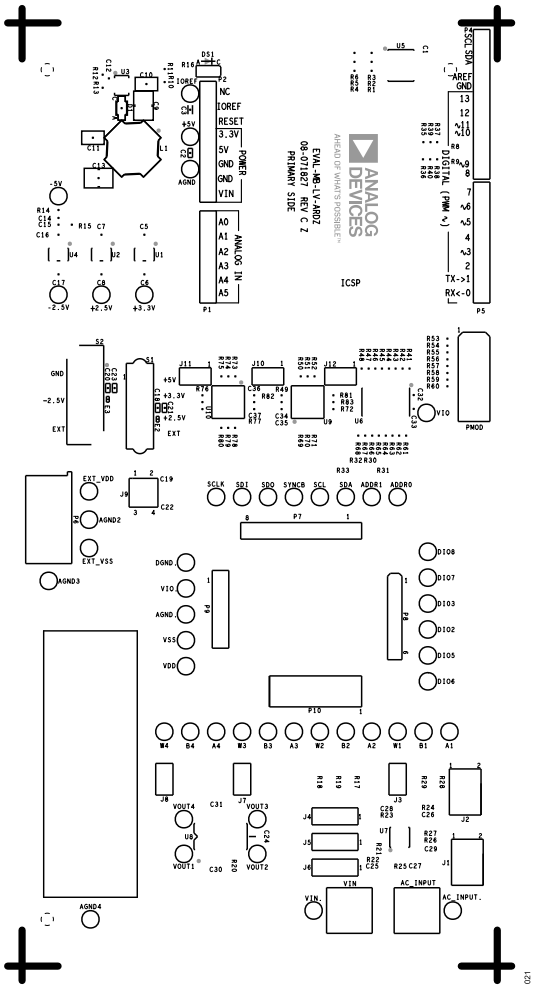

Figure 21. EVAL-MB-LV-ARDZ Board Layout Solder Mask Primary

EVALUATION BOARD SCHEMATICS AND ARTWORK

DAUGHTER BOARD

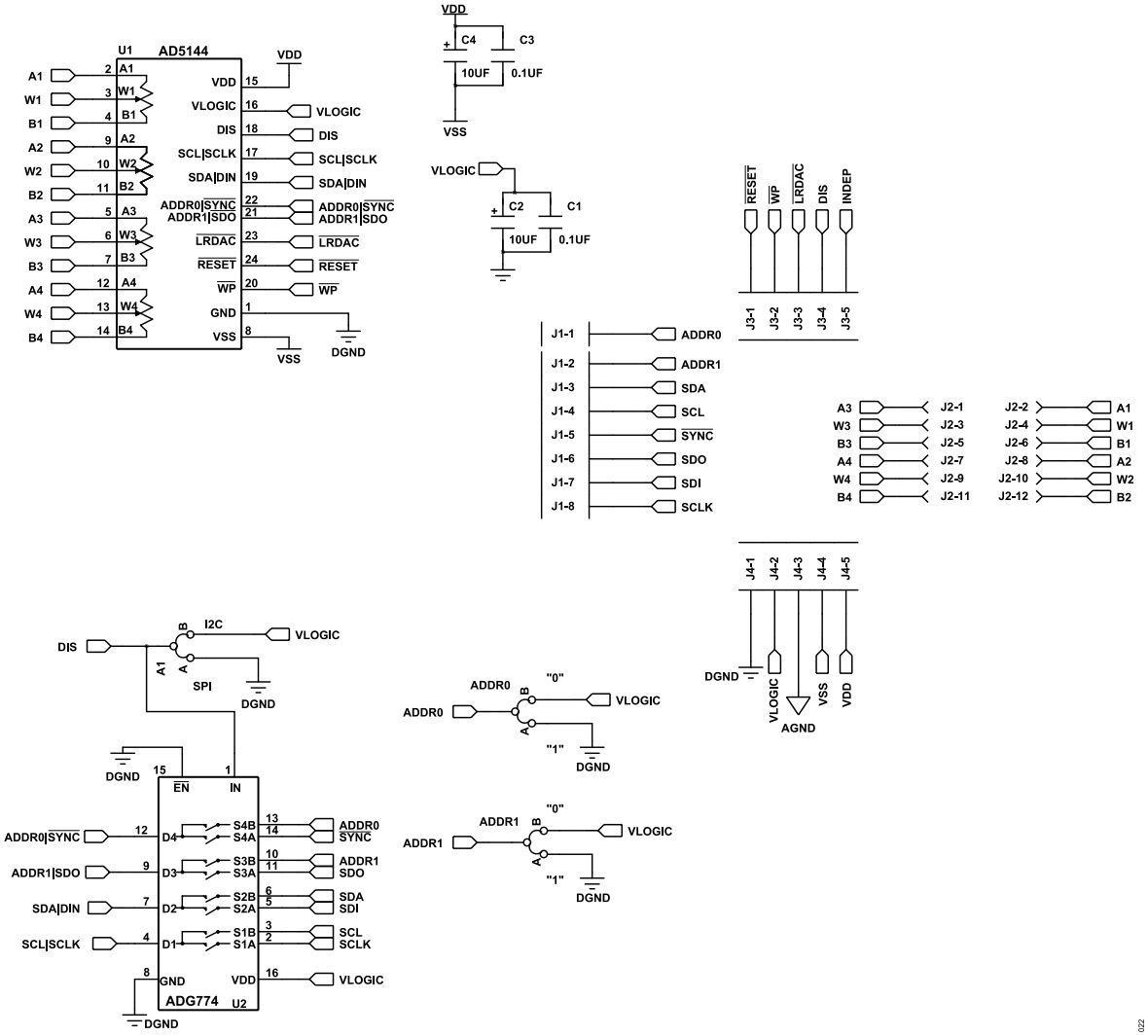

Figure 22. Schematic of the Daughter Board

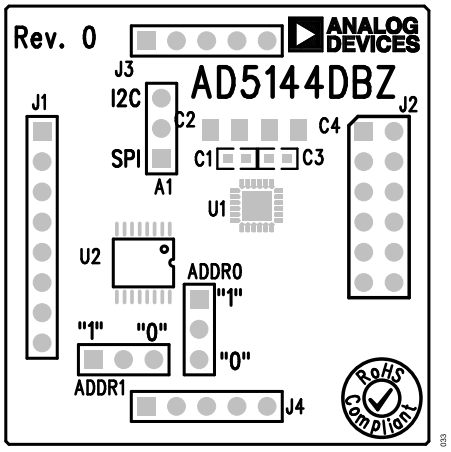

Figure 23. Component Side View of the Daughter Board

EVALUATION BOARD SCHEMATICS AND ARTWORK

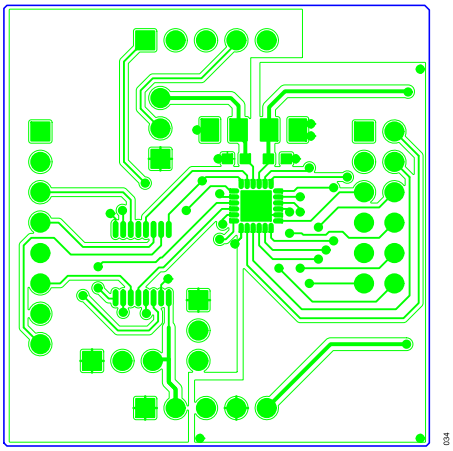

Figure 24. Component Placement Drawing of the Daughter Board

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions
By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Analog Way, Wilmington, MA 01887-2356, U.S.A. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed. All Analog Devices products contained herein are subject to release and availability.

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