Evaluating the AD5142A Digital Potentiometer

FEATURES

- Full featured evaluation board for the AD5142A in conjunction with low voltage digital potentiometer (digiPOT) motherboard (EVAL-MB-LV-ARDZ)
- Various test circuits
- Various power solutions
- Various AC/DC input signals
- PC control in conjunction with the Analog Devices, Inc., EVAL-SDP-CK1Z (SDP-K1) controller board

EVALUATION KIT CONTENTS

- EVAL-AD5142A-2DBZ: the AD5142A daughter board

HARDWARE REQUIRED

- EVAL-MB-LV-ARDZ digiPOT motherboard (purchased separately)
- EVAL-SDP-CK1Z (SDP-K1) controller board (purchased separately)
- PC running on Windows® 10 (32-bit or 64-bit) or later

SOFTWARE REQUIRED

- Analysis | Control | Evaluation (ACE) software, which is also available for download from the EVAL-AD5142A-2DBZ product page

GENERAL DESCRIPTION

This user guide describes the evaluation board for evaluating the AD5142A—a digital potentiometer with 256 positions and nonvolatile memory. With versatile programmability, the AD5142A allows multiple modes of operation, including read/write access in the RDAC and EEPROM registers, increment/decrement of resistance, resistance changes in ±6 dB scales, wiper setting readback, and extra electronically erasable programmable read-only memory (EEPROM) for storing user-defined information, such as memory data for other components or a lookup table.

The AD5142A supports a dual supply (±2.25V to ±2.75V) operation and a single supply (+2.3V to +5.5V) operation, making the device suitable for battery-powered applications and many other applications. The EVAL-MB-LV-ARDZ incorporates an internal power supply from the USB and provides on-board +5V, +3V, +2.5V/−2.5V supplies to the EVAL-AD5142A-2DBZ.

The EVAL-MB-LV-ARDZ interfaces with the USB port of a PC via the system demonstration platform (SDP-K1) controller board. The ACE software is available for download on the EVAL-AD5142A-2DBZ product page. This software enables the user to program the AD5142A. A peripheral module interface (PMOD) connection is also available that allows the connection of different microcontrollers to the EVAL-MB-LV-ARDZ without the SDP-K1 controller board. Note that when a microcontroller is used through the PMOD connection, the SDP-K1 board must be disconnected, and the user cannot use the ACE software.

Complete specifications for the AD5142A part can be found in the AD5142A data sheet, which is available from Analog Devices, and must be consulted in conjunction with this user guide when using the evaluation board.

TYPICAL EVALUATION SETUP

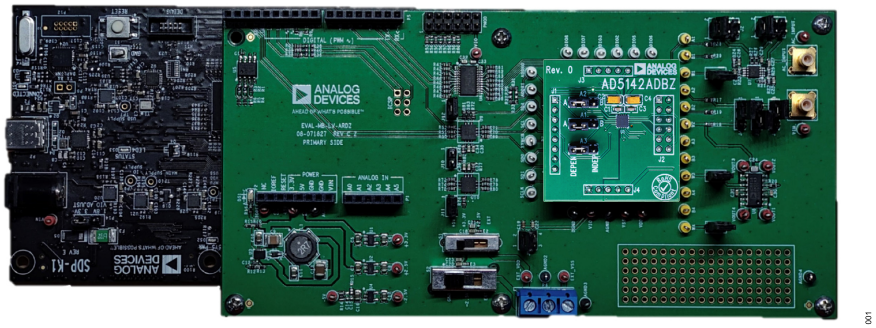

Figure 1. Digital Picture of Evaluation Board with Low Voltage DigiPOT Motherboard and System Demonstration Platform

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REVISION HISTORY

6/2025—Revision 0: Initial Version

EVALUATION BOARD SOFTWARE

INSTALLING ACE

The EVAL-AD5142A-2DBZ uses the ACE evaluation software that allows the evaluation and control of multiple evaluation systems.

The ACE installer comes with the necessary SDP-K1 drivers and the Microsoft® .NET Framework 4 by default. The ACE software is available for download from the ACE software page and must be installed before connecting the SDP-K1 board to the USB port of the PC to ensure that the SDP-K1 board is recognized as soon as it is connected to the PC. For full instructions on how to install and use this software, see the ACE software page on the Analog Devices website.

LOADING SDP-K1 FIRMWARE

A dedicated firmware to control the EVAL-AD5142A-2DBZ is required to be loaded to the SDP-K1. Right click the .bin file and send to the drive name **SDP-K1**, see Figure 2. A dialog box pops up showing the progress which takes a few seconds. The dialog box automatically disappears once the firmware is loaded.

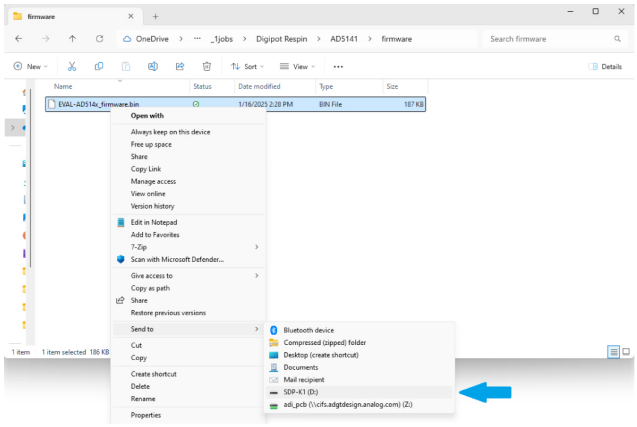

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Figure 2. Loading SDP-K1 Firmware

INSTALLING THE EVAL-AD5142A-2DBZ PLUGIN

A plugin for the EVAL-AD5142A-2DBZ is required to be installed on ACE to communicate with the firmware loaded on SDP-K1. To install the plugin, take the following steps:

1. Connect the evaluation board to the SDP-K1 board, and connect the USB cable between the SDP-K1 board and the PC.
2. Open ACE, go to **Plug-in Manager**. A dialog box occasionally pops up asking to reprogram the SDP-K1 with a standard firmware, always select **No** or **Cancel** as shown in Figure 3.

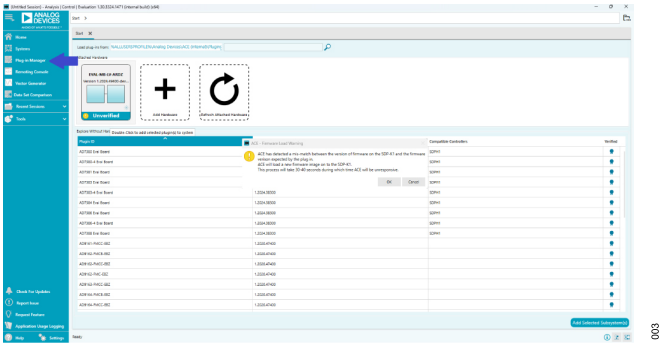
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Figure 3. Opening Plug-in Manager

3. Within **Plug-in Manager**, go to **Available Packages** and search for **Board.ADDigipots**. Select the available plugin and click **Install Selected**, see Figure 4.

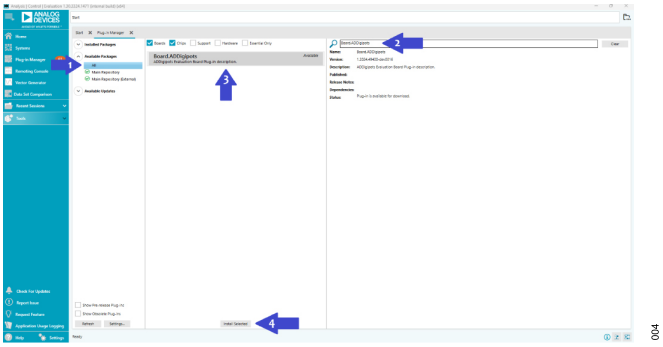
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Figure 4. Installing Board.ADDigipots Plugin

INITIAL SETUP

To set up the evaluation board, take the following steps:

1. Connect the evaluation board to the SDP-K1 board, and then connect the USB cable between the SDP-K1 board and the PC.
2. Load the SDP-K1 firmware.
3. Run the ACE application. The **EVAL-MB-LV-ARDZ** plug-in appears in the **Attached Hardware** section of the **Start** tab.

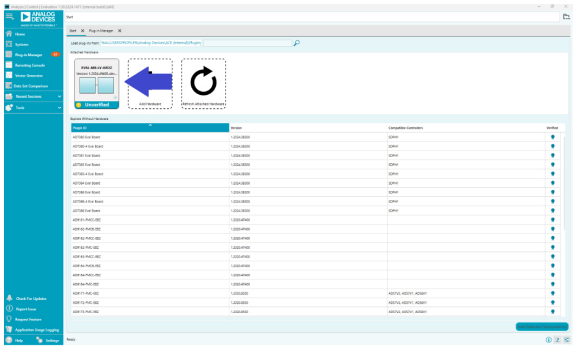
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Figure 5. EVAL-MB-LV-ARDZ as Attached Hardware

4. Double-click the board plug-in to open the board view. If the correct firmware in the SDP-K1 controller is missing or does not match, a dialogue box pops up and gives the option to flash the correct firmware. Click **Cancel** if the firmware is already loaded.

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5. In the **Device system_config Attributes** section, set the following information:
   a. **device_generic: AD5142A**
   b. **operating_mode: potentiometer**

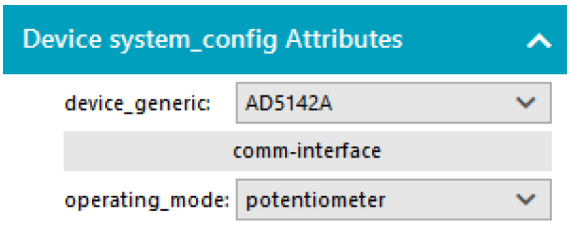

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Figure 6. Device System_Config Attributes

6. Click on **Reconfigure System** at the bottom of the system configuration window. The **System Config Summary** shows up, then click **Modify**.

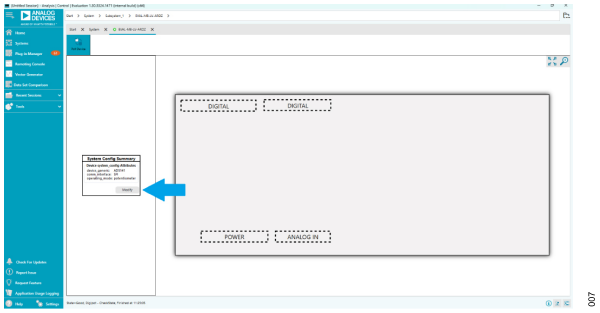

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Figure 7. EVAL-MB-LV-ARDZ Board View Configuration Window

7. Restart the ACE software and repeat step 4. Double click the block the **Digipot** block shown in the board view.

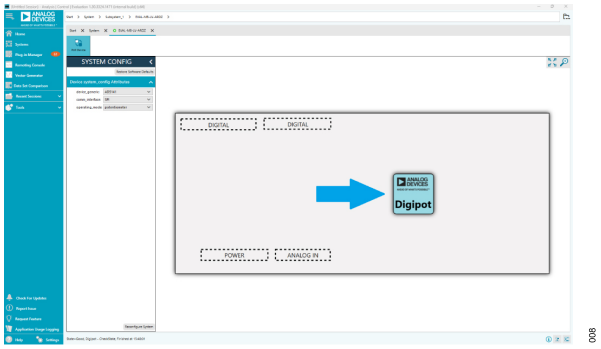

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Figure 8. EVAL-MB-LV-ARDZ Board View to Chip View

8. Change the values you want to modify and press the enter key to send it to the device.

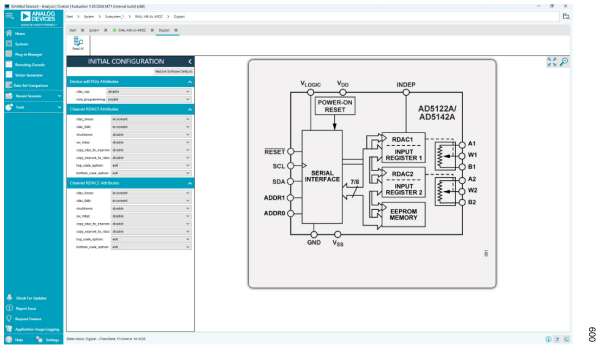

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Figure 9. Chip View

For more information about the ACE functionality for AD5142A, refer to the markdown documentation in ACE software.

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POWER SUPPLIES

The EVAL-MB-LV-ARDZ motherboard provides both on-board single (+5V, +3.3V) and dual (+2.5V/−2.5V) power supplies. Users can choose between voltages using S1 and S2. The output of S1 is connected to V_{DD} while S2 is connected to V_{SS}. For safety precaution, use the switch only if there is no power connected to the motherboard. V_{LOGIC} is connected to V_{DD} via J9 jumper pins by default. For the switch options, see Table 1.

The EVAL-AD5142A-2DBZ can also be powered externally through the P6 connectors if a different voltage supply is needed or if the PMOD connector is used, as described in Table 2. Remove the shunt connection of J9 if external supply is used.

All supplies are decoupled to ground using 10µF and 0.1µF capacitors.

Table 1. On-Board Power Supply Switch Options

Switch	Position	Option
S1	1	5V
	2	3.3V (default)
	3	2.5V
	4	EXT_VDD
S2	1	GND (default)
	2	−2.5V
	3	EXT_VSS

Table 2. External Power Supply Connectors

Connector Label	Voltage
EXT_VDD	External analog positive power supply. Recommended supply is +15 V.
GND	Ground.
EXT_VSS	External analog negative power supply. Recommended supply is −15 V.

LINK OPTIONS

Several link and switch options are incorporated in the EVAL-MB-LV-ARDZ motherboard, and EVAL-AD5142A-2DBZ daughterboard, and must be set up before using the board. The default positions of the links are configured to control the evaluation board via the SDP-K1 board using a PC. The functions of these link options are described in Table 3.

The EVAL-AD5142A-2DBZ has many on-board configuration options. One option is the ability to switch between I^2C and SPI as its communication interface via the A2 link. For more information, refer to Table 4.

Table 3. Motherboard Link Functions

Link No.	Option
J9	This link selects the V_{LOGIC} connection Position 1−2 Connects V_{LOGIC} to V_{DD} (default)
	Position 3−4 Connects V_{LOGIC} to IO_{REF} pin from SDP-K1
J10	Enables the step down translator for open drain lines Must be disconnected if V_{DD} is greater than 3.3 V (default) Must be connected if V_{DD} is less than 3.3V
J11	Enables the step up translator for open drain lines Must be connected if $V_{DD}$is greater than 3.3V (default) Must be disconnected if V_{DD} is less than 3.3V
J12	Enables the translator for push-pull lines Must be connected when using SDP-K1 (default) Must be disconnected when using PMOD

Table 4. Daughterboard Link Functions

Link No.	Option	Description
A1	A | B	See Table 5
A2	A | B	See Table 5
A3	DEPEN (default) INDEP	DGND (Potentiometer mode) V_{LOGIC} (Linear Gain Setting mode)

Table 5. I^2C Address Selection

A1 Jumper Position	A2 Jumper Position	Device Address
A	A	0101111 (default)
A	B	0100011
B	A	0101100
B	B	0100000

TEST CIRCUITS

The EVAL-MB-LV-ARDZ incorporates several test circuits in the output to evaluate the performance of the AD5142A in typical applications.

DAC

The digiPOT can be operated as a digital-to-analog converter (DAC), as shown in Figure 10. Table 6 describes the options available for the voltage references. This test circuitry is connected to Channel 1.

The output voltage is defined in Equation 1.

$$V_{OUT} = \left(V_A - V_B\right) \times \frac{RDAC1}{256} \quad (1)$$

where:
RDAC1 is the code loaded in the RDAC1 register.

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V_A is the voltage applied to Terminal A via J1.
V_B is the voltage applied to Terminal B via J2.

However, by changing the R28 and R29 external resistor values, the user can reduce the voltage of the voltage references. In this case, use the A1 and B1 test points to measure the voltage applied to Terminal A and Terminal B, and to recalculate V_A and V_B in Equation 1.

Table 6. DAC Voltage References

Terminal	Link	Position	Description
A1	J1	1 and 2	Connects Terminal A1 to V_{DD}
		3 and 4	Connects Terminal A1 to $V_{DD}/2$. Do not apply AC signal.
W1	J3		Connects Terminal W1 to an output buffer
B1	J2	1 and 2	Connects Terminal B1 to $V_{DD}/2$
		3 and 4	Connects Terminal B1 to V_{SS}
		5 and 6	Connects Terminal B1 to analog ground

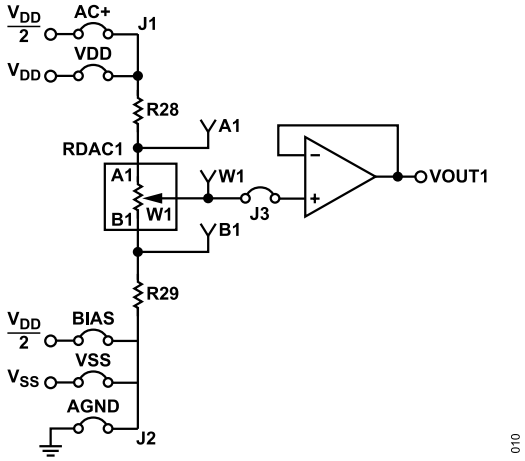

Figure 10. DAC

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AC Signal Attenuation

The RDAC can be used to attenuate an AC signal, which must be provided externally using the AC_INPUT connector, as shown in Figure 11.

Depending on the voltage supply rails and the DC offset voltage of the AC signal, various configurations can be used as described in Table 7.

The signal attenuation is defined in Equation 2.

$$Attenuation\ (\mathrm{dB}) = 20 \times \log\left(\frac{R_{WB1} + R_W}{R_{AB}}\right) \quad (2)$$

where:
R_W is the wiper resistance.
R_{AB} is the end-to-end resistance value.
R_{WB1} is the resistor between Terminal W1 and Terminal B1.

Table 7. AC Signal Attenuation Link Options

Voltage Supply	Maximum AC Signal Amplitude	Link	Position	Conditions
Single	V_{DD}	J1	3 and 4 (AC + BIAS)	No DC offset voltage; the AC signal is outside the voltage supply rails due to the DC offset voltage; or the DC offset voltage ≠ $V_{DD}/2$.[1]
			5 and 6 (AC_INPUT)	All other conditions.
		J2	3 and 4 (BIAS)	Use in conjunction with the AC + BIAS link.
			1 and 2 (AGND)	All other conditions.
Dual	V_{DD}/V_{SS}	J1	3 and 4 (AC + BIAS)	The AC signal is outside the voltage supply rails due to the DC offset voltage; the DC offset voltage ≠ 0 V_{DD}.[1]
			5 and 6 (AC_INPUT)	All other conditions.
		J2	1 and 2 (AGND)	Use in conjunction with the AC + BIAS link.
			5 and 6 (V_{SS})	All other conditions.

[1] Recommended to ensure optimal total harmonic distortion (THD) performance.

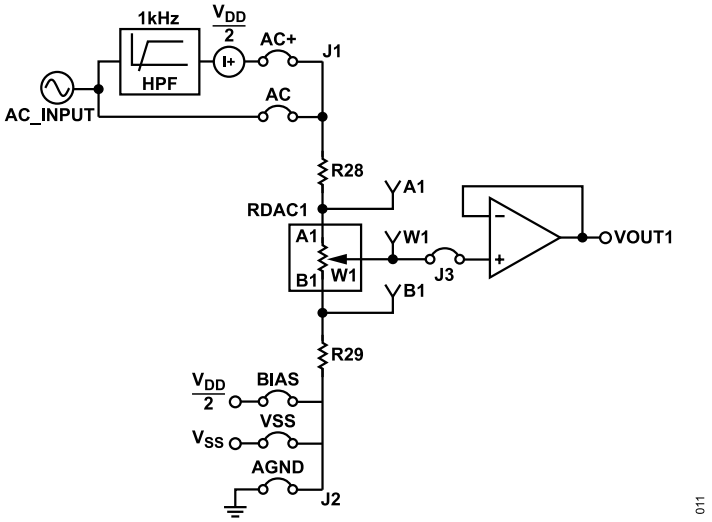

Figure 11. AC Signal Attenuator

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Signal Amplifier

The RDAC can be operated as an inverting or noninverting signal amplifier supporting linear or pseudologarithmic gains. Table 8 shows the available configurations. This test circuitry is connected to Channel 2.

The noninverting amplifier with linear gain is shown in Figure 12, and the gain is defined in Equation 3.

$$G = 1 + \frac{R_{WB2}}{R_{AW2}} \quad (3)$$

where:
R_{WB2} is the code loaded for the R_{WB2} resistance.
R_{AW2} is the code loaded for the R_{AW2} resistance.

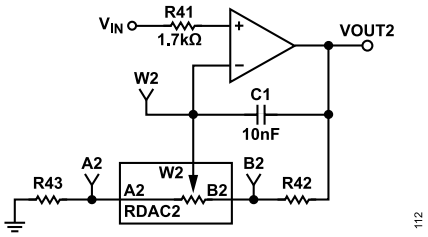

Figure 12. Linear Noninverting Amplifier

R17 and R19 can be used to set the maximum and minimum gain limits.

The noninverting amplifier with pseudologarithmic gain is shown in Figure 13, and the gain is defined in Equation 4.

$$G = 1 + \frac{RDAC2}{256 - RDAC2} \quad (4)$$

where: *RDAC2* is the code loaded in the RDAC2.

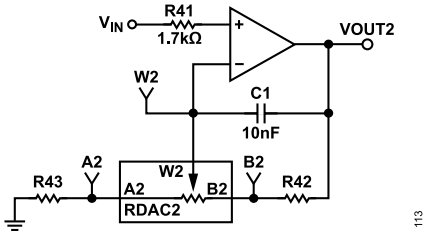

Figure 13. Pseudologarithmic Noninverting Amplifier

R17 and R19 can be used to set the maximum and minimum gain limits.

The inverting amplifier with linear gain is shown in Figure 14, and the gain is defined in Equation 5.

Note that the input signal, V_{IN}, must be negative.

$$G = -\frac{R_{WB2}}{R_{AW2}} \quad (5)$$

- where:
- R_{WB2} is the code loaded for the R_{WB2} resistance.
- R_{AW2} is the code loaded for the R_{AW2} resistance.

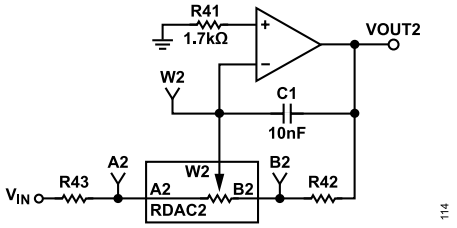

Figure 14. Linear Inverting Amplifier

R17 and R19 can be used to set the maximum and minimum gain limits.

The inverting amplifier with pseudologarithmic gain is shown in Figure 15, and the gain is defined in Equation 6.

$$G = -\frac{RDAC2}{256 - RDAC2} \quad (6)$$

where: *RDAC2* is the code loaded in the RDAC2.

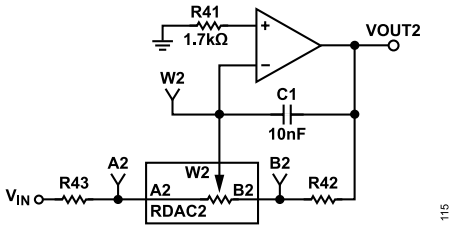

Figure 15. Pseudologarithmic Inverting Amplifier

R17 and R19 can be used to set the maximum and minimum gain limits.

Table 8. Amplifier Selection Link Options

Amplifier	Gain	Linear Setting Gain Mode Enabled	Link	Label
Noninverting	Linear	Yes	A7	LIN
			A6	N-INV
			A8	N-INV
	Pseudologarithmic	No	A7	LOG
			A6	N-INV
			A8	N-INV
Inverting	Linear	Yes	A7	LIN
			A6	INV

EVALUATION BOARD HARDWARE

Table 8. Amplifier Selection Link Options (Continued)

Amplifier	Gain	Linear Setting Gain Mode Enabled	Link	Label
			A8	INV
	Pseudologarithmic	No	A7	LOG
			A6	INV
			A8	INV

EVALUATION BOARD SCHEMATICS AND ARTWORK

EVAL-MB-LV-ARDZ (MOTHERBOARD)

ARDUINO UNO SHIELD (REV B)

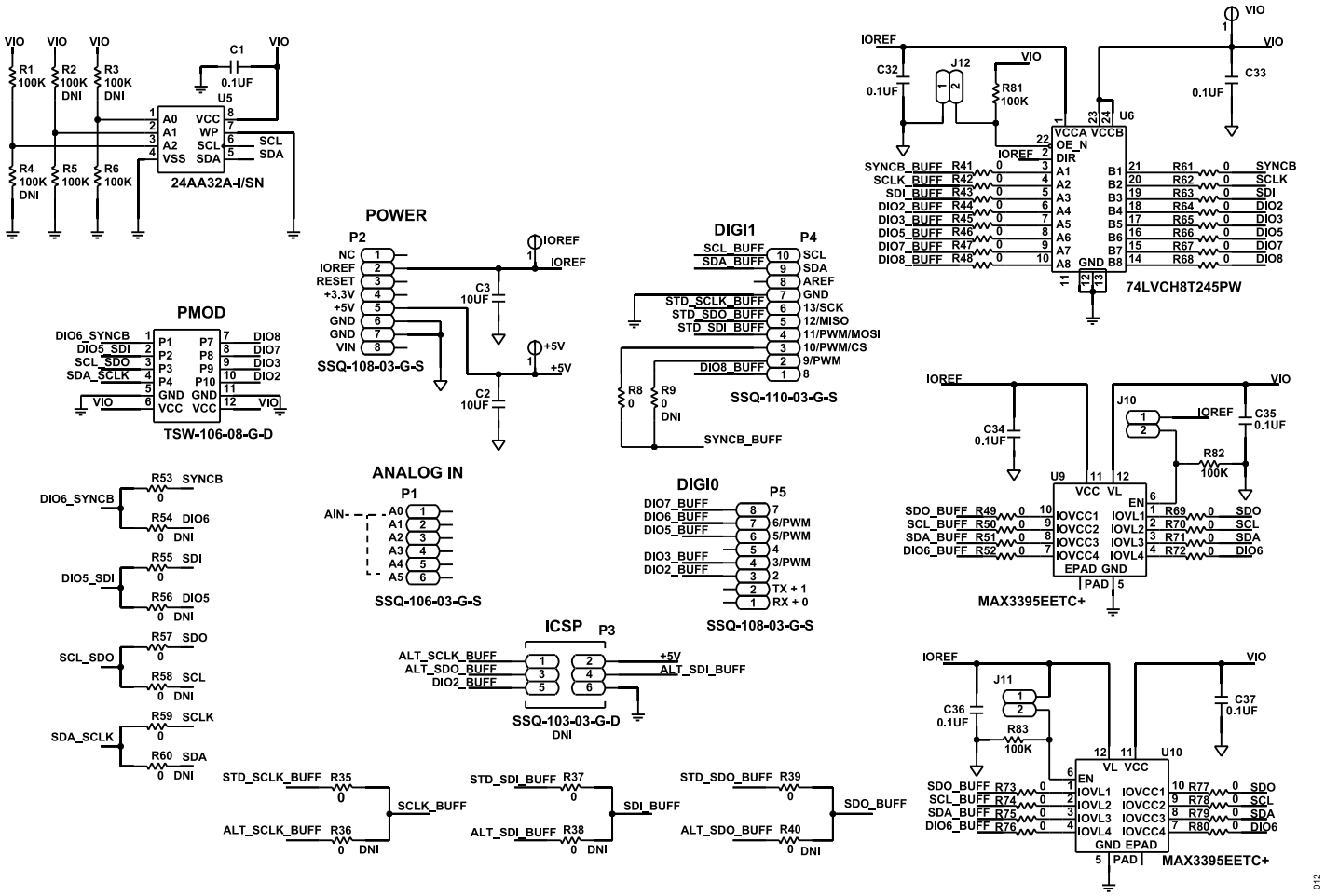

Figure 16. EVAL-MB-LV-ARDZ Schematic, SDP, Arduino-Compatible, PMOD Connectors, and Translators

EVALUATION BOARD SCHEMATICS AND ARTWORK

POWER CIRCUITRY

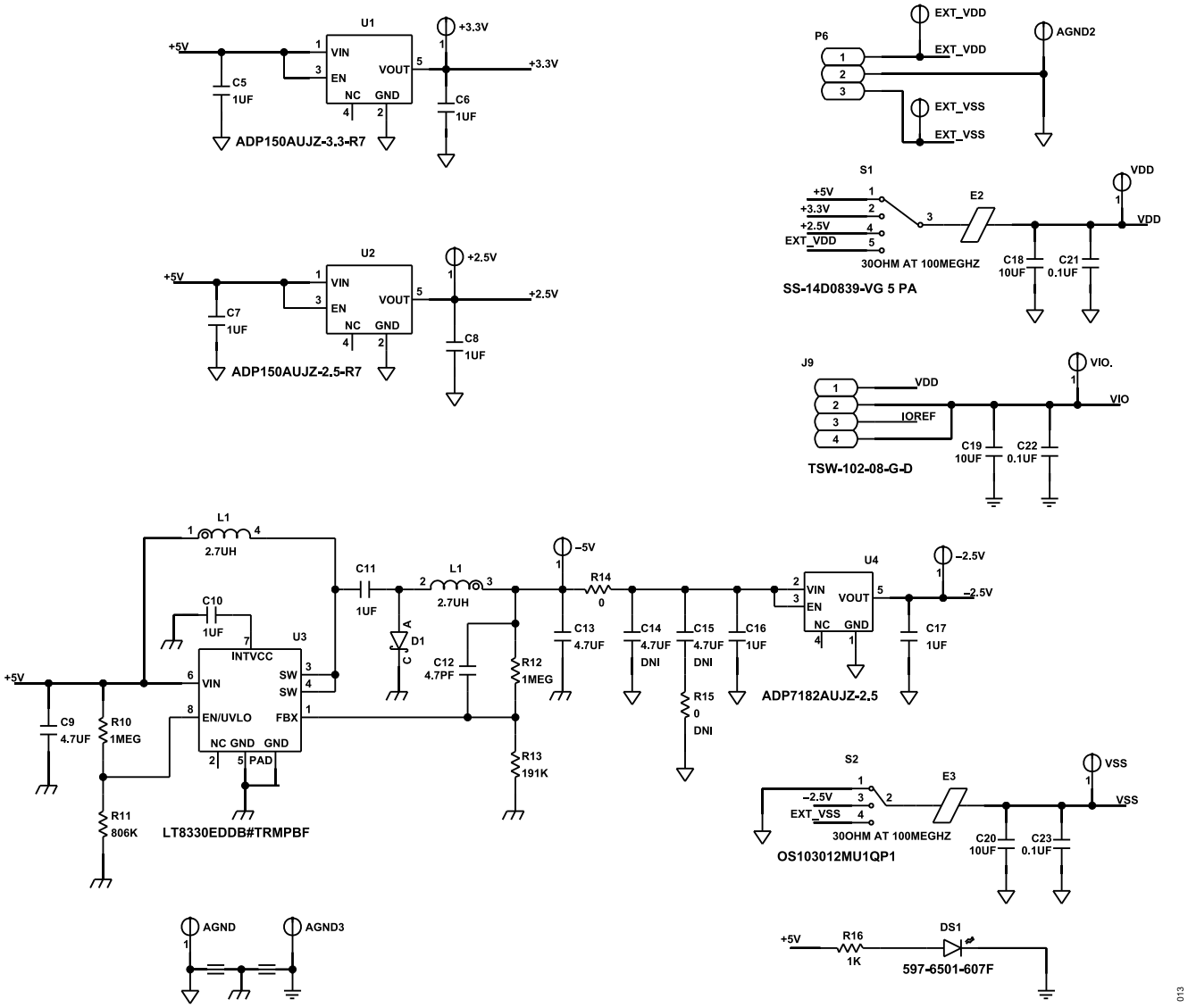

Figure 17. EVAL-MB-LV-ARDZ Schematic, Power Circuitry

EVALUATION BOARD SCHEMATICS AND ARTWORK

CONNECTORS AND OUTPUT CIRCUITRY

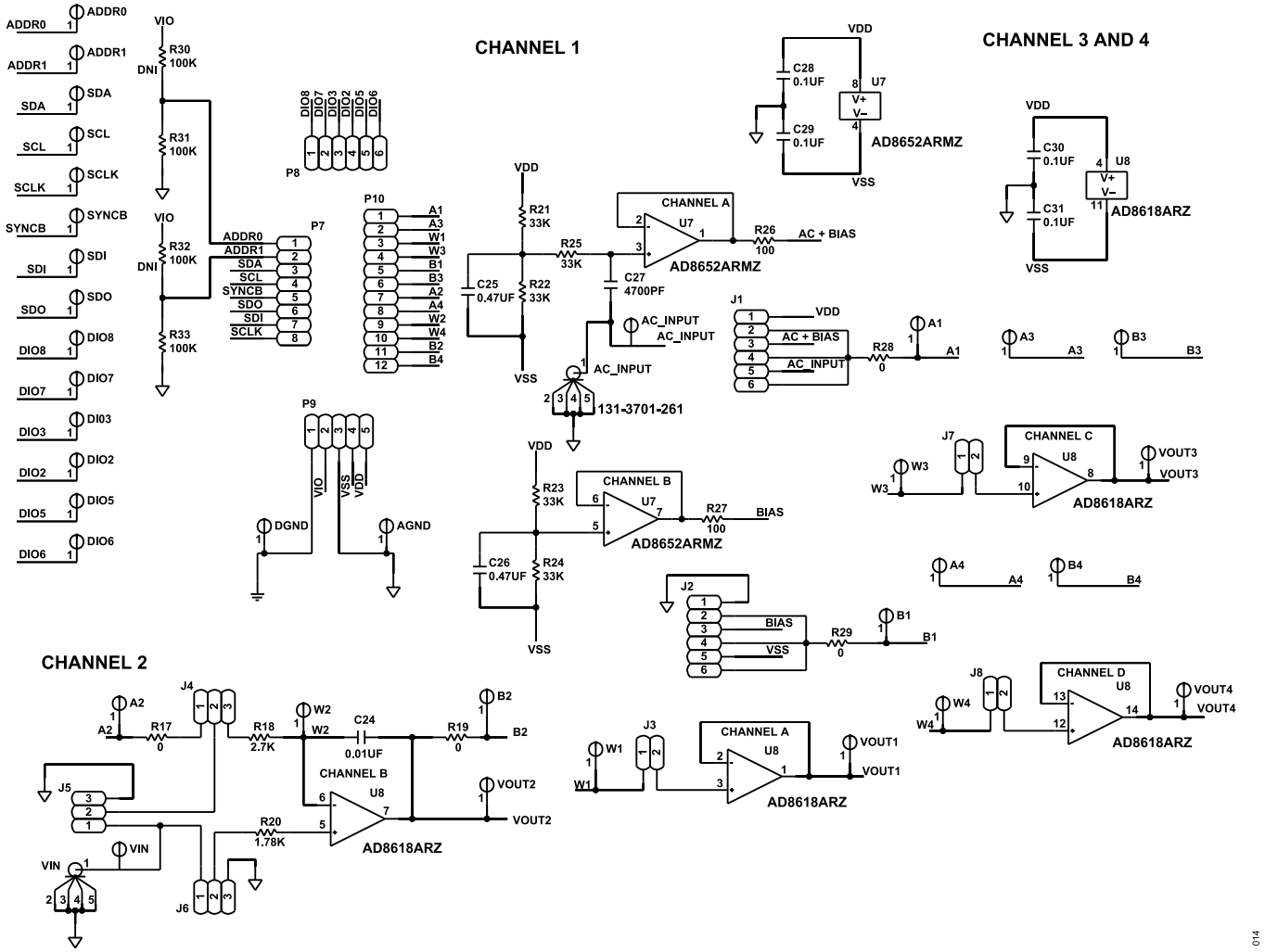

Figure 18. EVAL-MB-LV-ARDZ Schematic, Daughter Board Connectors, Test Points, and Output Circuitry

EVALUATION BOARD SCHEMATICS AND ARTWORK

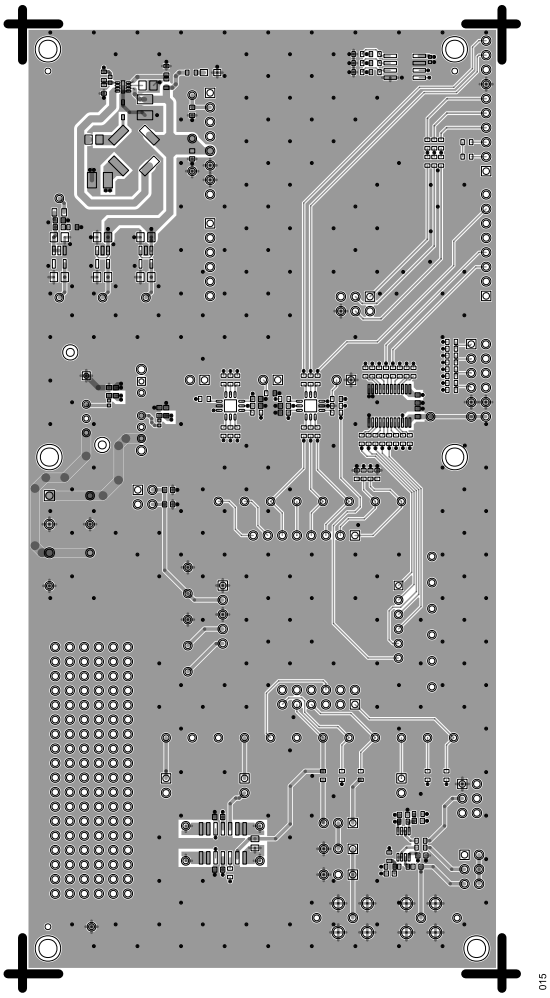

Figure 19. EVAL-MB-LV-ARDZ Board Layout L1 Primary

EVALUATION BOARD SCHEMATICS AND ARTWORK

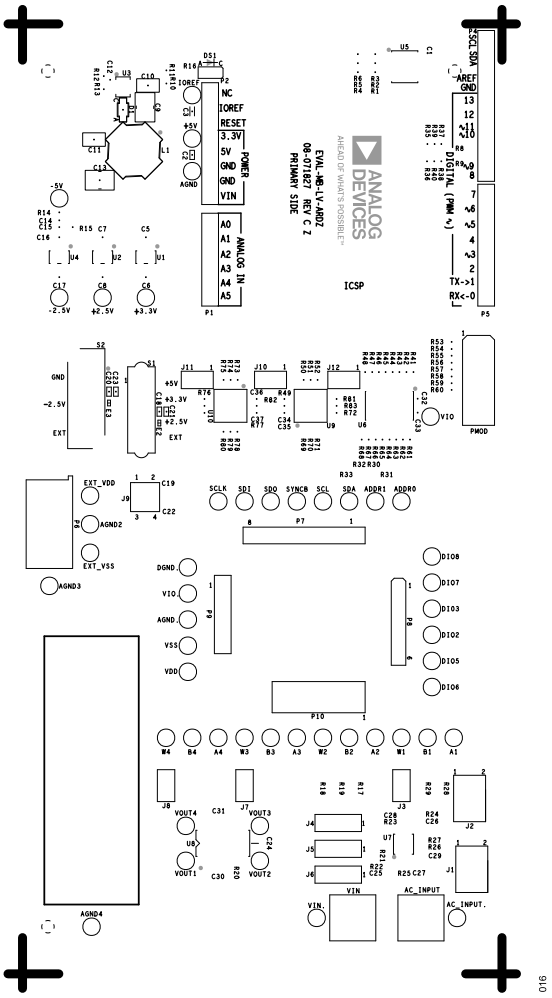

Figure 20. EVAL-MB-LV-ARDZ Board Layout Solder Mask Primary

EVALUATION BOARD SCHEMATICS AND ARTWORK

EVAL-AD5142A-2DBZ DAUGHTER BOARD

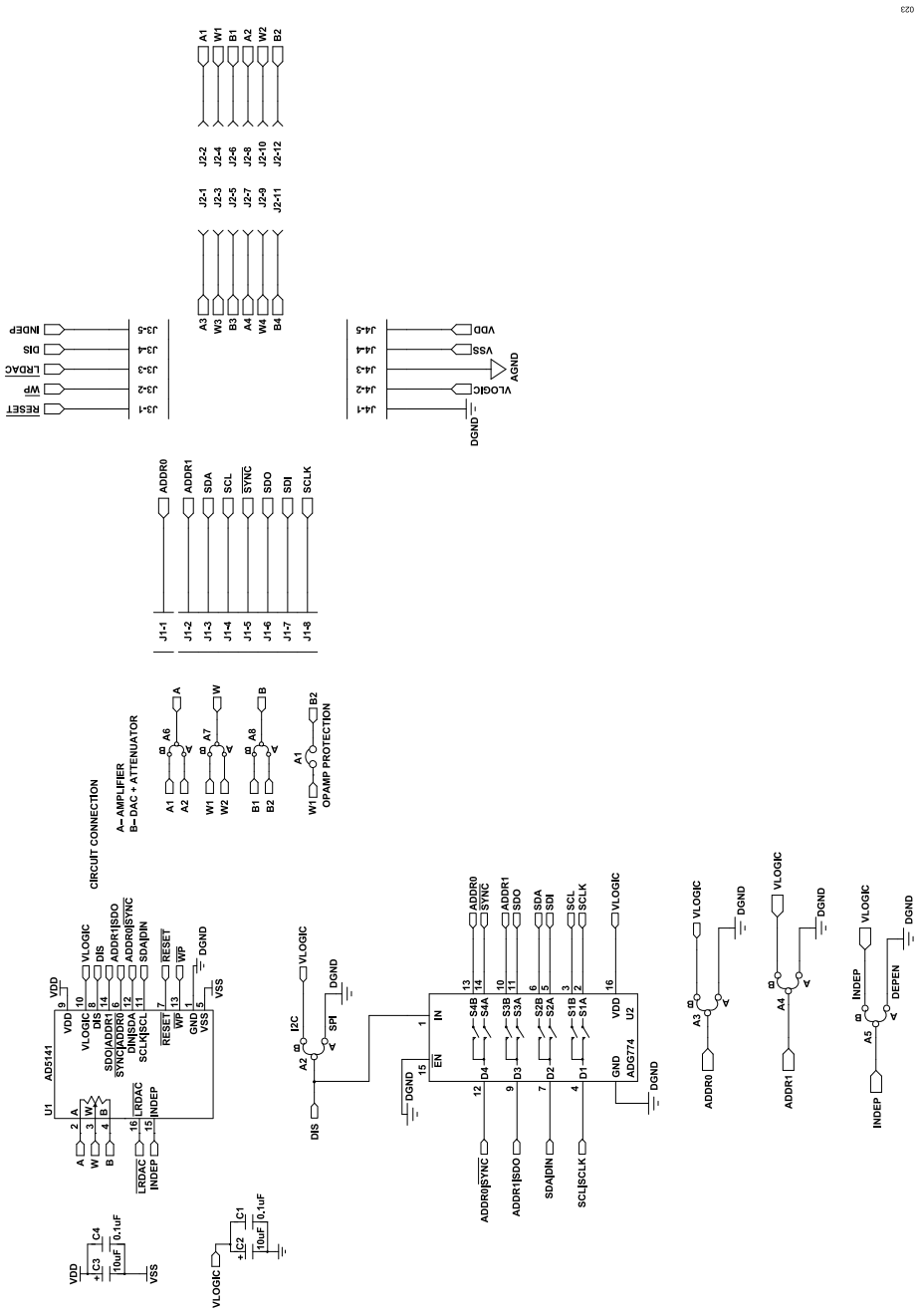

Figure 21. Schematic of EVAL-AD5142A-2DBZ

EVALUATION BOARD SCHEMATICS AND ARTWORK

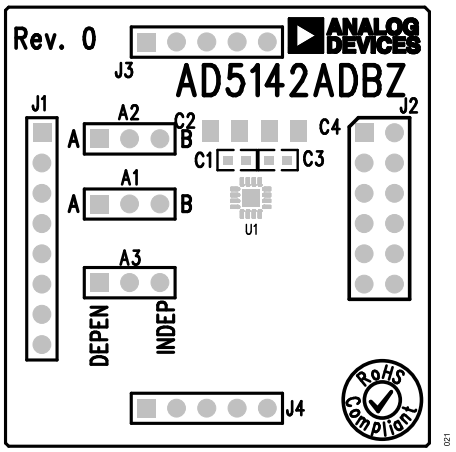

Figure 22. Component Side View of EVAL-AD5142A-2DBZ

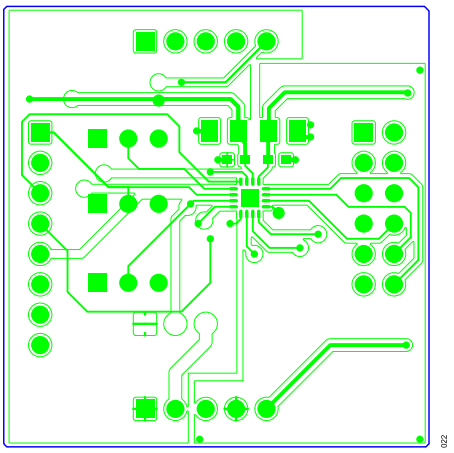

Figure 23. Component Placement Drawing of EVAL-AD5142A-2DBZ

ORDERING INFORMATION

BILL OF MATERIALS

Table 9. Motherboard

Qty	Reference Designator	Description	Sourcing
18	+2.5V, +3.3V, +5V, −2.5V, −5V, AC_INPUT, EXT_VDD, EXT_VSS, IOREF, VDD, VIN, VIO, VIO, VOUT1, VOUT2, VOUT3, VOUT4, VSS	Connector-PCB test point red	Generic
12	A1, A2, A3, A4, B1, B2, B3, B4, W1, W2, W3, W4 W2, W3, W4	Connector-PCB test point yellow	Generic
2	AC_INPUT, VIN	Connector-PCB coax surface-mount device (SMD) jack RF vertical pin center male connector (PCMNT) gold	Generic
14	ADDR0, ADDR1, DI03, DIO2, DIO5, DIO6, DIO7, DIO8, SCL, SCLK, SDA, SDI, SDO, SYNCB	Connector-PCB test point white	Generic
6	AGND, AGND., AGND2, AGND3, AGND4, DGND	Connector-PCB test point blank	Generic
1	C1	Ceramic capacitor 0.1µF 16V 10% X7R 0402 AEC-Q200	Generic
8	C5, C6, C7, C8, C10, C11, C16, C17	Ceramic capacitor 1µF 50V 10% X7R 0805 AEC-Q200	Generic
1	C12	Silicon capacitor 4.7pF 25V 0.1pF 0402 AEC-Q200	Generic
2	C9, C13	Ceramic capacitor 4.7µF 50V 10% X7R 1210 AEC-Q200	Generic
5	C2, C3, C18, C19, C20	Ceramic capacitor 10µF 16V 10% X5R 0603	Generic
9	C21, C22, C23, C32, C33, C34, C35, C36, C37	Ceramic capacitor 0.1µF 50V 10% X7R 0603	Generic
1	C24	Ceramic capacitor 0.01µF 50V 5% C0G 0805	Generic
2	C25, C26	Ceramic capacitor 0.47µF 25V 10% X7R 0603	Generic
1	C27	Ceramic capacitor 4700pF 50V 10% X7R 0603	Generic
4	C28, C29, C30, C31	Ceramic capacitor 0.1µF 16V 10% X7R 0603	Generic
1	D1	Dio Schottky barrier rectifier, 1A	Generic
1	DS1	LED 570nm SMD (green)	Generic
2	E2, E3	Inductor-chip ferrite bead	Generic
2	J1, J2	Connector-PCB 6 position male HDR unshrouded 0.635mm square post double row 5.84mm mating post, 2.54mm solder tail, 2.54mm pitch	Generic
6	J3, J7, J8, J10, J11, J12	Connector-PCB HDR two pin dual straight	Generic
3	J4, J5, J6	Connector-PCB 3 position male HDR unshrouded 0.635mm square post single row 5.84mm mating post, 2.54mm solder tail, 2.54mm pitch	Generic
1	J9	Connector-PCB HEADER 4P ST	Generic
1	L1	Inductor-power shielded wirewound 2.7µH 30% 100kHz 1.85A 0.0805Ω DCR	Generic
1	P1	Connector-PCB receptacle 25mil square post 2.54mm pitch	Generic
1	P10	Connector-PCB receptacle 12 position dual row	Generic
2	P2, P5	Connector-PCB receptacle 25mil square post 2.54mm pitch	Generic
1	P4	Connector-PCB receptacle 25mil square post 2.54mm pitch	Generic
1	P6	Connector 5mm pitch, terminal block (RA 16-22AWG) 3 position	Generic
1	P7	Connector-PCB receptacle 0.1mm 8 position single gold	Generic
1	P8	Connector-PCB Berg HDR ST female six pin	Generic
1	P9	Connector-PCB receptacle 25mil square post 2.54mm pitch	Generic
1	PMOD	Connector-PCB HDR ST male PMOD	Generic
8	R1, R5, R6, R31, R33, R81, R82, R83	Resistor SMD 100kΩ 1% 1/16W 0603	Generic
2	R10, R12	Resistor SMD 1MΩ 1% 1/4W 0603 AEC-Q200	Generic
1	R11	Resistor SMD 806kΩ 1% 1/10W 0603 AEC-Q200	Generic

ORDERING INFORMATION

Table 9. Motherboard (Continued)

Qty	Reference Designator	Description	Sourcing
1	R13	Resistor SMD 191kΩ 1% 1/10W 0603 AEC-Q200	Generic
1	R14	Resistor SMD 0Ω 1/10W 0805	Generic
1	R16	Resistor SMD 1kΩ 1% 1/10W 0603 AEC-Q200	Generic
4	R17, R19, R28, R29	Resistor SMD 0Ω jumper 1/3W 0603 AEC-Q200	Generic
1	R18	Resistor SMD 2.7kΩ 0.1% 1/10W 0603 AEC-Q200	Generic
1	R20	Resistor SMD 1.78kΩ 1% 1/10W 0603 AEC-Q200	Generic
5	R21, R22, R23, R24, R25	Resistor SMD 33kΩ 1% 1/10W 0603	Generic
2	R26,R27	Resistor SMD 100Ω 1% 1/10W 0603 AEC-Q200	Generic
39	R35, R37, R39, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R55, R57, R59, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80	Resistor SMD 0Ω JUMPER 1/10W 0603 AEC-Q200	Generic
1	R8	Resistor 0Ω jumper 1/10W 0603	Generic
1	S1	Switch top slide 4P4T, 0.3A	Generic
1	S2	Switch slide SP3T	Generic
1	U1	IC-Analog Devices ultralow noise, CMOS linear regulator LDO 3.3VOUT	ADP150AUJZ-3.3-R7
2	U9, U10	IC-Analog Devices voltage level translator 4-channel bidirectional	MAX3395EETC+
1	U2	IC-Analog Devices CMOS linear regulator LDO 2.5V	ADP150AUJZ-2.5-R7
1	U3	IC-Analog Devices low IQ boost/sepic/inverting converter with 1A, 60V switch	LT8330EDDB#TRMPBF
1	U4	IC-Analog Devices low noise, linear regulator	ADP7182AUJZ-2.5-R7
1	U5	IC 32kbit serial EEPROM	24AA32A-I/SN
1	U6	IC-TTL 8-bit dual supply transceiver	74LVCH8T245PW
1	U7	IC-Analog Devices low distortion and noise CMOS operational amplifier	AD8652ARMZ
1	U8	IC-Analog Devices quadruple precision CMOS rail-to-rail in/out operational amplifier	AD8618ARZ

Table 10. Daughter Board

Qty	Reference Designator	Description	Sourcing
3	A1, A2, A3	3 pin single in-line (SIL) header and shorting link	Generic
2	C1, C3	0.1uF 50V ±10% X7R ceramic capacitor	Generic
2	C2, C4	10uF 6.3V ±20% tantalum capacitor (Case-A)	Generic
1	J1	SIP-8P Header, 2.54mm, PCB, 1X8WAY	Generic
1	J2	12 pin (2×6) 0.1 inch pitch header	Generic
2	J3, J4	5 pin SIL header	Generic
1	U1	AD5142A digital potentiometer	AD5142ABCPZ10

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.