Evaluating the AD4880, Dual-Channel 20-Bit, 40MSPS, SAR ADC with Analog Front End

FEATURES

- Fully-featured evaluation board for the AD4880
- Analysis | Control | Evaluation (ACE) Software plug-in available for device configuration, data capture, and performance evaluation
- Flexible analog front end
- On-board power solution and precision reference
- On-board clock generation circuitry with sampling frequency control via the ACE Software
- FMC compatible

EVALUATION KIT CONTENTS

- EVAL-AD4880-FMCZ evaluation board
- Micro-SD memory card with SD adapter, containing system board boot software and Linux OS
- PCB stand-offs

EQUIPMENT NEEDED

- PC running Windows® 10 operating system or higher
- Digilent ZedBoard with 12V wall adapter power supply
- Precision signal source
- SMA cables to connect a signal source to the EVAL-AD4880-FMCZ

DOCUMENTS NEEDED

- AD4880 data sheet

GENERAL DESCRIPTION

The EVAL-AD4880-FMCZ evaluation board is designed to demonstrate the performance of the AD4880 dual channel ADC with integrated analog front end (AFE) and provide access to a limited set of features from the chip in the ACE Software environment. The EVAL-AD4880-FMCZ evaluation kit supports the following AD4880 features:

- Low-voltage digital signaling (LVDS) data output interface.
- Analog-to-digital converter (ADC) configuration via serial peripheral interface (SPI).
- Internal or external generation of 1.1V regulated supply rails.
- Sampling rate capability between 1.25MSPS and 40MSPS.

The EVAL-AD4880-FMCZ evaluation board is designed for use with the Digilent ZedBoard via the field programmable gate array (FPGA) mezzanine card (FMC) connector. The ZedBoard uses a Xilinx Zynq7000 system on chip (SoC) that runs Analog Devices Kuiper Linux and LIBIIO included on the SD card supplied in the evaluation board kit to facilitate communication with the EVAL-AD4880-FMCZ, enabling ADC configuration and data capture. The ZedBoard also provides the communication link to the host PC and the **ACE Software** plug-in.

Full specifications on the AD4880 are available in the AD4880 data sheet available from Analog Devices, Inc., and must be consulted with this user guide when using the EVAL-AD4880-FMCZ evaluation board.

For the current schematics, layouts, and bill of materials, refer to the EVAL-AD4880-FMCZ product page.

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REVISION HISTORY

4/2026—Revision 0: Initial Version

EVAL-AD4880-FMCZ EVALUATION BOARD PHOTOGRAPH

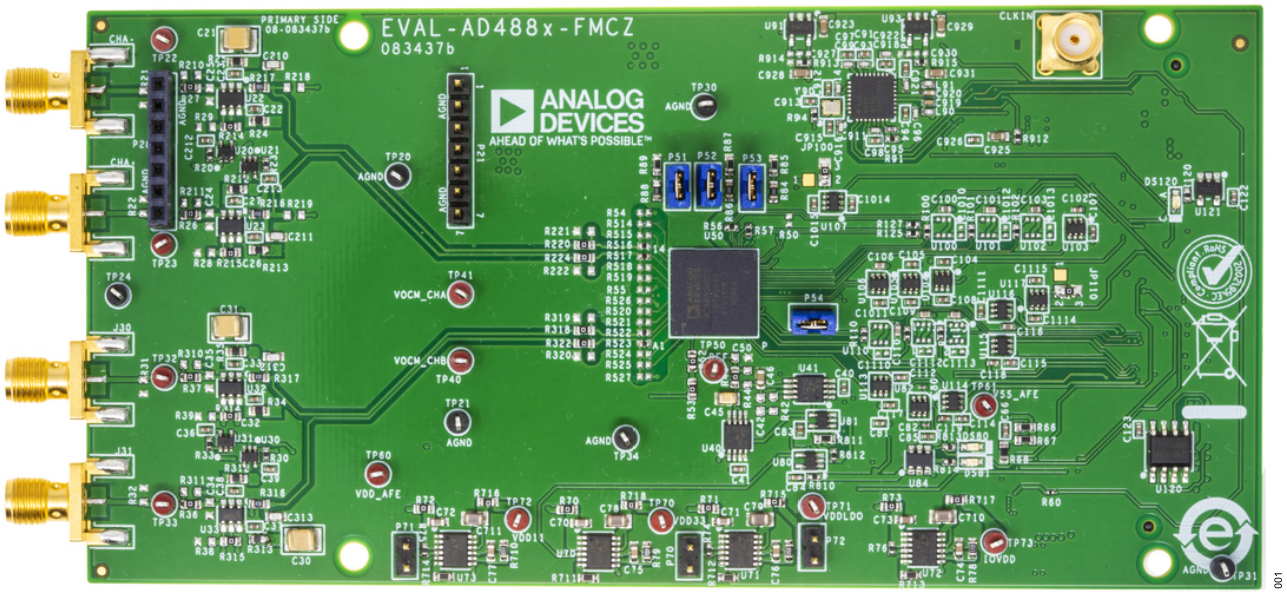

Figure 1. EVAL-AD4880-FMCZ Evaluation Board Photograph

EVALUATION BOARD HARDWARE GUIDE

HARDWARE OVERVIEW

A simplified block diagram of the EVAL-AD4880-FMCZ hardware is shown in Figure 2. This evaluation board showcases the performance and features of the AD4880 and highlights the recommended companion components.

The EVAL-AD4880-FMCZ enables simple evaluation of the AD4880. All circuitry necessary to operate the ADC is included on the EVAL-AD4880-FMCZ.

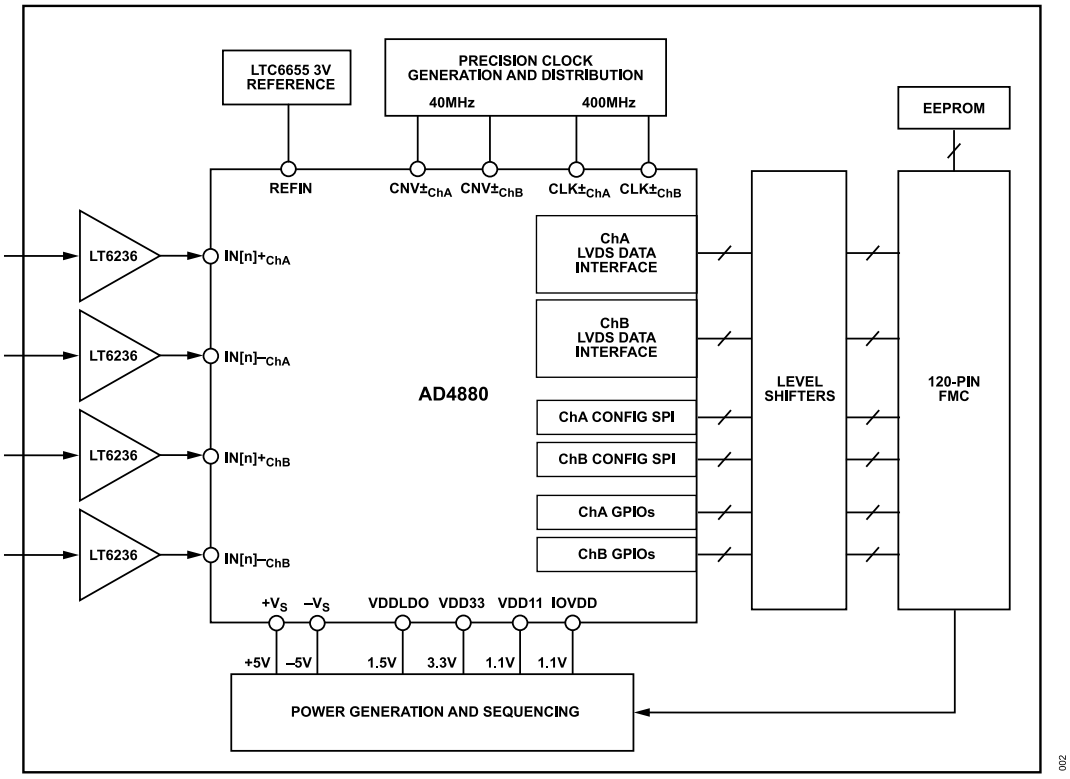

Figure 2. Simplified Block Diagram of the EVAL-AD4880-FMCZ

EVALUATION BOARD HARDWARE GUIDE

INPUT STAGE

The input stage for each AD4880 channel consists of a pair of LT6236 op amps (U22 and U23, U32 and U33). The LT6236 is selected for its exceptional wideband (90MHz), low noise, favorable distortion performance and low power consumption. The op amps are setup as unity-gain buffers, ensuring that a preceding signal source or sensor is presented with a high impedance. With supply rail values of +5V and −5V, the valid range at each input of this stage is −3V to +3.7V (factoring in the input requirements of both LT6236 and the FDA inside AD4880). As long as this valid range is respected, there is freedom to set the common mode of the driving signal. The input stage is designed in principle to take in a fully-differential signal, with a differential voltage span of ±2.91V, the full span of the ADC is exercised. A single-ended signal can also be applied at the input, but modifications such as adding gain or a bias level to one of the op amps might be needed to exercise the full span of the ADC, depending on the input signal characteristics.

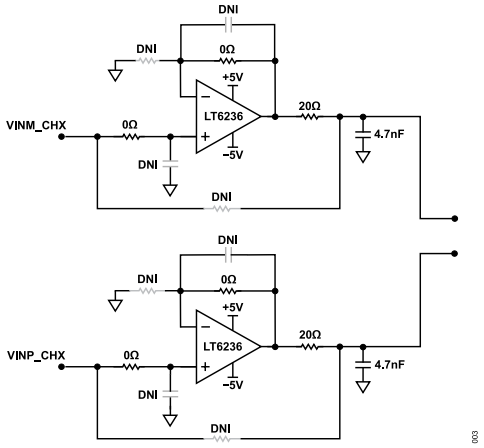

Figure 3. Input Stage Simplified Schematic for One Channel

The following can be configured in this stage:

- Stage bandwidth
  - Additional band limiting through RC input filter and/or capacitors across amplifier feedback
- Stage gain
  - Unity gain (default)
  - Noninverting gain setting
- Stage bypass
  - No bypass (default)
  - Bypass
  - Bypass via amplifier mezzanine card (AMC), this is an option for Channel A only

GAIN CONFIGURATION

By default, the EVAL-AD4880-FMCZ is configured with a gain of 1.03x, and 220pF capacitors (C52, C53, C54, and C55) fitted for noise filtering across the feedback network of the AD4880 on-chip FDAs. In this default configuration, an SNR of around 92.8dB is typically expected.

Changing the gain at the AD4880 FDA stage requires light rework on the PCB (removing/adding 0402 SMD resistors and/or shorting 0402 solder pads), to modify the arrangement of the internal AD4880 gain-setting resistors. For the possible gain options and node shorting requirements, refer to the AD4880 data sheet.

VOLTAGE REFERENCE

The AD4880 requires an external 3V voltage reference. To achieve the specified performance, a suitable precision, low-noise voltage reference must be used. The ADC does include an internal reference buffer and capacitor, which makes reference selection easier and eliminates the need for an external buffer.

The following can be configured in this circuit:

- Reference selection
  - The LTC6655-3 is the default. The evaluation hardware includes LTC6655-3 (U40) as the primary recommended option, providing exceptional noise performance (0.1Hz to 10Hz noise specification of 0.25ppm p-p), combined with an initial accuracy of 0.025%, and a low temperature drift of 2ppm/°C.
  - The LT6657-3 (U41) is also mounted and provided as a second option. For a comparison of recommended references, see Table 1.

Table 1. 3V Reference Comparison of the LT6657 and LTC6655

Parameter	LT6657	LTC6655
Accuracy	0.10%	0.025%
Temperature Coefficient (ppm/°C)	1.5	2
0.1Hz to 10Hz Noise (ppm p-p)	0.5	0.25
Maximum Load (mA)	±10	±5
Load Regulation (ppm/mA)	0.7	3
Maximum Supply	40V	13.2V
Shutdown	Yes	Yes
Reverse Supply Protected	Yes	No
Reverse Output Protected	Yes	No
Current Limit	Yes	Yes
Thermal Protection	Yes	No
Shunt Mode	Yes	No
Supply Current, I_S (mA)	1.2	5
T_A	−40°C to +125°C	−40°C to +125°C
100% Tested Temperatures	5	3

EVALUATION BOARD HARDWARE GUIDE

POWER SUPPLIES

The EVAL-AD4880-FMCZ is designed to operate from the 12V and 3.3V supplies provided from the host controller board via the FMC connector. The FMC supplies are regulated down using a combination of switching regulators and linear dropouts (LDOs) regulators to generate the necessary power rails for the on-board circuitry.

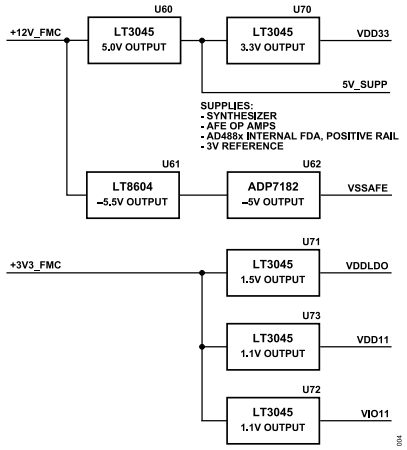

Figure 4. Evaluation Board Power Tree

ADC POWER SUPPLIES

The AD4880 requires three major power supplies:

- VDD33: 3.3V analog supply rail
- VDD11: 1.1V ADC core supply
- IOVDD: 1.1V digital interface supply

The AD4880 includes integrated power supply decoupling capacitors. Therefore, no external power supply decoupling are included on the evaluation board for the ADC power supply rails.

The following can be configured in this circuit:

- 1.1V rails (VDD11 and IOVDD) source
  - On-board generated rails (default): The rails are taken in from the LT3045 regulators (U72 and U73), as shown in Figure 4.
  - Internal AD4880 LDO regulator: An LDO internal to the ADC can be enabled and used to power both 1.1V rails. For more details pertaining to the power supply rails and requirements, refer to the AD4880 data sheet.
  - Off-board external supply.
- 3.3V rail source
  - On-board generated rail (default): The rail is supplied by an LT3045 LDO regulator (U71), as shown in Figure 4.
  - Off-board external supply.

AMPLIFIER POWER SUPPLIES

A +5V rail (VDDAFE) and a −5V rail (VSSAFE) are generated on the EVAL-AD4880-FMCZ evaluation board. These rails power all analog front end circuitry, which includes the four LT6236 discrete operational amplifiers (U22, U23, U32, and U33) in the input stage as well as the on-chip fully-differential amplifiers inside AD4880 (via the $+V_S$ and $-V_S$ pins).

CONVERSION AND DATA CLOCK GENERATION CIRCUIT

The EVAL-AD4880-FMCZ contains the necessary circuits to generate low jitter data (CLK+ and CLK−) and conversion (CNV+ and CNV−) clocks across the full operating range of the AD4880. This low jitter circuitry allows processing with fidelity full-scale input signals up to 4MHz.

The circuit consists of a 25MHz complementary metal-oxide semiconductor (CMOS) reference oscillator (Y90), the ADF4350 wideband synthesizer, and the AD9508 clock fan-out buffer, as shown in Figure 5. The synthesizer takes in the 25MHz signal from the oscillator and produces a higher frequency output with the frequency multiplication factor being programmable by the software. The synthesizer output is then fed to the clock buffer, which generates the clock (CLK+ and CLK−) and convert (CNV+ and CNV−) signals, from which, it can apply separate programmable frequency division factors. Therefore, the software sets the CLK and CNV signal frequencies by programming the ADF4350 and AD9508 through their serial interfaces. In practice, the user must change the sample rate through the interface offered by the ACE Software.

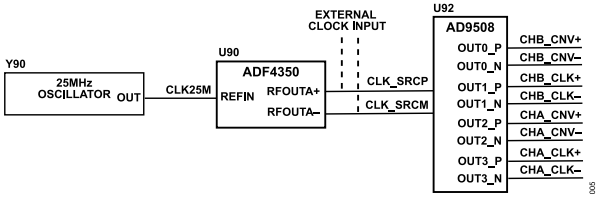

Figure 5. Simplified Diagram of the Clock Circuitry

DIGITAL INTERFACE

The EVAL-AD4880-FMCZ utilizes the FMC connector (P120) from the ZedBoard to support ADC device configuration via the 4-wire SPI, conversion result access using the LVDS interface, and conversion control in LVDS mode. The ZedBoard acts as the conduit for communication between the ACE Software plug-in and the EVAL-AD4880-FMCZ hardware.

The AD4880 operates with a 1.1V digital interface supply voltage. To translate between this 1.1V level and the digital interface voltage level of the ZedBoard (VADJ), SN74AVC1T45DCKR bidirectional level translators are used on the EVAL-AD4880-FMCZ hardware.

EVALUATION HARDWARE SETUP PROCEDURE

The following procedure must be followed to get the hardware ready for evaluation:

1. Insert the SD card from the EVAL-AD4880-FMCZ kit into the SD card slot (J12) of the ZedBoard.
2. Ensure that the ZedBoard boot configuration jumpers (JP7 to JP11) are set, as shown in Figure 6.

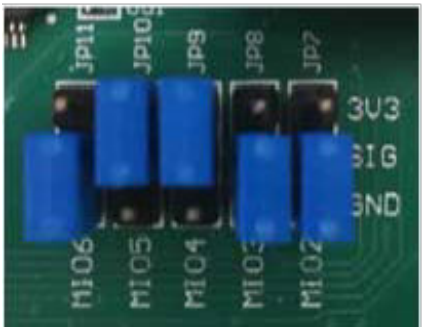

Figure 6. ZedBoard JP7 to JP11 Settings for the SD Card Mode

3. Ensure that the VADJ SELECT jumper (J18) is in the **2V5** position.
4. Connect the FMC connector (P3) of the EVAL-AD4880-FMCZ to the FMC connector (J1) of the ZedBoard.
5. Connect the 12V power supply included in the ZedBoard kit to the DC barrel jack (J20) of the ZedBoard, one USB cable between the PC and the USB on the go (OTG) connector (J13), and the other USB cable between the PC and the USB universal asynchronous receiver-transmitter (UART) connector (J14).
6. Slide the power switch (SW8) to the **ON** position to power up the ZedBoard and evaluation hardware.
   a. If using any external power supplies for the evaluation hardware, turn these supplies on with the ZedBoard.
7. The hardware is now ready to be used through the ACE Software.

SOFTWARE SUPPORT

EVALUATION SOFTWARE

The EVAL-AD4880-FMCZ hardware is controlled and configured through the ACE Software. ACE is a desktop software application that allows the evaluation and control of multiple evaluation systems from across the Analog Devices, Inc., product portfolio. The controller board supported by ACE with the EVAL-AD4880-FMCZ evaluation board is the ZedBoard.

For ACE installation and documentation instructions, refer to the ACE Software. Make sure to follow the instructions to install the necessary EVAL-AD4880-FMCZ board plug-in and do the following:

1. If the machine that ACE is installed on has internet access, a user can find/install/update plug-ins directly from the ACE application. For environments without internet access, a user can download these plug-ins from the previous link to portable storage and install them into ACE.

Note that the user can find the product specific documentation for the evaluation software within the ACE plug-in.

EMBEDDED SOFTWARE

The embedded software used for evaluation is built using open-source firmware examples, drivers, and HDL. When available, a user can find the links in the software section on relevant the product page.

Note that if a user does not find the embedded software available, then submit a request from the product page.

The EVAL-AD4880-FMCZ evaluation board comes with an SD card in the box. The SD card provides a version of Analog Devices Kuiper Linux for Evaluation that can boot the controller board. The ACE evaluation board plug-in provides product specific configuration data and files.

Note that if there is an issue with the provided SD Card or a user has an outdated version, download the latest version ADI Kuiper Linux for Evaluation image at Analog Devices Kuiper Linux. This page also provides details on how to format and set up your SD card correctly.

The latest version of ADI Kuiper Linux for Evaluation contains support Linux Runtime Configuration (LRC) of ACE Plug-Ins, via the ACE Software application. With the ACE application running, once a powered ZedBoard, with the EVAL-AD4880-FMCZ evaluation board fitted has been connected to the PC, the ACE application detects the connected evaluation board. If the ADI Kuiper Linux kernel running on from the SD card is not already configured for the connected evaluation board, the following pop-up appears, as shown in Figure 7. Click **OK** to install the updated kernel to support the connected hardware.

Note that once user clicks **OK**, the kernel update is downloaded to the board and the kernel is then reinitialized. Initialization takes approximately 60seconds to 80seconds to complete. Once completed, the ACE plug-in opens, as described in the Evaluating the AD4880 with the ACE Software section.

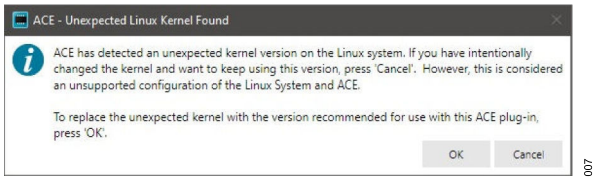

Figure 7. ACE LRC Reconfiguration of Kuiper Linux Prompt on Detection of EVAL-AD4880-FMCZ Board

HOST PC SOFTWARE

The embedded Linux stack is based on the IIO (Industrial I/O) architecture. This enables tools such as Python, through the pyadi-iio package, or MATLAB, with the Precision Toolbox, on a host PC to communicate with the evaluation and controller board. Where available, a user can find the links in the software section on the ADC product page.

Note that if a user does not find the Python or MATLAB software available, then submit a request from the product page.

There are generic, not product specific, IIO tools such as IIO Oscilloscope, Scopy, and IIO command line tools that provide basic, low-level functionality and work with any IIO platform.

EVALUATING THE AD4880 WITH THE ACE SOFTWARE

After the hardware setup is complete as per the Evaluation Hardware Setup Procedure section, and the software is installed as specified in the Software Support section, then run the ACE Software for evaluation.

When ACE opens, the EVAL-AD4880-FMCZ automatically detects and appears in the **Attached Hardware** panel, as shown in Figure 8.

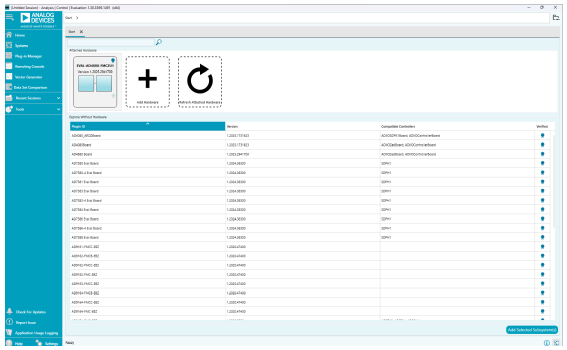

Figure 8. Auto Detection of the EVAL-AD4880-FMCZ in the ACE Start Tab

Double-click on the EVAL-AD4880-FMCZ icon and a new tab **EVAL-AD4880-FMCZ** opens that shows a block diagram of the EVAL-AD4880-FMCZ, as shown in Figure 9.

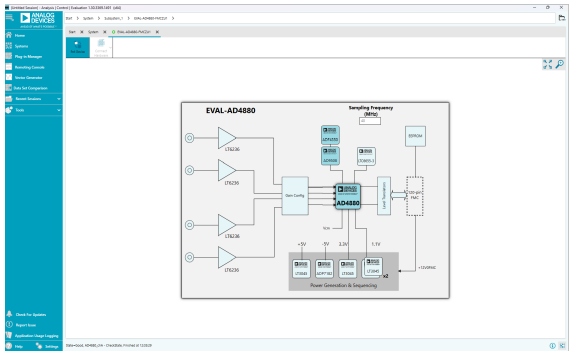

Figure 9. EVAL-AD4880-FMCZ Tab Open in the ACE Software

This offers a **Board Level** view of the EVAL-AD4880-FMCZ. The sampling frequency can be configured within this window because it can control the required configuration of the supporting clocking components, ADF4350 and AD9508, as well as controlling the synchronization of the EVAL-AD4880-FMCZ data with the ZedBoard. As a default, the **Sampling Frequency (MHz)** field is configured for 40MHz. Any required update to the sampling frequency, in the range of 1.25MHz to 40MHz, can be made to this field. When a new value is entered in this field, the supporting clock components are updated, and the ZedBoard interface is automatically resynchronized. The same sampling frequency is applied to both channel in this implementation.

From the block diagram, double-click on the AD4880 to open the **AD4880_cha** tab. This tab displays:

- A block diagram of the full AD4880 chip.
- An **INITIAL CONFIGURATION** pane on the left, showing device attributes and direct register access for Channel A. The ***sampling_frequency*** device attribute is only informative, the sampling frequency can be changed for both channels at the same time in the **Board Level** view. The ***filter_sel*** and ***sinc_dec_rate*** attributes control the digital filtering functionality of the AD4880. Any change to these parameters is applied to both Channel A and Channel B, this is a limitation of this evaluation board and associated software, in which both channels are simultaneously sampled and their displayed data is superimposed on one plot. In other applications, the sampling and digital filtering of each channel can be independently configured.
- A **Proceed to Channel B** button at the bottom left (open the **AD4880_chb** tab, which is similar to this one, but whose **INITIAL CONFIGURATION** pane shows device attributes and direct register access for Channel B).
- Two buttons in the lower-right corner (**Proceed to Memory Maps** and **Proceed to Analysis**), which are shown in Figure 10.

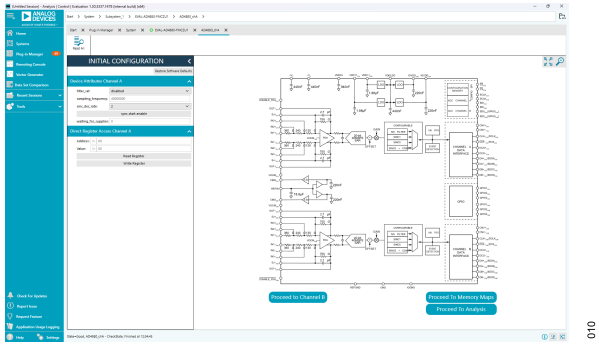

Figure 10. AD4880 Channel A Tab in the ACE Software

The tabs that are accessed through the **Proceed to Memory Maps** and **Proceed to Analysis** buttons provide the means to evaluate the AD4880 chip. For more details, see the AD4880 Memory Maps and the ANALYSIS Tab sections.

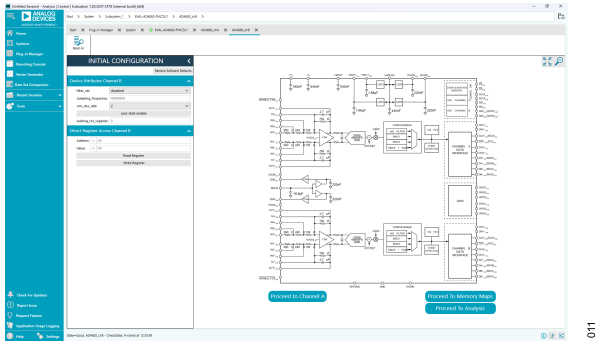

Figure 11. AD4880 Channel B Tab in the ACE Software

AD4880 MEMORY MAPS

Clicking on the **Proceed to Memory Maps** button within either the **AD4880_chA** or the **AD4880_chA** tab opens two tabs:

EVALUATING THE AD4880 WITH THE ACE SOFTWARE

AD4880_chA Memory Map and **AD4880_chB Memory Map**, as shown in Figure 12.

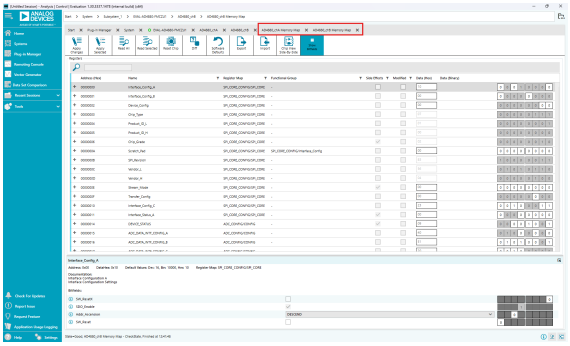

Figure 12. AD4880 Memory Map Tabs in the ACE Software

The **AD4880_chA Memory Map** shows the registers from Channel A, and the **AD4880_chb Memory Map** tab shows the registers for Channel B. These tabs allow reading and writing (if applicable) register contents. For basic operation of the evaluation kit, no modifications are required to the ADC registers.

ANALYSIS TAB

Click **Proceed to Analysis** within either the **AD4880_chA** or **AD4880_chA** tab to open the **ANALYSIS** tab. This tab is used for capturing data for both channels through the evaluation board and analyzing the obtained data. Data capture is simultaneous for both channels and at the same sampling rate. Same configuration of digital filtering is also forced.

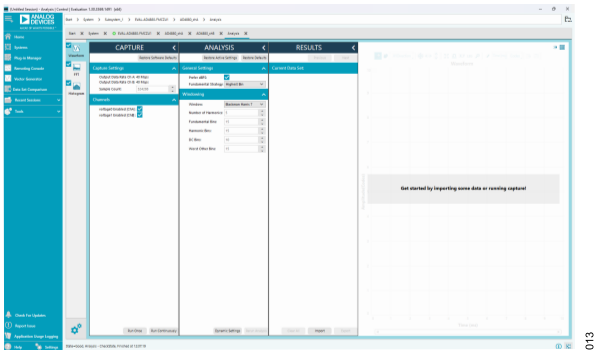

Figure 13. Analysis Tab in the ACE Software

The **ANALYSIS** tab contains three panels (**CAPTURE**, **ANALYSIS**, and **RESULTS**) and a data plot area to the right. To hide any of the three panels, click the arrow located to the right of the panel name and is useful to leave more space for the data plot area when needed.

- The **CAPTURE** panel allows setting the number of samples to be captured per data set, triggering the acquisition of a single data set, and initiating or stopping the continuous acquisition of a data set.
- The **ANALYSIS** panel shows options related to the frequency domain analysis.
- The **RESULTS** panel provides metrics for the current data set that appears in the plot area. Different metrics are provided depending on the kind of plot that is selected (for more details, see the Time Domain (Waveform) Plot, Frequency Domain (FFT) Plot, and Histogram Plot sections). This panel also allows navigating between the data sets acquired during the session, and importing and exporting data sets in the internal format used by the **ACE Software** is also facilitated.

The user has the option to display the acquired data sets as a time domain waveform (default option), a frequency domain plot through a fast Fourier transform (FFT) or as a histogram, which is selected by clicking on any of the three corresponding buttons located to the left of the **CAPTURE** panel (see Figure 13).

TIME DOMAIN (WAVEFORM) PLOT

The active data set appears as a time domain waveform by clicking on the **Waveform** area highlighted in red in Figure 14, which is the default view. Note that how the **CAPTURE** and **ANALYSIS** panels hide for an improved display of the plot.

When the data set is plotted as a time domain waveform, the **RESULTS** panel shows metrics relevant to time domain analysis: minimum, maximum, average, and RMS.

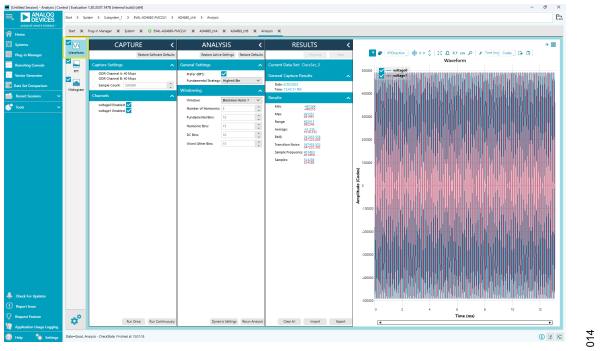

Figure 14. Data Set Plotted as Time Domain Waveform

EVALUATING THE AD4880 WITH THE ACE SOFTWARE

FREQUENCY DOMAIN (FFT) PLOT

The active data set appears as a frequency domain waveform by clicking on the **FFT** area highlighted in red in Figure 15. The plot then shows the FFT of the active data set. In this case, the **Log Scale** is selected for the **Frequency (MHz)** axis above the graph.

When the data set is plotted as a frequency domain waveform, the **RESULTS** panel shows metrics relevant to frequency domain analysis: signal-to-noise ratio (SNR) and total harmonic distortion (THD).

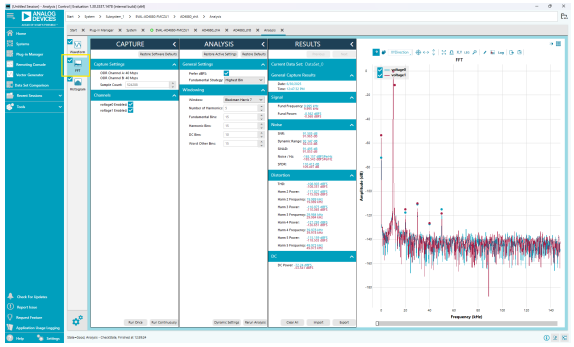

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Figure 15. Data Set Plotted in the Frequency Domain

HISTOGRAM PLOT

The active data set appears as a histogram by clicking on the **Histogram** area highlighted in red in Figure 16. In this view, the vertical axis shows occurrences (bin hits) and the horizontal one can be set to display either code or volt amplitude bins.

When the data set is plotted as a histogram, the **RESULTS** panel shows metrics relevant to histogram analysis, such as minimum code, maximum code, and RMS.

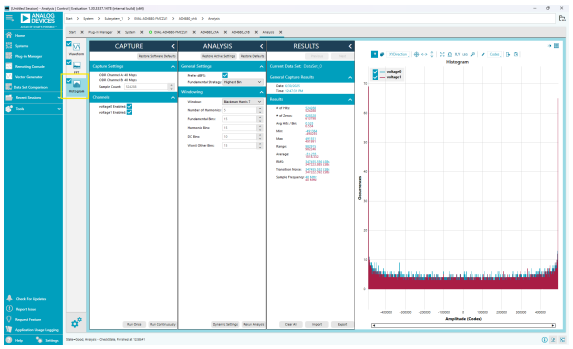

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Figure 16. Data Set Plotted as a Histogram

CONFIGURING THE AD4880 INTEGRATED DIGITAL FILTERS

The AD4880 includes the option of enabling integrated digital filters for applications where noise rejection by bandwidth limiting is required. For more details on the function and performance of these flexible filters, refer to the AD4880 product data sheet. While in principle each channel in AD4880 is fully independent, in the implementation for use with the ACE Software the same configuration is forced for both channels. The configuration can be done on any of the two channel tabs (**AD4880_chA** and **AD4880_chB**), in the INITIAL CONFIGURATION area, as shown in Figure 17 (with **AD4880_chA** tab). The set configuration is automatically applied to both channels by the ACE Software.

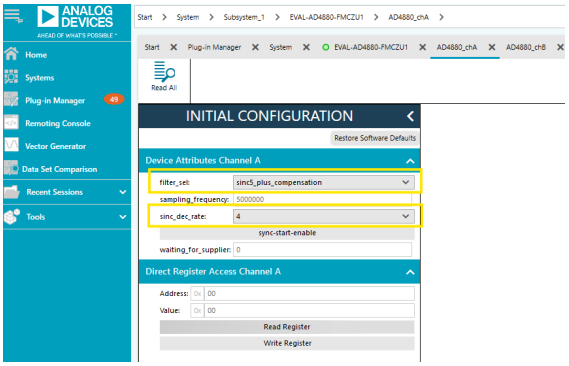

Figure 17. Digital Filter Configuration from the AD4880 Tab in the ACE Software

The values set in Figure 17 correspond to a sinc5 + compensation filter with a sinc decimation rate of 4. The ***sampling_frequency*** attribute is read only and shows the effective output data rate, which in this case results from dividing the (default) 40MHz sampling frequency by 8 (4x from the sinc, and an additional 2x by the compensation). Figure 18 shows measurement results for this scenario, where the improvement in SNR can be observed.

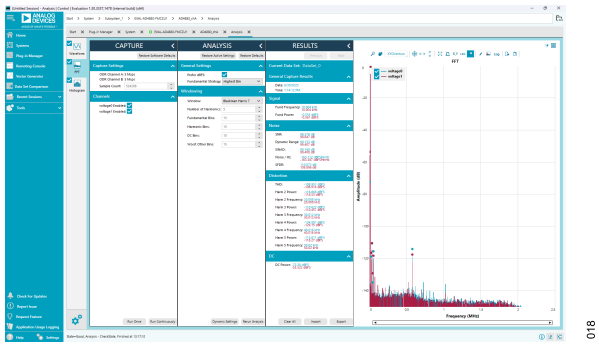

Figure 18. Increasing SNR with the Integrated Digital Filter

ORDERING INFORMATION

EVALUATION BOARDS

Evaluation Board[1]	Description
EVAL-AD4880-FMCZ	Evaluation Board

[1] Z = RoHS Compliant Part.

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.