

## Evaluating the AD4692 Family of Easy Drive Multiplexed SAR ADCs with Averaging Filters per Channel

### FEATURES

- ▶ Full featured evaluation board for the AD4692 family of multiplexed SAR ADCs
  - ▶ Demonstrates performance and functionality of the AD4691, AD4692, AD4693, and AD4694
- ▶ Two single-ended input channels available through SMA connectors for AC analysis
  - ▶ Six channels for on-board DC voltage analysis
- ▶ On-board reference circuitry and power tree designed for a USB power solution
- ▶ ACE plugin available for device configuration and data analysis in the time and frequency domains
- ▶ Compatible with SDP-K1 and other Arduino form factor controller boards

### EQUIPMENT NEEDED

- ▶ PC with Windows 10 or later operating system
- ▶ [SDP-K1](#) controller board and accompanying USB cable
- ▶ Precision signal generator with SMA output cables

### SOFTWARE NEEDED

- ▶ Analysis | Control | Evaluation ([ACE](#)) software
- ▶ The AD4692 ACE plugin from the plugin manager or the ACE plugin database

### EVALUATION BOARD KIT CONTENTS

- ▶ EVAL-AD4692-ARDZ evaluation board

### ONLINE RESOURCES

- ▶ [AD4691](#) product page
- ▶ [AD4692](#) product page
- ▶ [AD4693](#) product page
- ▶ [AD4694](#) product page
- ▶ [EVAL-AD4692-ARDZ](#) product page

### GENERAL DESCRIPTION

The EVAL-AD4692-ARDZ evaluation board is designed to demonstrate the performance of the AD4692 family of analog-to-digital converters (ADCs) and to provide access to included configuration options available in the ACE plugin graphical user interface (GUI). The AD4692 family are compact, high accuracy, 16-bit Easy Drive successive approximation register (SAR) ADCs optimized for high-density multichannel precision data acquisition solutions. This document includes a quick-start guide for using the EVAL-AD4692-ARDZ evaluation board with the EVAL-SDP-CK1Z (SDP-K1) controller board. Refer to the [Hardware Setup](#) section and [Evaluation Board Software](#) section for detailed instructions on setting up the hardware and software for board evaluation.

The SDP-K1 is the primary controller board for the EVAL-AD4692-ARDZ. The EVAL-AD4692-ARDZ evaluation board conforms to the Arduino® Uno Shield mechanical and electrical standards to interface with the SDP-K1 and various software development kits from other manufacturers.

The EVAL-AD4692-ARDZ evaluation solution includes the AD4692 industrial I/O (IIO) firmware application drivers for device configuration and ADC data capture and the AD4692 ACE plugin GUI for performance evaluation.

The EVAL-AD4692-ARDZ can also be used to evaluate the performance of the AD4691, AD4693, and AD4694 by limiting the sample rate and number of channels used in the evaluation software. Consult the data sheet for each product in conjunction with this user guide for more information.

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**REVISION HISTORY****2/2026—Revision 0: Initial Version**

EVALUATION BOARD PHOTOGRAPH

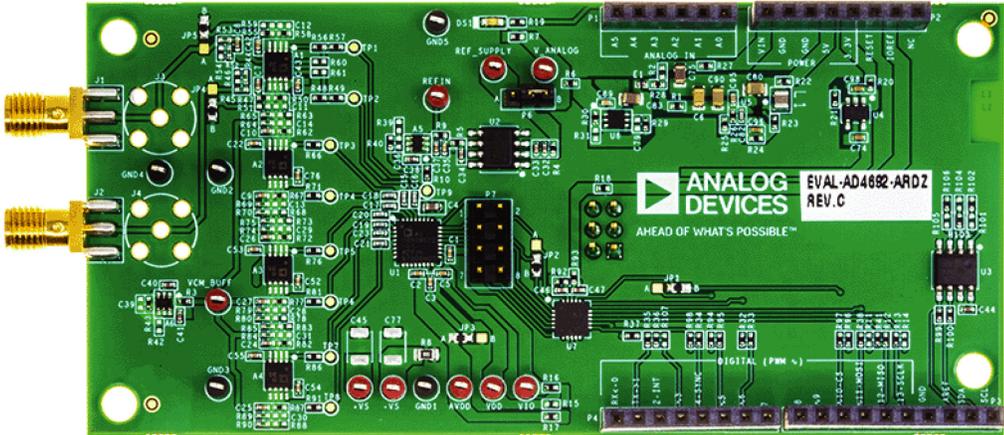


Figure 1. EVAL-AD4692-ARDZ Evaluation Board

**HARDWARE OVERVIEW**

The EVAL-AD4692-ARDZ peripheral circuitry is designed to simplify evaluation and achieve the typical performance characteristics of the AD4692 using a USB power solution. Optional configurations for the peripheral circuitry are available to accommodate a wide range of signal chain requirements for additional prototyping.

Figure 2 shows a simplified block diagram of the EVAL-AD4692-ARDZ circuitry. Figure 3 shows the physical locations of the circuit blocks on the EVAL-AD4692-ARDZ board. The factory default board includes the following chips:

- ▶ **AD4692BCPZ-RL7** SAR ADC converts analog signals into 16-bit digital codes
- ▶ **AD4540BRZ** voltage reference provides a low noise, 4.096V reference to the AD4692
- ▶ Four **ADA4807-2ARMZ** rail-to-rail amplifiers buffer and condition the AD4692 Channel 0 to Channel 7 analog inputs

- ▶ **ADG3308BCPZ** bidirectional level translator facilitates conversion between the 1.8V logic level of the AD4692 and the 3.3V logic level of the SDP-K1
- ▶ **ADP150AUJZ** linear regulator adjusts the 3.3V Arduino header voltage to 1.8V for the AD4692 internal I/O logic and  $V_{DD}$  voltage requirements
- ▶ **MAX17291** DC-DC converter boosts the 5V Arduino header to provide ample headroom for **ADP7118** chip
- ▶ **ADP7118ACPZN** linear regulator generates the 5V analog supply rail

These companion components were selected to simplify evaluation and achieve typical performance characteristics of the AD4692 and are not necessarily applicable to all system designs and use cases. The following sections will further detail the default and customizable hardware options present on the EVAL-AD4692-ARDZ.

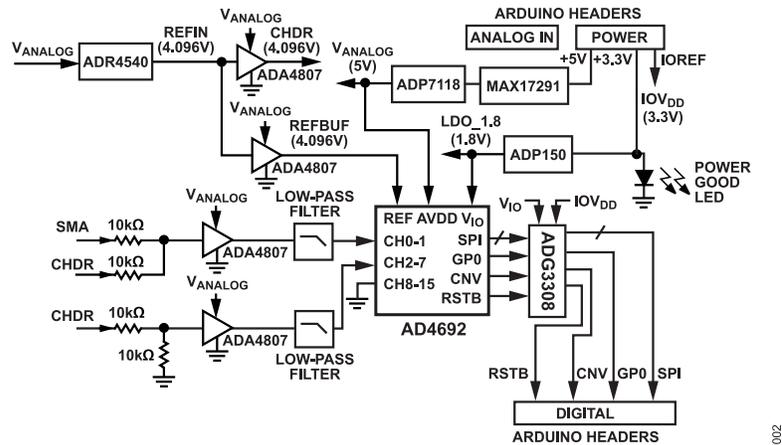


Figure 2. EVAL-AD4692-ARDZ Functional Block Diagram

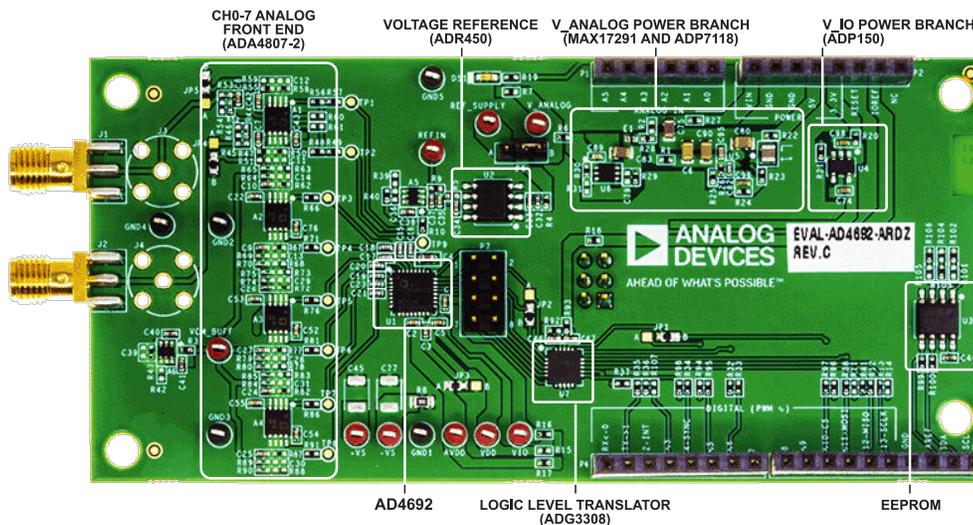


Figure 3. EVAL-AD4692-ARDZ Board Circuitry Locations

**HARDWARE OVERVIEW**

**POWER SUPPLY**

**Default Configuration**

Figure 4 shows the EVAL-AD4692-ARDZ power tree. In the factory default configuration, the analog front end (AFE) circuitry, voltage reference input, and ADC are all powered by an on-board 5V rail (named V\_ANALOG) that is supplied by the 5V pin of the controller board's Arduino header. To address the noisy nature of the header pin, the MAX17291 DC to DC converter boosts the 5V header to give headroom for the ADP7118 to regulate the voltage back down to a low-noise 5V rail (V\_ANALOG).

The ADC I/O logic level is powered by an on-board 1.8V rail, which is derived from the 3.3V supply from the Arduino header. The 3.3V input is regulated by the on-board ADP150 to generate the LDO\_1.8V rail, ensuring a stable supply for the ADC I/O logic.

It is assumed that the controller board will be operating at a 3.3V I/O logic level. Therefore, a logic level translator is used to convert between logic levels. The evaluation board-side logic level is tied to the LDO\_1.8V rail and the controller board-side of the logic level translator is tied to the controller board's 3.3V header pin. Refer to the Digital Interface section for more information on the logic level translator and the digital communications of the evaluation board.

By default, the EVAL-AD4692-ARDZ uses the AD4692 internal LDO regulator to supply its VDD with 1.8V automatically on power-up. In this default state, the LDO\_IN pin of the ADC must be powered either by the V\_ANALOG rail or an externally generated supply and the VDD pin of the ADC must be left floating (default configuration).

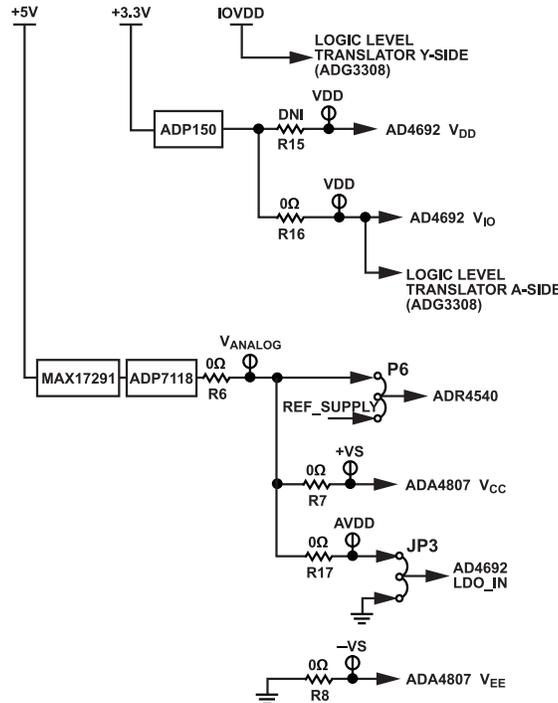


Figure 4. EVAL-AD4692-ARDZ Power Tree

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**HARDWARE OVERVIEW**

**Alternative Configuration**

The EVAL-AD4692-ARDZ provides options to power the V\_ANALOG, +VS, and -VS power rails of the board, as well as the VDD, VIO, and LDO\_IN pins of the AD4692 using external power supplies. Refer to the product data sheet for supply voltage ranges before applying an external supply.

As shown in Table 1 and Table 2, to power any of the rails with an external supply an associated resistor must be depopulated and the external signal must be applied to the correctly labeled test point.

**Table 1. Disconnecting the EVAL-AD4692-ARDZ Rails from the On-Board Supplies**

Rail Name	Connection Resistor	Test Point Label
V_ANALOG	R6	V_ANALOG
+V <sub>s</sub>	R7	+VS
-V <sub>s</sub>	R8	-VS

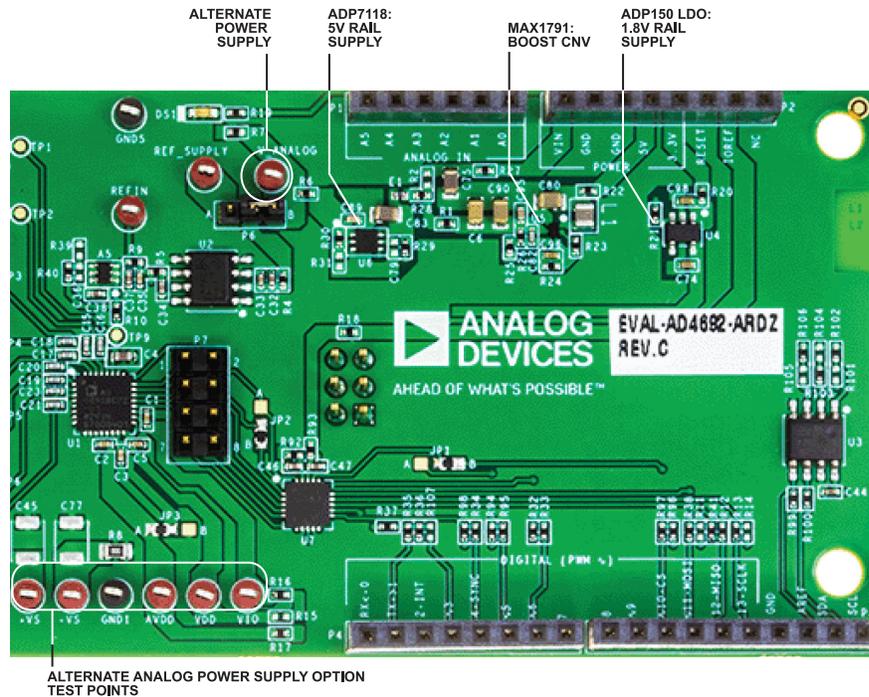
**Table 2. Disconnecting the AD4692 Pins from On-Board Supplies**

Pin Name	Connection Resistor	Test Point Label
LDO_IN	R17	AVDD
VIO	R16	VIO
VDD <sup>1</sup>	R15	VDD

<sup>1</sup> Jumper JP3 must be set Position B, and the LDO\_EN bit must be set to 0 in the SETUP register.

The VIO test point connects to both the AD4692 VIO supply and the level translator VCCA supply to set the I/O logic levels of both. VIO must be supplied with 1.8V when driven externally.

Instead of using an external supply or internal AD4692 LDO regulator, the evaluation board can be configured to power the AD4692 VDD pin using the on-board LDO\_1.8V rail. To do this, the R15 resistor must be populated with a 0Ω, and jumper JP3 must be set to Position B to tie the internal LDO regulator source (LDO\_IN) to ground. The AD4692 internal LDO regulator must also be disabled by setting the LDO\_EN bit to 0 in the SETUP register. At that point, the AD4692 VDD pin will be connected to the LDO\_1.8 rail.



**Figure 5. Location of Power Tree Circuitry on EVAL-AD4692-ARDZ**

**HARDWARE OVERVIEW**

**VOLTAGE REFERENCE**

**Default Configuration**

In the default configuration, the EVAL-AD4692-ARDZ includes an on-board precision voltage reference (ADR4540) and a reference buffer circuit (including the ADA4807-1) that provide a 4.096V  $V_{REF}$  voltage to the AD4692. The 5V  $V_{ANALOG}$  rail powers the ADR4540 to generate the high-precision 4.096V reference. An ADA4807 in the unity gain buffer configuration creates the REF\_BUF source which is driven into the AD4692 with a 1uF decoupling capacitor to ensure a stable 4.096V  $V_{REF}$  voltage.

The ADR4540 also generates the CHDR signal used to DC bias the on-board input channels (CH0 to CH7). By default, an ADA4807 in the unity gain buffer configuration is used to generate the CHDR signal.

**Alternative Configuration**

The EVAL-AD4692-ARDZ provides the option for driving the ADR4540 input externally. Jumper P6 selects between the on-board 5V analog rail (default setup, Position B) and an external power supply (Position A). In Position A, users can apply an external voltage to the REF\_SUPPLY test point (Figure 7) to drive the ADR4540. When applying an external voltage, refer to the ADR4540 data sheet for the allowable range of input voltages.

Alternatively, users can bypass the ADR4540 voltage reference and externally drive the reference signal by depopulating the R5 resistor and applying an external signal to the REFIN test point (Figure 7). This configuration still buffers the externally applied reference voltage through the ADA4807-1 buffer circuits, so when evaluating higher reference voltage levels considerations must be made to the supply rails (+VS) of the amplifier to satisfy their input/output headroom specifications. Note that the +VS and ADC power pins are tied to the same  $V_{ANALOG}$  rail by default. Refer to the Power Supply section for more information.

Both buffers to the AD4692 REF pin and the buffer CHDR signal use the same circuit configuration, which is shown in Figure 6. This configuration allows the option to apply noninverting gain and low-pass filtering through a selection of passive components. Please refer to the table below and the circuit schematic for proper passive configurations.

To drive CHDR with an external signal, the R3 resistor must be depopulated, and an external voltage applied to the VCM\_BUF test point (Figure 7). Since the external signal is not buffered by the ADA4807-1, check the expected current draw of the input channels and impedance of the signal generator used before applying a signal.

Table 3. Passive Settings for Reference Buffer Configurations

Configuration	AD4692 REF Pin Buffer	CHDR Buffer
Unity Gain	Populate: R40	Populate: R43
Noninverting Gain	Populate: R40, R39	Populate: R43, R42
Low-Pass Filter	Populate: R40, C36	Populate: R43, C39

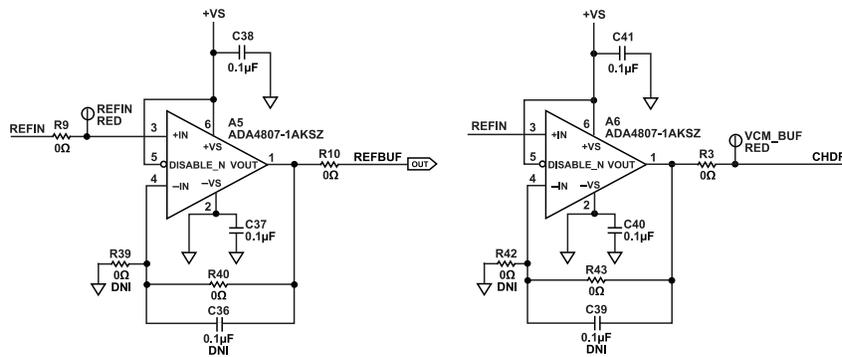


Figure 6. Reference Buffer Circuit Diagram

HARDWARE OVERVIEW

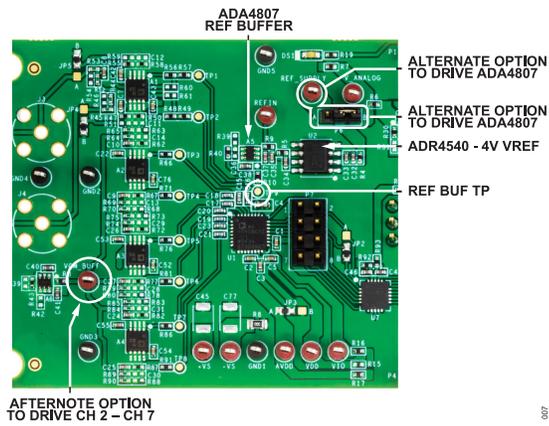


Figure 7. Location of Voltage Reference and Buffer Circuitry on EVAL-AD4692-ARDZ

**HARDWARE OVERVIEW**

**ANALOG FRONT END**

The EVAL-AD4692-ARDZ evaluation hardware has two channels (CH0 and CH1) configured for evaluating the AC performance of the AD4692 and six channels (CH2 to CH7) configured with a DC voltage. The remaining eight channels of the ADC are tied to ground.

By default, ADA4807-2 operational amplifiers (op amps) function as the ADC drivers for the AD4692 inputs (Figure 8). These drivers offer a low noise, low power solution suitable for ADC performance

evaluation and are powered with  $+V_S$  supplied from the V\_ANALOG rail (Figure 5) and  $-V_S$  connected to GND. Additionally, each driver comes in a common dual-amplifier, 8-lead MSOP package, allowing customers to populate alternative amplifiers for prototyping different ADC driver options with the AD4692.

At each AD4692 input, an RC filter is employed to limit the bandwidth of the input signal into the ADC. The RC values for the filter were optimized to maximize noise reduction in the input signal while still meeting the settling time of the ADC acquisition period.

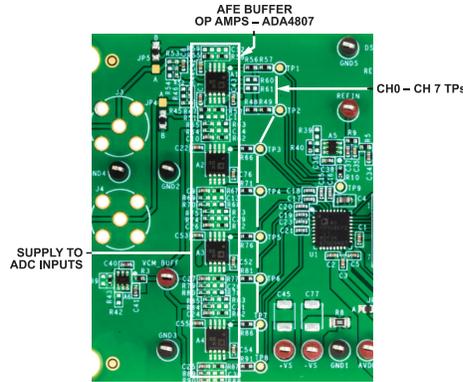


Figure 8. Location of Analog Front End Circuitry on EVAL-AD4692-ARDZ

## HARDWARE OVERVIEW

### AC Channels

For the AC input channels, female side launched Subminiature Version A (SMA) connectors are used to receive input signals from an external signal generator (additional SMA header locations are left unpopulated to add vertical facing SMA headers if preferred). To ensure the EVAL-AD4692-ARDZ supports bipolar and floating output signal generators, the SMA headers in the IN0 and IN1 channels are offset by a DC voltage (CHDR), as shown in [Figure 9](#). The DC voltage is generated by an on-board level-shift circuit via a summing junction. The following equation details how the signal applied to the noninverting terminal is generated from the combination of SMA headers and the summing resistors.

$$V_{INx} = \frac{V_{CHx} + V_{CHDR}}{2} \quad (1)$$

where:

$V_{INx}$  is the input voltage for Channel x of the AD4692.

**Table 4. Passive Component Settings for AC Channel Configurations**

Configuration	CH0	CH1
Unity Gain	Populate: R55, R58 JP5: Position B	Populate: R47, R50 JP4: Position B
Noninverting Gain	Populate: R55, R58, R59 JP5: Position B	Populate: R47, R50, R51 JP4: Position B
Inverting Gain	DNI: <sup>1</sup> R52, R53 Populate: R54, R58, R59 JP5: Position A	DNI: R44, R45 Populate: R46, R50, R51 JP4: Position A
1-Pole Low Pass Filter	Populate: R55, C8 JP5: Position B	Populate: R47, C7 JP4: Position B
2-Pole	Populate: R55, C8, R58, C12 JP5: Position B	Populate: R47, C7, R50, C11 JP4: Position B
Bypass	DNI: R55, R56 Populate: R61	DNI: R47, R48 Populate: R61

<sup>1</sup> DNI is do not install.

$V_{CHx}$  is the voltage applied to the Channel x SMA connectors.

$V_{CHDR}$  is the DC offset applied to all channels.

As described in the [Voltage Reference](#) section, the input range of the AD4692 is set by the  $V_{REF}$  voltage, meaning that the INx pins of the AD4692 have a voltage range of 0V to  $V_{REF}$ . Assuming unity gain configuration in the AFE and  $V_{CHDR}$  also being tied to  $V_{REF}$ , solve [Equation 1](#) to find that the  $V_{CHx}$  voltage has a range  $-V_{REF}$  to  $+V_{REF}$ .

The ADA4807-2 amplifiers driving the AC inputs are factory configured as unity-gain buffers but can be configured to implement common feedback topologies. By populating the surrounding passive components with reference to the table below, users can evaluate unity gain, noninverting with gain, and single-pole active filter configurations. When using optional feedback networks for gain, the input signals must be limited such that the output swings of the amplifiers stay within the AD4692 input range.

HARDWARE OVERVIEW

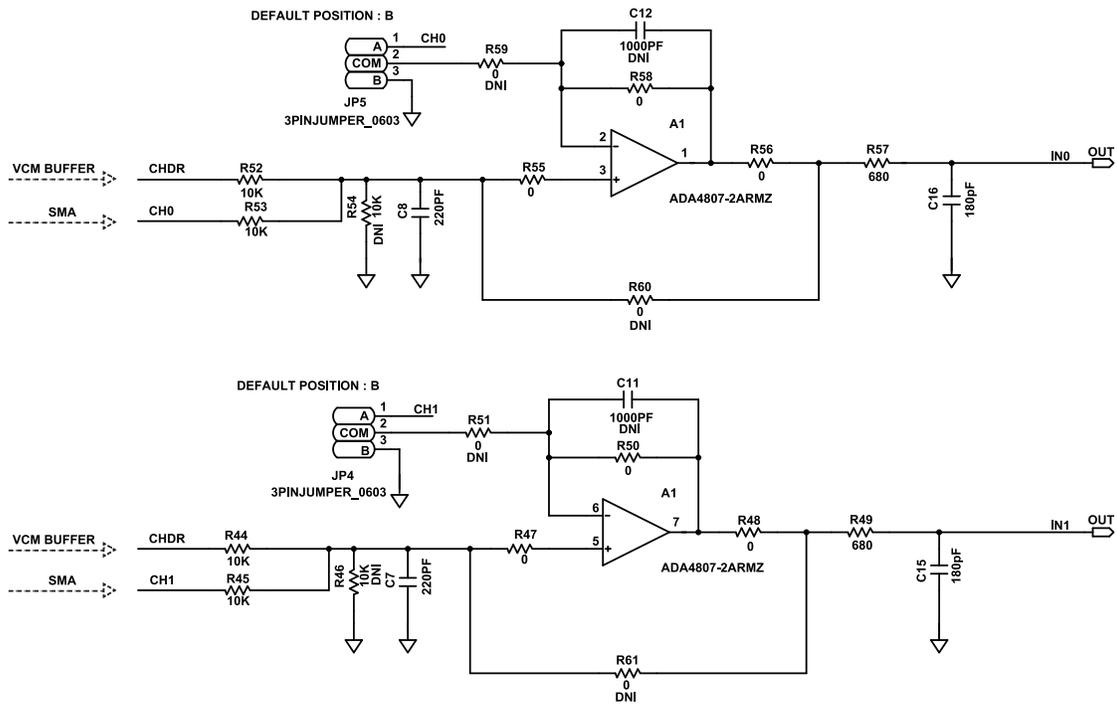


Figure 9. AC Channel Analog Front End Circuit Diagram

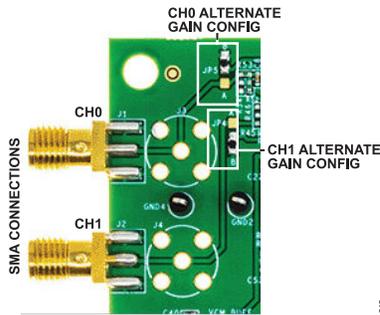


Figure 10. Location of AC Channel Inverting/Noninverting Jumper on the EVAL-AD4692-ARDZ

**HARDWARE OVERVIEW**

**DC Channels**

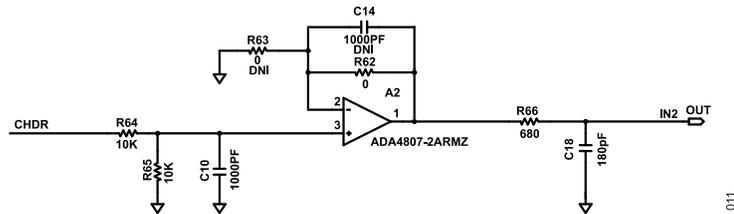
CH2 through CH7 are configured as DC channels and are provided to evaluate the settling accuracy performance when sequencing the multiplexer between channels or channel configurations. Figure 11 shows the circuit diagram for the DC channels. The inputs of the DC channels are driven by the CHDR signal fed through a resistor divider. By default, each resistor divider is populated with two 10kΩ resistors, meaning the voltage at the noninverting node of each ADC driver is set to VCM/2. Users can adjust the values

of the resistor divider values in order to individually set the DC voltage of each channel. Additionally, a 1nF capacitor is added on the noninverting terminals to band-limit and reject the thermal noise generated by the resistor divider circuits.

Additional noninverting gain and low-pass filtering are available to the DC channels through careful passive configuration. Please refer to the table below and the circuit schematic for proper passive configurations.

**Table 5. Passive Settings for DC Channel Configurations**

Configuration	CH2	CH3	CH4	CH5	CH6	CH7
Unity Gain	Populate: R62	Populate: R67	Populate: R72	Populate: R77	Populate: R82	Populate: R87
Noninverting Gain	Populate: R62, R63	Populate: R67, R68	Populate: R72, R73	Populate: R77, R78	Populate: R82, R83	Populate: R87, R88
Low Pass Filter	Populate: R62, C14	Populate: R67, C13	Populate: R72, C29	Populate: R77, C28	Populate: R82, C31	Populate: R87, C30



**Figure 11. DC Channel Analog Front End Circuit Diagram**

## HARDWARE OVERVIEW

### DIGITAL INTERFACE

The EVAL-AD4692-ARDZ uses serial peripheral interface (SPI) protocol for reading and writing data and a CNV input signal for initiating conversions. Digital signals are transmitted between the evaluation board and the controller board via the Arduino Uno digital headers (P3 and P4). The board follows the Arduino Uno standard for pin assignments, which are detailed in [Table 6](#). Refer to the EVAL-AD4692-ARDZ schematic PDF for additional details on the digital pin assignments and signal names.

The I/O logic levels of the AD4692 are set by the voltage applied to its  $V_{IO}$  pin. By default,  $V_{IO}$  is driven by the on-board LDO\_1.8V

supply rail, but an external voltage, up to a maximum of 1.8V, can be used to power the pin. If an external source is used, check with the AD4692 data sheet for the complete allowable range of  $V_{IO}$ .

In the default factory configuration, it is assumed that the controller board will be operating in the 3.3V I/O logic domain. To bridge the difference logic levels, a logic level translator is used to translate between domains. Please see the [Logic Level Translator](#) section for more details.

**Table 6. Arduino Header Pin Assignments**

Pin No.	Pin Name	Description
P2.2	IOREF	3.3 V supply to IOVDD rail.
P2.4	3.3V	Connected directly to the 3.3 V rail. See the <a href="#">Power Supply</a> section for details.
P2.5	5V	Connected directly to the 5 V rail. See the <a href="#">Power Supply</a> section for details.
P2.6	GND	Ground.
P2.7	GND	Ground.
P2.8	VIN	Connected to VIN rail as an alternative to power the evaluation board using DC power jack on the SDP-K1. Refer to the <a href="#">Power Supply</a> section for configuration details.
P3.3	10/PWM/CSB	Connected to CSB_1 with a 100k $\Omega$ pull up resistor.
P3.4	11/MOSI	Connected to MOSI_ARD with a 100k $\Omega$ pull up resistor.
P3.5	12/MISO	Connected to MISO_ARD with a 100k $\Omega$ pull up resistor.
P3.6	13/SCK	Connected to SCLK_ARD with a 100k $\Omega$ pull up resistor.
P3.7	GND	Ground.
P3.9	SDA	Connected to SDA_ARD feeding to the EEPROM. <sup>1</sup>
P3.10	SCL	Connected to SCL_ARD feeding to the EEPROM.
P4.2	TX + 1	Connected to GPO_ARD with a 100k $\Omega$ pull down resistor
P4.5	4	Connected to RSTb_ARD with a 100k $\Omega$ pull up resistor.
P4.6	5/PWM	Connected to CSB_2 with a 100k $\Omega$ pull down resistor.
P4.7	6/PWM	Connected to CNV_ARD with a 100k $\Omega$ pull up resistor.

<sup>1</sup> Electrically erasable programmable read-only memory.

## HARDWARE OVERVIEW

### Logic Level Translator

To accommodate the controller boards 3.3V logic level, an [ADG3308](#) logic level translator is included to translate to and from the AD4692 1.8V logic domain. The ADG3308 chip is split into two sides (Side A and Side Y), each with eight channels a set logic level.

By default, the chip is configured to translate between the 1.8V logic level of the AD4692 (Side A) and the 3.3V logic level of the SDP-K1 (Side Y). The A-side level is driven by the on-board LDO\_1.8V rail to ensure it matches the internal logic level of the board. The Y-side level is set by the 3.3V Arduino header of the controller board.

When making any changes to the logic level of either side, refer to the ADG3308 data sheet for the allowable voltage ranges.

### EEPROM

The EVAL-AD4692-ARDZ also includes an electrically erasable programmable read-only memory (EEPROM) to store the board ID. In production, the EEPROM is factory programmed to identify as the EVAL-AD4692-ARDZ. This information is polled by software to identify and connect to the board properly.

**HARDWARE SETUP**

This section details how to set up the EVAL-AD4692-ARDZ and SDP-K1 boards for use with the AD4692 ACE plugin. Refer to the [Hardware Overview](#) for detailed descriptions of the on-board circuit blocks and for descriptions of all jumpers referenced in the following instructions.

To setup the hardware, complete the following steps:

1. Disconnect both the evaluation board and the SDP-K1 from all sources of power before connecting them together.
2. Connect the two boards via the Arduino Uno compatible headers (P1 to P4 on the EVAL-AD4692-ARDZ).
  - a. Plug the headers on the bottom side of the evaluation board to the corresponding headers on the top side of the SDP-K1.
3. Set the P14 (VIO\_ADJUST) jumper on the SDP-K1 to 3.3V.
  - a. Although the AD4692 operates on 1.8V digital logic, the evaluation board uses a logic level translator to translate to a 3.3V logic domain for demonstrative purposes.

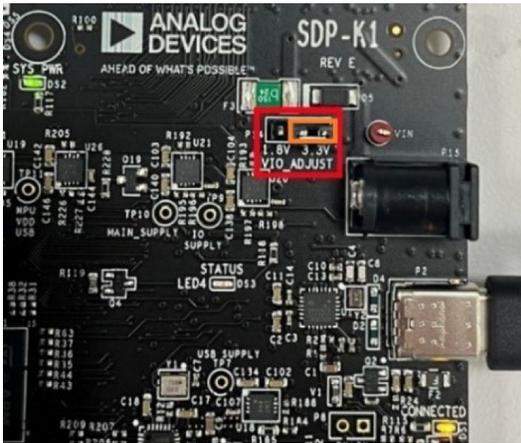


Figure 12. VIO\_ADJUST Jumper on SDP-K1 Board Set to 3.3V

4. Set the P6 jumper on the EVAL-AD4692-ARDZ to **Position B**.
  - a. **Position B** connects the reference circuitry of the evaluation board to the on-board power supply. To power the reference circuitry externally, set P6 to **Position A** and apply external power to the REF\_SUPPLY testpoint.



Figure 13. P6 Jumper on EVAL-AD4692-ARDZ Set to Position B

5. Connect the SDP-K1 to the PC via the USB-C to USB cable.
6. Ensure that the SDP-K1 is the only device on the PC's USB port (do not use a USB hub that is also connected to other devices).
7. The DS2 LED (SYS\_PWR) on the SDP-K1 and the DS1 LED on the evaluation board will illuminate to indicate both boards are receiving power from the USB.
8. The DS1 LED (CONNECTED) will illuminate to indicate the SDP-K1 has been detected and connected to the PC.



Figure 14. Power and Connection LED Locations for the IEVAL-AD4692-ARDZ and SDP-K1 Boards

9. Ensure the boards show up as a device in Windows device manager as the USB serial device.

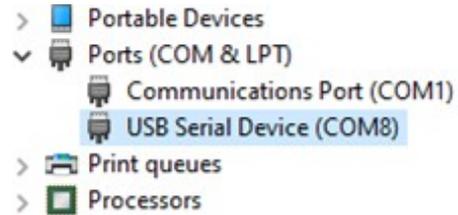


Figure 15. Device Manager Window with Hardware Connected via USB Port

**EVALUATION BOARD SOFTWARE**

The Analog Devices, Inc., [ACE](#) application provides a plug and play evaluation experience, enabling users to quickly configure controller board attributes, perform data captures, and analyze results. The AD4692 ACE plugin is the evaluation GUI that interfaces with the firmware on the SDP-K1 controller board to communicate with the connected EVAL-AD4692-ARDZ. ACE must be installed prior to installing and running the AD4692 ACE plugin.

**SOFTWARE INSTALLATION**

To evaluate the performance of the AD4692 and utilize the EVAL-AD4692-ARDZ with ACE, the following systems and software packages are required:

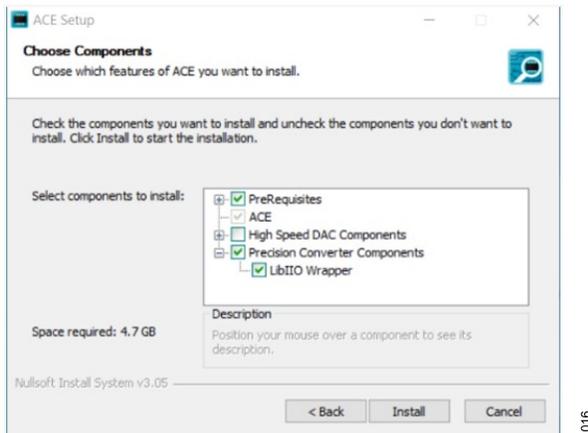
- ▶ PC with Windows 10 or later operating system
- ▶ ACE software tool
- ▶ AD4692 ACE plugin package

**Installing ACE and ACE Components**

The following are steps for installing ACE with the necessary components for the AD4692 ACE plugin.

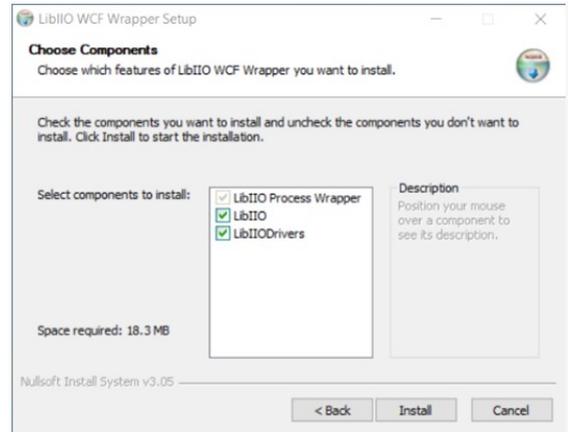
1. Download the ACE Installer from the ACE download page.
2. From the download menu, run the ACE Installer.

When selecting components to install, ensure that both **PreRequisites** and **Precision Converter Components** are included in the installation as shown in [Figure 16](#).



**Figure 16. ACE Installation Components**

When the following pops up as part of the **LibIIO Wrapper** installation, ensure all items are selected as shown in [Figure 17](#).

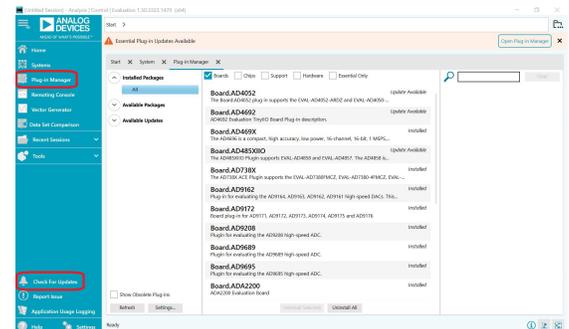


**Figure 17. LibIIO Wrapper Components**

If ACE is already installed, ensure the latest version is installed by using the **Check for Updates** option in the ACE sidebar (bottom left of the application). Also ensure the **LibIIO Process Wrapper** components are installed by clicking the **IIO WCF Wrapper Installer** in the **Help > Application Resources > IIO Resources > Installer Links**. This will run the **IIO WCF Wrapper Install**.

**Installing the AD4692 ACE Plugin**

1. Before installing the AD4692 plugin, make sure you have the latest version of ACE by using the **Check For Updates** button at the bottom of the ACE sidebar, as shown in [Figure 18](#).
2. Select the **Plug-in Manager** ([Figure 18](#)) from the ACE sidebar to see a list of all installed and available plugins for this version of ACE.



**Figure 18. ACE Plugin Manager**

3. Select **Available Packages** and search for the AD4692 board plugin. Once found, select the name and click **Install Selected** at the bottom of the window.

To manually install the plugin, perform the following steps:

1. Download the most recent AD4692 plugin from the [ACE web-site](#) as an .acezip file.
2. Open ACE, navigate to the settings menu, and open the plugin options.

## EVALUATION BOARD SOFTWARE

- Under **Zipped Plug-In Sources** you can select the plus symbol to add a custom ACE plugin.
- Name it **AD4692** and point the source to the .acezip file on your PC.

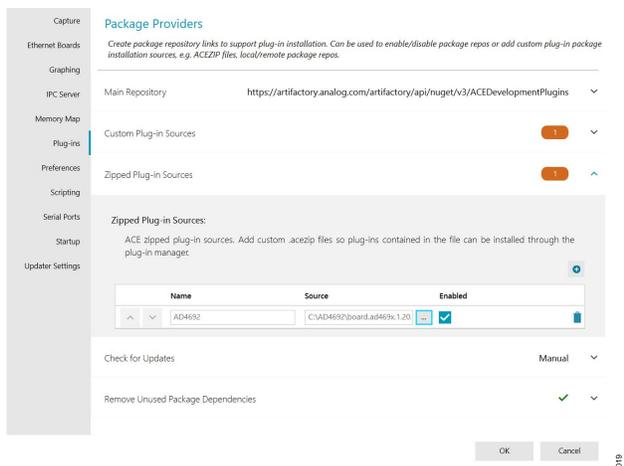


Figure 19. ACE Custom Plugin Settings

- Click **OK** at the bottom of the window and navigate to the **Plug-in Manager**.
- Select **Available Packages** and search for the AD4692 board plugin. Once found, select the name and click **Install Selected** at the bottom of the window.

Once it is done installing, close and reopen the ACE program. Navigating to the plugin manager, you should now see the **Board.AD4692** plugin under the **Installed Packages**. From here, open the **Available Updates** section to check to see if there is an update available for **Board.AD4692**. If an update is listed, please select and install the update to have the most recent release of the plugin. If an update is installed, ACE will need to be closed and reopened again for the changes to take effect.

LAUNCHING THE SOFTWARE

To start the ACE software, open the Windows start menu and search for ACE. Once found, open the software, and it will begin searching for connected boards. If the software does not recognize the EVAL-AD4692-ARDZ, press the reset button on the SDP-K1 and click **Refresh Attached Hardware** in the ACE homepage window. Once the board is recognized, the AD4692 ACE plugin icon will be populated in the **Attached Hardware** list by ACE.



Figure 20. ACE Attached Hardware List

When the software detects the SDP-K1 controller board, a prompt may appear asking whether to reprogram with standard firmware. Select **No** to stop ACE from overwriting the AD4692 firmware on the SDP-K1.

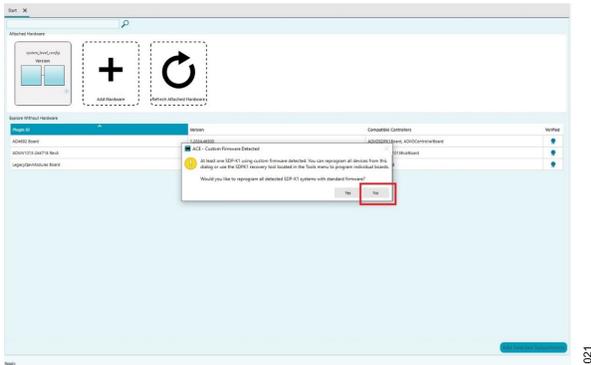


Figure 21. ACE Custom Firmware Detected Prompt

Selecting the AD4692 ACE plugin icon opens the EVAL-AD4692-ARDZ **Board View**. If there is a mismatch between the firmware loaded on the SDP-K1 and the expected firmware in ACE, another prompt will appear asking to load the expected version of the firmware. Select **Yes** to let ACE update the firmware to the expected version. During the loading process, the software will be unresponsive and the DS1 LED on the SDP-K1 board will begin flashing quickly. Once the update is complete, the DS1 LED will be a solid color again.

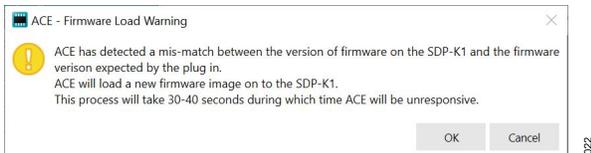


Figure 22. Firmware Mismatch Error

From the **Board View**, click on the AD4692 symbol to enter the **Chip View**. The **Chip View** offers a block level diagram of the AD4692 functionality and a configuration side-window. Click **Proceed to Documentation** at the bottom right-hand side of the

window to open the plugin documentation for descriptions of each window and feature within the plug-in as well as troubleshooting help.

Click **Proceed to Analysis** to navigate to the **Analysis** window. From here, choose the type of analysis to be performed by selecting the **Waveform** tab, **Histogram** tab, or **FFT** tab. Select **Run** to perform a data capture that will appear in the results section and the waveform plot window.

The **Waveform** tab displays data in the form of time vs. discrete data values, as shown in Figure 23. The user can zoom in on and pan over the waveform graph using the embedded waveform tool bar located above the graph. Select the channels to display in the **Channels** section.

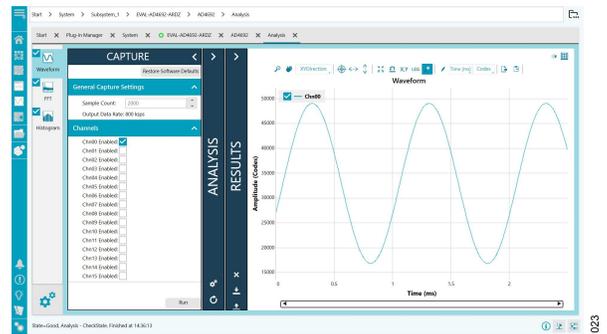


Figure 23. ACE Waveform Analysis Window

The **FFT** tab displays the Fast Fourier Transform (FFT) information for the last batch of samples captured (Figure 24). The **Results** panel shows AC performance metrics of the AD4692.

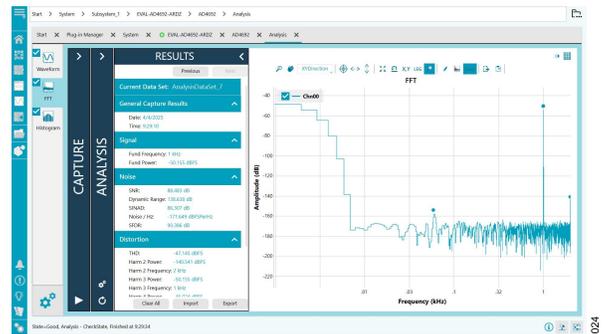


Figure 24. ACE FFT Analysis Window

The **Histogram** tab contains the histogram of the data points collected, with the **Results** panel displaying statistical information. This includes important noise information for DC signals.

### LAUNCHING THE SOFTWARE

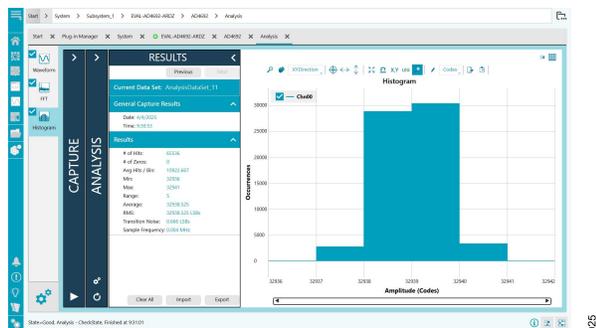


Figure 25. ACE Histogram Analysis Window

## ORDERING INFORMATION

## EVALUATION BOARDS

Table 7. Evaluation Boards

Model <sup>1</sup>	Description
EVAL-AD4692-ARDZ	AD4692 Evaluation Board

<sup>1</sup> Z = RoHS-Compliant Part.

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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