# Evaluating the AD4630-20/AD4632-20 20-Bit, 2MSPS/500kSPS Dual-Channel SAR ADCs

## FEATURES

- Fully-featured evaluation board for AD4630-20/AD4632-20
- Analysis | Control | Evaluation (ACE) Software plug-in available for device configuration, data capture, and performance evaluation
- On-board reference, reference buffer, clock source, and ADC drivers
- On-board power supplies
- FMC compatible

## EVALUATION KIT CONTENTS

- EVAL-AD4630-20FMCZ evaluation board
- Micro-SD memory card with SD adapter, which contains system board boot software and Linux OS
- Instructions to download software

## EQUIPMENT NEEDED

- Digilent ZedBoard® with 12V wall adapter power supply
- Precision signal source
- SMA cable(s) to connect a signal source to the EVAL-AD4630-20FMCZ evaluation board
- PC running Windows® 10 operating system or higher

## DOCUMENTS NEEDED

- AD4630-20/AD4632-20 data sheet

## SOFTWARE NEEDED

- ACE Software
- AD4630-20 ACE plug-in

## GENERAL DESCRIPTION

The EVAL-AD4630-20FMCZ is a fully-featured evaluation board designed to evaluate all the features of the AD4630-20 analog-to-digital converter (ADC). The AD4630-20 is a 2MSPS per channel, low power, dual-channel 20-bit successive approximation register (SAR) ADCs while the AD4632-20 is a dual-channel 24-bit precision SAR ADC that supports up to 500kSPS per channel. The evaluation board shows the performance of the AD4630-20/AD4632-20 and provides a configurable analog front end (AFE) for a variety of system applications.

The evaluation board is designed for use with the Digilent ZedBoard. The ZedBoard is used to control data capture and buffering. The evaluation board connects to the ZedBoard board by a field-programmable gate array (FPGA) mezzanine card (FMC) low-pin count (LPC) connector. The ZedBoard hosts a Xilinx® ZYNQ®7000 SoC, which has two processor cores and programmable FPGA fabric. The ZedBoard connects to the PC through USB. The ZedBoard controls the evaluation board through the USB port of the PC using the ACE Software, which is available for download from the ACE Software page.

Full specifications on the AD4630-20/AD4632-20 are available in the AD4630-20/AD4632-20 data sheet available from Analog Devices, Inc., and must be consulted with this user guide when using the EVAL-AD4630-20FMCZ evaluation board.

For the current schematics, printed circuit board (PCB) layouts, and bill of material (BOM), refer to the EVAL-AD4630-20FMCZ product page.

PLEASE SEE THE LAST PAGE FOR AN IMPORTANT
WARNING AND LEGAL TERMS AND CONDITIONS.

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## REVISION HISTORY

**6/2026—Revision 0: Initial Version**

## EVAL-AD4630-20FMCZ EVALUATION BOARD PHOTOGRAPH

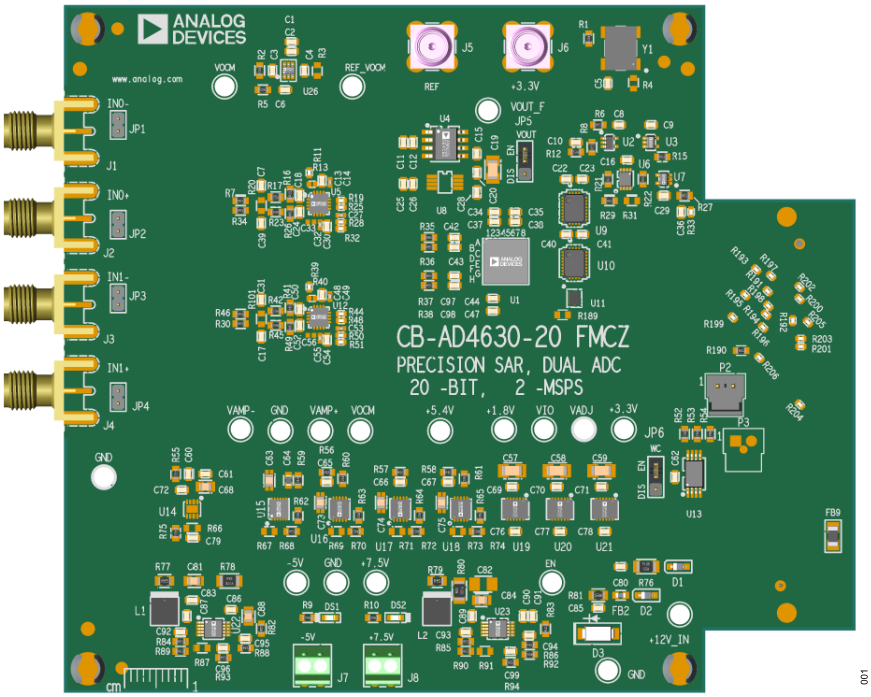


*Figure 1. EVAL-AD4630-20FMCZ Evaluation Board Photograph*

## QUICK START PROCEDURE

By default, the ZedBoard powers and controls the EVAL-AD4630-20FMCZ evaluation board. To evaluate the AD4630-20, do the following steps:

1. Download and install the ACE Software. If ACE Software is already installed, make sure to check the latest version is installed by using the **Check For Updates** option in the ACE sidebar.
2. An ACE Quick start guide is available here: ACE Quickstart - Using ACE and Installing Plug-ins.
3. Connect the EVAL-AD4630-20FMCZ evaluation board and ZedBoard firmly together through FMC connector (see Figure 2).
4. Insert the SD card provided with the EVAL-AD4630-20FMCZ evaluation board into the SD card slot of ZedBoard.
5. Connect the ZedBoard's USB OTG port (next to PMOD connector JE1) to the PC by the micro-USB cable.
6. Connect 12V wall wart adapter to ZedBoard and slide the POWER switch (SW8) on the ZedBoard to ON position.
7. Check if the Green POWER LED (LD13) and the Blue Done LED (LD12) on the ZedBoard turn on.
8. Wait for the Red LEDs (LD0, LD1) on the ZedBoard to start blinking.
9. Launch the ACE Software from the **ACE** subfolder in the **Analog Devices** folder in the **All Programs** menu.
10. Connect a precision signal source to the EVAL-AD4630-20FMCZ evaluation board differential inputs (J1, J2, J3, and J4), by using an XLR cable, and a SMA to XLR Adapter board. Typically, use a 3.3Vrms signal at 1kHz.
11. To monitor the results, see the Analysis Tab, Time Domain (Waveform) Plot, and Frequency Domain (FFT) Plot sections.

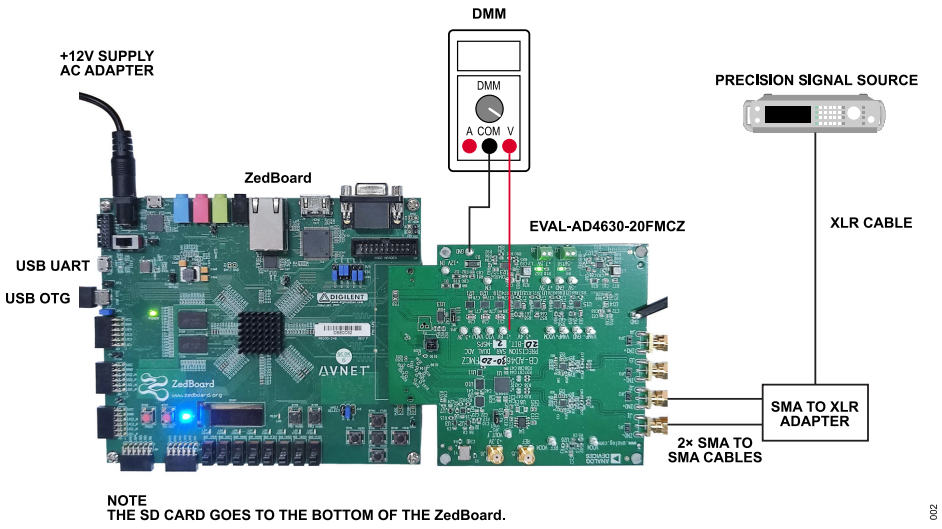


*Figure 2. EVAL-AD4630-20FMCZ ZedBoard (Left) Connected to the EVAL-AD4630-20FMCZ Evaluation Board (Right)*

## EVALUATION BOARD HARDWARE GUIDE

### POWER SUPPLIES

The EVAL-AD4630-20FMCZ evaluation board is designed to operate from a 12V power supply provided from the host controller board by the FMC connector (see Table 1). The 12V power supply is regulated to an intermediate voltage with switching regulators, then post-regulated to various voltage rails.

The block diagram in Figure 3 shows all the available power supply options on the EVAL-AD4630-20FMCZ evaluation board. In case necessary, it is possible to supply all the LDOs directly from external power supplies by J7 and J8. There are also two options for generating −3.3V, although only the LT3093 is mounted on the board.

*Table 1. Board Power Supplies*

| Power Supply | Voltage Range (V) | Description |
|---|---|---|
| +12V | 12 | Main board power supply by FMC for all internal voltage regulators. |
| GND | | Ground. |
| +3.3V | 3.3 ± 5% | 3.3V supply for various digital circuits. |
| +1.8V | 1.8 ± 5% | VDD_1.8V ADC supply. |
| VIO | 1.8 ± 5% | ADC digital input/output (I/O) interface supply. |
| +5.4V | 5.4 ± 5 % | VDD_5V ADC supply. |
| REFIN | 5 ± 5% | 5V ADC reference supply. |
| VAMP+ | 6.4 ± 5% | Amplifier positive power supply. |
| VAMP− | −3.3 ± 5% | Amplifier negative power supply. |

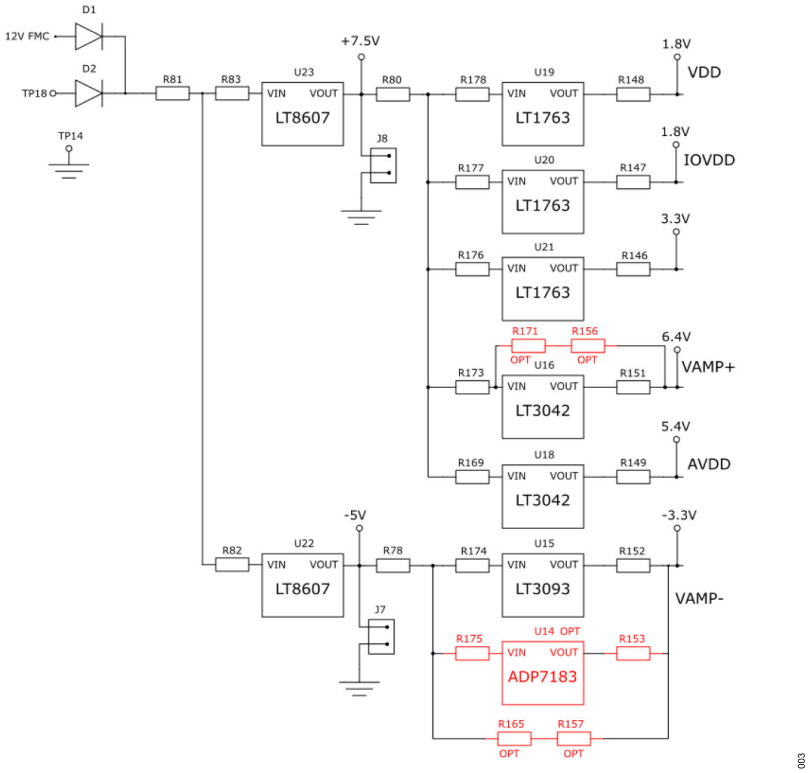


*Figure 3. Power Circuitry Diagram*

## EVALUATION BOARD HARDWARE GUIDE

### ADC POWER SUPPLIES

The AD4630-20 devices require the following three major power supplies:

- VDD_5V: 5.4V analog supply rail.
- VDD_1.8V: 1.8V ADC core supply.
- VIO: 1.8V: Digital I/O interface supply.

The AD4630-20 includes integrated power supply decoupling, therefore, no external power supply decoupling is included on the EVAL-AD4630-20FMCZ evaluation board for the ADC power supply rails.

A user can configure the following in this circuit:

- 1.8V rails (VDD and IOVDD) source:
  - On-board generated rails (default): The LT1763 regulators (U19 and U20) supply the rails in this circuit, as shown in Figure 3.
- 5.4V rail source:
  - On-board generated rail (default): An LT3042 LDO regulator (U18) supplies the rail, as shown in Figure 3.

### AMPLIFIER SUPPLIES

The signal conditioning circuitry of the EVAL-AD4630-20FMCZ evaluation board is designed to operate from +6.4V and −3.3V rails. The +6.4V VAMP+ rail and the −3.3V VAMP− rail supply the positive and negative rails of the fully-differential U5 and U12 amplifiers.

A resistor-divider network generates the VOCM from the on-board reference U4 and passes it through a common-mode buffer amplifier U26. This circuit configures the buffer for a unipolar power supply, the +6.4V VAMP+ rail provides the positive supply to U26, and ground connects to the negative supply rail.

### REFERENCE CIRCUIT

By default, the on-board ADR4550 provides a 5V reference to the AD4630-20. It drives the REFIN pin of the ADC through an R-C filter (R = 100Ω, C = 22µF) to reduce low-frequency noise. The REFIN pin is connected to an internal buffer, which eliminates the need for an external buffer. However, the user can connect an external reference to the J5 SMA connector to drive the internal buffer (see Figure 4). Populate R124 with a 0Ω resistor, and leave R116 and R123 open. Attach an external reference to the REF turret on the board to bypass the internal buffer. Disable the internal reference buffer to reduce the ADC power consumption (for more details, refer to the respective product's data sheets). There is also the option to mount the LTC6655 or the LTC6655LN reference, which is suitable to use it together with the unbuffered input of the ADC.

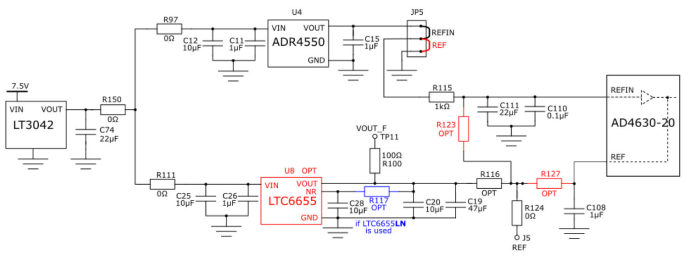


*Figure 4. EVAL-AD4630-20FMCZ Evaluation Board Reference Circuit*

### CLOCK CIRCUIT

The ZedBoard uses a 100MHz reference clock to generate its internal clocks as well as the sample clock for the AD4630-20. To simplify the system operation, an on-board 100MHz, low-jitter crystal oscillator (XO) on the EVAL-AD4630-20FMCZ evaluation board provides this clock by default, as shown in Figure 5. To use an external clock source, remove R1 and connect it to J6, the CLK IN SMA. The external clock frequency must be < 100MHz. Use a low-jitter clock source to achieve optimal system performance. Set the external clock level to 10dBm to 12dBm.

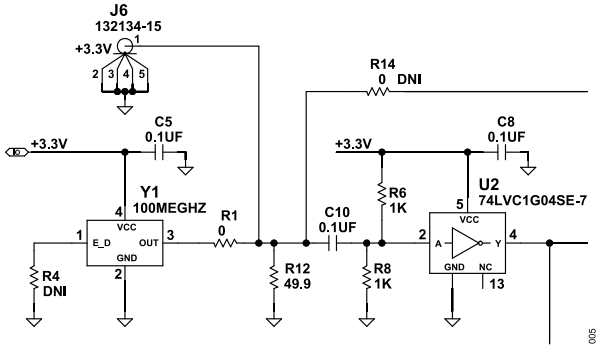


*Figure 5. EVAL-AD4630-20FMCZ Evaluation Board Clock Circuit*

### ANALOG FRONT END (AFE) CIRCUIT

The EVAL-AD4630-20FMCZ evaluation board uses a flexible, configurable driver network for various topologies. The default network is shown in Figure 6, where the ADA4945-1 fully-differential amplifier U5 and U12 drives the ADC. It can accommodate both single-ended and differential signal sources and drives the ADC differentially. As populated, it has a unity gain. Terminate the unused input with the equivalent source impedance when using a single-ended source. Note that, as implemented, the ADA4945-1 driver on the evaluation board preserves the differential value of IN+ − IN− (with appropriate gain scaling applied) but inverts the signal polarity injected to the ADC. Hence, apply a positive DC signal to IN_A/B− and a negative DC signal to IN_A/B+ to preserve the signal polarity.

## EVALUATION BOARD HARDWARE GUIDE

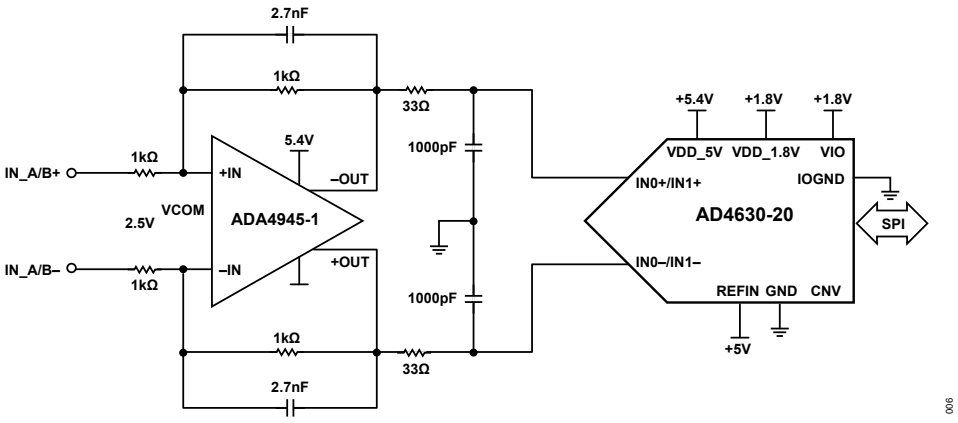


*Figure 6. Differential Driver AFE*

## CONTROLLER BOARD

The ZedBoard (the system controller board, see Figure 7) enables the configuration of the ADC and capture of data from the EVAL-AD4630-20FMCZ evaluation board by the PC by USB (or Ethernet). The AD4630-20 supports a multilane serial-port interface (SPI) for each data converter channel. The SPI interface for each channel is connected to the ZedBoard by the FMC connector (P1). The ZedBoard functions as the communication link between the PC and connected evaluation board. It buffers samples captured from the evaluation board in its DDR3 memory. The ZedBoard board requires power from a 12V wall adapter (included with the ZedBoard). It hosts a Xilinx ZYNQ7020 SoC, which contains two ARM® Cortex-A9 processors and a Series-7 FPGA with 85k programmable logic cells. A Linux OS runs on the host processor system. It communicates with the PC through either a USB 2.0 high speed port or a 10/100/1000 Ethernet port. The default software configuration uses USB.

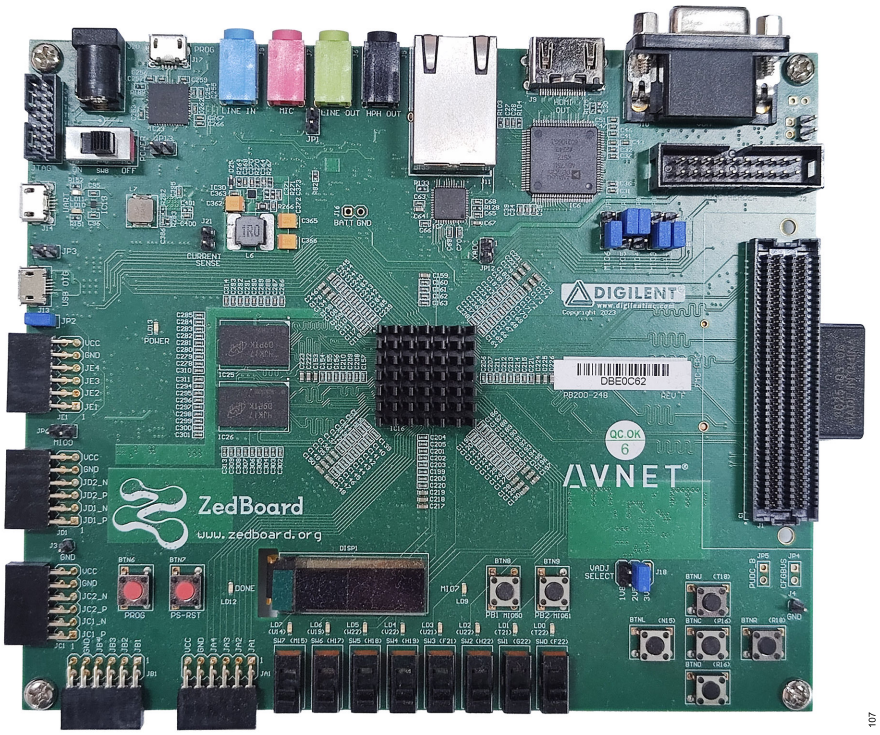


*Figure 7. Controller Board of the EVAL-AD4630-20FMCZ Evaluation Board*

## EVALUATION HARDWARE SETUP PROCEDURE

To get the hardware ready for the evaluation, do the following steps:

1. Insert the SD card from the EVAL-AD4630-20FMCZ evaluation kit into the SD card slot (J12) of the ZedBoard, as shown in Figure 8.
2. Ensure that the ZedBoard boot configuration jumpers (JP7 to JP11) are set, as shown in Figure 9.
3. Ensure that the VADJ SELECT jumper (J18) is in the **2V5** position, as shown in Figure 10.
4. Connect the FMC connector (P3) of the EVAL-AD4630-20FMCZ evaluation board to the FMC connector (J1) of the ZedBoard.
5. Connect the 12V power supply included in the ZedBoard kit to the DC barrel jack (J20) of the ZedBoard, one USB cable between the PC and the USB on the go (OTG) connector (J13), and the other USB cable between the PC and the USB universal asynchronous receiver-transmitter (UART) connector (J14).
6. Slide the power switch (SW8) to the **ON** position to power up the ZedBoard and evaluation hardware.
7. The hardware is now ready to be used through the ACE Software.

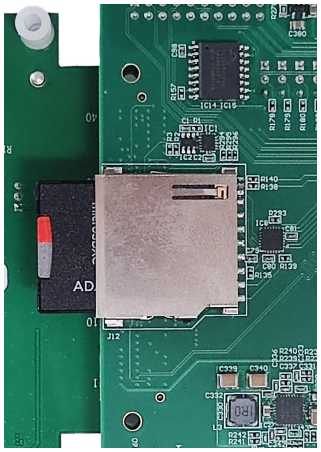

*Figure 8. Controller Board SD Card Slot*

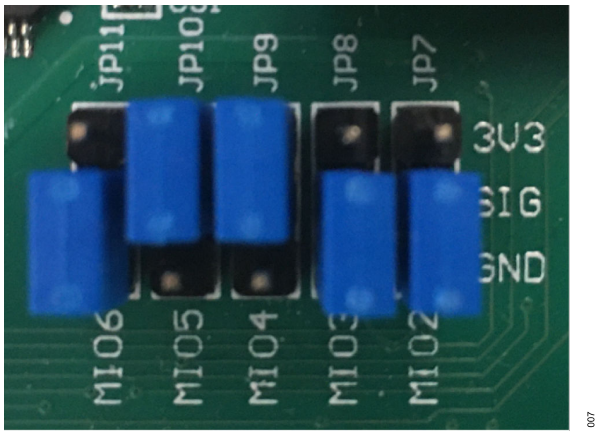


*Figure 9. Jumpers Configuration*


*Figure 10. Controller Board VADJ SELECT Jumper Configuration*

## SAMPLING RATE

Table 2 shows the maximum sampling rates achievable based on the device configuration. Note that the FPGA SPI engine only supports Zone 2 data transfers from the AD4630-20.

*Table 2. Maximum Sampling Rate by Device Configuration*

| Clocking Mode | Lane Mode (Per Channel) | Data Rate | Data Format | Maximum Sampling Rate (MSPS) |
|---|---|---|---|---|
| SPI | 1 | Single (SDR) | 32-bit | 1.75[1] |
| | 1 | SDR | 20-bit | 2 |
| | 1 | Dual (DDR) | 32 or 20-bit | 2 |
| | 2 | SDR or DDR | 32 or 20-bit | 2 |
| | 4 | SDR or DDR | 32 or 20-bit | 2 |
| Echo Clock | 1 | SDR | 32-bit | 1.75[1] |
| | 1 | SDR | 20-bit | 2 |
| | 1 | DDR | 32 or 20-bit | 2 |
| | 2 | SDR or DDR | 32 or 20-bit | 2 |
| | 4 | SDR or DDR | 32 or 20-bit | 2 |

[1] The sampling rate in single lane, 32-bit output formats in SDR mode is limited by the FPGA SPI engine, and this is not a limitation of the AD4630-20 device.

## SOFTWARE SUPPORT

### EVALUATION SOFTWARE

The EVAL-AD4630-20FMCZ evaluation board hardware is controlled and configured through the ACE Software. ACE is a desktop software application that allows the evaluation and control of multiple evaluation systems from across the Analog Devices product portfolio. The controller board supported by ACE for use with the EVAL-AD4630-20FMCZ evaluation board is the ZedBoard.

For the ACE installation and documentation instructions, refer to the ACE Software. To install the necessary EVAL-AD4630-20FMCZ evaluation board plug-in, the instructions are as follows:

- If ACE runs on a machine with internet access, then a user can find, install, and update plug-ins directly from the ACE application. For environments without internet access, a user can download these plug-ins from the previous link to portable storage and install them into ACE.
- Note that for the product-specific documentation for the evaluation software, check within the ACE plug-in.

### EMBEDDED SOFTWARE

Open-source firmware examples, drivers, and hardware description language (HDL) are used to build the embedded software for evaluation. When available, to find the links, refer to the software section on the relevant product page.

If the required embedded software is unavailable, then a user can submit a request from the product page.

The EVAL-AD4630-20FMCZ evaluation board comes with an SD card in the box. The SD card provides a version of the Analog Devices Kuiper Linux for evaluation image that can boot the controller board. The ACE evaluation board plug-in is capable of interacting with the installed image to identify the connected hardware and provide target specific configuration data and files.

Use the Troubleshooting Guide for ADI Kuiper Linux for ACE Evaluation when issues occur with the provided SD card. To recover a corrupted SD card image or to obtain the latest version of the Analog Devices Kuiper Linux for evaluation image, refer to the Linux Software. This page also provides details on how to format and set up the SD card correctly.

The latest version of the Analog Devices Kuiper Linux for evaluation contains support for Linux run-time configuration (LRC) of ACE plug-ins, by the ACE Software application. Once connected to the PC, the ACE application automatically detects the EVAL-AD4630-20FMCZ evaluation board connected to the ZedBoard. If the Analog Devices Kuiper Linux kernel running from the SD card is not configured for the connected evaluation board, an **ACE - Unexpected Linux Kernel Found** window appears, as shown in Figure 11. Click **OK** to install the updated kernel and establish connectivity with the hardware.

Note that once a user clicks **OK**, ACE downloads the kernel update to the carrier board (ZedBoard) and then reinitializes the kernel. Initialization takes approximately 60seconds to 80seconds to complete. Once the process completes, the ACE plug-in opens.

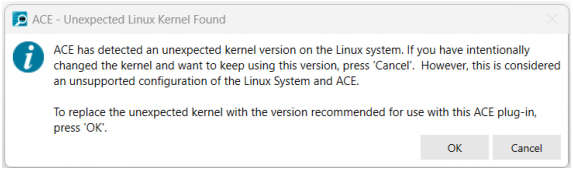


*Figure 11. ACE LRC Reconfiguration of Kuiper Linux Prompt on Detection of EVAL-AD4630-20FMCZ Evaluation Board*

### HOST PC SOFTWARE

The embedded Linux stack is based on the IIO (Industrial I/O) architecture. This enables tools such as Python, through the pyadi-iio package, or MATLAB with the precision toolbox license to communicate with the evaluation and controller board without the need for ACE. When supported, to find the links to example code, refer to the software section on the ADC product page.

If the Python or MATLAB software support is unavailable for the product, then a user can submit a request from the product page.

Generic, not product-specific, IIO tools such as the IIO Oscilloscope, Scopy, and IIO command line tools provide basic, low-level functionality and work with any IIO platform.

Once the hardware setup completes as per the Evaluation Hardware Setup Procedure section, and the software installs, as specified in the Software Support section, then run the ACE Software for evaluation. When ACE opens, it automatically detects and displays the EVAL-AD4630-20FMCZ evaluation board in the **Attached Hardware** panel, as highlighted in yellow in Figure 12.

Double-click the **EVAL-AD4630-20FMCZ** icon and a new tab, **EVAL-AD4630-20FMCZ**, opens that displays a block diagram of the EVAL-AD4630-20FMCZ, as shown in Figure 13.

This offers a board level view of the EVAL-AD4630-20FMCZ evaluation board. Double-click the AD4630-20 component in the board view to open an AD4630-20 tab. This tab displays an **INITIAL CONFIGURATION** pane, the **AD4630-20** device block diagram, and two buttons (**Proceed to Memory Map** and **Proceed to Analysis**) in the lower-right corner, as highlighted in yellow in Figure 14.

The tabs accessed through these two buttons provide the means to configure and to evaluate the AD4630-20. For more details, see the AD4630-20 Memory Map and the Analysis Tab sections.

## SOFTWARE SUPPORT

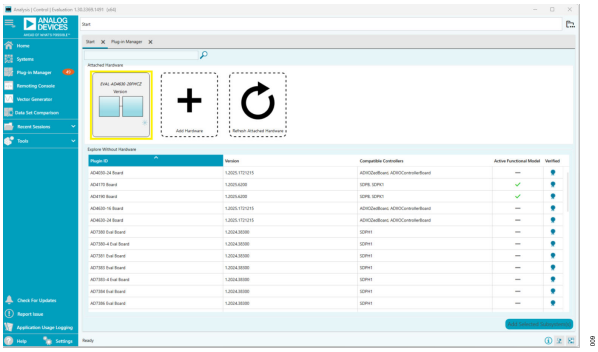

*Figure 12. Autodetection of the EVAL-AD4630-20FMCZ in the ACE Start Tab*

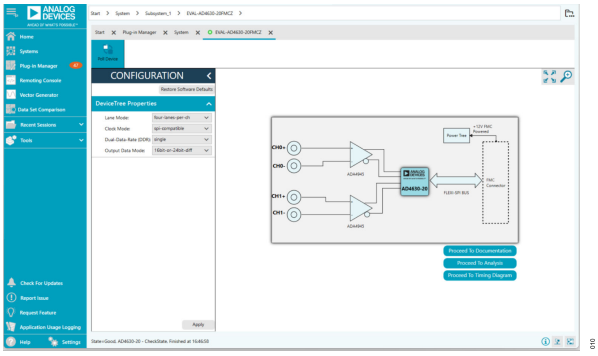

*Figure 13. EVAL-AD4630-20FMCZ Tab Open in the ACE Software*

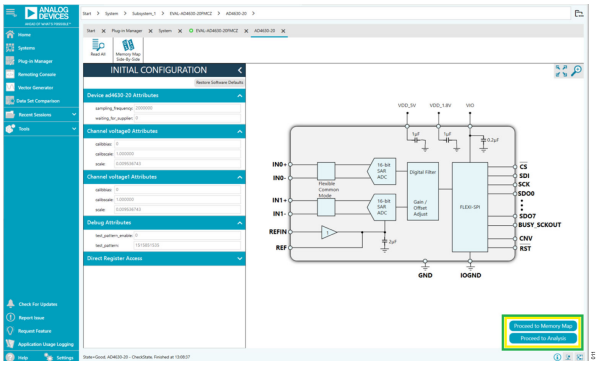

*Figure 14. AD4630-20 Tab in the ACE Software*

## AD4630-20 MEMORY MAP

Click **Proceed to Memory Map** within the **AD4630-20** tab to open the **AD4630-20 Memory Map** tab, as shown in Figure 15.

This tab displays the current register content from the AD4630-20 and facilitates content updates to the memory map through serial read or write (if applicable) operations. For the normal operation of the evaluation kit, no modifications are required to the ADC register content.

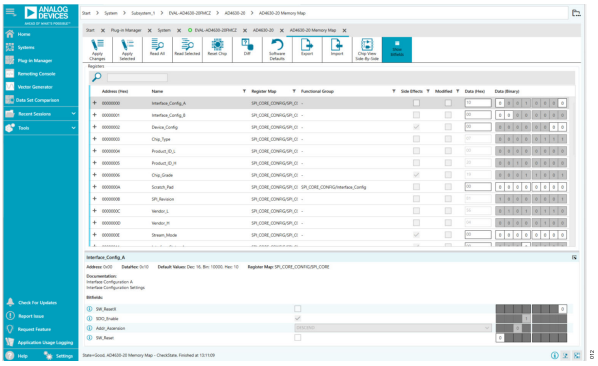

*Figure 15. AD4630-20 Memory Map Tab in the ACE Software*

## ANALYSIS TAB

Click **Proceed to Analysis** within the **AD4630-20** tab to open the **ANALYSIS** tab. This tab captures data from the evaluation board and displays the obtained data and corresponding analysis results.

The **Analysis** tab contains three collapsible panels (**CAPTURE**, **ANALYSIS**, and **RESULTS**) and a data plot area to the right. Clicking the arrow to the right of the panel name collapses any of the three panels and frees up more space for the data plot area when needed.

The functions of these panels are as follows:

- The **CAPTURE** panel allows a user to set the number of samples per dataset, trigger a single acquisition, and start or stop continuous acquisition of multiple datasets.
- The **ANALYSIS** panel displays options related to the frequency domain analysis.
- The **RESULTS** panel provides metrics for the current dataset displayed in the plot area. It provides different metrics, which depend on the selected plot type (for more details, see the Time Domain (Waveform) Plot, the Frequency Domain (FFT) Plot, and the Histogram Plot sections). This panel also allows navigating between the datasets acquired during the session and facilitates importing and exporting datasets in the internal format used by the ACE Software.

The user can display the acquired datasets as a time-domain waveform (default), a frequency-domain plot using a fast Fourier transform (FFT), or a histogram by clicking any of the three corresponding buttons to the left of the **CAPTURE** panel (see Figure 16).

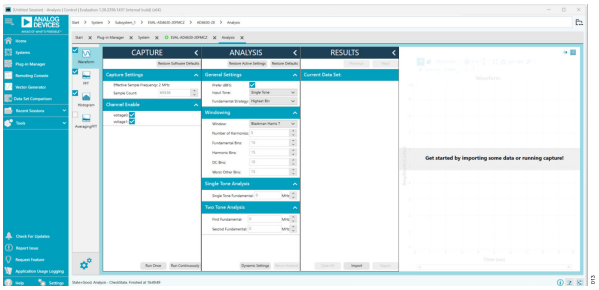

*Figure 16. Analysis Tab in the ACE Software*

## SOFTWARE SUPPORT

### TIME DOMAIN (WAVEFORM) PLOT

Click the **Waveform** area (highlighted in yellow in Figure 17) to display the active dataset as a time-domain waveform (default view). Note how collapsing the **CAPTURE** and **ANALYSIS** panels improves the plot display.

When the dataset is plotted as a time-domain waveform, the **RESULTS** panel displays metrics relevant to time-domain analysis, such as minimum, maximum, average, and RMS.

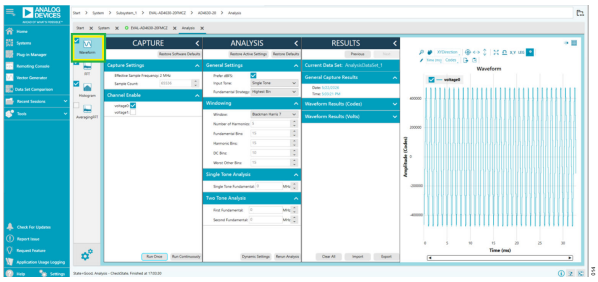

*Figure 17. Dataset Plotted as Time Domain Waveform*

### FREQUENCY DOMAIN (FFT) PLOT

Click the **FFT** area (highlighted in yellow in Figure 18) to display the active dataset as a frequency-domain waveform. The plot then displays the FFT of the active dataset. In this case, select **Log Scale** for the Frequency (MHz) axis above the graph.

When the dataset is plotted as a frequency-domain waveform, the **RESULTS** panel displays metrics relevant to frequency-domain analysis, such as signal-to-noise ratio (SNR) and total harmonic distortion (THD).

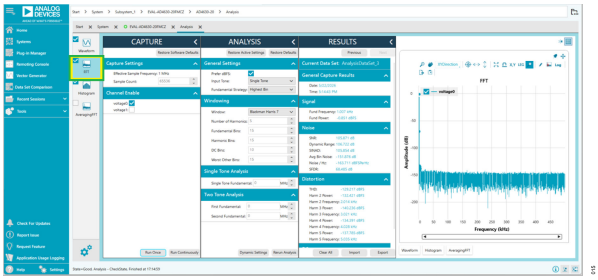

*Figure 18. Dataset Plotted in the Frequency Domain*

### HISTOGRAM PLOT

Click the **Histogram** area (highlighted in yellow in Figure 19) to display the active dataset as a histogram. In this view, the vertical axis represents occurrences (bin hits), and the user can set the horizontal axis to display either code or voltage amplitude bins.

When the dataset is plotted as a histogram, the **RESULTS** panel displays metrics relevant to histogram analysis, such as minimum code, maximum code, and RMS.

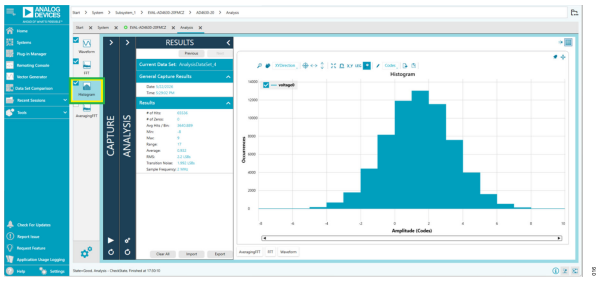

*Figure 19. Dataset Plotted as a Histogram*

## EVALUATION BOARD SCHEMATICS AND ARTWORK

### ADC EVALUATION BOARD—ADC DRIVERS AND ADC

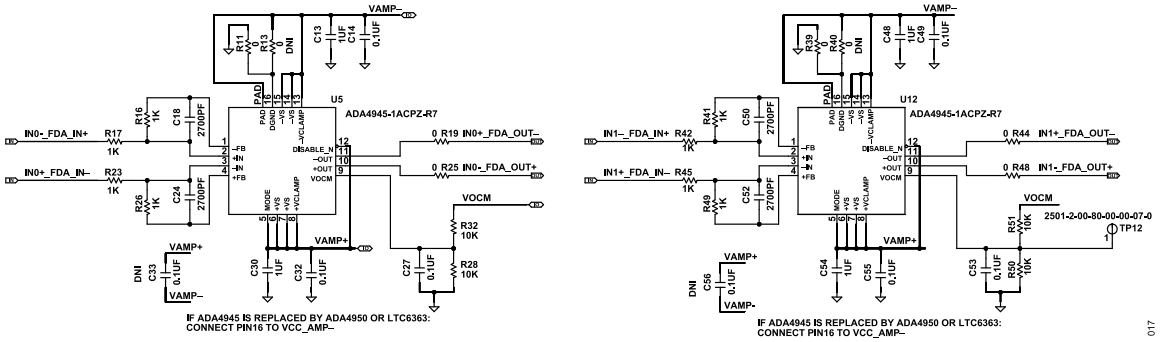


*Figure 20. ADC Drivers*

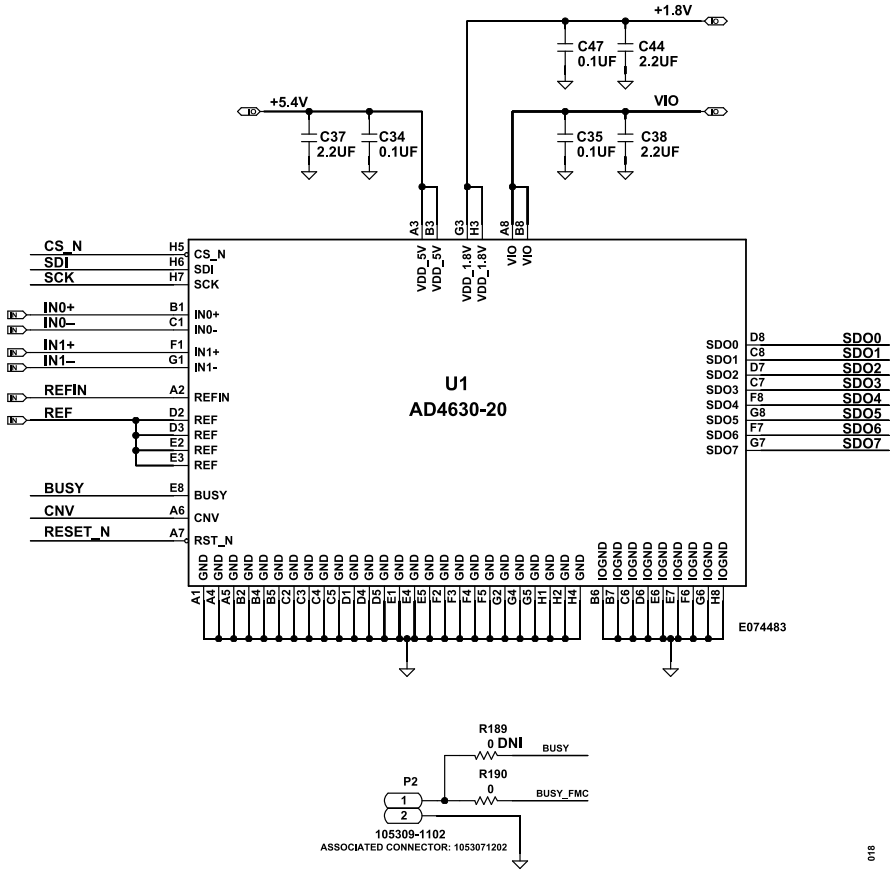


*Figure 21. ADC*

## EVALUATION BOARD SCHEMATICS AND ARTWORK

### ADC EVALUATION BOARD—CLOCK AND COMMON-MODE AND REFERENCE BUFFERS

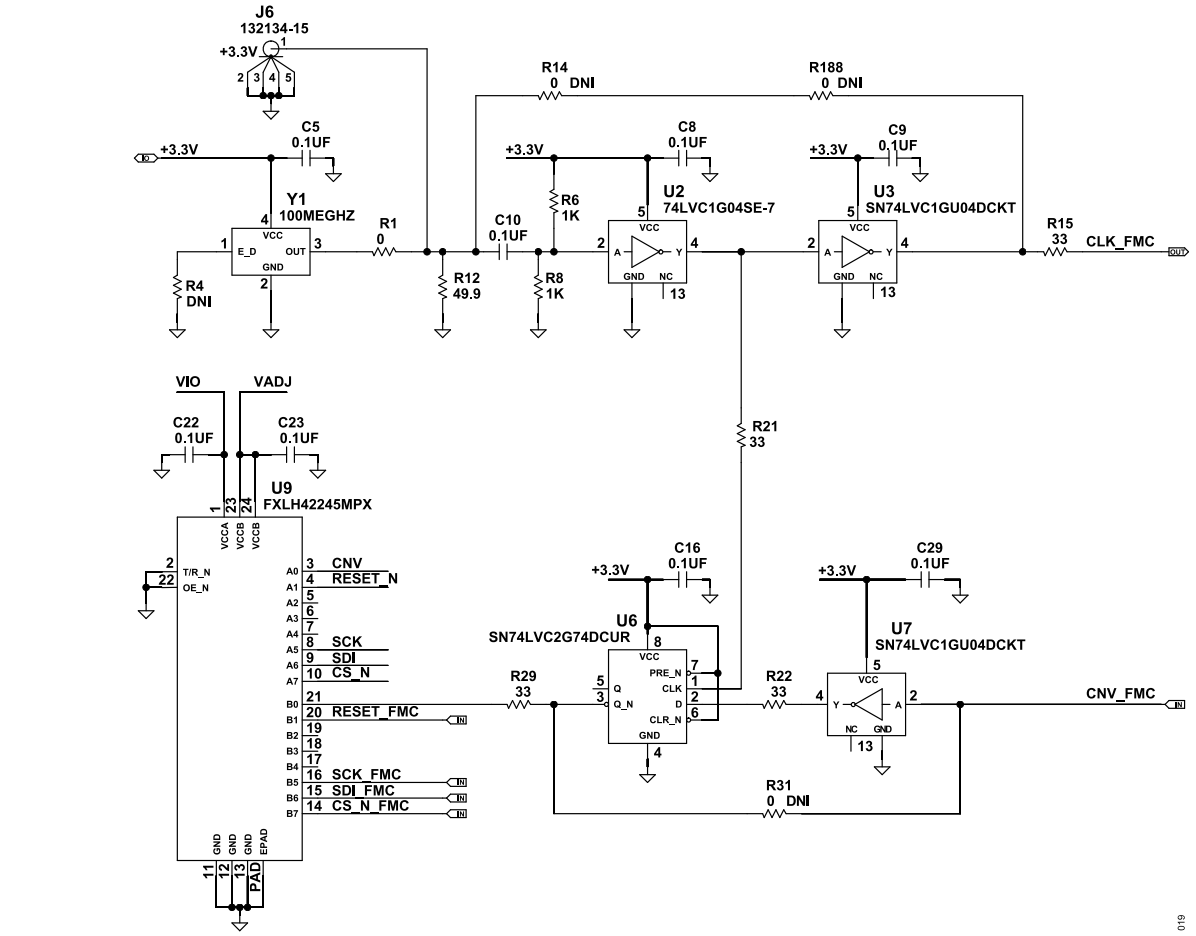


*Figure 22. Clock*

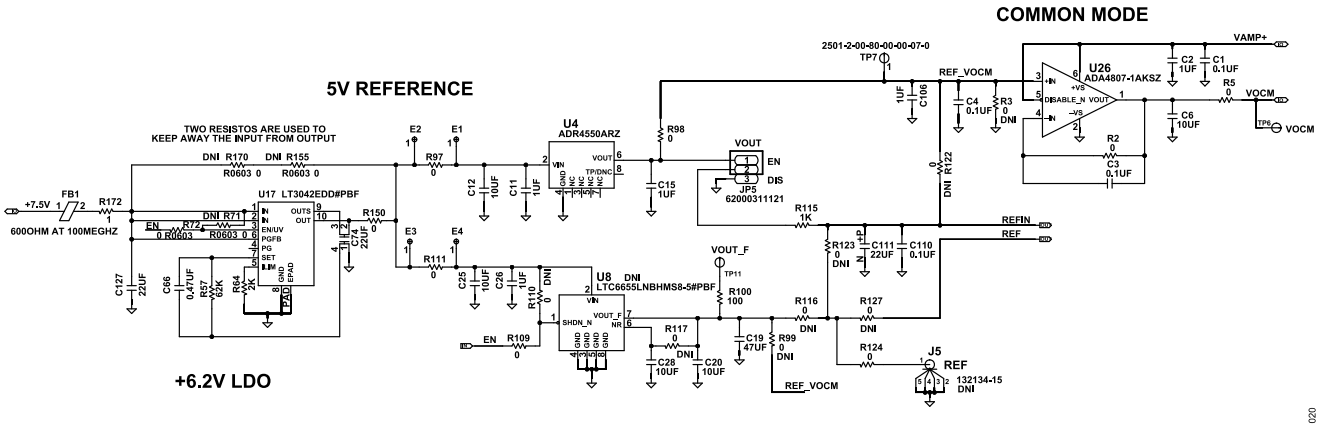


*Figure 23. Common-Mode and Reference Buffers*

## EVALUATION BOARD SCHEMATICS AND ARTWORK

### ADC EVALUATION BOARD—POWER SUPPLY

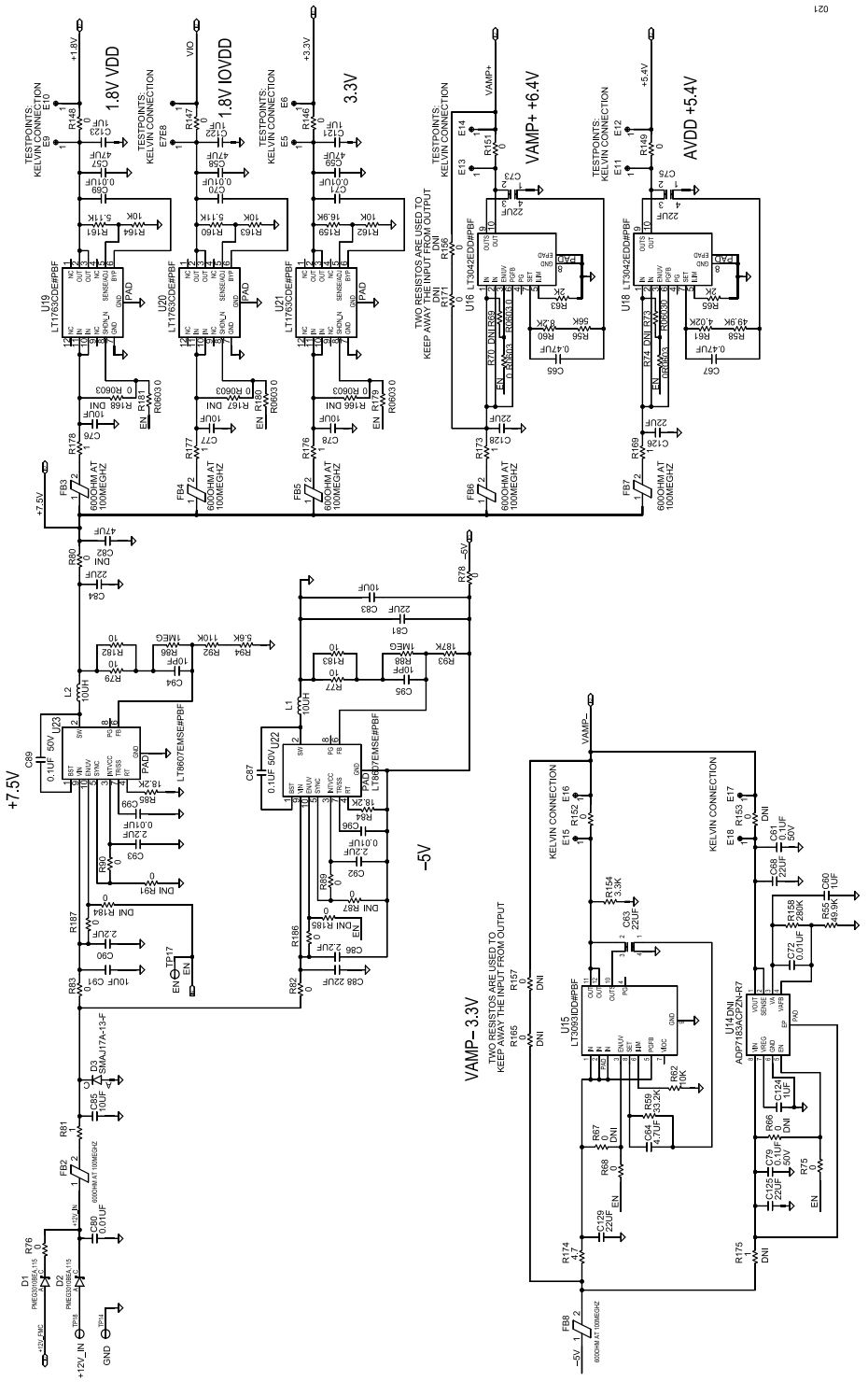


*Figure 24. Power Supply*

## ORDERING INFORMATION

### ORDERING GUIDE

| Model[1, 2] | Description |
|---|---|
| EVAL-AD4630-20FMCZ | Evaluation Board |

[1] Z = RoHS Compliant Part.

[2] A user can use the EVAL-AD4630-20FMCZ evaluation board to evaluate the AD4632-20.

**ESD Caution**
**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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